**MEMBER**

**NGO NGUYEN HOANG TIEN**  
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**I. PERSONAL INFORMATION**

Full name:                              **NGO NGUYEN HOANG TIEN**

Gender:                                  **male**

Date of birth:                          **12th August, 1989**

Nationality:                            **Vietnamese**

**University: Danang university of technology**

Home address:                        **92 Nguyen Chi Thanh, Hue city**

Email:                                     **h\_tien@brycen.com.vn**

Tel:            **0984573463**

Skype**: tienjoneey**

**II. STAGE OF EDUCATION AND WORK**

|  |  |  |  |
| --- | --- | --- | --- |
| **Year** | **Occupation** | **University/Company** | **Location** |
| 9/2007 – 3/2013 | Student | Danang University of Technology | Nguyen Luong Bang Street, Da Nang City, Viet Nam |
| 6/2012 | Freelancer | Freelancer.com | My home |
| 4/2013 – 12/2014 | Student | Aptech Hue | 06 Le Loi, Hue City, Viet Nam |
| 7/2013 – 12/2013 | Developer | Solaris outsource solution | 06 Le Loi, Hue City, Viet Nam |
| 12/2013 – 4/2013 | Freelancer | Freelancer.com | My home |
| 4/2014 – 12/2014 | Developer | Lotus outsourcing | 06 Le Loi, Hue City, Viet Nam |
| 1/2015 – Now | Developer | Brycen Vietnam | 25 Nguyen Van Cu, Hue City, Viet Nam |

**III. FOREIGN LANGUAGES *(Grade: 1\_ beginning; 5\_ expert)***

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Foreign languages** | **Listening** | **Speaking** | **Reading** | **Writing** |
| English | 1 **2** 3 4 5 | 1 **2** 3 4 5 | 1 2 **3** 4 5 | 1 2 **3** 4 5 |
| Japanese | **1** 2 3 4 5 | **1** 2 3 4 5 | **1** 2 3 4 5 | **1** 2 3 4 5 |

**IV. PROGRAMMING SKILLS ABOUT FPGA AND VERILOG**

|  |  |  |
| --- | --- | --- |
| **Skills** | **Months of experience** | **Rank**  *(Grade: 1\_ beginning; 5\_ expert)* |
| **Verilog** | **10** | 1 2 **3** 4 5 |
| **Electronics Digital** | **10** | 1 2 **3** 4 5 |
| **Testbench Verilog** | **10** | 1 2 **3** 4 5 |

**V.** **PROJECT EXPERIENCE**

|  |  |
| --- | --- |
| Project’s name: | **Design the 32 bits processor based on MIPS Pipeline architecture and improve processing speed by branch predicting** |
| Size:  *(number of taken people)* | 1 |
| Execution time | 4 months |
| Technology used: | * 1. **Hardware description language**       + Verilog HDL   2. **Tools** * Quartus II * Modelsim |
| Works in project: | * 1. **Design 32 bits processor with instruction set** * Load Word (LW) * Store Word (SW) * Add Immediate Word (ADDI) * And Immediate (ANDI) * Or Immediate (ORI) * Exclusive Or Immediate (XORI) * Add Word (ADD) * Subtract Word (SUB) * And Word (AND) * Or Word (OR) * Exclusive Or Word (XOR) * Shift Word Left Logical (SLL) * Jump (J) * Jump Register (JR) * Branch On Equal (BEQ) * Branch On Not Equal (BNE)   1. **Use Quartus II draw the block diagram of the hardware**   2. **Use Modelsim test the output of the hardware** * Write testbench * Test the waveform of hardware output |

**VI.** **PERSONAL SKILLS.**

* Working in high pressure.
* Reading technical documents
* Searching and using resources over the Internet.
* Ability to acquire knowledge and technology are quite.
* Having ability to work independently
* Having ability to work group
* Having ability to listen to and collect good ideas from others
* Hard –working

**DECLARATION**

I hereby declare that the above written particulars are true to the best of my knowledge and belief.

Thanks