

# NetSpeed Gemini

## *Release Notes*

**Version: GEMINI-16.09**

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# NetSpeed Gemini 16.09 Release Notes

## About This Document

This document lists the release notes for NetSpeed Gemini. Using NetSpeed NocStudio, users can define NoC architectures, describe specifications and requirements, optimize the NoC design and finally generate the NoC IP files such as RTL, testbench, synthesis scripts, NoC IP documentation etc.

## Audience

This document is intended for users of NocStudio:

- NoC Designers
- NoC Architects
- SoC Architects

## Prerequisite

Before proceeding, you should generally understand:

- Basics of NetSpeed Gemini IP Technology

## Related Documents

The following documents can be used as a reference to this document.

- NetSpeed NocStudio User Manual

## Customer Support

For technical support about this product, please contact [support@netspeedsystems.com](mailto:support@netspeedsystems.com)

For general information about NetSpeed products refer to: [www.netspeedsystems.com](http://www.netspeedsystems.com)

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## 1 Deliverables

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- NetSpeed NocStudio Package, N7 version supporting 16 layers and 256 bridges.
- NocStudio executable with interactive GUI.
- Verification checkers to be used in the DV environment.
- Sanity Test Bench.
- Documentation
  - a. NocStudio User Manual: The User Guide describes how to set up a system using NocStudio and how to use it to generate NetSpeed IP.
  - b. IP Integration Spec: The Integration Manual describes how to integrate a configured network into a larger subsystem.
  - c. Technical Reference Manual: The Technical Reference Manual describes how the functionality of the various NoC elements, the features and functions available, and how to dynamically change the functions using the programmer's mode.

## 2 Installation

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- NocStudio uses FlexLM based licensing.
  - Copy over the license file emailed separately into a folder, and point LM\_LICENSE\_FILE environment variable to this license file before launching NocStudio.
  - NOTE: When untarring Linux files, ensure it is done on a Linux machine. Untarring Linux files on a Windows machine causes problems with symbolic links.
  - The executable requires Linux CentOS 5.5 or higher.
- The release makes use of Qt libraries covered under LGPL:
  - <http://qt-project.org/downloads>

## 3 Feature Updates

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### 3.1 NoC CONSTRUCTION IMPROVEMENTS

#### 3.1.1 Isolate and reduce congestion

NocStudio can now take special consideration while mapping high bandwidth traffic (based on the traffic rate or overall load on the transmitting and receiving interfaces) to isolate them from other traffic so as to reduce congestion in the NoC.

- The user can also sort traffic flows so as to map high bandwidth traffic flows first using the option “high\_rate\_traffic\_flows” in the sort order argument to the map\_opt command. NocStudio also automatically uses “high\_rate\_traffic\_flows” as one of the many sort orders to sort traffic flows in each iteration of map\_opt.
- The user can choose to make NocStudio avoid the mapping of high rate traffic flows and low rate traffic flows on the same VC as part of its mapping algorithm by using the “separate\_high\_rate\_traffic\_flows” argument in map\_opt.

#### 3.1.2 Automated FIFO sizing

Automatic sizing of FIFO depth on VC's with high bandwidth traffic during tune\_links to prevent congestion in the NoC and head of line blocking.

#### 3.1.3 Automated tune\_links

*tune\_links* is now run automatically at the end of map\_opt to tune the link widths and FIFO depths. *tune\_links* is also a separate command that a customer can choose to run.

### 3.2 GUI ENHANCEMENTS

#### 3.2.1 Hide toolbars to increase screen real estate

Press Ctrl+H to hide/unhide the drawing toolbar and the top toolbar to increase the screen real estate.

#### 3.2.2 Minimize the toolbars and the property panels to side tabs

The drawing toolbar, top toolbar and the property toolbar can be minimized to the sides to appear as tabs.

#### 3.2.3 Hide inactive layers after mapping

The layers that don't have any traffic mapped on them are automatically hidden after mapping.

### 3.2.4 New way to add/remove link and port blockages in the Blockage View

In the blockage view, left click on a link to add/remove a link blockage (add/remove blockage to that link on all layers), and right click to add/remove a port blockage (add/remove blockage on the link only on the clicked layer).

### 3.2.5 Collapse all the buttons to add the different agents and bridges to single 'Add' button

The add buttons of different agents (CCC, IOCB, DVM, LLC, Cache, Bridge and SIB) are all collapsed into one 'Add' button.

### 3.2.6 Errored commands remain on console for editing

An errored command remains on the console so that the user can edit it rather than having to retype the entire command.

### 3.2.7 Change color of link when clicked

When a link is clicked, its color changes to pink so that the user knows which link he is currently viewing the state/properties of.

## 3.3 MULTI-NOC

RTL from multiple NoCs can now be integrated into the same design for simulation. Each NoC must have a unique mesh name and the following NocStudio property setting:

```
prop_default tag_project_name yes
```

Two or more NoCs can be integrated with no upper limit to the number of NoCs. Only one coherent NoC is supported per set of NoCs. Crux NoCs cannot be mixed with Orion/Gemini NoCs.

## 3.4 FUNCTIONAL SAFETY

For safe and reliable operation of the device, NocStudio now supports:

1. End to end transport error checking, including Data/Sideband ECC Protection, Data/Sideband Parity Error Detection
2. Hop to hop error checking of packet fields
3. Error reporting

For more details, please refer to Chapter "Safety and Reliability" in the TRM.



### 3.5 SYNCHRONIZER DEPTH AND FIFO SIZING

NocStudio now supports programmable synchronizer depths, both for general synchronizers (ns\_demet.v) and for reset synchronizers (ns\_rst\_n.v). Users may select synchronizer depths, based on their own library/process requirements, on a per-clock-domain granularity.

### 3.6 TRAFFIC CLASS OPTIMIZATION

In many cases, it may make sense to have requests and responses have different traffic classes. Traffic flows to memory, for instance, may want to have different traffic classes for the different requests. This is particularly true when different priorities are used for the traffic classes.

The response path may not need separate traffic classes. If a low priority response is stuck leaving the memory controller, it can block high priority responses as well. It will often make sense to have these responses share a single traffic class.

This can also significantly reduce area within a NoC. Traffic classes require separate virtual or physical channels, which requires more storage and possibly more links. While this may be useful for traffic going to memory, the expense of the response path may be unnecessary. And since data paths are often wider than request paths, this can be a significant area impact.

NocStudio allows each hop of a traffic flow to indicate a separate traffic class, to provide user with the flexibility to configure various requests and responses to either use different traffic classes or share them.

### 3.7 USER DEFINED SYSTEM RESOURCE OVERRIDE

Support for user defined NOC system level resource for compatibility of families of products. In NoC synthesis flow, the tool automatically calculates the resource needed for a given project to provide the most optimized solution. But in terms of derivative or re-spin, due to some ECO changes, NocStudio may expand the resource (e.g. AID width). In order for the NocStudio to preserve the NOC resource, SOC architect/designer needs to predict the address width, AID width, User width, etc. and use mesh\_prop "sys\_\*\_width <N>" to override the System level NOC resource.

### 3.8 NEW VERIFICATION FEATURES AND UPDATES

#### 3.8.1 LLC preload for fast initialization

Verification mechanism for 0-time backdoor preloading of LLC to enable fast initialization in RTL simulation.

### 3.8.2 CCC/LLC Performance and Debug

Verification support for additional mailboxes providing visibility into CCC and LLC activity has been added. This capability allows verification test benches to poll the mailbox to monitor for and obtain additional details about actions initiated within the CCC/LLC such as cache-line evictions.

### 3.8.3 Verification `define to allow forcing of coherency connect in simulation

Verification support for `define to enable forcing of connection to coherent fabric in simulation for coherent masters that have 'cc\_coherency\_connect' as 'register\_disconnected'. This allows ease of coherency testing when masters are not connected to coherency fabric by default.

### 3.8.4 Updated mailbox syntax

A new argument "proj\_tag" has been added as follows:

Old syntax:

```
`NS_E2E_CHECKER_TOP.ns_transaction_src_mbox.try_get(ns_src_transaction)
```

New syntax:

```
`NS_E2E_CHECKER_TOP.ns_transaction_src_mbox[proj_tag].try_get(ns_src_transaction)
```

where "proj\_tag" is a string that should be,

- Set to project\_name if the noc is using 'tag\_project\_name'
- Set to an empty string if the noc is not using 'tag\_project\_name'

## 3.9 32BYTE FAST TAP

Additional support for 32byte Fast Tap to reduce latency for wider ACE masters. Previous support was only for 16byte ACE masters. The Fast Tap is a more direct connection between an ACE master and the coherency controller. By having a direct connection, it is able to skip some of the network overhead of the system. Fast Tap does require dedicated wires as well as some additional storage, so it does not come for free. However, for many systems, the latency reduction may be worth the additional costs.

## 3.10 ACE OPTIMIZATION FOR DVM

Additional optimization for ACE Masters with no DVM. While ACE masters are assumed to support DVM, it is possible to specify that an ACE master does not support DVM. A NocStudio bridge property for the ACE master bridge called *acem\_dvm\_support* can be set to no. When disabled, the ACE master will not receive DVM snoops, cannot generate DVM requests, and will not power up the DVM when it performs a coherency connect.

### 3.11 LLC SCRATCHPAD INTERLEAVING

LLC Scratchpad now supports interleaving of address range across a RAM group. Part or all of the LLC can be configured as Scratchpad RAM. When multiple LLCs are added to a RAM group, it indicates that a single address range will be divided across the specified LLCs. Once the RAM group is created, an address range must be assigned to the RAM group. The range can now be divided and interleaved using slice bits or a hash function.

### 3.12 LLC EXCLUSIVE SUPPORT

Pegasus can be configured to provide AXI Exclusive functionality (see AXI/ACE specification section A7) when it is configured as a memory cache. Exclusive sequences require a monitor per agent to track whether a line has been modified between an Exclusive read and the Exclusive write. Pegasus can be configured with a variable number of Exclusive monitors.

### 3.13 LLC ALLOCATION CONTROLS

LLC supports way allocation controls. A new property called LLC Allocation Class is added in NocStudio to each master bridge that can talk to the LLC. This can be set to one of 8 allocation classes. Each allocation class has a set of allocation control capabilities which are programmable with defaults configurable in NocStudio. This includes selection of which ways in the cache a request can allocate into, as well as allocation rules. Pegasus also allows the option of controlling the allocation statically based on register setting or dynamically based on AXI control signals.

### 3.14 LLC FLUSH ENGINE

Pegasus supports a hardware Flush Engine to flush and invalidate the entries of the LLC. The flush engine is controlled by the LLC Way Flush register. The waygroups that you want to flush can be written to the wayflush register, and it will trigger the flush engine. Once the flush process has completed, the way flush control register will reset to zero.

### 3.15 LLC INDIRECT ACCESS

Both the Data RAMs and Tag RAMs are accessible through register based accesses. This allows a backdoor method of reading or write the arrays, which can be useful for debug, DFT follow up, or even for controlling stimulus in a test. The register-based accesses use two sets of registers. It uses the indirect content registers, and the indirect trigger register. The content registers hold data to be written to the RAMs, or data read from the RAMs.

### 3.16 LLC MemCache Area Optimization

The LLC can be configured to have a second slave port to allow a more latency optimized solution for coherent access in the memory cache mode. The second slave port is used when there are multiple masters talking to the LLC. This can happen in a variety of cases, including where CCC talks to LLC, but so do other masters in a memory cache mode. By using the second port, the CCC can talk directly to the LLC, allowing it to skip the bridges and routers if the ports are co-located in the same grid position in NocStudio. This can provide a significant performance improvement by reducing the latency of coherent requests.

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## 4 EDA Tool Compatibility

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- Cadence EDA tools were used for verification and synthesis of this product.
- Compatibility testing has been done with VCS. Issues, if any, might be seen in the verification IP for specific configurations. The NetSpeed IP Integration specification lists the various defines to be used to enable / disable Verification IP. NetSpeed support will be available to resolve any issues.

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## 5 Errata

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### 5.1 AHB

There could be a deadlock between AHB master bridge and the AHB master if master is waiting for HREADY to be asserted before removing the BUSY command. Workaround: remove BUSY as soon as the next command is available.

### 5.2 PRIORITY ADDRESS MAP

The Priority Address Map has a potential issue when some agents do not have access to a slave in a foreground range. Instead of getting a decode error when they attempt to access those ranges, they can hit against the background range and send the request to that slave.

### 5.3 GUI ADD\_BRIDGE COMMAND DOESN'T WORK PROPERLY

An extra -bridge\_id string is invoked which results an GUI error. Please repeat the same command without the -bridge\_id to workaround the issue.

### 5.4 NOCSTUDIO CALCULATED FIFO\_DEPTH MAY BE 1 ENTRY SHORT

NocStudio automatically derived FIFO depth on link based on traffic requirement. When ILDC (In Link Domain Crosser) is enabled with ECC, the calculated FIFO depth may not be ideal. Please note that this issue only applies to NOC boundaries (i.e. master bridge --> router or router --> slave bridge). User can workaround it with increased FIFO depth using link\_prop fifo\_depth <depth> command.

## 6 Changes to Commands and Properties

### 6.1 COMMAND CHANGES

| Command Name                    | Comment   |
|---------------------------------|---|
| add_output_reg_across_rtl_group | Name change. Previous name was add_output_reg_across_rtlgroup |
| show_project                    | New command to print the project name                         |
| set_clock_domain_sync_depth     | New command to set the synchronizer depth of a clock domain   |
| add_ram_group                   | New command to group LLC's that work as RAM (scratchpad)      |
| del_ram_group                   | New command to delete RAM groups                              |
| list_ram_group                  | New command to list the added RAM groups                      |
| map                             | This command has been deprecated                              |
| tune_route                      | This command has been deprecated                              |
| tune_links                      | This command has been deprecated                              |

### 6.2 DEFAULT PROPERTY CHANGES

| Property Name       | Default Value | Comment  |
|---------------------|---------------|--|
| msg_peak_bw         | 6.4           | This property has been deprecated  |
| msg_peak_rate       | 0.1           | This property has been deprecated  |
| peak_multiplier     | 1             | New property to specify the default multiplier to calculate peak rate/bw from average rate/bw when the peak rate/bw is not specified |
| sync_input_register | no            | New default property to enable or disable input registering at the bridge when there is no clock crossing at the bridge.             |

|                          |     |   |
|--------------------------|-----|---|
| synchronizer_depth       | 2   | New property to specify the default value of synchronizer depth for all clock domains.          |
| axi4m_logical_processors | 1   | New property to specify the default number of logical processors supported by the master bridge |
| axi4m_exclusive_support  | Yes | New property to specify if a master has AXI exclusive support by default                        |
| sysc_enable              | no  | Enable generation of SystemC LT model ( <b>Special License needed</b> )                         |
| read_burstiness          | 1   | The default value for this property has been changed from 3 to 1                                |

### 6.3 MESH PROPERTY CHANGES

| Property Name                | Default Value | Comment   |
|------------------------------|---------------|---|
| compact_regbus_address_space | Yes           | Default value of this property has changed from No to Yes                 |
| extra_bandwidth_provisioning | 0             | Default value of this property has changed from 25 to 0                   |
| sys_r_user_bits_per_byte     | -1            | New property to specify the default for the system R user width per byte. |
| sys_r_user_width             | -1            | New property to specify the default for the system R user width.          |
| sys_b_user_width             | -1            | New property to specify the default for the system B user width           |
| sys_ar_user_width            | -1            | New property to specify the default for the system AR user width          |
| sys_axi4_aw_aid_width        | -1            | New property to specify the default for the system AXI4 AW AID width.     |
| sys_mst_id_width             | -1            | New property to specify the default for the system master ID width        |



|                          |      |  |
|--------------------------|------|--|
| sys_aw_user_width        | -1   | New property to specify the default for the system AW user width.  |
| sys_axi4_addr_width      | -1   | New property to specify the default for the system AXI4 address width.                                       |
| sys_axi4_ar_aid_width    | -1   | New property to specify the default for the system AXI4 AR AID width.  |
| sys_w_user_bits_per_byte | -1   | New property to specify the default for the system W user width per byte.                                    |
| stats_level              | High | New property to specify the default level of statistics collection in NocStudio performance simulator        |
| errorcheck_granularity   | 502  | New property to specify the default upper limit of error check granularity ( <b>Special license needed</b> ) |

## 6.4 BRIDGE PROPERTY CHANGES

| Property Name              | Comment   |
|----------------------------|---|
| axi4s_logical_id_enb       | New property that indicates whether logical ID is enabled for read and write requests to a slave bridge |
| sync_input_register        | New property that enables input registering at the bridge when there is no clock crossing at the bridge |
| acem_dvm_support           | New property that enabled ACE masters to have connections to the DVM block                              |
| axi4m_logical_processors   | New property to specify the number of logical processors supported by the master bridge                 |
| axi4m_exclusive_support    | New property to specify if a master has AXI exclusive support   |
| axi4m_llc_allocation_class | Name change. Previous name was llc_allocation_class   |

## 6.5 HOST PROPERTY CHANGES

| Property Name | Comment |
|---------------|---------|
|---------------|---------|

|                                       |   |
|---------------------------------------|---|
| llc_class_write_allocate              | New property to specify how write allocation is controlled for each of the LLC classes.                                 |
| llc_class_read_allocate_use_arcache   | New property to specify whether read allocation for each LLC class is controlled by the ARCACHE bits                    |
| llc_class_read_allocate               | New property to specify how read allocation is controlled for each of the LLC classes.                                  |
| llc_class_write_allocate_use_awcache  | New property to specify whether write allocation for each LLC class is controlled by the AWCACHE bits.                  |
| llc_second_slave_port_connect         | New property to specify which master connects to the second LLC slave port (if it exists)                               |
| llc_slave_port2_read_max_outstanding  | New property to specify the number of outstanding read requests the second LLC slave port can support from all sources. |
| llc_slave_port2_write_max_outstanding | New property to specify the number of outstanding write requests the second LLC slave port can support from all sources |
| llc_class0_alloc_waygroups            | New property to specify which waygroups can be accessed by class 0 of the LLC   |
| llc_class1_alloc_waygroups            | New property to specify which waygroups can be accessed by class 1 of the LLC   |
| llc_class2_alloc_waygroups            | New property to specify which waygroups can be accessed by class 2 of the LLC   |
| llc_class3_alloc_waygroups            | New property to specify which waygroups can be accessed by class 3 of the LLC   |
| llc_class4_alloc_waygroups            | New property to specify which waygroups can be accessed by class 4 of the LLC   |
| llc_class5_alloc_waygroups            | New property to specify which waygroups can be accessed by class 5 of the LLC   |
| llc_class6_alloc_waygroups            | New property to specify which waygroups can be accessed by class 6 of the LLC   |

|                            |   |
|----------------------------|---|
| llc_class7_alloc_waygroups | New property to specify which waygroups can be accessed by class 7 of the LLC |
|----------------------------|---|

## 6.6 INTERFACE PROPERTY CHANGES

| Property Name     | Comment   |
|-------------------|---|
| internal_pipeline | New property to decide the type of registering between switch and protocol side for each host interface. One of these options can be enabled to remove timing paths between switch and protocol processing logic. |

## 6.7 LINK PROPERTY CHANGES

None

## 6.8 ROUTER PROPERTY CHANGES

None

## 6.9 VC PROPERTY CHANGES

None

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