

NetSpeed Gemini & Orion 16.04 Release Notes

Version: GEMINI-16.04

April 15, 2016

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NetSpeed Gemini & Orion 16.04 Release Notes

About This Document

This document lists the release notes for NetSpeed Gemini & Orion. Using NetSpeed NocStudio, users can define NoC architectures, describe specifications and requirements, optimize the NoC design and finally generate the NoC IP files such as RTL, testbench, synthesis scripts, NoC IP documentation etc.

Audience

This document is intended for users of NocStudio:

- NoC Designers
- NoC Architects
- SoC Architects

Prerequisite

Before proceeding, you should generally understand:

- Basics of NetSpeed Gemini IP Technology

Related Documents

The following documents can be used as a reference to this document.

- NetSpeed NocStudio User Manual

Customer Support

For technical support about this product, please contact support@netspeedsystems.com

For general information about NetSpeed products refer to: www.netspeedsystems.com

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1 DELIVERABLES

- NetSpeed NocStudio Package, N7 version supporting 16 layers and 256 bridges.
- NocStudio executable with interactive GUI.
- Verification checkers to be used in the DV environment.
- Sanity Test Bench.
- Documentation
 - a. NocStudio User Manual: The User Guide describes how to set up a system using NocStudio and how to use it to generate NetSpeed IP.
 - b. IP Integration Spec: The Integration Manual describes how to integrate a configured network into a larger subsystem.
 - c. Technical Reference Manual: The Technical Reference Manual describes how the functionality of the various NoC elements, the features and functions available, and how to dynamically change the functions using the programmers mode.

2 INSTALLATION

- NocStudio uses FlexLM based licensing.
 - Copy over the license file emailed separately into a folder, and point LM_LICENSE_FILE environment variable to this license file before launching NocStudio.
 - NOTE: When untarring Linux files, ensure it is done on a Linux machine. Untarring Linux files on a Windows machine causes problems with symbolic links.
 - The executable requires Linux CentOS 5.5 or higher.
- The release makes use of Qt libraries covered under LGPL:
 - <http://qt-project.org/downloads>

3 FEATURE UPDATES

3.1 FINE-GRAIN CLOCK GATING IMPROVEMENTS

Support for fine grained clock gating has been enabled for pipeline registers. Since the valid signals need to control the clock-gater, this will consume additional time in the cycle for the fanout and gating. The distance that can be travelled in a cycle will be reduced accordingly. Consequently, there is a potential tradeoff between power and latency. A new link property is created to enable this fine-grain clock gating support. The default property is set to enable this fine-grain clock-gating. This can be modified by changing the `prop_default`:

```
prop_default enable_fine_grain_clock_gating no
```

Alternatively, each link can be controlled individually using the link property, such as:

```
link_prop R0/18E.in enable_fine_grain_clock_gating no
```

3.2 COARSE-GRAIN CLOCK GATING FOR GEMINI

Gemini IP components (CCC, DVM, IOCB, and LLC) all support coarse-grain clock gating now. These components look for idle conditions and turn off the clock for the entire component. New requests may be delayed a cycle while the clock turns back on. These modules are controlled by hysteresis counters just like the other NoC components. The hysteresis count can be controlled per agent.

3.3 16 LAYER NOC SUPPORT

Maximum number of layers supported by NocStudio has been increased from 8 to 16 layers. This will enable even more sophisticated and complex designs to be designed through NocStudio.

3.4 SHARED INTERFACE MASTER BRIDGE

Support for a new bridge type called shared interface master bridge (SIB) has been added. Using this bridge, up to 4 AMBA hosts can share a master bridge on the NoC. A SIB contains a full master bridge and a port aggregator.

Here are the requirements for using the SIB:

- Single clock domain for all hosts

- Support for AXI4 and AXI3 protocols
- Maximum of 4 hosts aggregated
- Maximum of 16 ports aggregated
- The NocStudio command to add the SIB master bridge is the following:

```
add_sib -name <name> -pos <pos>
```

3.5 SHARED INTERFACE BRIDGE AND PORT CHECKING

The Shared Interface Bridge enables port-checking capability. Port-checking is used with two equivalent masters that run in lock-step. Port-checking compares all traffic going in an out ports for equivalence. When the two masters make a request, only one is treated as real within the NoC. When the response is returned, it is returned to both. If they ever make requests or transmit data that is not equivalent and on the same cycle, the Shared Interface Bridge will report an error.

The command to enable port-checking is:

```
set_sib_port_check_pairs -name <name> -pairs <m0>:<m1>  
[<m2>:<m3>]+
```

3.6 PROGRAMMABLE RELOCATION REGISTERS AND HASH FUNCTIONS

The support to program the relocation registers and hash functions is now available. The hash functions can be made programmable using the `add_hash_function` command.

For reloc registers, they can be enabled as follows.

In the `add_range` command, when `-reloc` flag is used, an address offset is set to determine how the address will be presented to the slave. To make that Slave Address programmable, the `add_range` command now has a `prog_reloc_slv` flag that can be set to 0 or 1.

In the `add_range_to_master` command, the `-base` flag is used to indicate that the Master Address is different from the System Address, then `reloc_sys` register will inherit the programming from the original `add_range` programmability option. So if the range was created as programmable, and an `add_range_to_master` is used, the `reloc_sys` will be a programmable register. In other words, since the `add_range` specified that the System Sddress was programmable, the `reloc_sys`, if used, will be programmable.

More details about the usage of these feature can be found in the NetSpeed Gemini Technical Reference Manual.

3.7 COMBINED RELOCATION AND HASHING FUNCTIONS

The support for combining the Relocation and Hashing Functions Features is now available. All hashing functions are performed on the System Address, and not the Master Address or Slave Address. This enables a consistent hashing for each address range.

3.8 RESET BYPASS FOR DFT

The ability to bypass reset for DFT is now available. This is needed for testability functionality. New inputs to the interconnect are provided to control the reset bypass.

3.9 PRIORITY ADDRESS MAP

The support for priority address map is now available. In the `add_range` command, a new argument called “background” can be used to create a background/default range. Requests first check the normal foreground ranges to determine if there is an address match. If they miss, they will look up the background ranges and can be sent there.

One use case would be to create a large background range that goes to memory, with smaller ranges that carve out smaller portions of that address range for other devices. A 4MB background address range with a 4KB carveout would only need two address ranges. If these were implemented as normal ranges, requiring power-of-2 sizes, it would require many ranges to fill in all of the gaps created by the 4K region.

This feature must be used with care. If some agents don’t have access to one of the foreground ranges, they will end up hitting on the background range and will send there requests to that slave, instead of getting a decode error.

More details about the usage of these feature can be found in the NetSpeed Gemini Technical Reference Manual.

3.10 REG BUS MASTER GUARANTEE OF FORWARD PROGRESS

The Reg Bus Master now guarantees forward progress to the dedicated port when the tunnel is used. If the main NoC layer goes down, it can potentially prevent responses being returned from the tunnel. In prior releases, this backpressure could affect the dedicated port. In this release, dedicated resources enable the dedicated port to make forward progress even if the tunnel is locked.

3.11 AHB SLAVE BYTE ENABLE SUPPORT

The AHB Slave byte enable support is now available. This provides the ability to handle packets where not all bytes are valid. AHB protocol does not have write strobe (byte enable). Therefore sparse writes need to be conveyed using HADDR and HSIZE.

3.12 AHB-LITE SLAVE AREA REDUCTION

The AHB-lite slave bridge has a new property that disabled write bursts and sends writes as a sequence of single-beat writes. This eliminates a significant data structure within the AHB-lite bridge, reducing area substantially. This reduction is enabled by default, but can be modified with the following NocStudio property:

```
bridge_prop ahbls_no_write_bursts_enable yes/no
```

3.13 APB MASTER INTERFACE FOR REG BUS

The APB Master Interface for reg bus is now available. When RegBus tunnel is used, the additional port can be configured to use APB. This allows an APB connection to the regbus layer for debug, as an example. The NoC registers have been modified to enable 32-bit access so the APB port can be used to access all registers.

The NocStudio property to enable this feature is:

```
host_prop tunnel_slv1_apb yes
```

3.14 MULTI-CLOCK REG BUS

The Multi-Clock reg bus is now available. The NocStudio property to enable this feature is:

```
prop_default use_dedicated_regbus_clk no
```

With this setting, in mapping NocStudio will use the node clock domain for regbus routers and ring master (rbs) instances. Just as with other layers, the clock domain assignments for regbus routers may be further tuned with router_prop clock_domain commands.

3.15 SEPARATE INTERRUPT PINS AT THE NOC LEVEL OPTION

The ability to have separate interrupt pins at the NOC level is now available.

This gives 2 options for interrupt signal pin aggregation:

- All interrupt signals are OR'd together into a single pin at the ns_soc_ip interface.
- All interrupt signals are brought directly out to pins on ns_soc_ip from each NoC element source.

The interrupt aggregation can be controlled by the following NocStudio Mesh Prop:

```
mesh_prop single_interrupt_for_noc yes/no
```

The default is set to yes, which will combine the interrupts into a single signal.

3.16 CENTRALIZED CLOCK CROSSING ON THE LINKS

Support for clock crossings on Noc links is now available. Previously all clock-domain crossings were done in noc bridges or routers. Now, for cases where it is desirable to have a clock-domain crossing on a noc link, either between two routers or between a bridge and a router, NocStudio will enable you to instantiate an asynchronous fifo on a link at a position you choose, and the clock crossing will occur there. This might be helpful, for instance, at the boundary between layout partitions, where the clocks must be kept internal to their respective partitions.

NocStudio provides two ways to instantiate clock crossings on links. The first is using a link_prop:

```
link_prop <link_name> domain_crosser_pos <position>
```

For example, "link_prop R0.7S domain_crosser_pos 7" will place an asynchronous clock cross fifo on link R0.7S at position 7. The second way to create asynchronous crossings links is to use the following NocStudio command:

```
create_async_crossers_between_groups
```

This command will create asynchronous link clock-domain crossing fifos on all links that go between rtl groups defined in NocStudio.

When either method is used, NocStudio will auto-configure the pre- and post-domain crossing pipeline depths and credits.

3.17 ADDING PIPELINE REGISTERS INTO THE DEF FILE

The DEF file now includes recommended placement information for pipeline registers.

3.18 VARIABLE SIZE GRID SUPPORT

The variable size grid support is now available. You can define the dimension of every column and row with different values. This gives the ability to model the floorplan more accurately. New commands to enable this feature are:

```
set_row_height <Row no> <value>  
set_column_width <Column no> <value>
```

3.19 DYNAMIC PRIORITY SUPPORT FOR ISOCHRONOUS TRAFFIC

The dynamic priority support for isochronous traffic is now available. This provides the capability for the priority to be dynamically changed for real time traffic such as audio or video traffic in order to meet the real time requirements.

Dynamic priority allows traffic classes to be specified with two priority levels. A side-band input will be created for each traffic class with alternative priority levels. The input will change the behavior of all bridges and routers to use the alternative priority. This will affect the behavior of all outstanding and new requests in that traffic class.

One intended use of this feature is to support isochronous traffic classes, such as display traffic. Display traffic would be given its own traffic class and two priorities. It should be given a low priority as its default value. When the display engine starts falling behind in its data prefetching, it can change the dynamic priority select control to switch to the alternative priority, which should be set to a high priority. This will allow the traffic to start as low priority but switch to high priority as the real-time requirement approaches.

3.20 MULTI-VOLTAGE LOW POWER SUPPORT

The Multi-Voltage Low Power Support is now available, allowing a voltage crossing to be present between the host and the bridges of the NoC.

3.21 EXPOSING VIRTUAL CHANNELS AT THE SLAVE BRIDGE

The support for Exposing Virtual Channels at the Slave Bridge is now available.

The number of virtual interfaces on a slave can be controlled by bridge properties `axi4s_ar_num_virtual_ifces` (to control the number of virtual channels on the AR interface) and `axi4s_aw_num_virtual_ifces` (to control the number of virtual channels on the AWW interface).

Here are the new properties to enable this feature:

```
bridge_prop axi4_ar_num_virtual_ifces host/bridge <num>
bridge_prop axi4_aw_num_virtual_ifces host/bridge <num>
```

3.22 RTL GROUPING FOR HIGH FANOUT NETS AND PIPELINE REGISTERS

The support for RTL grouping for high fanout nets and pipeline registers is now available.

3.23 ORIGINAL ID PROPAGATION

The AxID present to a slave interface will consist of a transaction ID plus the ID of the initiating master. However, when multi-hop traffic exists, such as a coherent read that goes to CCC, then LLC, and then to memory, the Master ID that arrives at the destination is the ID of the last master. In this case, the LLC.

It may be useful to know where the request originated. NocStudio allows a port to add an additional bus to the AR and AW channels, called the Original ID bus. This bus is separate from the ARID or AWID bus, and provides no ordering restrictions to the agent. This is just an information bus.

To enable the Original ID additional to the AR and AW bus, a slave may set the bridge properties as follows:

```
bridge_prop slave/port axi4_ar_org_id_enb yes/no
bridge_prop slave/port axi4_aw_org_id_enb yes/no
```

3.24 CR/CD TO R LATENCY IMPROVEMENT

CCC has reduced latency between a snoop response to the read response waiting for the snoop.

3.25 SPECULATIVE FETCH CONTROL FOR ACE-LITE AGENTS

Speculative fetch is the ability of the CCC to issue a read to LLC/memory before the directory has been accessed or the snoop responses returned. In the prior release, the speculative fetch programmability was limited to ACE agents and the IOCB. All agents talking through IOCB

(ACE-lite, ACE-lite+DVM, and AXI->ACE-lite converted) used the IOCB property. Now each agent can individually control whether to perform speculative fetch. The default value can be specified in NocStudio using a bridge property. This value can be reprogrammed.

```
bridge_prop master/port cc_axi4m_speculative_fetch yes/no
```

3.26 MULTIPLE SPLIT SIZES FOR GEMINI

The split sizes controlled at each master was forced to be 64B when the bridge accessed one of the Gemini IPs (CCC, IOCB, LLC). This is no longer required. The bridge determines if a request is to one of these destinations and will force a split of the request to 64B boundary if needed. But if the request targets another IP, the programmed split size will be used to determine whether to split and on what boundary.

3.27 EARLY WRITE RESPONSE AT CCC

CCC now has the ability to provide an early write response instead of waiting for the write to propagate to LLC or memory.

3.28 CCC PROVIDES READ RESPONSE WITHOUT WAITING FOR MEMORY

If the CCC issues a speculative fetch for a cache line, the snoop response may return with sufficient data to process the request immediately. If a read to memory was issued speculatively, the CCC used to wait for that to complete as well before satisfying the read. It will now return immediately.

3.29 LLC SCRATCHPAD RAM MODE

The LLC can now be configured or programmed to convert parts of the cache into a scratchpad RAM. This can be controlled on a way-group basis (4 ways). A range must be created that is the size of the LLC rounded up to the nearest power of 2. Then two properties can be set to determine the reset condition of the cache:

```
host_prop llc llc_waygroup_ram_mode_enable bit_vector  
host_prop llc llc_waygroup_ram_mode_secure bit_vector
```

The first property determines which of the waygroups is enabled by default as RAM. The second property determines the security requirements for each waygroup, since the scratchpad RAM acts as a backing store. A zero indicates non-secure access. A one indicates secure access.

3.30 LLC WAY ALLOCATION CONTROLS

LLC now support way allocation controls. A new property called LLC Allocation Class is added to each master bridge that can talk to the LLC. This can be set to one of 8 allocation classes. The LLC has a control register for each allocation class to determine which of the waygroups a line can allocation into by that agent. This can allow soft-partitioning of associativity in the LLC. The LLC Allocation Class is controlled by a bridge property.

```
bridge_prop master/port llc_allocation_class #class_num
```

3.31 CCC DIRECTORY NOW SUPPORTS PARITY

CCC directory already had the ability to be protected with ECC. It now includes the option to have parity protection as a lower-area solution. This can be enabled using the following CCC host property:

```
host_prop ccc cc_directory_parity_enabled yes/no
```

3.32 COHERENCY CONNECT/DISCONNECT

Gemini now supports a coherency connect/disconnect protocol for ACE and ACE-lite+DVM agents. When connected to coherency, they are able to issue coherent or DVM requests and receive snoops. When disconnected, no snoops will be sent to them and they can be safely reset or powered off. The connect/disconnect protocol can either be controlled by I/O pins to the agent (called SYSCOREQ and SYSCOACK), or they can be controlled through registers. If controlled through registers, an agent can be configured to be disconnected or connected after reset.

To control the connect default or whether to use pins or registers, use the following bridge property:

```
bridge_prop master/port cc_coherency_connect  
<io_pins/register_connected/register_disconnected>
```


3.33 HASHING OR SLICING FOR CCC, LLC, CACHE AND SLV GROUPS

The `add_ccc_group`, `add_llc_group`, `add_cache_group`, and `add_slv_group` commands now support either address slicing or address hashing to determine which of the agents in the group should receive a request.

3.34 IMG2 SIDEBAND OPTION

The new IMG2 sideband option is now supported. Please note that this feature violates the IMG2 protocol.

The user bit region is only needed for the command.

- The constraint to have same user bit width for command and data has been removed.
- The `img_user` signal is generated instead of `tag_sb` when command user bit is specified.
- The user bit is not used for response per the customer.

4 EDA TOOL COMPATIBILITY

- Cadence EDA tools were used for verification and synthesis of this product.
- Compatibility testing has been done with VCS. Issues if any might be seen in the verification IP for specific configurations. The NetSpeed Orion AMBA IP Integration specification lists the various defines to be used to enable / disable Verification IP. NetSpeed support will be available to resolve any issues.

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5 PROTOCOL & HW RESTRICTIONS

- Regbus master bridge implements a customized AXI protocol with 32b data width, AxLEN of 0, 1 to support 32b, 64b register accesses over a 32b down-sizeable NoC layer interface.
- AXI error handling has the following limitation
 - For reads responses for narrow transfers, if RRESP for the same response has mixture of different error types per beat, end-to-end checker may flag a false RRESP mismatch. This is a pathological case and not expected to be seen in normal usage.

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6 ERRATA

6.1 ORION LOW POWER SUPPORT

- User regbus bridges are not currently fully supported in low power mode
- Multi-voltage: AHBLM master bridge, and IMG2bus, APB & AHB slave bridges do not implement multi-voltage support.
- For regbus, the following restrictions apply:
 - The regbus feature has been tested only with limited directed tests where the power profiles were static.
 - The regbus tunnel feature has been tested only with limited directed tests where the power profiles were static.
 - The regbus tunnel local host interface is not supported in low power configurations.
 - Rebug tunnel power_domain assignments: NocStudio does not automatically keep power_domain_host of rbm/s instance in sync with rbm/s power_domain and power_domain_host/power_domain of rbm/m. User should take care to ensure all these properties are set the same for regbus tunnel deployments.
 - The host regbus feature is not supported in low power configurations.
- Bridge and host power domains: if left unassigned by the user, NocStudio may assign inappropriate power domains. Users should explicitly specify host and bridge power domains in their configurations.
- QACTIVE idle status indications may be incomplete for host and bridge power domains for AHBLM and SIB aggregated hosts and ports. It may also be incomplete for bridge and host power domains where there is a voltage crossing. However, proper fencing and draining functionality supporting safe power transitions is maintained in all cases.
- Support has not been implemented for:
 - DVFS.
 - UPF power intent format
 - Impacts LP simulation and synthesis with Synopsys tools

6.2 GEMINI LOW POWER SUPPORT

Gemini Low Power configurations have some restrictions. While voltage domain crossings can exist within a link or at the interface between a host and a bridge, Gemini does not currently

support the voltage crossing between the host and bridge for Gemini IP (CCC, DVM, IOCB, LLC) or ACE bridges (ACE, ACE-lite, ACE-lite+DVM).

Gemini Low Power also currently expects that the coherent components are part of auto-wake power domains. If they are added to decode-error power domains, some coherent requests may fail. DVM requests, for instance, cannot handle decode errors.

Gemini Low Power support is an Alpha Release. While there are no known bugs, verification is still in progress.

6.3 ROUTER CHECKER

The router checker has been removed from this release.

6.4 AHB

There could be a deadlock between AHB master bridge and the AHB master if master is waiting for HREADY to be asserted before removing the BUSY command. Workaround: remove BUSY as soon as the next command is available. This will be addressed in the next release.

6.5 PRIORITY ADDRESS MAP

As noted in the Feature Updates section, the Priority Address Map has a potential issue when some agents do not have access to a slave in a foreground range. Instead of getting a decode error when they attempt to access those ranges, they can hit against the background range and send the request to that slave.

6.6 SPYGLASS

Please see the Waiver document about the spyglass waivers.

6.7 USER REG BUS LIMITATIONS

For user reg bus, below are the limitations of the support:

- 1) Transaction size needs to equal the interface size:
 - a. If you have a 32 bit rb native interface, 32 bit user reg bus accesses are supported
 - b. If you have a 64 bit rb native interface, 64 bit user reg bus accesses are supported. 32 bit access are not supported.
- 2) Host errors returned from the rb native interface are not supported.
- 3) Async interface at rb native is not supported.
- 4) Write strobes (byte enables) are not supported. This is similar to what we support for the NOC internal registers.

7 CHANGES TO COMMANDS AND PROPERTIES

7.1 COMMAND CHANGES

Command Name	Comment
add_bridge	New to add bridge after add_host command has been specified
add_sib	New command to add a shared interface bridge
create_async_crossers _between_groups	New command to auto configure async crossing properties based on RTL grouping
del_bridge	New to delete bridge after add_host command has been specified
json_dump	New command to output a JSON structure of NoC
list_sibs	New command to list shared interface bridges within a design
list_vifce_aid_entries	New command that lists the number of AID entries for each virtual interface of a given interface
list_vifce_class	New command that lists virtual interfaces associated with each class value for a given interface
list_vifce_credits	New command that lists number of credits for each virtual interface for a given interface
set_auto_pd_prefix	New command to set prefix to automatically created power domain.
set_column_width	New command to set per column grid cell size
set_row_height	New command to set per row grid cell size
set_vifce_aid_entries	New command to set AID entries for each virtual interface
set_vifce_class	New command to set traffic class for each virtual interface
set_vifce_credits	New command to set number of credits for each virtual interface
show_layers	Command to show specified number of layers in GUI
add_ccc_group	Command syntax has been changed to accommodate hash functions
add_llc_group	Command syntax has been changed to accommodate hash functions
add_cache_group	Command syntax has been changed to accommodate hash functions

7.2 DEFAULT PROPERTY CHANGES

Property Name	Default Value	Comment
archive_project_dir	yes	New property to disable automatic archiving of project directories
axi4_ar_org_id_enb	no	New properties that indicates whether original ID is enabled for read requests from all AXI4/ACEL slave bridges
axi4_aw_org_id_enb	no	
axi4m_prog_addrs_range	no	Property has been deprecated
credit_flop_to_output_ns	0.8	New properties that set default values for the credit return path
credit_pipeline_depth	0	
enable_fine_grain_clock_gating	yes	New property that enables fine grained clock gating withing each link in design
tag_project_name	no	This property will not be supported for Orion and Gemini designs in this release
use_dedicated_regbus_clk	yes	New property that enables/disables the use of a dedicated regbus clock

7.3 MESH PROPERTY CHANGES

Property Name	Default Value	Comment
def_blockage_top_routing_layer	0	New property that indicates the top routing layer in a def file
def_scale	1	New property to control the scaling factor of generated box size in DEF.
enable_detailed_logging	yes	New property, when disabled, will speed up performance simulation runtime
enable_sib_autoconnect	no	New property that indicates if compatible masters can be automatically connected to a shared interface bridge
ipxact_compact_version	no	New property to skip memory map section in

		IPXACT generation. This property is visible only if default property ipxact_enable is set to yes.
--	--	---

7.4 BRIDGE PROPERTY CHANGES

Property Name	Comment
axi4_ar_num_virtual_ifces	New bridge property for supporting virtual AXI interface
axi4_ar_org_id_enb	New prooperty that indicates whether original ID is enabled for read requests from a bridge
axi4_aw_num_virtual_ifces	New bridge property for supporting virtual AXI interface
axi4m_prog_addrs_range	This bridge property has been deprecated
cc_axi4m_speculative_fetch	Support has been added to acel amd aceldm slaves
cc_coherency_connect	New bridge property for coherency connect signals
llc_allocation_class	New property for setting LLC allocation class
rw_full_throughput	Property has been enabled for Gemini configurations

7.5 HOST PROPRERTY CHANGES

Property Name	Comment
llc_waygroup_ram_mode_enable	Bit vector that specifies which of the LLC waygroups work as a RAM

7.6 LINK PROPERTY CHANGES

Property Name	Comment
credit_flop_to_output_ns	New properties to set a link's credit return path
credit_pipeline_depth	
enable_fine_grain_clock_gating	New property to enable / disable fine grained clock gating on a link

domain_crosser_fifo_depth	New properties to set on a link with ILDC (In link domain crossing). Please see NocStudio help menu for usage details.
domain_crosser_output_register	
domain_crosser_pos	
domain_crosser_credit_output_register	New properties to set on a link with ILDC (In link domain crossing). Please see NocStudio help menu for usage details.
post_domain_crosser_credit_pipeline_depth	
post_domain_crosser_pipeline_depth	

7.7 ROUTER PROPERTY CHANGES

None.

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