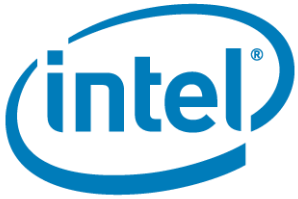

CFG IP Integration Specification Addendum – Trace Probe

Version: 19.07L

Revision: 0.0

Intel Confidential

CFG AMBA IP Integration Specification: Trace Probe Addendum

About this document

This document describes the architecture of the CFG AMBA Trace Probe. This includes details of the IP components and instructions on how to add the trace probing feature to CFG AMBA bridges and how to configure and use it.

Audience

This document is intended for users of NocStudio:

- NoC architects, designers and verification engineers
- SoC architects, designers and verification engineers

Prerequisites

Before proceeding, you should generally understand:

- Basics of Network on Chip technology
- AMBA 4 specification and ARM CoreSight architecture

Related documents

The following documents can be used as a reference to this document.

- CFG NocStudio Orion | Gemini User Manual
- CFG Orion | Gemini IP Integration Specification
- CFG Orion | Gemini Technical Reference Manual

Customer support

For technical support about this product and general information, contact CFG Support.

Revision History

Revision	Date	Updates
0.0	Jul 19, 2019	Initial Version

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1 TRACE PROBE OVERVIEW

NocStudio provides a bridge property that allows the user to add trace probing functionality to the ACE core of any bridge of the NoC. The trace probe logic captures address and control information from any AR/R, AW/B or AC/CR channels that are in use within the bridge and encodes it into a trace data stream that is delivered out of a dedicated ATB interface.

The trace probe, together with supporting logic in the CFG NoC implements an ARM CoreSight reusable component that may be integrated into a standard CoreSight debug implementation on an SoC.

1.1 LIMITATIONS

- The trace probe does not implement topology detection features, including topology detection registers.

1.2 TRACE PROBE CONFIGURATION

A trace probe is added to a bridge in NocStudio by setting the *trace_enable* bridge property to "yes."

```
bridge_prop h0/s trace_enable yes
```

Once this is done, an additional bridge property, *trace_clock_domain*, and a number of trace related interface properties become visible for many or all of the host interfaces as well as the *atbm* (ATB transport interface). *Trace_clock_domain* may be set to any valid clock domain in the NoC.

1.2.1 Configuring Traced Interfaces

Each host interface of the bridge that is to be sampled by the trace probe must be enabled for tracing by setting its *trace_enable* interface property.

```
ifce_prop h0/s.ar.in trace_enable yes
```

The following ACE bridge interfaces may be enabled for tracing:

- Request channels: AR, AWW, AC
- Response channels: R, B, CRCD

Within each traced interface the specific fields that may be captured into the trace stream is configured using the *trace_req_capture_mask* or *trace_resp_capture_mask* as appropriate. These are

bit masks where a 1 in a bit position indicates that the corresponding field is included, and a 0 indicates it is to be excluded.

One other interface property, *trace_fifo_depth*, applies to each traced interface. This sets the depth of the trace capture FIFO that exists within each interface's trace sampling logic, and it is described in further detail in section 2.2. Figure 1 depicts NocStudio configuration GUI pane and related hardware structure.

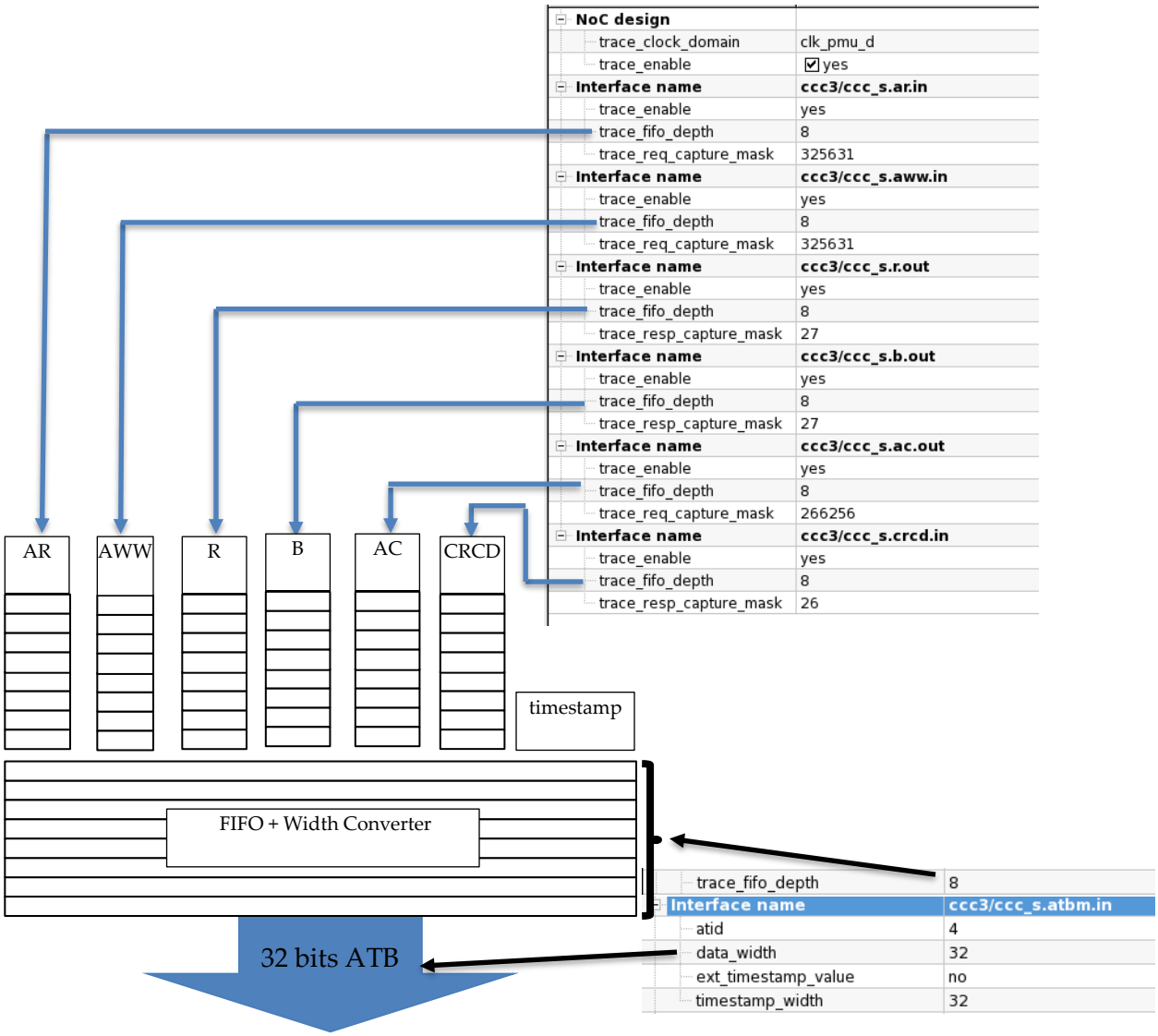

Figure 1 Trace Probe FIFO Configurability

1.1.1.1 Request Channel Capture Mask

The table below shows the encoding of the *trace_req_capture_mask* which covers all the fields that may be configured for trace capture for the AR, AWW and AC channels. Note that the capture

mask represents a superset of fields across these channels, and some fields do not apply to all these channels. NocStudio constrains allowed values for the capture mask based on the type of bridge.

Bit #	Field	Notes
0	AxID	AR/AWW only
1	AxLEN	AR/AWW only
2	AxSIZE	AR/AWW only
3	AxBURST	AR/AWW only
4	AxPROT	
5	AxLOCK	AR/AWW only
6	AxCACHE	AR/AWW only
7	AxREGION	AR/AWW only
8	AxQOS	AR/AWW only
9	AxOrigid	AR/AWW only
10	AxLogid	AR/AWW only
11	AxUSER	AR/AWW only
12	AxSNOOP	(ACE only)
13	AxDOMAIN	AR/AWW only (ACE only)
14	AxBAR	AR/AWW only (ACE only)
15	AxMstrid	AR/AWW only
16	ACcrtid	AC only
17	ACslvid	AC only
18	Address	

Table 1 *Request Channel Capture Mask Bit # to Field Mapping*

Note: for AWW channel, the AxSNOOP field is comprised of {AWUNIQUE, AWSNOOP[2:0]}.

The sample size for request channels is limited to 92 bits in total width, which possibly includes some amount of padding to nibble boundaries for the STP protocol. The address field, if captured, is separately padded by up to 3 extra bits. The rest of the fields that are captured are

packed together, and the aggregate is also padded by up to 3 extra bits. The worstcase padding overhead is 6 bits.

NocStudio executes the following check when *gen_ip* is executed, and it will abort with an error message that enumerates the calculated size with the listing of all the fields activated by the capture mask and their specific sizes. The user must then update the *trace_req_capture_mask* to meet this requirement.

sample_size = cm[18] & (addr_width + padding) + cm[17:0] & (field_widths + padding) <= 92

An example to configure 19 bits request capture mask from bit vector to hex value in NocStudio is illustrated in Figure 2.

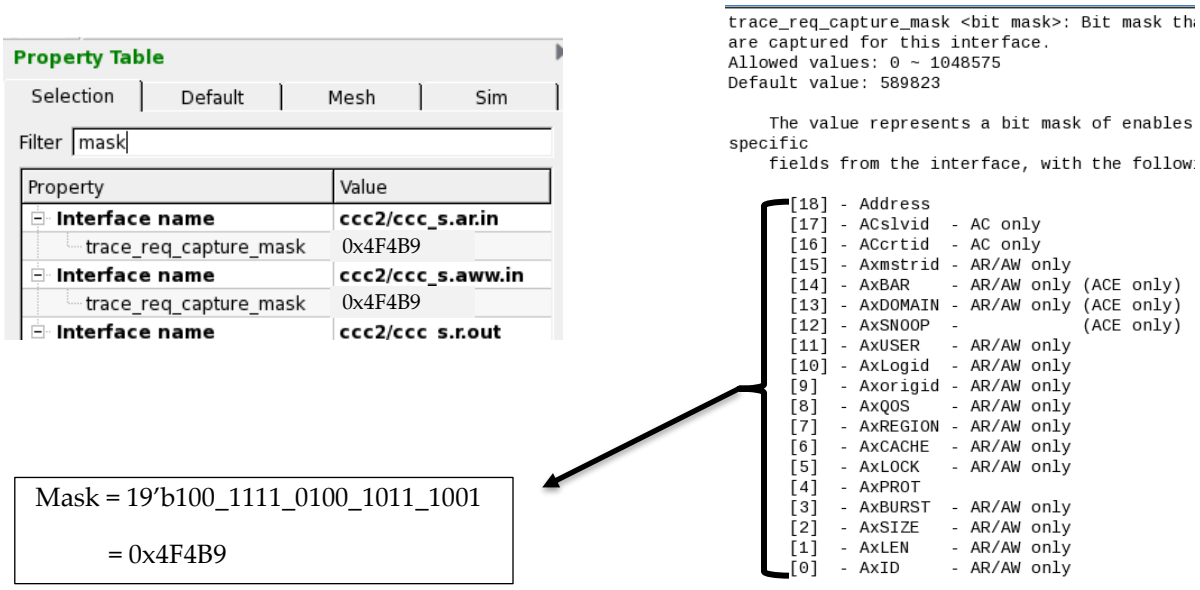

Figure 2 Request_Capture_Mask Example

1.1.1.2 Response Channel Capture Mask

The table below shows the encoding of the *trace_resp_capture_mask* which covers all the fields that may be configured for trace capture for the R, B and CR channels. Note that the capture mask represents a superset of fields across these channels, and some fields do not apply to all of these channels. NocStudio constrains allowed values for the capture mask based on the type of bridge.

Bit #	Field	Notes
0	xID	R/B only
1	xRESP	
2	xUSER	R/B only

3	xCRtid	CR only
4	xSlvid/xMstrid	

***Table 2** Response Channel Capture Mask Bit # to Field Mapping*

The sample size for request channels is limited to 28 bits in total width, which possibly includes some amount of padding to nibble boundaries for the STP protocol. However, it may exceed this width if the timestamp width is reduced from its maximum size of 28 bits. The fields that are captured are packed together, and the aggregate may be padded by up to 3 extra bits to reach a nibble boundary.

NocStudio executes a check when *gen_ip* is executed, and it will abort with an error message that enumerates the calculated size with the listing of all the fields activated by the capture mask and their specific sizes. The calculation accounts for extra room that may be available due to a reduced width timestamp. The formula is complex as it must account for details of STP encoding such that there is not a simple linear relationship between timestamp width and extra width available for the captured sample. A high-level representation of this calculation follows:

sample_size = cm[4:0] & (field_widths + nibble_padding) <= 28

else

sample_size = cm[4:0] & (field_widths + nibble_padding) + ts_width + STP_overhead <= 64

1.2.2 ATB Interface Configuration

The following interface properties are available for configuring the ATB interface of the trace probe:

- *atid*: sets the reset value of the CS_TRACE_CFG_STS.ID field, which holds the value that is transmitted over the ATID pins of the ATB interface. NocStudio requires this to be set to a unique value relative to the same setting for any other trace enabled bridges in the NoC, though it may be changed by writing this register field in operation (and there is no logic that enforces uniqueness).
- *data_width*: sets the width of the ATDATA bus, legal values being 32, 64 or 128.
- *timestamp_width*: sets the width of the timestamp field that may be added to capture trace samples. It also sets the width of the TSVALUE bus if *ext_timestamp_value* is set to "yes." Legal values are integer multiples of 4, maximum of 28. The maximum width is subject to restriction as described above in section 0.
- *ext_timestamp_value*: enables TSVALUE interface to provide the timestamp value. Default is "no," in which case the timestamp value is derived from an internal counter running at in the bridge's clock domain (not *trace_clock_domain*).

- *atb_fifo_depth*: sets ATB FIFO depth for asynchronous configurations (described in detail in section 2.1.1).

1.3 TRACE PROBE CONFIGURATION REGISTERS

As a CoreSight reusable component, the CFG trace probe implements the standard 4KB block of CoreSight registers as required of all CoreSight components. This includes a set of standard CoreSight registers as well as configuration registers that are specific to the implementation of the trace probe. Access to the trace probe configuration registers is provided via regbus.

The configuration registers have the following properties:

- They are secured, which means they may only be accessed via secure transactions (e.g., AXI AxPROT[1] == 0).
- They are only present in bridges that have trace enabled.
- They occupy a single CoreSight 4KB space at offset 0x2000-0x2FFF within the bridge's 16KB regbus address space.
- Each register is 32-bits wide (per CoreSight specs), aligned to 32-bit boundaries.
    - The registers are accessible with either 32-bit or 64-bit wide regbus transactions, in the latter case as pairs via 64-bit aligned 64-bit regbus transactions.
- Unimplemented locations within the 4KB address space respond without error to transactions (as required by CoreSight) behaving as read-only locations that return 0.

1.3.1 Connecting to CoreSight Debug APB

To connect the CFG trace probe configuration registers to the CoreSight Debug APB, users should use the CFG regbus tunnel, which provides an APB interface to regbus. Users must ensure that the CoreSight DAP that drives the APB interface issues secure transactions when targeting the regbus tunnel APB interface.

1.3.2 Programming Register Base Address into CoreSight ROM Table

Part of a CoreSight deployment is a ROM table (or set of ROM tables) that enumerates the base address of the CoreSight register space for each component in the deployment. To determine the base address of each CFG trace probe in the NoC, the user may refer to any of several files generated by NocStudio that list the specific addresses of the regbus registers and search for the address of the CS_TRACE_CFG_STS register, which is at base (0x0 offset) of the CoreSight register block of the trace probe.

References for regbus addresses include:

- noc_reference_manual.html

- noc_registers.csv
- noc_soc_ip.xml (IPXACT)

1.4 TRACE DATA FORMAT

Each interface trace probe encodes the captured trace samples into a data stream using MIPI STP v2.2 protocol. STP protocol is nibble based, and it provides standard opcodes for packing data, carrying timestamp and other control information, and multiplexing data from multiple channels. The stream from each interface is multiplexed by an arbiter that packs the aggregated stream into the byte-oriented ATB transport format that is transmitted out of the ATB interface.

CFG provides a utility program that can decode the ATB data and the MIPI STP encoded data stream within it to extract the trace samples.

2 PHYSICAL INTEGRATION

Bridges that are enabled for tracing will bring out an ATB master (TX) interface as well as some other trace related interfaces. These interfaces are exposed and the top-level of the NoC (ns_soc_ip.v), where they all are given a prefix of "<bridge_name>_ATB_."

Following are the interfaces signals that provide the ATB transport of the trace data stream.

Signal	Direction	Width	Description
ATCLK	input	1	Clock input for ATB interface. Interface operates synchronously w/respect to this clock.
ATBYTES	output	$\log_2$(*atb_data_width*) - 4	Number of valid bytes in ATDATA.
ATDATA	output	*atb_data_width*	Trace data.
ATID	output	7	ID that uniquely identifies source of trace.
ATREADY	input	1	Downstream ATB slave is ready to accept data.
ATVALID	output	1	Transfer valid this cycle.
AFVALID	input	1	Flush request.
AFREADY	output	1	Flush acknowledgement.
SYNCREQ	input	1	Synchronization request.

Table 3 *ATB Interface Signals*

There are some additional interface signals that are added to support tracing.

Signal	Direction	Width	Description
TSVALUE	input	*timestamp_width*	External timestamp value, encoded as natural binary number. Synchronous to noc_clk.
HWEVENTS	input	2	CTI inputs.
TRIGOUT	output	2	CTI outputs.

ASYNCOUT	output	1	CTI output, asserted for one cycle when ASYNC-VERSION goes out on ATB interface (see STM-500 TRM p A-12).
DBGEN	input	1	Invasive debug enable. Synchronous to ATCLK.
NIDEN	input	1	Non-invasive debug enable. Synchronous to ATCLK.
SPIDEN	input	1	Secure invasive debug enable. Synchronous to ATCLK.
SPNIDEN	Input	1	Secure non-invasive debug enable. Synchronous to dbg_ATCLK.

***Table 4** Other Trace-Related Signals*

2.1 CLOCKING

Trace capture happens within the core of the bridge, operating in the clock domain specified by the bridge property *clock_domain*. Internally in the design this is *noc_clk.* The ATB interface runs off of ATCLK, and the clock domain for it is specified with the bridge property *trace_clock_domain.* ATCLK may be synchronous or asynchronous with respect to *noc_clk.* NocStudio automatically determines the relationship, and if it is asynchronous, an additional clock crossing FIFO structure, the "ATB FIFO," is inferred in the design.

2.1.1 Configuring the ATB FIFO

The ATB FIFO sits beyond the trace probe arbiter which is clocked by *noc_clk,* arbitrating and multiplexing the trace data from all the independent channels that are being traced into the ATB interface. It is only present if ATCLK is asynchronous with respect to *noc_clk*, and it provides a clean clock crossing between the arbiter and the ATB interface pins. NocStudio calculates a minimum FIFO depth that is required to sustain full throughput on the ATB interface, which is used to configure the ATB FIFO.

NocStudio provides an *atb_fifo_depth* interface property for the *atbm* interface, which allows the user to increase the depth of this FIFO over the minimum depth that NocStudio calculates. This is useful when there is a significant bandwidth mismatch due to both clock and width differences between the trace capture logic and the ATB interface. In cases where the trace bandwidth can exceed the capacity of the ATB interface and/or downstream ATB infrastructure, it may be

beneficial to increase the depth of the ATB FIFO to provide local buffer to capture and hold bursts of host interface activity.

Note if *atb_fifo_depth* is set to a value that is less than the minimum depth calculated by NocStudio, the ATB will be sized to the NocStudio calculated depth. I.e., the ATB FIFO depth is the maximum of NocStudio calculate depth and the *atb_fifo_depth* setting.

Note also that *atb_fifo_depth* has no effect in the generated IP if ATCLK is synchronous with *noc_clk* as no ATB FIFO will be present in the design.

2.2 Configuring Host Interface Probe FIFOs

Each active host interface of the bridge that has been configured for tracing (by setting the *trace_enable* interface property) has dedicated sampling logic that includes a FIFO for storing captured samples. The depth of this FIFO may be configured via the *trace_fifo_depth* interface property.

The width of this FIFO is 136 bits for request channels: AR, AW and AC; the width is 71 bits for response channels: R, B and CR. The actual trace sample size varies based on both static factors, such as configuration choices of which fields to include in the trace sample, and dynamic factors, such as whether or not timestamping is enabled, but in any case, the sample width may never exceed the FIFO row width.

Because the channels operate independently, there will generally be cycles where multiple interfaces are active simultaneously, producing sample data at the same time as one another. Since the trace probe arbiter can only accept data from one interface probe at a time, local storage must be provided to hold the data until it is accepted by the arbiter. If it is anticipated that there may be extended periods during trace capture where the aggregate bandwidth of the trace stream across all interfaces exceeds the bandwidth that can be accepted through the arbiter, it may be desirable to increase the depth of these FIFOs. Conversely, there may be deployment scenarios where it is useful to reduce the size of these FIFOs, particularly area sensitive deployments and/or where the transaction pattern is not so demanding.

2.3 TSVALUE and Timestamp Width

The TSVALUE interface is used when timestamps are to originate from a source that is external to the bridge. This choice is controlled via the NocStudio *atbm* interface property *ext_timestamp_value,* which must be set to "yes" (default is "no") to enable this interface. If *ext_timestamp_value* is set to "no," the TSVALUE interface is tied off internally and it will not appear in the top-level NoC interface (ns_soc_ip.v).

The TSVALUE interface is synchronous to the bridge *clock_domain* (*noc_clk*). Clock crossing, width conversions, and any timestamp resynchronization must be handled by logic outside the NoC. ARM provides standard CoreSight components that implement these functions.

The width TSVALUE is determined by the width of the timestamp that may be appended to trace samples in the trace stream, which is controlled by the NocStudio *atbm* interface property *timestamp_width*.

2.4 THE AUTHENTICATION INTERFACE

ARM CoreSight architecture defines the Authentication Interface, which is implemented in the CFG Trace Probe. It is comprised of the signals DBGEN, NIDEN, SPIDEN and SPNIDEN. ARM documentation, including the CoreSight Architecture Specification, should be consulted for a full description.

The Authentication Interface controls access to trace and debug functionality. It defines secure debug and invasive debug, and it controls whether secure debug and/or invasive debug is allowed, and it controls whether any debug at all is allowed. The state of the 4 signals of the Authentication Interface determines the type of debug allowed by the CFG trace probe, superseding any CoreSight register controls.

The ARM CoreSight Architecture Specification defines four non-exclusive allowed debug levels that are determined from a decoding of the Authentication Interface, which is implemented in the trace probe. These are:

Level	Description	Authentication Signal Decode
NSID	Non-secure Invasive debug (Note: CFG trade probe does not implement this level.)	DBGEN
NSNID	Non-secure Non-invasive debug	DBGEN | NIDEN
SID	Secure Invasive debug	DBGEN & SPIDEN
SNID	Secure Non-invasive debug	((SPIDEN & DBGEN) | SPNIDEN) & (DBGEN | NIDEN)

***Table 5** Authentication Interface Decode into Debug Levels*

CS_AUTHSTATUS, a standard CoreSight register, reports the debug level status combined with indication of whether or not a particular level is implemented in the component. The value returned for the NSID field by the trace probe is 2'b00, indicating this level is not implemented. The other 3 levels are implemented by the trace probe.

The minimum level required to do any tracing is NSNID. If this level is not active, the trace probe is forced inactive, as if the CS_TRACE_CFG_STS.EN bit were set to 0 (regardless of its actual

state). Other levels, SNID and SID, are required to enable secure and invasive debug features, described further below.

Note, the Authentication Interface is expected to be static during trace probe operation. Behavior is undefined if the state of any of the Authentication Interface signals changes while the probe is active.

2.4.1 Secure Debug

Secure debug is allowed if either SNID or SID is active. When secure debug is not allowed, secure transactions (AxPROT[1] == 0) are not captured. The effect is the same as if trace filters were programmed to exclude all transactions with AxPROT[1] == 0.

2.4.2 Invasive Debug

Invasive debug, in the context of trace probe operation, allows the interface probes to backpressure (aka stall) the mission mode interface being probed when the trace FIFO would otherwise overflow. This avoids losing trace samples with the trade-off of perturbing the mission mode behavior of the system. It is only allowed when SID is active.

Invasive debug is further controlled by the <Ifce>_V bits of the CS_TRACE_CFG_STS register. Each interface must be separately enabled by setting the corresponding bit to 1 (reset default value is 0).

Normal (non-invasive) debug behavior is that the trace samples are dropped when the FIFO overflows. The drops are counted and reported in the trace data stream (the count saturates above 63 consecutive drops, resetting back to 0 when the next captured transaction).

3 USING THE TRACE PROBE

The CFG trace probe, as a CoreSight reusable component, is configured via register transactions over the Debug APB, which connects to the CFG regbus though the APB port of the regbus tunnel.

3.1 BASIC OPERATION

The trace probe comes out of reset in an idle/inactive state. This is indicated by the CS_TRACE_CFG_STS.BSY bit reading 0. In this state, it is permissible to update any of the probe's CoreSight configuration registers. While it is always permissible to read the CoreSight registers (subject to the restriction that only secure transactions are allowed), it is not safe to write to any of the registers except CS_TRACE_CFG_STS, and then only to change the EN bit (global trace enable), from 1 to 0. Undefined behavior may result when other writes occur while the CS_TRACE_CFG_STS.BSY bit reads 1.

The following sequence should be followed to configure the trace probe and to enable it to generate a trace data stream. This sequence presumes the Authentication Interface is driven to enable the debug level necessary to perform the desired tracing operations.

1. Power on the DUT, including bringing the bridge power domain into Q_RUN state.
    a. The trace probe comes up in an idle/inactive state (CS_TRACE_CFG_STS.EN == 0).
2. Configure the probe for the desired mode of operation, including any transaction filtering (via Debug APB access to CoreSight registers).
3. Enable the probe: put it in the busy/active state by writing to set CS_TRACE_CFG_STS.EN = 1.
    a. The trace probe is active, generating trace data according to its configuration and transporting out of the ATB interface. CS_TRACE_CFG_STS.BSY reads as 1.
4. Disable the probe when desired testing scenario has been traced: write to set CS_TRACE_CFG_STS.EN = 0.
    a. The trace probe gracefully transitions to idle/inactive state by halting trace sampling at all interfaces, flushing captured data though the interface trace FIFOs and the ATB trace FIFO (if present), and waiting until all trace data has drained before deasserting CS_TRACE_CFG_STS.BSY.
5. Poll CS_TRACE_CFG_STS.BSY to wait until it transitions from 1 to 0 before returning to step 2 to repeat the process.

3.2 FILTERING

The trace probe implements a set of comparators in the request channel interface tracing logic that can be configured and used to control which transactions are included in the trace stream. It is important to note that all fields that are active for an interface are available to these comparators, so that filtering may be done based on field values for fields that may not be included in the trace sample. In other words, the trace comparators are fully independent of the *trace_req_capture_mask.*

3.2.1 Channel Comparator Resources

Each of the request channel's trace probe logic contains a set of comparators for address and control fields. They are organized in a specific way described below that allows sharing of configuration register controls, but they all have a common implementation, where a mask register (CS_*_MATCH_*_MASK_*) is ANDed with the incoming transaction data to zero out bits that are don't cares, and the resulting value is compared for equality against a corresponding value register (CS_*_MATCH_*_VAL_*).

```
hit = ((incoming_data & mask) == value);
```

Note that the user must zero out bits in the value register that correspond to zero values in the mask register.

Following is a list of comparator resources…

- Address: 3 copies, AxADDR width, in AR, AWW and AC channels
  - incoming_data: AxADDR
  - Register Names:
    CS_ADDR_MATCH_HI_MASK_<0|1|2>
    CS_ADDR_MATCH_LO_MASK_<0|1|2>
    CS_ADDR_MATCH_VAL_<0|1|2>
    CS_ADDR_MATCH_LO_VAL_<0|1|2>
- AC Control: 2 copies, width of incoming data (max 15), in AR, AWW and AC channels
  - incoming_data:{AxAGNid[7:0],AxSNOOP[3:0], AxPROT[2:0]}
    - Note: for AWW, use {AWUNIQUE, AWSNOOP[2:0]}
    - Note: AxAGNid only applies to AC channel, AR and AWW just PROT and SNOOP.
  - Register Names:
    CS_ACCTRL_MATCH_MASK_<0|1>
    CS_ACCTRL_MATCH_VAL_<0|1>
- Control: 2 copies, width of incoming data (max 26), in AR and AWW

    - incoming_data: {AxQOS[3:0], AxREGION[3:0], AxCACHE[3:0], AxLOCK, AxBURST[1:0], AxSIZE[2:0], AxLEN[7:0]}
    - Register Names:
      CS_CTRL_MATCH_MASK_<0|1>
      CS_CTRL_MATCH_VAL_<0|1>
- AxID: 1 copy, width of AxID upto 32 lsbs, in AR and AW
    - incoming_data: AxID[31:0] (or smaller)
    - Register Names: CS_ID_MATCH_MASK, CS_ID_MATCH_VAL
- Origid, Logid, Mstrid: 1 copy, width of these fields, in AR and AW
    - incoming_data: {AxOrigid[7:0], AxLogid[7:0], AxMstrid[7:0]}
        - Note: for master bridges, Axmstrid is unused.
    - Register Names: CS_LOM_ID_MATCH_MASK, CS_LOM_ID_MATCH_VAL

For all these comparators, the logic may be generated so that bits of incoming data that don't exist (because fields are narrower or unused in that particular bridge instance) are completely left out of the logic, and the corresponding bits from the control registers may read-only as 0.

The configuration registers are shared across all interfaces, but each interface's trace probe logic has its own dedicated comparator resources that are simultaneously active.

3.2.2 Match Signals

A set of registers controls logic within each request channel that selects which comparator outputs to use to generate 3 different match signals. As opposed to the comparator controls, which are shared across all 3 request channels, each channel gets its own match signal control register.

The match signal control registers are: CS_MATCH_AR_CFG, CS_MATCH_AW_CFG and CS_MATCH_AC_CFG.

There are 3 sets of 9 control bits within these registers, 1 for each of the 3 match signals. The bits are:

[8] M0_LOM_ID	selects Origid/Logid/Mstrid comparator output
[7] M0_ID	selects AxID output
[6] M0_CTRL1	selects control comparator 1 output
[5] M0_CTRL0	selects control comparator 0 output
[4] M0_ACCTRL1	selects AC control comparator 1 output
[3] M0_ACCTRL0	selects AC control comparator 0 output
[2] M0_ADDR2	selects ADDR comparator 2 output

[1] M0_ADDR1 selects ADDR comparator 1 output

[0] M0_ADDR0 selects ADDR comparator 0 output

Bit's 8:5 are UNUSED for AC channel (they exist in registers as read-only 0's). Bits 17:9 repeat this set of bits for match signal 1, and bits 26:18 are for match signal 2.

The function for the match signal is:

match0 = (~M0_LOM_ID | hit_lom) & (~M0_ID | hit_axid) & (~M0_CTRL1 | hit_ctrl1) & (~M0_CTRL0 & hit_ctrl0) & (~M0_ACCTRL1 | hit_acctrl1) & (~M0_ACCTRL0 | hit_acctrl0) & (~M0_ADDR2 & hit_addr2) & (~M0_ADDR1 & hit_addr1) & (~M0_ADDR0 & hit_addr0);

3.2.3 Trace Filter Control

The register CS_TRACE_FILT_CTRL configures how the above match signals are used to include or exclude transactions. It also configures whether the address lookup table match signals are used to control inclusion (master bridges only). This register contains bit fields for each of the 3 request channels AR, AWW and AC.

Following a description of the fields of the CS_TRACE_FILT_CTRL register…

Field Name	Bit Range	RW	Reset Value	Description
AC_EXC_ONLY	30	RW	0x1	1: Include all AC transactions, only apply exclusion filters. 0: Apply both inclusion and exclusion AC filters.
AW_EXC_ONLY	29	RW	0x1	1: Include all AW transactions, only apply exclusion filters and AW_ERR_INC. 0: Apply both inclusion and exclusion AW filters.
AR_EXC_ONLY	28	RW	0x1	1: Include all AR transactions, only apply exclusion filters and AR_ERR_INC. 0: Apply both inclusion and exclusion AR filters.
AW_ERR_INC	27	RW	0x1	1: For master bridges only: include AW transactions that miss the address table or generate other errors in address decode, even if they are otherwise excluded. This bit is only settable in master bridges. 0: Do not force inclusion of AW error transactions.

AW_TBL_EXC	26	RW	0x1	1: For master bridges only: exclude AW transactions do NOT hit an address table entry enabled in the CS_TBL_MATCH registers. This bit is only settable in master bridges. 0: Do not exclude any transactions based on AW table lookup results.
AR_ERR_INC	25	RW	0x1	1: For master bridges only: include AR transactions that miss the address table or generate other errors in address decode, even if they are otherwise excluded. This bit is only settable in master bridges. 0: Do not force inclusion of AR error transactions.
AR_TBL_EXC	24	RW	0x1	1: For master bridges only: exclude AR transactions do NOT hit an address table entry enabled in the CS_TBL_MATCH registers. This bit is only settable in master bridges. 0: Do not exclude any transactions based on AR table lookup results.
RSVD_23	23	R	0x0	Reserved for future use. SW should write and read 0.
AC_EXC	22:20	RW	0x0	Bit mask where a 1 selects the corresponding AC channel match signal (2-0) to exclude AC transactions.
RSVD_19	19	R	0x0	Reserved for future use. SW should write and read 0.
AC_INC	18:16	RW	0x0	Bit mask where a 1 selects the corresponding AC channel match signal (2-0) to include AC transactions.
RSVD_15	15	R	0x0	Reserved for future use. SW should write and read 0.
AW_EXC	14:12	RW	0x0	Bit mask where a 1 selects the corresponding AW channel match signal (2-0) to exclude AW transactions.

RSVD_11	11	R	0x0	Reserved for future use. SW should write and read 0.
AW_INC	10:8	RW	0x0	Bit mask where a 1 selects the corresponding AW channel match signal (2-0) to include AW transactions.
RSVD_7	7	R	0x0	Reserved for future use. SW should write and read 0.
AR_EXC	6:4	RW	0x0	Bit mask where a 1 selects the corresponding AR channel match signal (2-0) to exclude AR transactions.
RSVD_3	3	R	0x0	Reserved for future use. SW should write and read 0.
AR_INC	2:0	RW	0x0	Bit mask where a 1 selects the corresponding AR channel match signal (2-0) to include AR transactions.

Table 6 *CS_TRACE_FILT_CTRL fields*

The following function describes how the fields in the CS_TRACE_FILT_CTRL register control whether or not a given trace sample will be included in the trace stream for the AR channel in a master bridge (subject to Authentication Interface control).

```
sample_incl = (tbl_err & AR_ERR_INC) |
              (~(|(match_ar[2:0] & AR_EXC[2:0]) | (~tbl_match & AR_TBL_EXC)) &
              (|(match_ar[2:0] & AR_INC[2:0]) | AR_EXC_ONLY));
```

Note that if AR_INC[2:0] == 3'b000, then AR_EXC_ONLY must be set or only tbl_err transactions, subject to AR_ERR_INC, will be included.

The function for AWW channel is identical, swapping in AWW channel signals and register fields.

For the AC channel of a master bridge, there is no address look up table and no corresponding AC_ERR_INC and AC_TBL_EXC fields in the control register, so the function looks like the following…

```
sample_incl = ~(|(match_ac[2:0] & AC_EXC[2:0]) &
              (|(match_ac[2:0] & AC_INC[2:0]) | AC_EXC_ONLY));
```

For slave bridges, there is no address look up table for any of the channels, so all the sample include functions look like the master bridge AC function, and the A[RW]_ERR_INC and A[RW]_TBL_EXC fields are read-only as 0.

4 PROGRAMMERS MODEL

All Trace Probe registers have the CS_ prefix for easy reference. For Orion based designs, please ignore all reference to AMBA ACE4 coherency protocol channels and fields.

Table 7 Trace Probe Register Summary

Offset	Name	Short Description
0x2000	CS_TRACE_CFG_STS	Trace Probe Configuration Register
0x2004	CS_TRACE_TS_CFG	Timestamp Configuration Register
0x200c	CS_TRACE_FILT_CTRL	Trace Filtering Control Register
0x2010	CS_MATCH_AR_CFG	Match signal selector for AR channel
0x2014	CS_MATCH_AW_CFG	Match signal selector for AW channel
0x2018	CS_MATCH_AC_CFG	Match signal selector for AC channel
0x2040	CS_TR_FIELDS_AR_L0	Trace Fields Lower Set for AR Format 0
0x2044	CS_TR_FIELDS_AR_U0	Trace Fields Upper Set for AR Format 0
0x2048	CS_TR_FIELDS_AR_L1	Trace Fields Lower Set for AR Format 1
0x204c	CS_TR_FIELDS_AR_U1	Trace Fields Upper Set for AR Format 1
0x2050	CS_TR_FIELDS_AW_L0	Trace Fields Lower Set for AW Format 0
0x2054	CS_TR_FIELDS_AW_U0	Trace Fields Upper Set for AW Format 0
0x2058	CS_TR_FIELDS_AW_L1	Trace Fields Lower Set for AW Format 1
0x205c	CS_TR_FIELDS_AW_U1	Trace Fields Upper Set for AW Format 1
0x2060	CS_TR_FIELDS_AC_0	Trace Fields for AC Format 0
0x2064	CS_TR_FIELDS_AC_1	Trace Fields for AC Format 1
0x2068	CS_TR_FIELDS_R_0	Trace Fields for R Format 0
0x206c	CS_TR_FIELDS_R_1	Trace Fields for R Format 1
0x2070	CS_TR_FIELDS_B_0	Trace Fields for B Format 0

0x2074	CS_TR_FIELDS_B_1	Trace Fields for R Format 1
0x2078	CS_TR_FIELDS_CR_0	Trace Fields for CR Format 0
0x207c	CS_TR_FIELDS_CR_1	Trace Fields for CR Format 1
0x2080	CS_ADDR_MATCH_LO_VAL_0	Address comparator 0 match value low
0x2084	CS_ADDR_MATCH_HI_VAL_0	Address comparator 0 match value high
0x2088	CS_ADDR_MATCH_LO_MASK_0	Address comparator 0 mask low
0x208c	CS_ADDR_MATCH_HI_MASK_0	Address comparator 0 mask high
0x2090	CS_ADDR_MATCH_LO_VAL_1	Address comparator 1 match value low
0x2094	CS_ADDR_MATCH_HI_VAL_1	Address comparator 1 match value high
0x2098	CS_ADDR_MATCH_LO_MASK_1	Address comparator 1 mask low
0x209c	CS_ADDR_MATCH_HI_MASK_1	Address comparator 1 mask high
0x20a0	CS_ADDR_MATCH_LO_VAL_2	Address comparator 2 match value low
0x20a4	CS_ADDR_MATCH_HI_VAL_2	Address comparator 2 match value high
0x20a8	CS_ADDR_MATCH_LO_MASK_2	Address comparator 2 mask low
0x20ac	CS_ADDR_MATCH_HI_MASK_2	Address comparator 2 mask high
0x20c0	CS_ACCTRL_MATCH_VAL_0	ACE control comparator 0 match value
0x20c4	CS_ACCTRL_MATCH_MASK_0	ACE control comparator 0 mask
0x20c8	CS_ACCTRL_MATCH_VAL_1	ACE control comparator 1 match value
0x20cc	CS_ACCTRL_MATCH_MASK_1	ACE control comparator 1 mask
0x20d0	CS_CTRL_MATCH_VAL_0	Control comparator 0 match value
0x20d4	CS_CTRL_MATCH_MASK_0	Control comparator 0 mask
0x20d8	CS_CTRL_MATCH_VAL_1	Control comparator 1 match value
0x20dc	CS_CTRL_MATCH_MASK_1	Control comparator 1 mask
0x20e0	CS_ID_MATCH_VAL	ID comparator match value
0x20e4	CS_ID_MATCH_MASK	ID comparator mask

0x20e8	CS_LOM_ID_MATCH_VAL	logid/orgid/mstrid comparator match value
0x20ec	CS_LOM_ID_MATCH_MASK	logid/orgid/mstrid comparator mask
0x2100	CS_TBL_MATCH_0	Trace Address Table Match Register 0
0x2104	CS_TBL_MATCH_1	Trace Address Table Match Register 1
0x2108	CS_TBL_MATCH_2	Trace Address Table Match Register 0
0x210c	CS_TBL_MATCH_3	Trace Address Table Match Register 0
0x2110	CS_TBL_MATCH_4	Trace Address Table Match Register 0
0x2114	CS_TBL_MATCH_5	Trace Address Table Match Register 0
0x2118	CS_TBL_MATCH_6	Trace Address Table Match Register 0
0x211c	CS_TBL_MATCH_7	Trace Address Table Match Register 0
0x2e8c	CS_TSFREQR	Timestamp Frequency Register
0x2fb8	CS_AUTHSTATUS	CoreSight Authentication Status Register
0x2fbc	CS_DEVARCH	CoreSight Device Architecture Register
0x2fc8	CS_DEVID	CoreSight Device Configuration Register
0x2fcc	CS_DEVTYPE	CoreSight Device Type Identifier Register
0x2fd0	CS_PIDR4	CoreSight Peripheral ID Register 4
0x2fd4	CS_PIDR5	CoreSight Peripheral ID Register 5
0x2fd8	CS_PIDR6	CoreSight Peripheral ID Register 6
0x2fdc	CS_PIDR7	CoreSight Peripheral ID Register 7
0x2fe0	CS_PIDR0	CoreSight Peripheral ID Register 0
0x2fe4	CS_PIDR1	CoreSight Peripheral ID Register 1
0x2fe8	CS_PIDR2	CoreSight Peripheral ID Register 2
0x2fec	CS_PIDR3	CoreSight Peripheral ID Register 3
0x2ff0	CS_CIDR0	CoreSight Component ID Register 0
0x2ff4	CS_CIDR1	CoreSight Component ID Register 1

0x2ff8	CS_CIDR2	CoreSight Component ID Register 2
0x2ffc	CS_CIDR3	CoreSight Component ID Register 3

4.1 GLOBAL REGISTERS

Please refer to noc_registers.csv for design specific (DS) reset value.

4.1.1 Register: CS_TRACE_CFG_STS

Name: Trace Probe Configuration Register
Offset: 0x2000
Description: This register provides basic configuration settings and status for the trace probe.

Table 8 CS_TRACE_CFG_STS

Field Name	Bit Range	RW	Reset Value	Description
RSVD_31_30	31:30	R	0x0	Reserved for future use. SW should write and read 0.
CR_F	29	RW	0x0	1: Selects format set 1 for CR channel captured trace information. 0: Selects format set 0 for CR channel captured trace information.
AC_F	28	RW	0x0	1: Selects format set 1 for AC channel captured trace information. 0: Selects format set 0 for AC channel captured trace information.
B_F	27	RW	0x0	1: Selects format set 1 for B channel captured trace information. 0: Selects format set 0 for B channel captured trace information.
R_F	26	RW	0x0	1: Selects format set 1 for R channel captured trace information. 0: Selects format set 0 for R channel captured trace information.
AW_F	25	RW	0x0	1: Selects format set 1 for AW channel captured trace information. 0: Selects format set 0 for AW channel captured trace information.
AR_F	24	RW	0x0	1: Selects format set 1 for AR channel captured trace information.

				0: Selects format set 0 for AR channel captured trace information.
BSY	23	R	0x0	1: Indicates that trace probe is busy, meaning that trace capture may be in progress and/or internal buffers are not empty. No changes should be made to probe configuration registers in this state. 0: Trace probe is idle. It is safe to program probe configuration registers.
ID	22:16	RW	0x1	Value of ATID [6:0] transmitted on the ATB interface. Legal values are 0x1 through 0x6F. Values of 0x0 or >0x6F may lead to unpredictable behavior.
CR_V	15	RW	0x0	1: Enables invasive tracing on the CR channel if both DBGEN and SPIDEN of the authentication interface are 1, in which case trace probe will back pressure bridge interfaces to avoid losing trace data due to buffer overflow. 0: Non-invasive tracing mode, probe will not back pressure CR channel bridge interfaces. Trace data is lost when buffers overflow.
AC_V	14	RW	0x0	1: Enables invasive tracing on the AC channel if both DBGEN and SPIDEN of the authentication interface are 1, in which case trace probe will back pressure bridge interfaces to avoid losing trace data due to buffer overflow. 0: Non-invasive tracing mode, probe will not back pressure AC channel bridge interfaces. Trace data is lost when buffers overflow.
B_V	13	RW	0x0	1: Enables invasive tracing on the B channel if both DBGEN and SPIDEN of the authentication interface are 1, in which case trace probe will back pressure bridge interfaces to avoid losing trace data due to buffer overflow. 0: Non-invasive tracing mode, probe will not back pressure B channel bridge interfaces. Trace data is lost when buffers overflow.
R_V	12	RW	0x0	1: Enables invasive tracing on the R channel if both DBGEN and SPIDEN of the authentication interface are 1, in which case trace probe will back pressure bridge interfaces to avoid losing trace data due to buffer overflow. 0: Non-invasive tracing mode, probe will not back pressure R channel bridge interfaces. Trace data is

				lost when buffers overflow.
AW_V	11	RW	0x0	1: Enables invasive tracing on the AW channel if both DBGEN and SPIDEN of the authentication interface are 1, in which case trace probe will back pressure bridge interfaces to avoid losing trace data due to buffer overflow. 0: Non-invasive tracing mode, probe will not back pressure AW channel bridge interfaces. Trace data is lost when buffers overflow.
AR_V	10	RW	0x0	1: Enables invasive tracing on the AR channel if both DBGEN and SPIDEN of the authentication interface are 1, in which case trace probe will back pressure bridge interfaces to avoid losing trace data due to buffer overflow. 0: Non-invasive tracing mode, probe will not back pressure AR channel bridge interfaces. Trace data is lost when buffers overflow.
RSVD_9_4	9:4	R	0x0	Reserved for future use. SW should write and read 0.
AC	3	RW	0x1	1: Trace capture of AC/CR channels is enabled, qualified by EN. 0: Trace capture of AC/CR channels is disabled.
AW	2	RW	0x1	1: Trace capture of AW/B channels is enabled, qualified by EN. 0: Trace capture of AW/B channels is disabled.
AR	1	RW	0x1	1: Trace capture of AR/R channels is enabled, qualified by EN. 0: Trace capture of AR/R channels is disabled.
EN	0	RW	0x0	1: Trace capture is globally enabled. Configuration registers should not be written. 0: Trace capture is globally disabled. Configuration registers may be safely written if BUSY reads as 0.

4.1.2 Register: CS_TRACE_TS_CFG

Name: Timestamp Configuration Register
Offset: 0x2004
Description: This register controls timestamping behavior and reports information about width and source of time stamp values.

Table 9 CS_TRACE_TS_CFG

Field Name	Bit Range	RW	Reset Value	Description
RSVD_31	31	R	0x0	Reserved for future use. SW should write and read 0.
C_SFT	30:24	R	DS	Reports the number of bits by which timer value is right shifted when operating in coarse grained mode (CRS == 1).
EXT	23	R	DS	1: Timer value comes from external timer interface pins (dbg_TSVALUE). 0: Timer value comes from internal counter.
TS_WID	22:16	R	DS	Reports the full bit width of the timestamp timer (max 28 bits).
CRS	15	RW	0x0	1: Selects coarse grained timestamping, where timer values are right shifted by the number of bits specified in the C_SFT field before they are used for timestamping. 0: Selects normal timestamping, where full non-shifted timer values are used for timestamping.
CMP	14	RW	0x1	1: Timestamp logical difference compression is enabled. 0: Timestamp compression disabled.
RSVD_13_6	13:6	R		Reserved for future use. SW should write and read 0.
CR	5	RW	0x0	1: Enable timestamping for CR channel. 0: Disable timestamping for CR channel.
AC	4	RW	0x0	1: Enable timestamping for AC channel. 0: Disable timestamping for AC channel.
B	3	RW	0x0	1: Enable timestamping for B channel. 0: Disable timestamping for B channel.
R	2	RW	0x0	1: Enable timestamping for R channel. 0: Disable timestamping for R channel.
AW	1	RW	0x0	1: Enable timestamping for AW channel. 0: Disable timestamping for AW channel.
AR	0	RW	0x0	1: Enable timestamping for AR channel. 0: Disable timestamping for AR channel.

4.1.3 Register: CS_TRACE_FILT_CTRL

Name: Trace Filtering Control Register
Offset: 0x200c
Description: This register controls trace filtering to determine which transactions are included

in the trace output.

Table 10 CS_TRACE_FILT_CTRL

Field Name	Bit Range	RW	Reset Value	Description
AC_EXC_ONLY	30	RW	0x1	1: Include all AC transactions, only apply exclusion filters. 0: Apply both inclusion and exclusion AC filters.
AW_EXC_ONLY	29	RW	0x1	1: Include all AW transactions, only apply exclusion filters and AW_ERR_INC. 0: Apply both inclusion and exclusion AW filters.
AR_EXC_ONLY	28	RW	0x1	1: Include all AR transactions, only apply exclusion filters and AR_ERR_INC. 0: Apply both inclusion and exclusion AR filters.
AW_ERR_INC	27	RW	0x1	1: For master bridges only: include AW transactions that miss the address table or generate other errors in address decode, even if they are otherwise excluded. This bit is only settable in master bridges. 0: Do not force inclusion of AW error transactions.
AW_TBL_EXC	26	RW	0x1	1: For master bridges only: exclude AW transactions do NOT hit an address table entry enabled in the CS_TBL_MATCH registers. This bit is only settable in master bridges. 0: Do not exclude any transactions based on AW table lookup results.
AR_ERR_INC	25	RW	0x1	1: For master bridges only: include AR transactions that miss the address table or generate other errors in address decode, even if they are otherwise excluded. This bit is only settable in master bridges. 0: Do not force inclusion of AR error transactions.
AR_TBL_EXC	24	RW	0x1	1: For master bridges only: exclude AR transactions do NOT hit an address table entry enabled in the CS_TBL_MATCH registers. This bit is only settable in master bridges. 0: Do not exclude any transactions based on AR table lookup results.
RSVD_23	23	R	0x0	Reserved for future use. SW should write and read 0.
AC_EXC	22:20	RW	0x0	Bit mask where a 1 selects the corresponding AC channel match signal (2-0) to exclude AC transactions.

RSVD_19	19	R	0x0	Reserved for future use. SW should write and read 0.
AC_INC	18:16	RW	0x0	Bit mask where a 1 selects the corresponding AC channel match signal (2-0) to include AC transactions.
RSVD_15	15	R	0x0	Reserved for future use. SW should write and read 0.
AW_EXC	14:12	RW	0x0	Bit mask where a 1 selects the corresponding AW channel match signal (2-0) to exclude AW transactions.
RSVD_11	11	R	0x0	Reserved for future use. SW should write and read 0.
AW_INC	10:8	RW	0x0	Bit mask where a 1 selects the corresponding AW channel match signal (2-0) to include AW transactions.
RSVD_7	7	R	0x0	Reserved for future use. SW should write and read 0.
AR_EXC	6:4	RW	0x0	Bit mask where a 1 selects the corresponding AR channel match signal (2-0) to exclude AR transactions.
RSVD_3	3	R	0x0	Reserved for future use. SW should write and read 0.
AR_INC	2:0	RW	0x0	Bit mask where a 1 selects the corresponding AR channel match signal (2-0) to include AR transactions.

4.2 CHANNEL MATCH REGISTERS

4.2.1 Register: CS_MATCH_AR_CFG

Name: Match signal selector for AR channel
Offset: 0x2010
Description: This register selects which comparators are used in AR channel to generate match signals 0, 1 and 2, which feed into filtering, start/stop, and triggering functions.

Table 11 CS_MATCH_AR_CFG

Field Name	Bit Range	RW	Reset Value	Description
M2_LOM_ID	26	RW	0x0	When set, AR channel match[2] signal includes logid/orgid/mstrid comparator result.
M2_ID	25	RW	0x0	When set, AR channel match[2] signal includes AxID

				comparator result.
M2_CTRL1	24	RW	0x0	When set, AR channel match[2] signal includes control comparator 1 result.
M2_CTRL0	23	RW	0x0	When set, AR channel match[2] signal includes control comparator 0 result.
M2_ACCTRL1	22	RW	0x0	When set, AR channel match[2] signal includes ACE control comparator 1 result.
M2_ACCTRL0	21	RW	0x0	When set, AR channel match[2] signal includes ACE control comparator 0 result.
M2_ADDR2	20	RW	0x0	When set, AR channel match[2] signal includes address control comparator 2 result.
M2_ADDR1	19	RW	0x0	When set, AR channel match[2] signal includes address control comparator 1 result.
M2_ADDR0	18	RW	0x0	When set, AR channel match[2] signal includes address control comparator 0 result.
M1_LOM_ID	17	RW	0x0	When set, AR channel match[1] signal includes logid/origid/mstrid comparator result.
M1_ID	16	RW	0x0	When set, AR channel match[1] signal includes AxID comparator result.
M1_CTRL1	15	RW	0x0	When set, AR channel match[1] signal includes control comparator 1 result.
M1_CTRL0	14	RW	0x0	When set, AR channel match[1] signal includes control comparator 0 result.
M1_ACCTRL1	13	RW	0x0	When set, AR channel match[1] signal includes ACE control comparator 1 result.
M1_ACCTRL0	12	RW	0x0	When set, AR channel match[1] signal includes ACE control comparator 0 result.
M1_ADDR2	11	RW	0x0	When set, AR channel match[1] signal includes address control comparator 2 result.
M1_ADDR1	10	RW	0x0	When set, AR channel match[1] signal includes address control comparator 1 result.
M1_ADDR0	9	RW	0x0	When set, AR channel match[1] signal includes address control comparator 0 result.
M0_LOM_ID	8	RW	0x0	When set, AR channel match[0] signal includes logid/origid/mstrid comparator result.
M0_ID	7	RW	0x0	When set, AR channel match[0] signal includes AxID comparator result.
M0_CTRL1	6	RW	0x0	When set, AR channel match[0] signal includes control comparator 1 result.
M0_CTRL0	5	RW	0x0	When set, AR channel match[0] signal includes control comparator 0 result.

M0_ACCTRL1	4	RW	0x0	When set, AR channel match[0] signal includes ACE control comparator 1 result.
M0_ACCTRL0	3	RW	0x0	When set, AR channel match[0] signal includes ACE control comparator 0 result.
M0_ADDR2	2	RW	0x0	When set, AR channel match[0] signal includes address control comparator 2 result.
M0_ADDR1	1	RW	0x0	When set, AR channel match[0] signal includes address control comparator 1 result.
M0_ADDR0	0	RW	0x0	When set, AR channel match[0] signal includes address control comparator 0 result.

4.2.2 Register: CS_MATCH_AW_CFG

Name: Match signal selector for AW channel
Offset: 0x2014
Description: This register selects which comparators are used in AW channel to generate match signals 0, 1 and 2, which feed into filtering, start/stop, and triggering functions.

Table 12 CS_MATCH_AW_CFG

Field Name	Bit Range	RW	Reset Value	Description
M2_LOM_ID	26	RW	0x0	When set, AW channel match[2] signal includes logid/origid/mstrid comparator result.
M2_ID	25	RW	0x0	When set, AW channel match[2] signal includes AxID comparator result.
M2_CTRL1	24	RW	0x0	When set, AW channel match[2] signal includes control comparator 1 result.
M2_CTRL0	23	RW	0x0	When set, AW channel match[2] signal includes control comparator 0 result.
M2_ACCTRL1	22	RW	0x0	When set, AW channel match[2] signal includes ACE control comparator 1 result.
M2_ACCTRL0	21	RW	0x0	When set, AW channel match[2] signal includes ACE control comparator 0 result.
M2_ADDR2	20	RW	0x0	When set, AW channel match[2] signal includes address control comparator 2 result.
M2_ADDR1	19	RW	0x0	When set, AW channel match[2] signal includes address control comparator 1 result.
M2_ADDR0	18	RW	0x0	When set, AW channel match[2] signal includes address control comparator 0 result.
M1_LOM_ID	17	RW	0x0	When set, AW channel match[1] signal includes

				logid/origid/mstrid comparator result.
M1_ID	16	RW	0x0	When set, AW channel match[1] signal includes AxID comparator result.
M1_CTRL1	15	RW	0x0	When set, AW channel match[1] signal includes control comparator 1 result.
M1_CTRL0	14	RW	0x0	When set, AW channel match[1] signal includes control comparator 0 result.
M1_ACCTRL1	13	RW	0x0	When set, AW channel match[1] signal includes ACE control comparator 1 result.
M1_ACCTRL0	12	RW	0x0	When set, AW channel match[1] signal includes ACE control comparator 0 result.
M1_ADDR2	11	RW	0x0	When set, AW channel match[1] signal includes address control comparator 2 result.
M1_ADDR1	10	RW	0x0	When set, AW channel match[1] signal includes address control comparator 1 result.
M1_ADDR0	9	RW	0x0	When set, AW channel match[1] signal includes address control comparator 0 result.
M0_LOM_ID	8	RW	0x0	When set, AW channel match[0] signal includes logid/origid/mstrid comparator result.
M0_ID	7	RW	0x0	When set, AW channel match[0] signal includes AxID comparator result.
M0_CTRL1	6	RW	0x0	When set, AW channel match[0] signal includes control comparator 1 result.
M0_CTRL0	5	RW	0x0	When set, AW channel match[0] signal includes control comparator 0 result.
M0_ACCTRL1	4	RW	0x0	When set, AW channel match[0] signal includes ACE control comparator 1 result.
M0_ACCTRL0	3	RW	0x0	When set, AW channel match[0] signal includes ACE control comparator 0 result.
M0_ADDR2	2	RW	0x0	When set, AW channel match[0] signal includes address control comparator 2 result.
M0_ADDR1	1	RW	0x0	When set, AW channel match[0] signal includes address control comparator 1 result.
M0_ADDR0	0	RW	0x0	When set, AW channel match[0] signal includes address control comparator 0 result.

4.2.3 Register: CS_MATCH_AC_CFG

Name: Match signal selector for AC channel
Offset: 0x2018
Description: This register selects which comparators are used in AC channel to generate match

signals 0, 1 and 2, which feed into filtering, start/stop, and triggering functions.

Table 13 CS_MATCH_AC_CFG

Field Name	Bit Range	RW	Reset Value	Description
M2_ACCTRL1	22	RW	0x0	When set, AR channel match[2] signal includes ACE control comparator 1 result.
M2_ACCTRL0	21	RW	0x0	When set, AR channel match[2] signal includes ACE control comparator 0 result.
M2_ADDR2	20	RW	0x0	When set, AC channel match[2] signal includes address control comparator 2 result.
M2_ADDR1	19	RW	0x0	When set, AC channel match[2] signal includes address control comparator 1 result.
M2_ADDR0	18	RW	0x0	When set, AC channel match[2] signal includes address control comparator 0 result.
RSVD_17_14	17:14	R	0x0	Reserved for future use. SW should write and read 0.
M1_ACCTRL1	13	RW	0x0	When set, AR channel match[1] signal includes ACE control comparator 1 result.
M1_ACCTRL0	12	RW	0x0	When set, AR channel match[0] signal includes ACE control comparator 0 result.
M1_ADDR2	11	RW	0x0	When set, AC channel match[1] signal includes address control comparator 2 result.
M1_ADDR1	10	RW	0x0	When set, AC channel match[1] signal includes address control comparator 1 result.
M1_ADDR0	9	RW	0x0	When set, AC channel match[1] signal includes address control comparator 0 result.
RSVD_8_5	8:5	R	0x0	Reserved for future use. SW should write and read 0.
M0_ACCTRL1	4	RW	0x0	When set, AR channel match[0] signal includes ACE control comparator 1 result.
M0_ACCTRL0	3	RW	0x0	When set, AR channel match[0] signal includes ACE control comparator 0 result.
M0_ADDR2	2	RW	0x0	When set, AC channel match[0] signal includes address control comparator 2 result.
M0_ADDR1	1	RW	0x0	When set, AC channel match[0] signal includes address control comparator 1 result.
M0_ADDR0	0	RW	0x0	When set, AC channel match[0] signal includes address control comparator 0 result.

4.3 CHANNEL FIELDS REGISTERS

4.3.1 Register: CS_TR_FIELDS_AR_L0

Name: Trace Fields Lower Set for AR Format 0
Offset: 0x2040
Description: This register describes the bit widths of the lower set of fields that are included in the trace for captured AR channel transactions when AR channel tracing is enabled and AR Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 14 CS_TR_FIELDS_AR_L0

Field Name	Bit Range	RW	Reset Value	Description
QOS	26:24	R	DS	Width of the AxQOS field, 0 if not captured.
REGN	23:21	R	DS	Width of the AxREGION field, 0 if not captured.
CACHE	20:18	R	DS	Width of the AxCACHE field, 0 if not captured.
LOCK	17:16	R	DS	Width of the AxLOCK field, 0 if not captured.
PROT	15:14	R	DS	Width of the AxPROT field, 0 if not captured.
BT	13:12	R	DS	Width of the AxBURST field, 0 if not captured.
SIZE	11:10	R	DS	Width of the AxSIZE field, 0 if not captured.
LEN	9:6	R	DS	Width of the AxLEN field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.2 Register: CS_TR_FIELDS_AR_U0

Name: Trace Fields Upper Set for AR Format 0
Offset: 0x2044
Description: This register describes the bit widths of the upper set of fields that are included in the trace for captured AR channel transactions when AR channel tracing is enabled and AR Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 15 CS_TR_FIELDS_AR_U0

Field Name	Bit Range	RW	Reset Value	Description
ADDR	30:25	R	DS	Width of the AxADDR field, 0 if not captured.
MID	24:21	R	DS	Width of the mstrid field. This field is only used in slave bridges, and it indicates contains the internal ID of the immediately upstream bridge that sourced

				the transaction.
BAR	20:19	R	DS	Width of the AxBAR field, 0 if not captured.
DMN	18:17	R	DS	Width of the AxDOMAIN field, 0 if not captured.
SNP	16:14	R	DS	Width of the AxSNOOP field, 0 if not captured.
USER	13:8	R	DS	Width of the AxUSER field, 0 if not captured.
LID	7:4	R	DS	Width of the logid field. This field is unused in most cases, but it may be provided by host logic to a master bridge to distinguish between upstream sources of the transaction (e.g., to distinguish between cores in a multi-core CPU complex).
OID	3:0	R	DS	Width of the orgid field. This field is unused in most cases, but where there are traffic paths that pass through intermediary bridges, this indicates the internal ID of the originator of the transaction.

4.3.3 Register: CS_TR_FIELDS_AR_L1

Name: Trace Fields Lower Set for AR Format 1
Offset: 0x2048
Description: This register describes the bit widths of the lower set of fields that are included in the trace for captured AR channel transactions when AR channel tracing is enabled and AR Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 16 CS_TR_FIELDS_AR_L1

Field Name	Bit Range	RW	Reset Value	Description
QOS	26:24	R	DS	Width of the AxQOS field, 0 if not captured.
REGN	23:21	R	DS	Width of the AxREGION field, 0 if not captured.
CACHE	20:18	R	DS	Width of the AxCACHE field, 0 if not captured.
LOCK	17:16	R	DS	Width of the AxLOCK field, 0 if not captured.
PROT	15:14	R	DS	Width of the AxPROT field, 0 if not captured.
BT	13:12	R	DS	Width of the AxBURST field, 0 if not captured.
SIZE	11:10	R	DS	Width of the AxSIZE field, 0 if not captured.
LEN	9:6	R	DS	Width of the AxLEN field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.4 Register: CS_TR_FIELDS_AR_U1

Name: Trace Fields Upper Set for AR Format 1

Offset: 0x204c

Description: This register describes the bit widths of the upper set of fields that are included in the trace for captured AR channel transactions when AR channel tracing is enabled and AR Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 17 CS_TR_FIELDS_AR_U1

Field Name	Bit Range	RW	Reset Value	Description
ADDR	30:25	R	DS	Width of the AxADDR field, 0 if not captured.
MID	24:21	R	DS	Width of the mstrid field. This field is only used in slave bridges, and it indicates contains the internal ID of the immediately upstream bridge that sourced the transaction.
BAR	20:19	R	DS	Width of the AxBAR field, 0 if not captured.
DMN	18:17	R	DS	Width of the AxDOMAIN field, 0 if not captured.
SNP	16:14	R	DS	Width of the AxSNOOP field, 0 if not captured.
USER	13:8	R	DS	Width of the AxUSER field, 0 if not captured.
LID	7:4	R	DS	Width of the logid field. This field is unused in most cases, but it may be provided by host logic to a master bridge to distinguish between upstream sources of the transaction (e.g., to distinguish between cores in a multi-core CPU complex).
OID	3:0	R	DS	Width of the orgid field. This field is unused in most cases, but where there are traffic paths that pass through intermediary bridges, this indicates the internal ID of the originator of the transaction.

4.3.5 Register: CS_TR_FIELDS_AW_L0

Name: Trace Fields Lower Set for AW Format 0

Offset: 0x2050

Description: This register describes the bit widths of the lower set of fields that are included in the trace for captured AW channel transactions when AW channel tracing is enabled and AW Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 18 CS_TR_FIELDS_AW_L0

Field Name	Bit Range	RW	Reset Value	Description

QOS	26:24	R	DS	Width of the AxQOS field, 0 if not captured.
REGN	23:21	R	DS	Width of the AxREGION field, 0 if not captured.
CACHE	20:18	R	DS	Width of the AxCACHE field, 0 if not captured.
LOCK	17:16	R	DS	Width of the AxLOCK field, 0 if not captured.
PROT	15:14	R	DS	Width of the AxPROT field, 0 if not captured.
BT	13:12	R	DS	Width of the AxBURST field, 0 if not captured.
SIZE	11:10	R	DS	Width of the AxSIZE field, 0 if not captured.
LEN	9:6	R	DS	Width of the AxLEN field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.6 Register: CS_TR_FIELDS_AW_U0

Name: Trace Fields Upper Set for AW Format 0
Offset: 0x2054
Description: This register describes the bit widths of the upper set of fields that are included in the trace for captured AW channel transactions when AW channel tracing is enabled and AW Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 19 CS_TR_FIELDS_AW_U0

Field Name	Bit Range	RW	Reset Value	Description
ADDR	30:25	R	DS	Width of the AxADDR field, 0 if not captured.
MID	24:21	R	DS	Width of the mstrid field. This field is only used in slave bridges, and it indicates contains the internal ID of the immediately upstream bridge that sourced the transaction.
BAR	20:19	R	DS	Width of the AxBAW field, 0 if not captured.
DMN	18:17	R	DS	Width of the AxDOMAIN field, 0 if not captured.
SNP	16:14	R	DS	Width of the AxSNOOP field, 0 if not captured.
USER	13:8	R	DS	Width of the AxUSER field, 0 if not captured.
LID	7:4	R	DS	Width of the logid field. This field is unused in most cases, but it may be provided by host logic to a master bridge to distinguish between upstream sources of the transaction (e.g., to distinguish between cores in a multi-core CPU complex).
OID	3:0	R	DS	Width of the orgid field. This field is unused in most cases, but where there are traffic paths that pass through intermediary bridges, this indicates the internal ID of the originator of the transaction.

4.3.7 Register: CS_TR_FIELDS_AW_L1

Name: Trace Fields Lower Set for AW Format 1
Offset: 0x2058
Description: This register describes the bit widths of the lower set of fields that are included in the trace for captured AW channel transactions when AW channel tracing is enabled and AW Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 20 CS_TR_FIELDS_AW_L1

Field Name	Bit Range	RW	Reset Value	Description
QOS	26:24	R	DS	Width of the AxQOS field, 0 if not captured.
REGN	23:21	R	DS	Width of the AxREGION field, 0 if not captured.
CACHE	20:18	R	DS	Width of the AxCACHE field, 0 if not captured.
LOCK	17:16	R	DS	Width of the AxLOCK field, 0 if not captured.
PROT	15:14	R	DS	Width of the AxPROT field, 0 if not captured.
BT	13:12	R	DS	Width of the AxBURST field, 0 if not captured.
SIZE	11:10	R	DS	Width of the AxSIZE field, 0 if not captured.
LEN	9:6	R	DS	Width of the AxLEN field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.8 Register: CS_TR_FIELDS_AW_U1

Name: Trace Fields Upper Set for AW Format 1
Offset: 0x205c
Description: This register describes the bit widths of the upper set of fields that are included in the trace for captured AW channel transactions when AW channel tracing is enabled and AW Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 21 CS_TR_FIELDS_AW_U1

Field Name	Bit Range	RW	Reset Value	Description
ADDR	30:25	R	DS	Width of the AxADDR field, 0 if not captured.
MID	24:21	R	DS	Width of the mstrid field. This field is only used in slave bridges, and it indicates contains the internal ID of the immediately upstream bridge that sourced

				the transaction.
BAR	20:19	R	DS	Width of the AxBAW field, 0 if not captured.
DMN	18:17	R	DS	Width of the AxDOMAIN field, 0 if not captured.
SNP	16:14	R	DS	Width of the AxSNOOP field, 0 if not captured.
USER	13:8	R	DS	Width of the AxUSER field, 0 if not captured.
LID	7:4	R	DS	Width of the logid field. This field is unused in most cases, but it may be provided by host logic to a master bridge to distinguish between upstream sources of the transaction (e.g., to distinguish between cores in a multi-core CPU complex).
OID	3:0	R	DS	Width of the orgid field. This field is unused in most cases, but where there are traffic paths that pass through intermediary bridges, this indicates the internal ID of the originator of the transaction.

4.3.9 Register: CS_TR_FIELDS_AC_0

Name: Trace Fields for AC Format 0
Offset: 0x2060
Description: This register describes the bit widths of the fields that are included in the trace for captured AC channel transactions when AC channel tracing is enabled and AC Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 22 CS_TR_FIELDS_AC_0

Field Name	Bit Range	RW	Reset Value	Description
ADDR	18:13	R	DS	Width of the AxADDR field, 0 if not captured.
AGID	12:9	R	DS	Width of the slvid/agnid field. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	8:5	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
SNP	4:2	R	DS	Width of the AxSNOOP field, 0 if not captured.
PROT	1:0	R	DS	Width of the AxPROT field, 0 if not captured.

4.3.10 Register: CS_TR_FIELDS_AC_1

Name: Trace Fields for AC Format 1
Offset: 0x2064
Description: This register describes the bit widths of the fields that are included in the trace for captured AC channel transactions when AC channel tracing is enabled and AC Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 23 CS_TR_FIELDS_AC_1

Field Name	Bit Range	RW	Reset Value	Description
ADDR	18:13	R	DS	Width of the AxADDR field, 0 if not captured.
AGID	12:9	R	DS	Width of the slvid/agnid field. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	8:5	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
SNP	4:2	R	DS	Width of the AxSNOOP field, 0 if not captured.
PROT	1:0	R	DS	Width of the AxPROT field, 0 if not captured.

4.3.11 Register: CS_TR_FIELDS_R_0

Name: Trace Fields for R Format 0
Offset: 0x2068
Description: This register describes the bit widths of the fields that are included in the trace for captured R channel transactions when R channel tracing is enabled and R Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 24 CS_TR_FIELDS_R_0

Field Name	Bit Range	RW	Reset Value	Description
MSID	22:19	R	DS	Width of the slvid/mstrid field. For master bridges, this is the slvid field, and in slave bridges, this is the mstrid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.

CID	18:15	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
USER	14:9	R	DS	Width of the AxUSER field, 0 if not captured.
RESP	8:6	R	DS	Width of the AxRESP field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.12 Register: CS_TR_FIELDS_R_1

Name: Trace Fields for R Format 1
Offset: 0x206c
Description: This register describes the bit widths of the fields that are included in the trace for captured R channel transactions when R channel tracing is enabled and R Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 25 CS_TR_FIELDS_R_1

Field Name	Bit Range	RW	Reset Value	Description
MSID	22:19	R	DS	Width of the slvid/mstrid field. For master bridges, this is the slvid field, and in slave bridges, this is the mstrid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	18:15	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
USER	14:9	R	DS	Width of the AxUSER field, 0 if not captured.
RESP	8:6	R	DS	Width of the AxRESP field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.13 Register: CS_TR_FIELDS_B_0

Name: Trace Fields for B Format 0
Offset: 0x2070
Description: This register describes the bit widths of the fields that are included in the trace for captured B channel transactions when B channel tracing is enabled and B Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 26 CS_TR_FIELDS_B_0

Field Name	Bit Range	RW	Reset Value	Description
MSID	22:19	R	DS	Width of the slvid/mstrid field. For master bridges, this is the slvid field, and in slave bridges, this is the mstrid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	18:15	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
USER	14:9	R	DS	Width of the AxUSER field, 0 if not captured.
RESP	8:6	R	DS	Width of the AxRESP field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.14 Register: CS_TR_FIELDS_B_1

Name: Trace Fields for R Format 1
Offset: 0x2074
Description: This register describes the bit widths of the fields that are included in the trace for captured R channel transactions when R channel tracing is enabled and R Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 27 CS_TR_FIELDS_B_1

Field Name	Bit Range	RW	Reset Value	Description
MSID	22:19	R	DS	Width of the slvid/mstrid field. For master bridges, this is the slvid field, and in slave bridges, this is the mstrid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	18:15	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
USER	14:9	R	DS	Width of the AxUSER field, 0 if not captured.
RESP	8:6	R	DS	Width of the AxRESP field, 0 if not captured.
ID	5:0	R	DS	Width of the AxID field, 0 if not captured.

4.3.15 Register: CS_TR_FIELDS_CR_0

Name: Trace Fields for CR Format 0
Offset: 0x2078
Description: This register describes the bit widths of the fields that are included in the trace for captured CR channel transactions when CR channel tracing is enabled and CR Trace Format 0 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 28 CS_TR_FIELDS_CR_0

Field Name	Bit Range	RW	Reset Value	Description
MSID	10:7	R	DS	Width of the slvid/agnid field. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	6:3	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges participating in the coherent domain. It is a snoop request ID.
RESP	2:0	R	DS	Width of the AxRESP field, 0 if not captured.

4.3.16 Register: CS_TR_FIELDS_CR_1

Name: Trace Fields for CR Format 1
Offset: 0x207c
Description: This register describes the bit widths of the fields that are included in the trace for captured CR channel transactions when CR channel tracing is enabled and CR Trace Format 1 is selected in CS_TRACE_CFG_STS.FMT. A value of 0 indicates that the associated field is not included in the trace data.

Table 29 CS_TR_FIELDS_CR_1

Field Name	Bit Range	RW	Reset Value	Description
MSID	10:7	R	DS	Width of the slvid/agnid field. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction.
CID	6:3	R	DS	Width of the crtid field. This is an internal field, only present in a Gemini coherent NoC for bridges

				participating in the coherent domain. It is a snoop request ID.
RESP	2:0	R	DS	Width of the AxRESP field, 0 if not captured.

4.4 ADDRESS MATCH REGISTERS

4.4.1 Register: CS_ADDR_MATCH_LO_VAL_0

Name: Address comparator 0 match value low
Offset: 0x2080
Description: This register specifies the value used in the lower 32-bits of address comparator 0 in AR, AW and AC channel probes.

Table 30 CS_ADDR_MATCH_LO_VAL_0

Field Name	Bit Range	RW	Reset Value	Description
MATCH_VALUE	31:0	RW	0x0	Value to match, must be 0 in bit locations where corresponding MASK has a 0.

4.4.2 Register: CS_ADDR_MATCH_HI_VAL_0

Name: Address comparator 0 match value high
Offset: 0x2084
Description: This register specifies the value used in the upper 32-bits of address comparator 0 in AR, AW and AC channel probes.

Table 31 CS_ADDR_MATCH_HI_VAL_0

Field Name	Bit Range	RW	Reset Value	Description
MATCH_VALUE	31:0	RW	0x0	Value to match, must be 0 in bit locations where corresponding MASK has a 0.

4.4.3 Register: CS_ADDR_MATCH_LO_MASK_0

Name: Address comparator 0 mask low
Offset: 0x2088
Description: This register specifies the mask used in the lower 32-bits of address comparator 0 in AR, AW and AC channel probes.

Table 32 CS_ADDR_MATCH_LO_MASK_0

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0x0	Mask of bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VALUE bit must also be set to 0.

4.4.4 Register: CS_ADDR_MATCH_HI_MASK_0

Name: Address comparator 0 mask high
Offset: 0x208c
Description: This register specifies the mask in the upper 32-bits of address comparator 0 in AR, AW and AC channel probes.

Table 33 CS_ADDR_MATCH_HI_MASK_0

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0x0	Mask of bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VALUE bit must also be set to 0.

4.4.5 Register: CS_ADDR_MATCH_LO_VAL_1

Name: Address comparator 1 match value low
Offset: 0x2090
Description: This register specifies the value used in the lower 32-bits of address comparator 1 in AR, AW and AC channel probes.

Table 34 CS_ADDR_MATCH_LO_VAL_1

Field Name	Bit Range	RW	Reset Value	Description
MATCH_VALUE	31:0	RW	0x0	Value to match, must be 0 in bit locations where corresponding MASK has a 0.

4.4.6 Register: CS_ADDR_MATCH_HI_VAL_1

Name: Address comparator 1 match value high
Offset: 0x2094
Description: This register specifies the value used in the upper 32-bits of address comparator 1 in AR, AW and AC channel probes.

Table 35 CS_ADDR_MATCH_HI_VAL_1

Field Name	Bit Range	RW	Reset Value	Description
MATCH_VALUE	31:0	RW	0x0	Value to match, must be 0 in bit locations where corresponding MASK has a 0.

4.4.7 Register: CS_ADDR_MATCH_LO_MASK_1

Name: Address comparator 1 mask low
Offset: 0x2098
Description: This register specifies the mask used in the lower 32-bits of address comparator 1 in AR, AW and AC channel probes.

Table 36 CS_ADDR_MATCH_LO_MASK_1

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0x0	Mask of bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VALUE bit must also be set to 0.

4.4.8 Register: CS_ADDR_MATCH_HI_MASK_1

Name: Address comparator 1 mask high
Offset: 0x209c
Description: This register specifies the mask in the upper 32-bits of address comparator 1 in AR, AW and AC channel probes.

Table 37 CS_ADDR_MATCH_HI_MASK_1

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0x0	Mask of bits to be included in comparison, set to 1

				for each bit location to be included. Where set to 0, corresponding MATCH_VALUE bit must also be set to 0.

4.4.9 Register: CS_ADDR_MATCH_LO_VAL_2

Name: Address comparator 2 match value low
Offset: 0x20a0
Description: This register specifies the value used in the lower 32-bits of address comparator 2 in AR, AW and AC channel probes.

Table 38 CS_ADDR_MATCH_LO_VAL_2

Field Name	Bit Range	RW	Reset Value	Description
MATCH_VALUE	31:0	RW	0x0	Value to match, must be 0 in bit locations where corresponding MASK has a 0.

4.4.10 Register: CS_ADDR_MATCH_HI_VAL_2

Name: Address comparator 2 match value high
Offset: 0x20a4
Description: This register specifies the value used in the upper 32-bits of address comparator 2 in AR, AW and AC channel probes.

Table 39 CS_ADDR_MATCH_HI_VAL_2

Field Name	Bit Range	RW	Reset Value	Description
MATCH_VALUE	31:0	RW	0x0	Value to match, must be 0 in bit locations where corresponding MASK has a 0.

4.4.11 Register: CS_ADDR_MATCH_LO_MASK_2

Name: Address comparator 2 mask low
Offset: 0x20a8
Description: This register specifies the mask used in the lower 32-bits of address comparator 2 in AR, AW and AC channel probes.

Table 40 CS_ADDR_MATCH_LO_MASK_2

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0x0	Mask of bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VALUE bit must also be set to 0.

4.4.12 Register: CS_ADDR_MATCH_HI_MASK_2

Name: Address comparator 2 mask high
Offset: 0x20ac
Description: This register specifies the mask in the upper 32-bits of address comparator 2 in AR, AW and AC channel probes.

Table 41 CS_ADDR_MATCH_HI_MASK_2

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0x0	Mask of bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VALUE bit must also be set to 0.

4.5 CONTROL MATCH REGISTERS

4.5.1 Register: CS_ACCTRL_MATCH_VAL_0

Name: ACE control comparator 0 match value
Offset: 0x20c0
Description: This register specifies the value used in ACE control comparator 0 in AR, AW and AC channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 42 CS_ACCTRL_MATCH_VAL_0

Field Name	Bit Range	RW	Reset Value	Description
AGID	14:7	RW	0x0	Value of the slvid/agnid field of the AC channel to match (not present in AR and AW), must be 0 in bit locations where corresponding MASK has a 0. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is

				the internal ID of the bridge at the other end of the transaction. Note: filtering based on agnid in slave bridges is presently not supported.
SNP	6:3	RW	0x0	Value of the AxSNOOP field to match, must be 0 in bit locations where corresponding MASK has a 0.
PROT	2:0	RW	0x0	Value of the AxPROT field to match, must be 0 in bit locations where corresponding MASK has a 0.

4.5.2 Register: CS_ACCTRL_MATCH_MASK_0

Name: ACE control comparator 0 mask
Offset: 0x20c4
Description: This register specifies the mask used in ACE control comparator 0 in AR, AW and AC channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 43 CS_ACCTRL_MATCH_MASK_0

Field Name	Bit Range	RW	Reset Value	Description
AGID	14:7	RW	0x0	Mask of bits to be included in comparison for the slvid/agnid field of the AC channel (not present in AR and AW), set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction. Note: filtering based on agnid in slave bridges is presently not supported.
SNP	6:3	RW	0x0	Mask of the AxSNOOP field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
PROT	2:0	RW	0x0	Mask of the AxPROT field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.

4.5.3 Register: CS_ACCTRL_MATCH_VAL_1

Name: ACE control comparator 1 match value
Offset: 0x20c8
Description: This register specifies the value used in ACE control comparator 1 in AR, AW and AC channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 44 CS_ACCTRL_MATCH_VAL_1

Field Name	Bit Range	RW	Reset Value	Description
AGID	14:7	RW	0x0	Value of the slvid/agnid field of the AC channel to match (not present in AR and AW), must be 0 in bit locations where corresponding MASK has a 0. For master bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction. Note: filtering based on agnid in slave bridges is presently not supported.
SNP	6:3	RW	0x0	Value of the AxSNOOP field to match, must be 0 in bit locations where corresponding MASK has a 0.
PROT	2:0	RW	0x0	Value of the AxPROT field to match, must be 0 in bit locations where corresponding MASK has a 0.

4.5.4 Register: CS_ACCTRL_MATCH_MASK_1

Name: ACE control comparator 1 mask
Offset: 0x20cc
Description: This register specifies the mask used in ACE control comparator 1 in AR, AW and AC channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 45 CS_ACCTRL_MATCH_MASK_1

Field Name	Bit Range	RW	Reset Value	Description
AGID	14:7	RW	0x0	Mask of bits to be included in comparison for the slvid/agnid field of the AC channel (not present in AR and AW), set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0. For master

				bridges, this is the slvid field, and in slave bridges, this is the agnid field. In both cases, this is the internal ID of the bridge at the other end of the transaction. Note: filtering based on agnid in slave bridges is presently not supported.
SNP	6:3	RW	0x0	Mask of the AxSNOOP field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
PROT	2:0	RW	0x0	Mask of the AxPROT field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.

4.5.5 Register: CS_CTRL_MATCH_VAL_0

Name: Control comparator 0 match value
Offset: 0x20d0
Description: This register specifies the value used in control comparator 0 in AR and AW channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 46 CS_CTRL_MATCH_VAL_0

Field Name	Bit Range	RW	Reset Value	Description
QOS	25:22	RW	0x0	Value of the AxQOS field to match, must be 0 in bit locations where corresponding MASK has a 0.
REGN	21:18	RW	0x0	Value of the AxREGION field to match, must be 0 in bit locations where corresponding MASK has a 0.
CACHE	17:14	RW	0x0	Value of the AxCACHE field to match, must be 0 in bit locations where corresponding MASK has a 0.
LOCK	13	RW	0x0	Value of the AxLOCK field to match, must be 0 in bit locations where corresponding MASK has a 0.
BT	12:11	RW	0x0	Value of the AxBURST field to match, must be 0 in bit locations where corresponding MASK has a 0.
SIZE	10:8	RW	0x0	Value of the AxSIZE field to match, must be 0 in bit locations where corresponding MASK has a 0.
LEN	7:0	RW	0x0	Value of the AxLEN field to match, must be 0 in bit locations where corresponding MASK has a 0.

4.5.6 Register: CS_CTRL_MATCH_MASK_0

Name: Control comparator 0 mask
Offset: 0x20d4
Description: This register specifies the mask used in control comparator 0 in AR and AW channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 47 CS_CTRL_MATCH_MASK_0

Field Name	Bit Range	RW	Reset Value	Description
QOS	25:22	RW	0x0	Mask of the AxQOS field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
REGN	21:18	RW	0x0	Mask of the AxREGION field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
CACHE	17:14	RW	0x0	Mask of the AxCACHE field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
LOCK	13	RW	0x0	Mask of the AxLOCK field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
BT	12:11	RW	0x0	Mask of the AxBURST field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
SIZE	10:8	RW	0x0	Mask of the AxSIZE field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
LEN	7:0	RW	0x0	Mask of the AxLEN field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.

4.5.7 Register: CS_CTRL_MATCH_VAL_1

Name: Control comparator 1 match value
Offset: 0x20d8
Description: This register specifies the value used in control comparator 1 in AR and AW channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 48 CS_CTRL_MATCH_VAL_1

Field Name	Bit Range	RW	Reset Value	Description
QOS	25:22	RW	0x0	Value of the AxQOS field to match, must be 0 in bit locations where corresponding MASK has a 0.
REGN	21:18	RW	0x0	Value of the AxREGION field to match, must be 0 in bit locations where corresponding MASK has a 0.
CACHE	17:14	RW	0x0	Value of the AxCACHE field to match, must be 0 in bit locations where corresponding MASK has a 0.
LOCK	13	RW	0x0	Value of the AxLOCK field to match, must be 0 in bit locations where corresponding MASK has a 0.
BT	12:11	RW	0x0	Value of the AxBURST field to match, must be 0 in bit locations where corresponding MASK has a 0.
SIZE	10:8	RW	0x0	Value of the AxSIZE field to match, must be 0 in bit locations where corresponding MASK has a 0.
LEN	7:0	RW	0x0	Value of the AxLEN field to match, must be 0 in bit locations where corresponding MASK has a 0.

4.5.8 Register: CS_CTRL_MATCH_MASK_1

Name: Control comparator 1 mask
Offset: 0x20dc
Description: This register specifies the mask used in control comparator 1 in AR and AW channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 49 CS_CTRL_MATCH_MASK_1

Field Name	Bit Range	RW	Reset Value	Description
QOS	25:22	RW	0x0	Mask of the AxQOS field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding

				MATCH_VAL bit must also be set to 0.
REGN	21:18	RW	0x0	Mask of the AxREGION field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
CACHE	17:14	RW	0x0	Mask of the AxCACHE field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
LOCK	13	RW	0x0	Mask of the AxLOCK field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
BT	12:11	RW	0x0	Mask of the AxBURST field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
SIZE	10:8	RW	0x0	Mask of the AxSIZE field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.
LEN	7:0	RW	0x0	Mask of the AxLEN field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.

4.5.9 Register: CS_ID_MATCH_VAL

Name: ID comparator match value
Offset: 0x20e0
Description: This register specifies the value used in the ID comparator in AR and AW channel probes. Where the capture size of AxID is > 32 bits, only the lowest 32 bits may be matched in the comparator.

Table 50 CS_ID_MATCH_VAL

Field Name	Bit Range	RW	Reset Value	Description
ID	31:0	RW	0x0	Value of the lowest 32 bits of the AxID field to match, must be 0 in bit locations where corresponding MASK has a 0.

4.5.10 Register: CS_ID_MATCH_MASK

Name: ID comparator mask
Offset: 0x20e4
Description: This register specifies the mask used in the ID comparator in AR and AW channel probes. Where the capture size of AxID is > 32 bits, only the lowest 32 bits may be matched in the comparator.

Table 51 CS_ID_MATCH_MASK

Field Name	Bit Range	RW	Reset Value	Description
ID	31:0	RW	0x0	Mask of the lowest 32 bits of the AxID field bits to be included in comparison, set to 1 for each bit location to be included. Where set to 0, corresponding MATCH_VAL bit must also be set to 0.

4.5.11 Register: CS_LOM_ID_MATCH_VAL

Name: Logid/Orgid/Mstrid comparator match value
Offset: 0x20e8
Description: This register specifies the value used in the logid/orgid/mstrid comparator in AR and AW channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 52 CS_LOM_ID_MATCH_VAL

Field Name	Bit Range	RW	Reset Value	Description
OID	23:16	RW	0x0	Value of the orgid field to match, must be 0 in bit locations where corresponding MASK has a 0. This field is unused in most cases, but where there are traffic paths that pass through intermediary bridges, this indicates the internal ID of the originator of the transaction.
LID	15:8	RW	0x0	Value of the logid field to match, must be 0 in bit locations where corresponding MASK has a 0. This field is unused in most cases, but it may be provided by host logic to a master bridge to distinguish between upstream sources of the transaction (e.g., to distinguish between cores in a multi-core CPU complex).

MID	7:0	RW	0x0	Value of the mstrid field to match, must be 0 in bit locations where corresponding MASK has a 0. This field is only used in slave bridges, and it indicates contains the internal ID of the immediately upstream bridge that sourced the transaction.

4.5.12 Register: CS_LOM_ID_MATCH_MASK

Name: Logid/Orgid/Mstrid comparator mask
Offset: 0x20ec
Description: This register specifies the mask used in the logid/orgid/mstrid comparator in AR and AW channel probes. Unused fields and/or unused MSBs within the fields are read-only returning zeroes.

Table 53 CS_LOM_ID_MATCH_MASK

Field Name	Bit Range	RW	Reset Value	Description
OID	23:16	RW	0x0	Mask of bits to be included in comparison for the orgid field, set to 1 for each bit location to be included. This field is unused in most cases, but where there are traffic paths that pass through intermediary bridges, this indicates the internal ID of the originator of the transaction.
LID	15:8	RW	0x0	Mask of bits to be included in comparison for the logid field, set to 1 for each bit location to be included. This field is unused in most cases, but it may be provided by host logic to a master bridge to distinguish between upstream sources of the transaction (e.g., to distinguish between cores in a multi-core CPU complex).
MID	7:0	RW	0x0	Mask of bits to be included in comparison for the mstrid field, set to 1 for each bit location to be included. This field is only used in slave bridges, and it indicates contains the internal ID of the immediately upstream bridge that sourced the transaction.

4.5.13 Register: CS_TBL_MATCH_0

Name: Trace Address Table Match Register 0

Offset: 0x2100
Description: This register contains a bit mask that selects address table entries 0-31 that will generate a table hit event.

Table 54 CS_TBL_MATCH_0

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.14 Register: CS_TBL_MATCH_1

Name: Trace Address Table Match Register 1
Offset: 0x2104
Description: This register contains a bit mask that selects address table entries 32-63 that will generate a table hit event.

Table 55 CS_TBL_MATCH_1

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.15 Register: CS_TBL_MATCH_2

Name: Trace Address Table Match Register 2
Offset: 0x2108
Description: This register contains a bit mask that selects address table entries 64-95 that will generate a table hit event.

Table 56 CS_TBL_MATCH_2

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.16 Register: CS_TBL_MATCH_3

Name: Trace Address Table Match Register 3
Offset: 0x210c
Description: This register contains a bit mask that selects address table entries 96-127 that will generate a table hit event.

Table 57 CS_TBL_MATCH_3

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.17 Register: CS_TBL_MATCH_4

Name: Trace Address Table Match Register 4
Offset: 0x2110
Description: This register contains a bit mask that selects address table entries 128-159 that will generate a table hit event.

Table 58 CS_TBL_MATCH_4

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.18 Register: CS_TBL_MATCH_5

Name: Trace Address Table Match Register 5
Offset: 0x2114
Description: This register contains a bit mask that selects address table entries 160-191 that will generate a table hit event.

Table 59 CS_TBL_MATCH_5

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.19 Register: CS_TBL_MATCH_6

Name: Trace Address Table Match Register 6
Offset: 0x2118
Description: This register contains a bit mask that selects address table entries 192-223 that will generate a table hit event.

Table 60 CS_TBL_MATCH_6

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.5.20 Register: CS_TBL_MATCH_7

Name: Trace Address Table Match Register 7
Offset: 0x211c
Description: This register contains a bit mask that selects address table entries 224-255 that will generate a table hit event.

Table 61 CS_TBL_MATCH_7

Field Name	Bit Range	RW	Reset Value	Description
MASK	31:0	RW	0xffffffff	When bit is 1, selects corresponding address table entry to include in table hit event.

4.6 DEVICE AND TIMESTAMP REGISTERS

4.6.1 Register: CS_TSFREQR

Name: Timestamp Frequency Register
Offset: 0x2e8c
Description: Timestamp Frequency Register indicates the clock frequency of bridge being probed specified in Hz. Included in the STP FREQ packet that is part of the trace stream ASYNC sequence.

Table 62 CS_TSFREQR

Field Name	Bit Range	RW	Reset Value	Description
FREQ	31:0	RW	0x0	Clock frequency of bridge being probed specified in

				Hz.

4.6.2 Register: CS_AUTHSTATUS

Name: CoreSight Authentication Status Register
Offset: 0x2fb8
Description: CoreSight Authentication Status Register: provides read-only status information about the state of the CoreSight authentication interface. This is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 63 CS_AUTHSTATUS

Field Name	Bit Range	RW	Reset Value	Description
SNID	7:6	R	DS	2'b11: Secure non-invasive debug enabled: ((SPNIDEN | (SPIDEN & DBGEN)) & (NIDEN | DBGEN)) == 1. Secure transactions may be traced. 2'b10: Secure non-invasive debug disabled: ((SPNIDEN | (SPIDEN & DBGEN)) & (NIDEN | DBGEN)) != 1. Secure transactions are not traced.
SID	5:4	R	DS	2'b11: Secure invasive debug enabled: (SPIDEN & DBGEN) == 1. Invasive debug is allowed. Secure transactions may be traced. 2'b10: Secure invasive debug disabled: (SPIDEN & DBGEN) != 1. Invasive debug is not allowed. Secure transactions may be traced if SNID is active.
NSNID	3:2	R	DS	2'b11: Non-secure non-invasive debug enabled: (NIDEN | DBGEN) == 1. Must have this status for any tracing to be done. 2'b10: Non-secure non-invasive debug disabled: (NIDEN | DBGEN) != 1. No tracing at all is possible when NSNID is not active.
NSID	1:0	R	DS	2'b00: Non-secure invasive debug is not supported. Invasive debug is only allowed when SID is active - when (SPIDEN & DBGEN) == 1.

4.6.3 Register: CS_DEVARCH

Name: CoreSight Device Architecture Register
Offset: 0x2fbc

Description: CoreSight Device Architecture Register: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 64 CS_DEVARCH

Field Name	Bit Range	RW	Reset Value	Description
ARCHITECT	31:21	R	0x49a	CFG is the architect of the component, bits[31:28] == JEP106 continuation code (0x9), bits[27:21] == JEP106 identification code (0x1A).
PRESENT	20	R	0x1	Returns 1 to indicate the presence of the CS_DEVARCH registers.
REVISION	19:16	R	0x0	Architecture revision == CS_PIDR2.REVISION (0x0).
ARCHID	15:0	R	0x0	Architecture ID of the component, bits 15:12 == 0x0, bits 11:8 == CS_PIDR1.PART_1 (0x0), and bits 7:0 == CS_PIDR0.PART_0 (0x00 for master bridge, 0x01 for slave bridge).

4.6.4 Register: CS_DEVID

Name: CoreSight Device Configuration Register
Offset: 0x2fc8
Description: CoreSight Device Configuration Register 1: this is a standard CoreSight component register whose definition is implementation defined. In the CFG trace probe, it provides some basic information about which channels may be traced, along with some other information about the nature of the bridge to which the probe is attached.

Table 65 CS_DEVID

Field Name	Bit Range	RW	Reset Value	Description
CCC	4	R	0x1	1: Bridge is attached to a Gemini CCC agent. 0: Bridge is not attached to a Gemini CCC agent.
SLV	3	R	0x1	1: Probe is inside a slave bridge. 0: Probe is inside a master bridge.
AC	2	R	0x1	1: Trace probe for AC/CR channels is present, enabled by CS_TRACE_CFG_STS.AC. 0: Trace probe for AC/CR channels is not present.
AW	1	R	0x1	1: Trace probe for AW/B channels is present, enabled by CS_TRACE_CFG_STS.AW.

				0: Trace probe for AW/B channels is not present.
AR	0	R	0x1	1: Trace probe for AR/R channels is present, enabled by CS_TRACE_CFG_STS.AR. 0: Trace probe for AR/R channels is not present.

4.6.5 Register: CS_DEVTYPE

Name: CoreSight Device Type Identifier Register
Offset: 0x2fcc
Description: CoreSight Device Type Identifier Register: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 66 CS_DEVTYPE

Field Name	Bit Range	RW	Reset Value	Description
SUB	7:4	R	0x4	Sub type 0x4 == Associated with a Bus, stimulus derived from bus activity.
MAJOR	3:0	R	0x3	Major type 0x3 == Trace Source.

4.7 PERIPHERAL REGISTERS

4.7.1 Register: CS_PIDR0

Name: CoreSight Peripheral ID Register 0
Offset: 0x2fe0
Description: CoreSight Peripheral ID Register 0: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 67 CS_PIDR0

Field Name	Bit Range	RW	Reset Value	Description
PART_0	7:0	R	DS	8'h01: Slave bridge probe. 8'h00: Master bridge probe.

4.7.2 Register: CS_PIDR1

Name: CoreSight Peripheral ID Register 1

Offset: 0x2fe4

Description: CoreSight Peripheral ID Register 1: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 68 CS_PIDR1

Field Name	Bit Range	RW	Reset Value	Description
DES_0	7:4	R	0xa	CFG JEDEC JEP106 ID code bits 3:0 (0xA).
PART_1	3:0	R	0x0	Returns 0x0.

4.7.3 Register: CS_PIDR2

Name: CoreSight Peripheral ID Register 2

Offset: 0x2fe8

Description: CoreSight Peripheral ID Register 2: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 69 CS_PIDR2

Field Name	Bit Range	RW	Reset Value	Description
REVISION	7:4	R	0x0	Indicates revision number of the CFG trace probe design.
JEDEC	3	R	0x1	Returns 0x1.
DES_1	2:0	R	0x1	CFG JEDEC JEP106 ID code bits 6:4 (0x1).

4.7.4 Register: CS_PIDR3

Name: CoreSight Peripheral ID Register 3

Offset: 0x2fec

Description: CoreSight Peripheral ID Register 3: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 70 CS_PIDR3

Field Name	Bit Range	RW	Reset Value	Description
REVAND	7:4	R	0x0	Returns 0x0.
CMOD	3:0	R	0x0	Returns 0x0.

4.7.5 Register: CS_PIDR4

Name: CoreSight Peripheral ID Register 4
Offset: 0x2fd0
Description: CoreSight Peripheral ID Register 4: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 71 CS_PIDR4

Field Name	Bit Range	RW	Reset Value	Description
SIZE	7:4	R	0x0	
DES_2	3:0	R	0x9	CFG JEDEC JEP106 ID continuation code (0x9).

4.7.6 Register: CS_PIDR5

Name: CoreSight Peripheral ID Register 5
Offset: 0x2fd4
Description: CoreSight Peripheral ID Register 5: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 72 CS_PIDR5

Field Name	Bit Range	RW	Reset Value	Description
RSVD	7:0	R	0x0	

4.7.7 Register: CS_PIDR6

Name: CoreSight Peripheral ID Register 6
Offset: 0x2fd8
Description: CoreSight Peripheral ID Register 6: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 73 CS_PIDR6

Field Name	Bit	RW	Reset	Description

	Range		Value	
RSVD	7:0	R	0x0	

4.7.8 Register: CS_PIDR7

Name: CoreSight Peripheral ID Register 7
Offset: 0x2fdc
Description: CoreSight Peripheral ID Register 7: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 74 CS_PIDR7

Field Name	Bit Range	RW	Reset Value	Description
RSVD	7:0	R	0x0	

4.8 COMPONENT REGISTERS

4.8.1 Register: CS_CIDR0

Name: CoreSight Component ID Register 0
Offset: 0x2ff0
Description: CoreSight Component ID Register 0: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 75 CS_CIDR0

Field Name	Bit Range	RW	Reset Value	Description
PRMBL_0	7:0	R	0xd	Returns 0x0D.

4.8.2 Register: CS_CIDR1

Name: CoreSight Component ID Register 1
Offset: 0x2ff4
Description: CoreSight Component ID Register 1: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 76 CS_CIDR1

Field Name	Bit Range	RW	Reset Value	Description
CLASS	7:4	R	0x9	Returns 0x9, indicating this a CoreSight component.
PRMBL_1	3:0	R	0x0	Returns 0x0.

4.8.3 Register: CS_CIDR2

Name: CoreSight Component ID Register 2
Offset: 0x2ff8
Description: CoreSight Component ID Register 2: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 77 CS_CIDR2

Field Name	Bit Range	RW	Reset Value	Description
PRMBL_2	7:0	R	0x5	Returns 0x05.

4.8.4 Register: CS_CIDR3

Name: CoreSight Component ID Register 3
Offset: 0x2ffc
Description: CoreSight Component ID Register 3: this is a standard CoreSight component register. Please refer to the ARM CoreSight Architecture Specification for a full description.

Table 78 CS_CIDR3

Field Name	Bit Range	RW	Reset Value	Description
PRMBL_3	7:0	R	0xb1	Returns 0xB1.

5 ERRATA

5.1 EVENT SIGNALING INTERFACE

The events signaling interface is not currently implemented. This includes the *dbg_HWEVENTS[1:0]*, *<brdg>_TRIGOUT[1:0]*, and *<brdg>_ASYNCOUT* interface pins.

CFG recommends connecting these interfaces into a CoreSight deployment if it is anticipated that they would be useful, allowing them to be used via a local design update when support is implemented.

5.2 PARTIAL SUPPORT FOR MASTER BRIDGE

Trace probe support on master bridge are for early access customer only. Please contact CFG support if this is a required feature for your design.

5.3 NO DVM SUPPORT

Please contact CFG support if this is a required feature for your design.

5.4 LOW POWER

The AFREADY signal is tied off to 1'b0 internally. The trace probe will transition to inactive state if the power domain of the bridge leaves the Q_RUN state. Similar behavior can be observed when CS_TRACE_CFG_STS.EN register bit is set with 1'b0.

5.5 TIMESTAMPING – LIMITED SUPPORT

- No Compression Mode:
  There is a known issue when CS_TRACE_TS_CFG.CMP is set to 1'b0.
  The bit should be set as 1'b1 at all times.
- Coarse Timestamping:
  There are known issues when CS_TRACE_TS_CFG.CRS is set to 1'b1.
  This bit should be set to 1'b0 at all times.
- External Timestamping:
  Please contact CFG support if this is a required feature for your design.

5.6 FILTERING – LIMITED SUPPORT

- AGNID filtering on slave bridges is currently not supported
  The AGID fields of the CS_ACCTRL_MATCH_VAL_[1:0] and CS_ACCTRL_MATCH_MASK_[1:0] registers are read-only.

5.7 USER CONFIGURABLE FORMAT SET 1 IN NOCSTUDIO

NocStudio does not support user configuration of the format set 1 and applies a simple reduced mask to the *trace_req_capture_mask* and *trace_resp_capture_mask* settings in current release. Please contact CFG support if 2nd set of trace probe register support is needed in your design.

5.8 TRACE DATA DECODE SPECIFICATION

Detailed description of the trace data decode will be provided in next release.

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