

# NetSpeed Gemini

## *Release Notes*

**Version: GEMINI-17.10**

**Revision A.0**

January 22, 2018

# NetSpeed Gemini 17.10 Release Notes

## About This Document

This document lists the release notes for NetSpeed Gemini. Using NetSpeed NocStudio, users can define NoC architectures, describe specifications and requirements, optimize the NoC design and finally generate the NoC IP files such as RTL, testbench, synthesis scripts, NoC IP documentation etc.

## Audience

This document is intended for users of NocStudio:

- NoC Designers
- NoC Architects
- SoC Architects

## Prerequisite

Before proceeding, you should generally understand:

- Basics of NetSpeed Gemini IP Technology

## Related Documents

The following documents can be used as a reference to this document.

- NetSpeed NocStudio User Manual

## Customer Support

For technical support about this product, please contact [support@netspeedsystems.com](mailto:support@netspeedsystems.com)

For general information about NetSpeed products refer to: [www.netspeedsystems.com](http://www.netspeedsystems.com)

## Revision History

| Revision | Date         | Updates  |
|----------|--------------|--|
| 0.0      | Oct 24, 2017 | Initial  |
| 0.1      | Nov 7, 2017  | Release candidate  |
| A.0      | Jan 22, 2018 | <ol style="list-style-type: none"><li>1. Added property support “axi4_input_register” for regbus master bridge</li><li>2. Corrected an issue regarding split size calculation</li><li>3. Revised LLC replacement policy to match 1704 release performance</li><li>4. Revised latency calculation in NocStudio to better model split transactions</li></ol> |

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## 1 Deliverables

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- NetSpeed NocStudio Package and one of the license options:
  - N7 version supporting 16 layers and 256 bridges
  - N6 version supporting 4 layers and 128 bridges
  - N5 version supporting 4 layers and 60 bridges
  - N4 version supporting 2 layers and 32 bridges
  - N3 version supporting 1 layers and 12 bridges
- NocStudio executable with interactive GUI.
- Verification checkers to be used in the DV environment.
- Sanity Test Bench.
- Documentation
  - a. NocStudio User Manual: The User Guide describes how to set up a system using NocStudio and how to use it to generate NetSpeed IP.
  - b. IP Integration Spec: The Integration Manual describes how to integrate a configured network into a larger subsystem.
  - c. Technical Reference Manual: The Technical Reference Manual describes how the functionality of the various NoC elements, the features and functions available, and how to dynamically change the functions using the programmer's mode.

## 2 Installation

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- NocStudio uses FlexLM based licensing.
  - Linux CentOS 5.5 or higher
  - For node-locked license file, copy over the license file under NocStudio installation directory and renamed it as “license.dat”. If the license file resides in a separated folder, please set environment variable LM\_LICENSE\_FILE with the proper path.
  - For floating licensing scheme, please download and extract netspeed.flexlmpkg.tar.gz for 32- or 64-bit license daemon and follow FlexLM documentation.

NOTE: Please use a linux machine to unpack release tarball set. Unpack linux tarball set on Windows machines may cause problems with symbolic links.

- The release makes use of Qt libraries covered under LGPL:
  - <http://qt-project.org/downloads>



## 3 Feature Update: Design Methodology

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### 3.1 NEW LOOK OF NOCSTUDIO GUI

Fresh new look of NocStudio GUI. Key features include (1) dock / float support of individual sub-windows (2) added support for new\_soc with fine grained physical specification of Host IPs (3) Re-designed toolbar icons (4) Merging of selective GUI icons to minimize window real estate (5) new command “highlight” is supported with significantly increased color choices. (6) tune\_sibs, tune\_router\_conn, tune\_max\_outstanding and build\_low\_area added for automatic area optimization.

Please note that “Selection”, “Default”, “Mesh” and “Sim” tabs are moved to lower right corner of the screen by default.

### 3.2 CREATING DESIGN WITH UNIFIED DOMAIN MODE

New release allows user to define a unified domain with a common clock, voltage and power domain. All modules within the domain will be part of a RTL group. GUI visualization has been enhanced with outline in the floorplan view.

### 3.3 GUI VISUALIZATION ENHANCEMENTS DURING PERFORMANCE ANALYSIS

GUI tooltip window displays complete detailed information of all links of a router, including lists of flows and traffic activities. The pop-up window can be disabled by setting “prop\_default tooltip\_on no”.

### 3.4 GUI SUPPORT FOR INDIVIDUAL FONT SIZE CONTROL

Each of the Icon size, Console Font, Main Tabs font and Side panel font can now be controlled by the user by clicking “view → Resize Icon and Size”.

### 3.5 NEW HEAT MAP SUPPORT AND POWER MODELING WITH GUI

#### VISUALIZATION DURING SIMULATION – PRELIMINARY

New default property “heatmap\_enabled” can be set to yes for user to visualize the NOC heatmap / activities during simulation. Please refer to NocStudio help manual and search for keyword “heatmap”.

### **3.6 NEW DISPLAY\_NODE\_AS\_X\_Y PROPERTY TO SWITCH BETWEEN NODE ID AND [X,Y]**

This added property allows user to switch GUI node ID display to [x, y] coordinate. The feature improves usability for user to extensively specify [x, y] in the design script file and eases host/bridge relocation and mesh resizing. Please refer to command “resize\_mesh” for details.

### **3.7 NEW COMMAND “RESIZE\_MESH”**

This newly added command allows user to increase / decrease rows and columns in the mesh. Setting “prop\_default display\_node\_as\_x\_y yes” should be used to create highly scalable design flow.

### **3.8 NEXT GEN SOC PHYSICAL FLOORPLAN VIEW – PRELIMINARY**

User specified fine grained definition of the Host IP dimension. Instead of grid/mesh based Host IP size specification with new\_mesh, user can draw the actual size (with um granularity) using new\_soc command. The “chip\_view” in prior releases has been replaced with command “generate\_chip\_view”.

### **3.9 DESIGN CONFIG RULE CHECK (LINT) SUPPORT**

New command “lint” is now supported to check the integrity of the design configuration. Similar to logic linting flow, user can define their own waiver rule file based on the design criteria on per project basis or a corporate wide defined rule.

### **3.10 A SET OF AUTOMATIC AREA OPTIMIZATION COMMANDS AND OPTIONS**

New commands “tune\_sibs” and “tune\_router\_conn” have been added in this release to explore usage of shared interface bridges and optimize router connections. These commands would display a list of applicable property changes in the console window for user review. Invoke the command the 2<sup>nd</sup> time with -apply option to actually apply to a design.

For customers with machine learning licenses, these optimizations are part of the ml\_build - low\_area option.

Thirdly, new command “tune\_max\_outstanding” has been incorporated in this release to automatically optimize max\_outstanding setting based on performance simulations.

### **3.11 SYSTEMC MODELING SUPPORT FOR NON-COHERENT ORION AND PEGASUS DESIGN**

New default property “sysc\_enable” is now supported for Orion and Pegasus product families to generate all files needed for FT (Fast-timed) address-aware systemC modeling environment.

Coming soon: Gemini systemC modeling environment. Please contact NetSpeed support for availability.

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## 4 Feature Updates: System Interconnect

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### 4.1 NEW DEFAULT PROPERTY GEN\_PASSTHROUGHS HAS BEEN ADDED

A new default property “gen\_passthroughs” has been added for design with multiple RTL grouping which allows wires between group A and C to pass through group B. Group B is physically located between A and C.

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## 5 Feature Updates: Non-Coherent Components

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### 5.1 NEW INTERFACE PROPERTY LOW\_LATENCY\_ENABLE FOR BRIDGE LATENCY OPTIMIZATION

A new interface property has been added in this release for both master and slave bridges running at lower frequency to bypass the internal pipeline stages. Each of the AR, AWW, R and B channel can be set individually for user to make best design tradeoffs between latency and frequency.

### 5.2 AHB MASTER BRIDGE AREA REDUCTION

The AHB master bridge has been redesigned to reduce flop cost. Default 32-bits AHB master bridge has shown more than 50% area reduction.

### 5.3 SRAM WRAPPER ENHANCEMENT

Enhancement has been made to RTL generator to define RAM wrapper with generate statement based on the parameters of the RAM configuration.

### 5.4 NEW BRIDGE PROPERTY AXI4M\_TRUSTED\_MASTER

When set, transaction through this master bridge will use the setting in address lookup table for all outgoing transactions (injected) to the NOC.

### 5.5 PROGRAMMABLE HASH FUNCTION SUPPORT IN LLC PRE-LOADER

The LLC pre-loader has been enhanced to support programmable hash function through regbus.

### 5.6 ADDED SUPPORT OF AXI4\_INPUT\_REGISTER FOR RBM

When set, input register flops are added at its inputs. Please note that the property can be set globally using prop\_default or individually using bridge\_prop.

## 6 Feature Updates: Coherent Components

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### 6.1 ADDED SUPPORT FOR NON-COHERENT TRAFFIC SHARING THE COHERENT PATH THROUGH INTEGRATED CCC AGENT

New license controlled feature allows the mapping of non-coherent traffic flow shares with the coherent path – through CCC.

### 6.2 REGFILE SUPPORT FOR CCC PREFETCH BUFFER AND IOCB READ/WRITE BUFFER AND LLC READ BUFFER

A new set of properties to support regfile implementation has been added. Please refer to NocStudio help manual and search for keyword “regfile”.

### 6.3 GLOBAL COHERENCY TRACKER (GCT) STATE RESET SUPPORT

The GCT state can now be cleared during RTL simulation when hardware reset signal is asserted.

## 7 EDA Tool Compatibility

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- Cadence EDA tools were used for verification and synthesis of this product.
  - Incisive RTL Simulator 15.22-s012
  - Genus RTL Synthesis 16.22-s033\_1
  - HAL Linting tool 15.20-s027
  - Conformal 16.20-s240
- Compatibility testing has been done with VCS vcs-mx/L-2016.06 and Synopsys Design Compiler L-2016.03-SP5.
- Please contact NetSpeed support team ([support@netspeedsystems.com](mailto:support@netspeedsystems.com)) for additional platform and tool compatibility details.

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## 8 Errata: System Interconnect

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None

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## 9 Errata: Non-Coherent Components

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None

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## 10 Errata: Coherent Components

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None

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## 11 Errata: Coherent Components

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### 11.1 SYSCOREQ HANDSHAKING FOR ACE MASTER

If using a Netspeed provided voltage-domain crossing with an ACE master, and using a Q-channel to control power-management, then SYSCOREQ shall not be asserted until the Q-channel handshake has reached the Q\_RUN state

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## 12 Errata: Coherent Components

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### 12.1 SYSCOREQ HANDSHAKING FOR ACE MASTER

If using a Netspeed provided voltage-domain crossing with an ACE master, and using a Q-channel to control power-management, then SYSCOREQ shall not be asserted until the Q-channel handshake has reached the Q\_RUN state.

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## 13 Changes to Commands and Properties

Please refer to NocStudio Help → User Manual Supplement for details.

### 13.1 COMMAND CHANGES

| Command Name   | Comment  |
|--|--|
| add_column / del_column  | Add / delete a column to the logical mesh at the position specified in the physical floorplan view   |
| add_domain / del_domain / list_domains                         | Add / delete a single domain with a clock domain, power domains and an RTL group.<br>List all domains  |
| add_row / del_row  | Add / delete a row to the logical mesh at the position specified in the physical floorplan view  |
| add_to_region / del_from_region / list_regions / move_region   | Add / delete a physical region and specify clock domains, power domains, RTL groups.<br>List or move region(s)   |
| add_unwaiver / del_unwaiver / list_unwaivers / reset_unwaivers | This command adds / deletes / resets or lists one or more IDs and/or one or more categories and/or one or more strings to the waiver list used for lint. |
| add_waiver / del_waiver / list_waivers / reset_waivers         | This command adds / deletes / reset or lists one or more IDs and/or one or more categories and/or one or more strings to the waiver list used for lint.  |
| analyze_interface_perf_ratios                                  | Report on interface performance ratios of last sim run   |
| build_low_area   | Build a NoC with lowest possible area  |
| expand_var   | Expand variable and print the result   |
| generate_chip_view   | Draws a physical chip view of the NoC  |
| highlight  | Highlights the filtered NoC components in the specified color (default color is automatically chosen by NocStudio)                                       |
| lint   | This command runs a design verification check (or lint check) on the current NoC,  |

|                               |   |
|-------------------------------|---|
|                               | and presents a report with the errors and warnings that might hinder rtl generation                               |
| list_rtl_groups               | Lists RTL elements in each group  |
| list_channel_tooltips         | <b>Renamed with list_tooltips</b>   |
| load_waiver_list              | This command loads a list of waived/unwaived IDs and/or categories and/or strings for lint                        |
| new_soc                       | This command creates a new blank SoC on which hosts can be drawn using physical coordinates                       |
| permute_router_conn           | Changes the router connections of all provided bridges  |
| reset_node_physical_positions | Resets the physical position of all nodes in the logical grid   |
| reset_upgraded_warning        | Reset the given upgraded warning ID(s) to be warning(s) again   |
| resize_mesh                   | This command is used to change the number of rows and columns in the mesh   |
| save_lint_report              | Save the lint report as a .csv file   |
| set_node_physical_position    | Set the physical position of a node in the logical grid   |
| set_pmf                       | Set the Probability Mass function associated with a name  |
| transform_soc                 | This command transforms the physical floorplan view into the logical mesh view                                    |
| tune_max_outstanding          | Tune the max_outstanding_requests attribute on TX interfaces  |
| tune_router_conn              | Tunes the bridges router connections to minimize the number of distinct routers that the bridges are connected to |
| tune_sibs                     | Automatically adds shared interface bridges wherever possible to reduce the bridge area                           |
| upgrade_warning               | Upgrade the given warning ID to be an error   |

## 13.2 MESH PROPERTY CHANGES

| Property Name                   | Comment                           |
|---------------------------------|-----------------------------------|
| enable_address_aware_simulation | Enables address aware simulation. |

|                                 |  |
|---------------------------------|--|
| flop_density                    | Indicates the flop density (number of flops per um2) for chip view display mode.                                 |
| interrupt_mode                  | Controls the type of interrupt signals that are exposed in ns_soc_ip.v   |
| link_wire_density               | Indicates the wire density (number of wires per um).   |
| link_wire_width_nm              | deprecated   |
| logical_transform_tolerance_cap | The maximum tolerance that can be used to transform the physical positions of objects into the logical positions |
| max_distance_from_sib           | The maximum allowed Manhattan distance in mm between a bridge and an SIB.  |
| register_area_nm2               | deprecated   |
| soc_view_reference_line         | Choose type of lines to show in the SoC view.  |
| soc_view_wire_width_scale       | Scaling factor for width of wires in the SoC view.   |
| tooltip_on                      | deprecated   |
| virtual_ok                      | deprecated   |

### 13.3 HOST PROPERTY CHANGES

| Property Name                               | Comment  |
|---|--|
| cc_directory_hash_mode                      | The type of hashing used in the directory for the CCC.                       |
| cc_interrupt_mask_value                     | This bit vector specifies which events should trigger interrupts in the CCC. |
| cc_pfb_memory_enable                        | Enable regfile implementation for pre-fetch buffer                           |
| cc_pfb_memory_in_width                      | Pre-fetch buffer input width   |
| cc_pfb_memory_out_width                     | Pre-fetch buffer output width  |
| iocb_master_port_rd_buffer_memory_enable    | Enable regfile implementation for the IOCB read buffer                       |
| iocb_master_port_rd_buffer_memory_in_width  | Read buffer input width  |
| iocb_master_port_rd_buffer_memory_out_width | Read buffer output width   |
| iocb_slave_port_wr_buffer_memory_enable     | Enable regfile implementation for the IOCB write buffer                      |
| iocb_slave_port_wr_buffer_memory_in_width   | Write buffer input width   |

|  |   |
|--|---|
| iocb_slave_port_wr_buffer_memory_out_width | Write buffer output width   |
| llc_interrupt_mask_value                   | This bit vector specifies which events should trigger interrupts in the LLC.            |
| llc_master_port_wr_buffer_ram_enable       | deprecated  |
| llc_master_port_wr_buffer_ram_in_width     | deprecated  |
| llc_master_port_wr_buffer_ram_out_width    | deprecated  |
| llc_partialwrite_alloc                     | Specifies whether partial write will trigger read fetch first.                          |
| llc_poison_support                         | Specifies if the ICCC should store poison bits in the data array.                       |
| llc_read_max_outstanding                   | Specifies the number of outstanding read requests the LLC can support from all sources. |
| llc_slave_port_rd_buffer_memory_enable     | Enable regfile implementation for LLC read buffer                                       |
| llc_slave_port_rd_buffer_memory_in_width   | Read buffer input width   |
| llc_slave_port_rd_buffer_memory_out_width  | Read buffer output width  |
| llc_slave_port2_rd_buffer_memory_enable    | Enable regfile implementation for LLC read buffer on 2 <sup>nd</sup> port               |
| llc_slave_port2_rd_buffer_memory_in_width  | Read buffer input width   |
| llc_slave_port2_rd_buffer_memory_out_width | Read buffer output width  |
| llc_write_max_outstanding                  | Specifies the number of outstanding write requests the LLC can support from all sources |

### 13.4 BRIDGE PROPERTY CHANGES

| Property Name                 | Comment   |
|-------------------------------|---|
| allowed_positions             | Sets the positions that this bridge is allowed to move to.                                    |
| axi4_input_register           | enables input registering at the bridge.  |
| axi4m_ar_rob_memory_enable    | renamed _ram_ with _memory_   |
| axi4m_ar_rob_memory_in_width  | renamed _ram_ with _memory_   |
| axi4m_ar_rob_memory_out_width | renamed _ram_ with _memory_   |
| axi4m_trusted_master          | specify if a master should use the address table to determine secure status of a transaction. |



|  |  |
|--|--|
| chi_addr_width<br>chi_cache_stash_en<br>chi_cc_cache_capacity<br>chi_data_check_en<br>chi_data_width<br>chi_direct_cache_transfer_en<br>chi_direct_memory_transfer_en<br>chi_enhanced_features_en<br>chi_hnrn_req_max_outstanding<br>chi_hnrn_snp_max_outstanding<br>chi_node_id_width<br>chi_poison_en<br>chi_rnf_logical_processors<br>chi_rx_dat_output_register<br>chi_rx_req_output_register<br>chi_rx_rsp_output_register<br>chi_rx_snp_output_register<br>chi_rxdат_rsvdc<br>chi_rxreq_rsvdc<br>chi_txdат_link_buffer_depth<br>chi_txdат_rsvdc<br>chi_txreq_link_buffer_depth<br>chi_txreq_rsvdc<br>chi_txrsp_link_buffer_depth<br>chi_txsnp_link_buffer_depth<br>chi_version | CHI support is available upon request.<br>Please contact NetSpeed support for details.               |
| color  | choices of bridge colors are significantly enhanced  |
| lock   | lock/unlock the position of a bridge   |
| run_sib_compatibility_checks   | Allows masters that do not have matching traffic and address ranges to be connected to the same sib. |
| sync_input_register  | deprecated   |

### 13.5 INTERFACE PROPERTY CHANGES

| Property Name                 | Comment  |
|-------------------------------|--|
| host_max_outstanding_requests | Maximum number of outstanding messages from the host's perspective on this interface if its response_id is set (by default, response_id for both tx and rx |

|                    |   |
|--------------------|---|
|                    | Amba request interfaces are set per Amba protocol but are not set for NSIP interfaces). |
| low_latency_enable | Enable pipeline stages internal to the interface channel to be bypassed.                |
| stream_data_packet | If true, then the interface is will stream any data packets that arrive on it.          |

### 13.6 LINK PROPERTY CHANGES

| Property Name          | Comment  |
|------------------------|--|
| domain_crosser_phy_pos | The physical position of the crosser for this link |

### 13.7 ROUTER PROPERTY CHANGES

None

### 13.8 VC PROPERTY CHANGES

None

### 13.9 DEFAULT PROPERTY CHANGES

| Property Name   | Comment  |
|---|--|
| axi4_input_register   | This property applies to AXI4M, AXI3M, ACELM, ACEM, ACELDM, AXI4S, ACELS bridges. If yes, input registering is enabled at the input to the bridge from the host.   |
| axi4m_ar_rob_memory_enable<br>axi4m_ar_rob_memory_in_width<br>axi4m_ar_rob_memory_out_width | renamed _ram_ with _memory_  |
| axi4m_trusted_master  | This property applies to ACELM, ACELDM, AXI4M, AXI3M, AXI4LM, AHBLM bridges. When this property is set, address lookup table is used for filtering and marking security status of outgoing transactions. |

|  |   |
|--|---|
| cc_pfb_memory_enable<br>cc_pfb_memory_in_width<br>cc_pfb_memory_out_width  | renamed _ram_ with _memory_   |
| check_name_validity  | When checking if a name is valid, by default NocStudio will scan many categories of names to see  |
| chi_addr_width<br>chi_cache_stash_en<br>chi_cc_cache_capacity<br>chi_data_check_en<br>chi_data_width<br>chi_direct_cache_transfer_en<br>chi_direct_memory_transfer_en<br>chi_enhanced_features_en<br>chi_poison_en<br>chi_rnf_logical_processors<br>chi_rx_dat_output_register<br>chi_rx_req_output_register<br>chi_rx_rsp_output_register<br>chi_rx_snp_output_register<br>chi_rxdat_rsvdc<br>chi_rxreq_rsvdc<br>chi_txdat_link_buffer_depth<br>chi_txdat_rsvdc<br>chi_txreq_link_buffer_depth<br>chi_txreq_rsvdc<br>chi_txrsp_link_buffer_depth<br>chi_txsnp_link_buffer_depth | A list of bridge property defaults for CHI support  |
| display_node_as_x_y  | This prop can be used to display Node ids as x,y values so the row and column of a node can be quickly identified.  |
| domain_region_show   | This property allows users to control how domain regions are shown in the SoC view  |
| dynamic_power_equation   | This property allows users to provide a formula for computing dynamic power of NoC logic.   |
| gen_passthroughs   | Enabling this flag changes RTL generation to automatically create passthroughs for internal wires whose logical path would pass through a node with rtl group that is |

|   |  |
|---|--|
|   | neither the source nor destination of that wire.   |
| heatmap_enabled   | If yes, NocStudio will compute the power consumption during performance simulation runs, and in a separate tab display the heatmap of the NoC based on the power consumption at various routers and bridges and link |
| heatmap_include_static_power  | If yes, the power computation for heatmap would include the static power consumption.  |
| heatmap_pixels_mm   | The pixel granularity of power sim heatmap.  |
| host_max_outstanding_requests   | This parameter limits the maximum number of outstanding command messages through this interface at a requester/master device for all responder/slave devices   |
| iocb_master_port_rd_buffer_memory_enable<br>iocb_master_port_rd_buffer_memory_in_width<br>iocb_master_port_rd_buffer_memory_out_width | renamed _ram_ with _memory_  |
| iocb_slave_port_wr_buffer_memory_enable<br>iocb_slave_port_wr_buffer_memory_in_width<br>iocb_slave_port_wr_buffer_memory_out_width    | renamed _ram_ with _memory_  |
| llc_master_port_wr_buffer_ram_enable<br>llc_master_port_wr_buffer_ram_in_width<br>llc_master_port_wr_buffer_ram_out_width             | Deprecated   |
| List_region_corners   | This property allows the user to control the format in which regions are printed.  |
| llc_slave_port_rd_buffer_memory_enable<br>llc_slave_port_rd_buffer_memory_in_width<br>llc_slave_port_rd_buffer_memory_out_width       | renamed _ram_ with _memory_  |
| llc_slave_port2_rd_buffer_memory_enable<br>llc_slave_port2_rd_buffer_memory_in_width<br>llc_slave_port2_rd_buffer_memory_out_width    | Renamed _ram_ with _memory_  |
| next_gen_bridge   | This property is used to turn on certain area or performance optimizations in NocStudio that are not yet available in the bridge and router RTL  |
| run_sib_compatibility_checks  | This property can be set to yes to allow masters that have different address ranges  |

|                                   |  |
|-----------------------------------|--|
|                                   | and traffic to connect to the same shared interface bridge                                     |
| shared_doc_enable                 | Indicates generation of redistributable documents is enabled when running gen_ip for this NoC. |
| show_flow_list_in_channel_tooltip | Whether to show the mapped/simulated flows list in VC/Ifce tooltip or not                      |
| static_power_equation             | This property allows users to provide a formula for computing static power of NoC logic.       |
| sync_input_register               | <b>deprecated</b>  |
| sysc_enable                       | Indicates whether SystemC model generation is enabled when running gen_ip for this NoC.        |
| tooltip_on                        | Indicates whether to display tool-tip in NoC display.  |
| wire_power_equation               | This property allows users to provide a formula for computing dynamic power of NoC logic       |

## 14 Hot fixes

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### **14.1 CORRECTED SPLIT SIZE CALCULATION IN NOCSTUDIO**

An issue with split size calculation in NocStudio has been corrected where split size is set greater than the slave range granularity, based on slice bits or defined hash function.

### **14.2 LLC REPLACEMENT POLICY CHANGE**

In 1710 release, the LLC behavior has changed (from 1704) to improve LLC utilization with a better hit rate. However, in certain traffic profiles, the throughput has been degraded. In 1710a release, LLC replacement policy has been reverted back to 1704 like behavior. A property to define LLC replacement policy will be implemented in future release.

2870 Zanker Road,

Suite 210,

San Jose, CA 95134

(408) 617-5209

<http://www.netspeedsystems.com>