NetSpeed Gemini

Release Notes

Version: GEMINI-18.04

Revision: B.2

NetSpeed Gemini 18.04 Release Notes

About This Document

This document lists the release notes for NetSpeed Gemini. Using NetSpeed NocStudio, users can define NoC architectures, describe specifications and requirements, optimize the NoC design and finally generate the NoC IP files such as RTL, testbench, synthesis scripts, NoC IP documentation etc.

Audience

This document is intended for users of NocStudio:

- NoC Designers
- NoC Architects
- SoC Architects

Prerequisite

Before proceeding, you should generally understand:

- Basics of NetSpeed Gemini IP Technology

Related Documents

The following documents can be used as a reference to this document.

- NetSpeed NocStudio User Manual

Customer Support

For technical support about this product, please contact support@netspeedsystems.com

For general information about NetSpeed products refer to: www.netspeedsystems.com

Revision History

Revision	Date	Updates
0.0	Jun 16, 2018	Initial Release
A.0	Jul 02, 2018	FuSa Release
B.0	Aug 15, 2018	Write reorder buffer support on ACE master bridge
B.1	Aug 22, 2018	• Cosmetic fix with confidential watermark • Clarify add_range … –memory_type description • Clarify tune_router_conn description • Removed static_muxing_enable, moved to 1801 release note
B.2		• Added comment for ns_cmn_2p_rf.v parameter change • Rephrase Hot fixes 12.4 with clarification • Added missing performance optimization with reorder buffer

Contents

1 Deliverables

- NetSpeed NocStudio Package and one of the license options:
  - N7 version supporting 16 layers and 256 bridges
  - N6 version supporting 4 layers and 128 bridges
  - N5 version supporting 4 layers and 60 bridges
  - N4 version supporting 2 layers and 32 bridges
  - N3 version supporting 1 layers and 12 bridges
- NocStudio executable with interactive GUI.
- Verification checkers to be used in the DV environment.
- Sanity Test Bench.
- Documentation
  a. NocStudio User Manual: The User Guide describes how to set up a system using NocStudio and how to use it to generate NetSpeed IP.
  b. IP Integration Spec: The Integration Manual describes how to integrate a configured network into a larger subsystem.
  c. Technical Reference Manual: The Technical Reference Manual describes how the functionality of the various NoC elements, the features and functions available, and how to dynamically change the functions using the programmer's mode.

2 Installation

- NocStudio uses FlexLM based licensing.
  - Linux CentOS 5.5 or higher
  - For node-locked license file, copy over the license file under NocStudio installation directory and renamed it as "license.dat". If the license file resides in a separated folder, please set environment variable LM_LICENSE_FILE with the proper path.
  - For floating licensing scheme, please download and extract netspeed.flexlmpkg.tar.gz for 32- or 64-bit license daemon and follow FlexLM documentation.

  NOTE: Please use a Linux machine to unpack release tarball set. Unpack Linux tarball set on Windows machines may cause problems with symbolic links.

- The release makes use of Qt libraries covered under LGPL:
  - http://qt-project.org/downloads

3 Feature Update: Design Methodology

3.1 REGBUS LAYER POWER DOMAINS

The new release enables users to assign power domains to the routers in the regbus layer from GUI.

3.2 SIB GUI ENHANCEMENT

The new and improved GUI enables the users to view the connections of the master bridges to their respective SIBs.

3.3 NOTICEABLE COMMAND CHANGES

- A new option has been added to add_range command to specify the memory type. This allows user to define the AxCACHE [1] bit override behavior.
    - Memory type = "unspecified" (default). The master bridge transports the AxCACHE bits from the external AMBA host to the NOC as is.
    - Memory type = "device". Some legacy AMBA host or host with software restriction who cannot assert AxCACHE [1] dynamically, user can define such range as "device" for the master bridge to override AxCACHE [1] as non-modifiable (1'b0) all the time.
    - Memory type = "normal". The master bridge will always override AxCACHE [1] as modifiable (1'b1) for transactions targeting this particular range.

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3.4 APB INTERFACE TO SUPPORT USER BITS

User can now enable user sideband on APB interfaces which allows NOC transport of these bits from AXI or ACE masters to APB slaves. These bits are user specific implementation; the NOC doesn't care their value at all times as long as they meet standard interface timing, like all other AMBA signals.

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3.5 ENHANCED LLC PRELOADER CAPABILITY WHEN PROGRAM LLC IN RAM MODE

NetSpeed Pegasus supports preload API task to shorten the simulation start-up time. When the Pegasus in a design has been configured to support both Cache and the RAM mode, the

preloader_init API has been enhanced to preload according to the programmed configuration (from Pegasus registers) instead of the original (default) configuration.

3.6 HIERARCHICAL GENERATION OF NOC_REFERENCE_MANUAL.HTML

In this release, the noc_reference_manual.html by "gen_ip" has two changes: (1) the file has been broken into multiple chapters for minimum wait time while opening (2) all supporting files (chapter*.html) including the top level noc_reference_manual.html has been moved under the <project>/reference_manual sub-folder.

3.7 DUAL PORT REGFILE SUPPORT IN SRAM SANITY TESTBENCH

The SRAM sanity testbench has been enhanced with dual-port regfile support. In addition to the standard tests for single ported RAM and regfile, concurrent read / write test has been added.

Please note that a new module parameter P_NO_INPUT_REG has been added to module "ns_cmn_2p_rf.v" to support all possible regfile implementations.

4 Feature Updates: System Interconnect

4.1 SUPPORT FOR AW CHANNEL REORDER BUFFER FOR ACE MASTER BRIDGE

Due to high probability of coherent system deadlock, in release 1710 and 1801, the ACE master bridge doesn't support reorder buffer. The performance impact may be significant even the coherent host is performing non-coherent accesses.

In this release, NocStudio has removed such restriction and user can now set axi4m_aw_reorder_enable = "yes" on ACEM bridges which will improve non-coherent write, therefore system performance.

5 Feature Updates: Non-Coherent Components

TBD

6 Feature Updates: Coherent Components

TBD

7 EDA Tool Compatibility

- Cadence EDA tools were used for verification and synthesis of this product.
  - Incisive RTL Simulator 15.22-s018
  - Genus RTL Synthesis 16.22-s033_1
  - HAL Linting tool 15.20-s027
  - Conformal 16.20-s240
- Compatibility testing has been done with VCS vcs-mx/L-2016.06 and Synopsys Design Compiler L-2016.03-SP5.
- Please contact NetSpeed support team (support@netspeedsystems.com) for additional platform and tool compatibility details.

8 Errata: System Interconnect

8.1 Low Power Regression

A regression failure is still under debug at the time of the release. For low power design, please contact NetSpeed support for further details.

9 Errata: Non-Coherent Components

None

10 Errata: Coherent Components

None

11 Changes to Commands and Properties

Please refer to NocStudio Help → User Manual Supplement for details. Highlighted text is for the latest sub release version.

11.1 Command Changes

Command Name	Comment
tune_router_conn	New command to automatically configure router connections of bridges to build a NOC topology logically when the floorplan information is not available.
reset_router_conn	New command to undo the effects of tune_router_conn.
gather_bridges	New command to move the position of a bridge near a specified node. In conjunction with tune_router_conn, certain manual steps can be eliminated.

11.2 Mesh Property Changes

None.

11.3 Host Property Changes

llc_master_port_wr_buffer_memory_enable	deprecated for Pegasus and ICCC
llc_master_port_wr_buffer_memory_in_width	deprecated for Pegasus and ICCC
llc_master_port_wr_buffer_memory_out_width	deprecated for Pegasus and ICCC

11.4 Bridge Property Changes

Property Name	Comment

axi4m_firewall_enable	New property to enable firewall security on a master bridge
axi4m_firewall_secure_groups	New property to specify the number of secure groups a master bridge support
sib_allow_different_ranges	New default property allows master bridges that connect to a SIB to have different address ranges
sib_compress_range_groups	New property to use a common set of address range registers in the SIB for masters that have identical ranges. This property is only settable when the SIB supports different address ranges on masters.
ahb_rd_undefined_increment_mode	New property to set the type of read undefined increment mode used by the AHB master
flop_structure_parity_enb	New property to enable flop structure parity on structures inside a bridge
flop_structure_parity_granularity	New property to set the granularity of flop structure parity on a bridge
axi4m_ar_support_interleaved_resp	This property is now available on ACE master bridges
apb_user_bits_enabled	New property to enable user bit ports on APB bridges
axi4m_aw_reorder_enable	This property is now extended to support ACE master bridges

11.5 Interface Property Changes

None

11.6 Link Property Changes

None

11.7 Router Property Changes

None

11.8 VC Property Changes

None

11.9 Default Property Changes

Property Name	Comment
show_flow_list_in_channel_tooltip	deprecated
axi4m_firewall_enable	New default property to enable firewall security on all master bridges
axi4m_firewall_secure_groups	New default property to specify the number of secure groups a master bridge support
sib_allow_different_ranges	New default property allows master bridges that connect to a SIB to have different address ranges
flop_structure_parity_enb	New default property to enable flop structure parity on structures inside all bridges
flop_structure_parity_granularity	New default property to set the granularity of flop structure parity on all bridges
gui_latency_histogram_num_ranges	New default property to set the number of ranges in latency histogram plots generated by the performance simulator

12 Hot Fixes

12.1 Corrected Missing Interface In Perf Sim

An issue with interface missing in the perf sim report has been corrected. The root cause was related to how NocStudio models round-robin arbitration. After reordering part of the modeling code sequence in NocStudio at flit-boundary, the issue has been resolved.

12.2 Corrected Missing Registers In NOC_REGISTERS.CSV

A missing register "llc_read_discard_dirty" in noc_registers.csv has been corrected in this release.

12.3 Correctable ECC Error Behavior Change

When an ECC capable design is configured to support separated fatal and non-fatal interrupt wires, any correctable ECC error would trigger the non-fatal interrupt in this release. In prior release(s), the same error would trigger the fatal interrupt instead. Please contact NetSpeed support for details.

12.4 Latency number discrepancy reported by NocStudio

The LLC Data RAM property is a configurable property in NocStudio. In prior release, the latency set by the user was not properly taken into account when NocStudio generates the latency summary table in noc_reference_manual.html. The issue has been corrected in this release.

12.5 Rate Limiter discrepancy among documentation

The rate limiter register (BTRL) has 12-bits of starting weight. In various places in TRM or noc_reference_manual.html, it was mistakenly described as 8 or 16 bits. All documentation has been corrected.

12.6 Incorrect derivation of axi4s_r_interleave parameter to AHB and APB slave protocol modules with prop_default

The property was incorrectly applied to AHB and APB protocol bridges when using prop_default. Users can simply workaround the issue using individually applied bridge_prop. The problem has been corrected in this release.

12.7 INCORRECTLY DEFINED SDC CONSTRAINTS WITH RTL GROUPS

A synthesis constraint generation mistake (on set_clock_groups) has been corrected with RTL grouping feature enabled.

12.8 INCORRECT SCRATCHPAD RANGE CHECK IN NOCSTUDIO

A false LLC add_range check (ERROR [2867]) has been corrected. The configuration file parser incorrectly detects number of bits in the mask field.

12.9 OPTIMIZATION FOR TRANSACTION ORDERING WITH REORDER BUFFER

The purpose of reorder buffer in master bridge is to resolve the ordering hazard so it can deliver the request(s) early and manage out-of-order response(s) using its reorder buffer. There were cases the master bridge stalls (with pessimism) even when reorder buffer is enabled, likely due to different VC to different slaves originated with the same AID.

NocStudio has been enhanced to detect certain condition during mapping and set newly added Verilog parameter P_*_COS_STALL_ENB accordingly.

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None

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12.10 MISSING DEF FILES FOR RTL GROUPS

A DEF file generation issue with set_rtl_group has been corrected in this release.

12.11 SIB REQUEST SPLIT SIZE PROPERTY SET TO DEFAULT ACCIDENTALLY

A property derivation issue has been corrected in this release. In designs using SIB (Shared Interface Bridge), NocStudio may incorrectly override the axi4m_request_split_size which was set by the user previously. The issue may impact on performance, but not on functionality.

12.12 PEGASUS CACHE FLUSH ENGINE FAILS TO INVALIDATE CLEAN LINES

An issue has been corrected regarding hardware based cache lines invalidation. In prior release, system firmware engineer can work-around the issue using software based approach. Please contact NetSpeed support for details.

12.13 REMOVAL OF FUNCTIONAL SAFETY RELATED SIGNALING IN GENERATED RTL WHEN FEATURE NOT ENABLED

In this release, NocStudio RTL generator has been corrected to skip RTL signals when FuSa feature (ECC / Parity) are not enabled.

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