



CFG Orion

Release Notes

Version: ORION-19.07L

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CFG Orion 19.07L Release Notes

About This Document

This document lists the release notes for CFG Orion. Using CFG NocStudio, users can define NoC architectures, describe specifications and requirements, optimize the NoC design and finally generate the NoC IP files such as RTL, testbench, synthesis scripts, NoC IP documentation etc.

Audience

This document is intended for users of NocStudio:

- NoC Architects
- NoC Designers
- SoC Architects

Prerequisite

Before proceeding, you should generally understand:

- Basics of Network on Chip technology
- AMBA interconnect standards

Related Documents

The following documents can be used as a reference to this document.

- CFG NocStudio Orion User Manual
- CFG Orion IP Integration Spec

Customer Support

For technical support about this product and general information, contact CFG Support.

Revision History

Revision	Date	Updates
0.0	Jul 19, 2019	Initial Version

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1 DELIVERABLES

- CFG NocStudio Package contains N7 version of the tool supporting 16 layers and 256 bridges.
- NocStudio executable with interactive GUI.
- Verification checkers to be used in the DV environment.
- Sanity Test Bench.
- Documentation
 - a. NocStudio User Manual: The User Guide describes how to set up a system using NocStudio and how to use it to generate CFG IP.
 - b. IP Integration Spec: The Integration Manual describes how to integrate a configured network into a larger subsystem.
 - c. Technical Reference Manual: The Technical Reference Manual describes how the functionality of the various NoC elements, the features and functions available, and how to dynamically change the functions using the programmer's mode.

2 INSTALLATION

2.1 LICENSING

NocStudio uses FlexLM based licensing hosted by Intel Central Licensing group using two dedicated license servers: one in Santa Clara and the other is located in Israel.

In addition to LM_PROJECT, a linux environmental variable *NETSPD_LICENSE_FILE* shall be set as shown below in order to access the licenses. The LM_PROJECT is essential for users not to check out the wrong combination of license features by accident.

```
setenv NETSPD_LICENSE_FILE
```

```
7010@netspeed01p.elic.intel.com:7010@netspeed02p.elic.intel.com
```

For teams without LM_PROJECT defined, a node-locked license file may be issued. Simply copy over the license file under NocStudio installation directory and renamed it as “license.dat”. If the license file resides in a separated folder, user may set environment variable *LM_LICENSE_FILE* before opening NocStudio.

2.2 DELIVERABLES / TARBALL SET

The CFG IPs and their configuration tool NocStudio have been packaged individually for maximum flexibility allowing mix and match. Each release is tagged with <yy><mm> where yy is the last 2 digits of the year and mm is the month in integer. As an example, release in Jan 2019 will be referenced as 1901 release. Un-tar all individual tarballs delivered as part of the tarball set using the command below.

```
linux% tar zxvf <tarball_name>.tar.gz
```

Here is a snippet of tarball set in 1907L release: netspeed-<release>.<package>.tar.gz

Tarball name	Description	Category
netspeed-1907L.tar.gz	NocStudio	Base
netspeed-1907L.cruxpkg.tar.gz	Crux IP package (non-AMBA)	NSIP IP
netspeed-1907L.orionpkg.tar.gz	Orion IP package	AMBA IP
netspeed-1907L.geminipkg.tar.gz	Gemini IP package	AMBA IP
netspeed-1907L.pegasuspkg.tar.gz	Pegasus IP package	AMBA IP



netspeed-1907L.ocppkg.tar.gz	OCP support package	Connectivity
netspeed-1907L.daupkg.tar.gz	Deadlock Avoidance Unit	System
netspeed-1907L.syscpkg.tar.gz	SysC (PA) support package	Flow
netspeed-1907L.cpp61pkg.tar.gz	C++ Modeling API support package for gcc 6.1	Flow

Note:

The release makes use of Qt libraries covered under LGPL: <http://qt-project.org/downloads>

3 FEATURE UPDATES

3.1 GUI ENHANCEMENTS

In this release, a few GUI enhancements have been implemented for ease of access, as follows:

- Double-clicking on a layer performs fit-view for that layer. Double-clicking again returns to the default view.
- GUI “File” menu now lists the history of the recent config files sourced by NocStudio.

3.2 SINGLE NOCSTUDIO RELEASE

In this release, CFG has merged traditional NocStudio (Orion, Gemini and Crux) and SCF NocStudio into a single binary. The license key feature “SCF” and NocStudio command “enter_scf_mode” enables the corresponding product features for Intel specific CMS, CRS, SBO, CHA and so on. A separated license “COREKIT” can be enabled to generate Collage compatible corekit collaterals for server SOC project.

3.3 NOC_REGISTERS.XML

In this release, in addition to standard noc_registers.csv and noc_reference_manual.html, NocStudio also generates the NOC Registers in XML which is easier for RDL conversion.

3.4 TRACE AND DEBUG FEATURE WILL BE DEPRECATED IN 1910

In order to support CFG long term strategy to be compliant with Intel chassis, PMON, VISA .. etc. strategy, Trace Probe will no longer be supported in next 1910 release and onwards. For existing AMBA based design, please explore UltraSOC, ARM or any externally available 3rd party tools for coreSight support.

3.5 MULTIPLE REGBUS SUPPORT

In this release, NocStudio supports multiple RegBus layers in a design. During new_mesh creation, user can specify the number of regbus layers in addition to NOC layers. Use *set_node_regbus_layer* to specify all nodes to be included in a specific regbus layer.

3.6 SPYGLASS CDC

In this release, a “cdc” folder has been created by NocStudio during “gen_ip” to provide preliminary support for CDC waiver file which allows user to invoke Spyglass flow and get an abstract model.

3.7 UPF 2.0

In this release, NocStudio generates UPF 2.0 for low-power designs. CFG plans to deprecate UPF 1.0 support so customer should migrate to UPF 2.0 based flow as soon as possible. Please contact CFG Support for more details.

3.8 SECURITY INTERRUPT CHANGES

In this release, in addition to existing combined, per-module interrupt options, NocStudio allows users to enable separate security interrupt(s) only for security (firewall) violation purpose. Please refer to Technical Reference Manual Interrupt section for details.

3.9 USER DEFINED TIME UNIT FOR SDC CONSTRAINTS

Due to library implementation difference, new default property *“prop_default sdc_time_unit [ps|ns]”* is now supported for NocStudio to generate SDC constraints in “ns” or “ps” time unit. For compatibility purpose, the prop defaults to “ns”.

3.10 CONFIGURABLE SLAVE BLOCK FEATURE COMPLETE

CFG has completed all intended feature for Configurable Slave Block in this release and will transition to maintenance mode.

3.11 SINGLE POISON BIT IN LLC

The feature allows user to specify 1 poison bit for every 256 bits of data instead 4-bits in prior releases. A new property *“P_LLC_SINGLE_BIT_POISON”* has been added, please refer to NocStudio help manual for details.

3.12 STAMPING ENHANCEMENT

In this release, node-stamping flow has been enhanced to support for low-power and ILDC (In-Link Domain Crosser) based designs with limitations. New naming support for user to specify pipeline stages separately on data link and credit link has been added. Please refer to Technical Reference Manual Stamping Support chapter for details.

3.13 MODELING API AND PA-ULTRA COMPATIBILITY ENHANCEMENT

In this release, the NOC modeling API has been enhanced to support unique AID and QoS override enabled design.

4 HOT FIXES

4.1 CLOCK GATING SIGNAL PROPAGATION FOR ILDC

An issue with the clock gating signal *cg_busy* not propagating through the ILDC has been corrected. Without this fix, the NOC may miss clock gating opportunity, resulting higher power consumption.

4.2 PIPELINE LOCATION IN DEF FILE

A mis-calculated pipeline location in DEF files has been corrected. On any link spanning long distance, the pipeline modules in the DEF file should be placed uniformly across in this release.

4.3 GUI FIXES

- The show_latency related to SIB on latency breakdown has been corrected.
- An issue with bandwidth report when there is partial transfer has been corrected.

5 EDA TOOL COMPATIBILITY

- Cadence EDA tools were used for verification and synthesis of this product.
 - Xcelium 19.03-s003
 - Design Compiler RTL Synthesis N-2017.09-SP3
 - HAL Linting tool 15.20.027
 - Conformal 16.20.s240
- Compatibility testing has been done with VCS N-2017.12-SP2-4.
- For Platform Architect, used GCC version is gcc-6.1.0a. (Backward compatible upto gcc-5.2.0-64)
- Please refer to IP Integration specification to enable/disable specific CFG checker in order to resolve or workaround any verification related issues, if any.

Contact your CFG or Synopsys support team for assistance.

6 ERRATA

6.1 STAMPING RESTRICTION

Node-stamping doesn't support user inserted pipeline stages between the regbus layer router and regbus ring slave. Please contact CFG support if your design requires such configuration options.

6.2 UPF SUPPORT

UPF 2.0 support for VCLP is limited to single NOC design. There is known issue in UPF 1.0 flow in this release, please contact CFG support for designs can't migrate to UPF 2.0.

7 CHANGES TO COMMANDS AND PROPERTIES

7.1 COMMAND CHANGES

None

7.2 DEFAULT PROPERTY CHANGES

Property Name	Default Value	Comment
axi4m_ar_rob_memory_in_width	0	This property sets the number of info bits needed as input to the regfiles in the read reorder buffers.
axi4m_ar_rob_memory_out_width	0	This property sets the number of info bits needed as output from the regfiles in the read reorder buffers.
llc_master_port_wr_buffer_memory_in_width	0	This property sets the number of info bits needed as input to the regfiles in the LLC/ICCC master port write reorder buffer.
llc_master_port_wr_buffer_memory_out_width	0	This property sets the number of info bits needed as output from the regfiles in the LLC/ICCC master port write reorder buffer.
llc_slave_port2_rd_buffer_memory_in_width	0	This property is available on all LLC hosts that have an llcs2 bridge. The number of info bits needed as input to the regfiles in the LLC second slave port read reorder buffer.
llc_slave_port2_rd_buffer_memory_out_width	0	This property is available on all LLC hosts that have an llcs2 bridge. The number of info bits needed as output from the regfiles in the LLC second slave port read reorder buffer.
llc_slave_port_rd_buffer_memory_in_width	0	This property is available on all LLC and ICCC hosts that have an llcs bridge. The number of info bits needed as input to the regfiles in the LLC slave port read reorder buffer.

llc_slave_port_rd_buffer_memory_out_width	0	This property is available on all LLC and ICCS hosts that have an llcs bridge. The number of info bits needed as output from the regfiles in the LLC slave port read reorder buffer.
arbitration_mode	Static	This property is used to control the type of arbitration used for the output port of the bridge/router.
compress_strap_enable	No	This property when enabled sets the Strap drivevalue ports to local. config_strap_id command is used as mux to pass values.
tcl_print_mode	Warn-only	This property enables printing all warning messages in tcl mode.

7.3 MESH PROPERTY CHANGES

Property Name	Default Value	Comment
security_interrupt_enable	no	This property is used to expose/tie-off a security interrupt signal from all modules.

7.4 BRIDGE PROPERTY CHANGES

Property Name	Default Value	Comment
sim_aid_enable	no	Deprecated
axi4m_ar_rob_memory_in_width	0	This property sets the number of info bits needed as input to the regfiles in the read reorder buffers.
axi4m_ar_rob_memory_out_width	0	This property sets the number of info bits needed as output from the regfiles in the read reorder buffers.
arbitration_mode	static	This property is used to control the type of arbitration used for the output port of the bridge.



ocp_posted_wr_earlyrsp_enable	no	This property if yes, posted writes with early response are enabled on this master bridge.
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7.5 HOST PROPERTY CHANGES

Property Name	Default Value	Comment
llc_mem_data_out_width	0	This property is available on all LLC and ICC hosts. This property specifies the number of info bits needed as output to the data ram.
llc_mem_data_in_width	0	This property is available on all LLC and ICC hosts. This property specifies the number of info bits needed as input to the data ram.
llc_mem_tag_out_width	0	This property is available on all LLC and ICC hosts. This property specifies the number of info bits needed as output to the tag ram.
llc_mem_tag_in_width	0	This property is available on all LLC and ICC hosts. This property specifies the number of info bits needed as input to the tag ram.
llc_master_port_wr_buffer_memory_in_width	0	This property is available on all LLC and ICC hosts. The number of info bits needed as input to the regfiles in the LLC/ICC master port write reorder buffer.
llc_master_port_wr_buffer_memory_out_width	0	This property is available on all LLC and ICC hosts. The number of info bits needed as output from the regfiles in the LLC/ICC master port write reorder buffer.
llc_slave_port_rd_buffer_memory_in_width	0	This property is available on all LLC and ICC hosts that have an llcs bridge. The number of info bits needed as input to the regfiles in the LLC slave port read reorder buffer.
llc_slave_port_rd_buffer_memory_out_width	0	This property is available on all LLC and ICC hosts that have an llcs bridge. The number of info bits needed as output

		from the regfiles in the LLC slave port read reorder buffer.
llc_slave_port2_rd_buffer_memory_in_width	0	This property is available on all LLC hosts that have an llcs2 bridge. The number of info bits needed as input to the regfiles in the LLC second slave port read reorder buffer.
llc_slave_port2_rd_buffer_memory_out_width	0	This property is available on all LLC hosts that have an llcs2 bridge. The number of info bits needed as output from the regfiles in the LLC second slave port read reorder buffer.

7.6 INTERFACE PROPERTY CHANGES

None

7.7 LINK PROPERTY CHANGES

None

7.8 ROUTER PROPERTY CHANGES

Property Name	Default Value	Comment
arbitration_mode	static	This property is used to control the type of arbitration used for the output port of the router.

7.9 VC PROPERTY CHANGES

None

7.10 CSB STORAGE PROPERTY CHANGES

None

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