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iMCP HTNB32L-XXX - DATABRIEF

Databrief for iMCP HTNB32L-XXX System-in-Package

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Doc. Type: DATABRIEF

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SUMMARY

1. PRODUCT OVERVIEW

iMCP HTNBAT32L-XXX is a highly compact and low-power wireless communication device based on Qualcomm QCX-212 LTE IoT Modem, supporting single-mode 3GPP Release 14 Cat. NB2 IoT connectivity.

FEATURES

- CPU: ARM Cortex M3 @ 204MHz/102MHz/26MHz
- 4 MB NOR flash
- 272Kb SRAM: 256Kb + 16Kb instruction cache
- Digital Interfaces
  - 2x I^2C,
  - 3x UART,
  - 2x SPI,
  - 2-Channel 12-bit ADC,
  - 10x GPIOs:
    - 6x PWM,
    - 4x Timer
    - 1x WAKEUP
    - 1x AON (keeping output during deep sleep)
- Power Supply (range): 2.5 - 4.3V, typical 3.3V (3GPP min. 3.0V)
- Operating temperature: TBD
- Frequency range:
  - LTE low bands: 5, 8, 12, 13, 14, 17, 18, 19, 20, 26, 28, and 85 (698-960MHz)
  - LTE mid bands: 1, 2, 3, 4, 25, 66, and 70 (1710-2200MHz)
- Low-power mode (4 levels):
  - PSM: sub 1uA (M3 idle ~20mA)
  - DRX (2.56 s): 110 µA typically
  - Rx: 10 mA typically
  - Tx: 24 mA typically
- TX output power: up to 14, 20 and 23 dBm
- Antenna Pin Impedance: 50 ohms

PACKAGE

- Type: LGA
- Size: 13x13x1.5mm
- HW Integration:
  - 26 MHz crystal
  - 32.768KHz RTC crystal
  - RF filters and matching networks
  - SP6T Switch (SKY13416)
- eSIM

- Spray shielding (FCC requirement)

INTERFACES

- uSIM: external connection

CERTIFICATIONS

- FCC/ISED
- CE
- ANATEL

SECURITY

- Hardware encryption and decryption module (AES and SHA)
- Flash encryption
- True random number generator
- Non-Removable UICC
- Secure boot
- Secure Sockets Layer (SSL), Transport Layer Security (TLS), Datagram Transport Security (DTLS).

SOFTWARE FEATURES

- Location: ECID, OTDOA (LTE-based positioning) – network dependent
- FreeRTOS
- Control via AT Commands according to 3GPP TS27.005, 27.007 and customized AT commands.
- CMSIS
- OpenCPU
- IPv4, IPv6 and non-IP
- User Datagram Protocol (UDP), Transmission Control Protocol (TCP)
- MQTT, CoAP and HTTPS
- Lightweight M2M (LwM2M)

2. PINOUT

2.1. BLOCK DIAGRAM

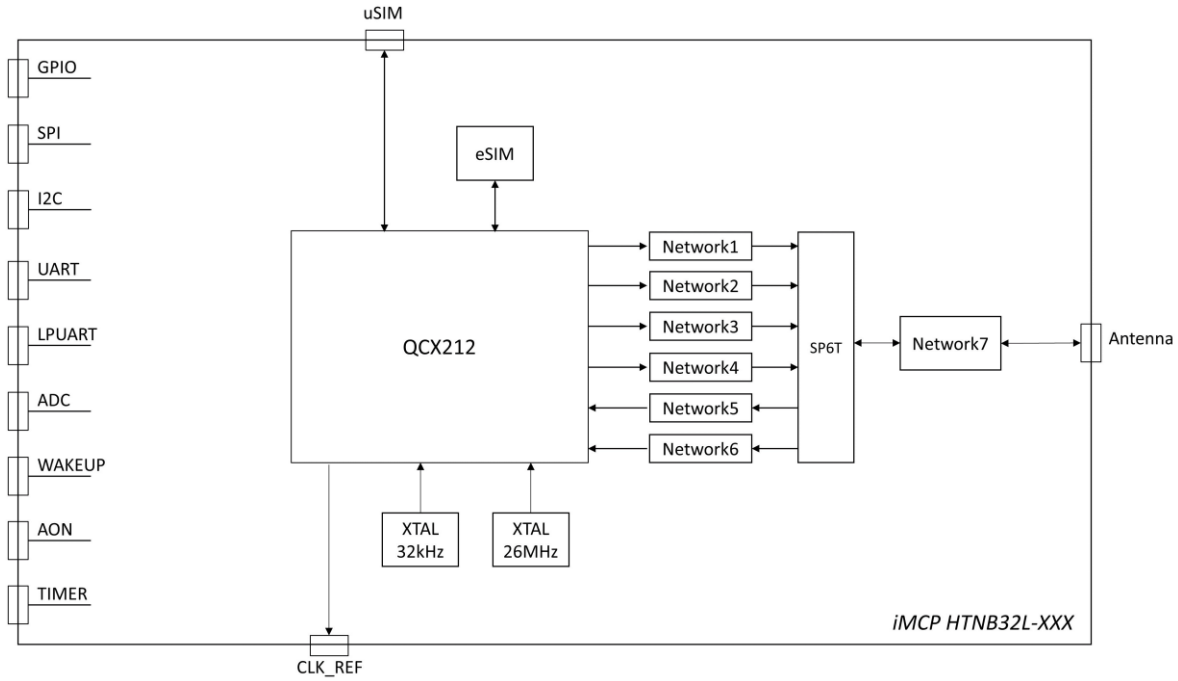


Figure 1: iMCP HTNB32L-XXX block diagram.

2.2. PINOUT

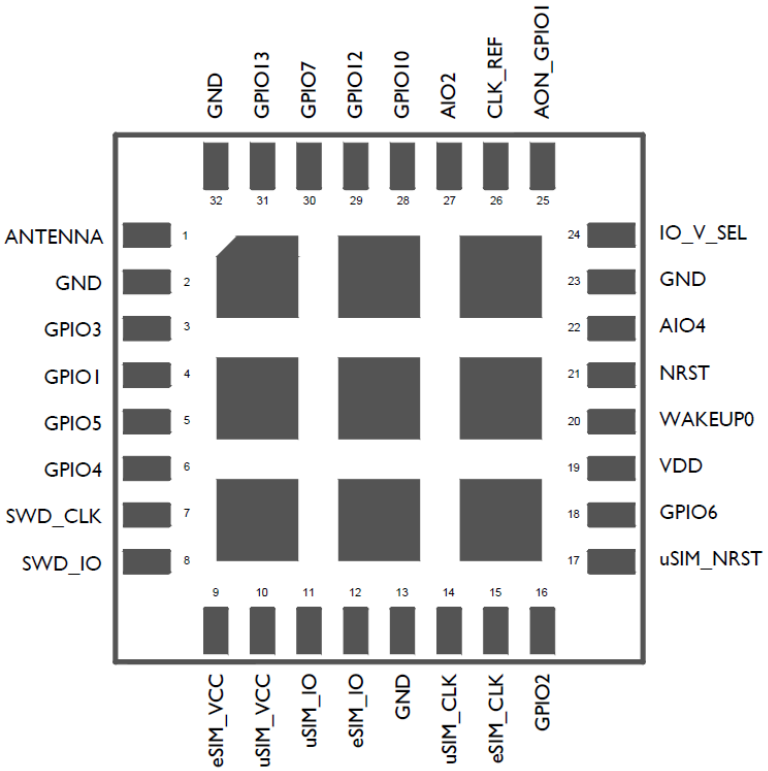


Figure 2: iMCP HTNB32L-XXX pinout.

2.3. PIN DIAGRAM

Table 1: Pinout an alternative function.

Pin Number	PAD name and/or function	Alt. Functions	Type	Functional Description
1	ANTENNA	–	RF	RF Input/Output
2	GND	–	Ground	–
3	GPIO3	UART0_CTSn UART2_TXD SPI1_MOSI PWM1	B-PU:nppd DI DO DO DO	Configurable I/O UART0 clear to send UART2 transmit data SPI1 master out/slave in Pulse-width modulation 1
4	GPIO1	UART2_TXD BOOT_CONFIG	B-PU:nppd DO DI	Configurable I/O UART2 transmit data Boot configuration control bit
5	GPIO5	UART0_TXD I2C1_SCL SPI1_SCLK PWM3	B-PU:nppd DO DO DO DO	Configurable I/O UART0 transmit data I2C1 serial clock SPI1 serial clock Pulse-width modulation 3
6	GPIO4	UART0_RXD I2C1_SDA SPI1_MISO PWM2	B-PU:nppd DI B DI DO	Configurable I/O UART0 receive data I2C1 serial data SPI1 master in/slave out Pulse-width modulation 2
7	SWD_CLK	–	DIO	Serial wire debug clock
8	SWD_IO	–	DIO	Serial wire debug data
9	eSIM_VCC	-	VI	eSIM voltage input
10	uSIM_VCC	-	VO	SIM card voltage output
11	uSIM_IO	-	DIO	SIM card I/O
12	eSIM_IO	-	DIO	eSIM I/O
13	GND	–	Ground	–
14	uSIM_CLK	-	DIO	SIM card clock
15	eSIM_CLK	-	DIO	eSIM clock
16	GPIO19	UART2_TXD PWM5 TIMER [4]	B-PU:nppd DO DO DIO	Configurable I/O UART2 transmit data Pulse-width modulation 5 Counter time [4]
17	uSIM_NRST	-	DIO	SIM card reset
18	eSIM_NRST	–	DIO	eSIM reset
19	VDD	–	Power	Input Power (2.5 ~ 3.6V)
20	WAKEUP0	-	AI	External wakeup source
21	NRST	-	AI	System reset / Active-low
22	WAKEUP3	-	AI	External wakeup source
23	GND	–	Ground	–
24	IO_V_SEL	-	AI	I/O voltage selection Floating 1.8V 0: 3.3V
25	AON_GPIO1	AON_GPIO1 GPIO20	DIO-PD:nppu	Always on I/O Configurable I/O

		TIMER [5]		Counter time [5]
26	GND	-	Ground	–
27	AIO2	-	AIO	ADC channel
28	GND	–	Ground	-
29	GPIO12	SPI0_SCLK I2C1_SCL UART1_TXD PWM1	B-PU:nppd DO DO DO DO	Configurable I/O SPI0 serial clock I2C1 serial clock UART1 transmit data Pulse-width modulation 1
30	GPIO7	SPI0_MOSI I2C0_SCL UART1_CTSn PWM5	B-PU:nppd DO DO DI DO	Configurable I/O SPI0 master out/slave in I2C0 serial clock UART1 clear to send Pulse-width modulation 5
31	GPIO13	SPI0_MISO I2C1_SDA UART1_RXD PWM0	B-PU:nppd DI B DI DO	Configurable I/O SPI0 master in/slave out I2C1 serial data UART1 receive data Pulse-width modulation 0
32	GND	–	Ground	–

2.4. Pin Alternate Functions

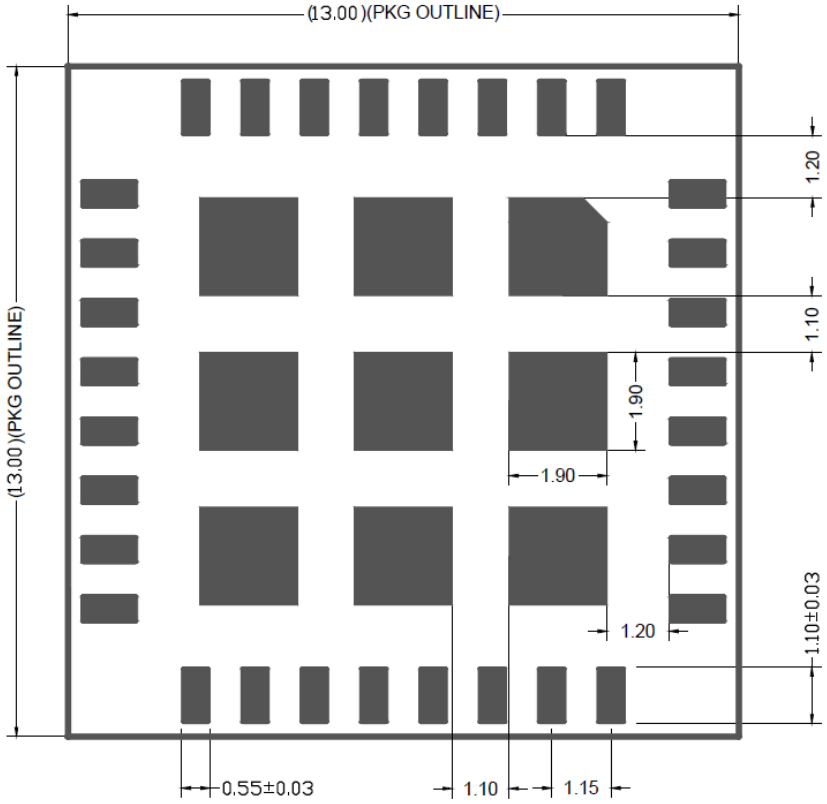
Table 2: Pin alternate functions.

Pad Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
GPIO3	GPIO3	UART0_CTSn	UART2_TXD	SPI1_MOSI	–	PWM1	–	–
GPIO1	GPIO1	–	UART2_TXD	–	–	–	–	–
GPIO5	GPIO5	UART0_TXD	I2C1_SCL	SPI1_SCLK	–	PWM3	–	–
GPIO4	GPIO4	UART0_RXD	I2C1_SDA	SPI1_MISO	–	PWM2	–	–
SWD_CLK	SWD_CLK	–	UART2_RXD	UART1_RTSn	–	PWM4	–	GPIO18
SWD_IO	SWD_IO	–	UART2_TXD	UART1_CTSn	–	PWM5	–	GPIO19
GPIO2	GPIO2/Timer0	UART0_RTSn	UART2_RXD	SPI1_SSn0	–	PWM0	–	–
GPIO6	GPIO6/Timer1	SPI0_SSn0	I2C0_SDA	UART1_RTSn	–	PWM4	–	–
WAKEUP0	–	–	–	–	–	–	–	–
AIO4	–	–	–	–	–	–	–	–
IO_1833_SEL	–	–	–	–	–	–	–	–
AON_GPIO1	GPIO20/Timer5	–	–	–	–	–	–	–
CLK_REF	–	–	–	–	–	–	–	–
AIO2	–	–	–	–	–	–	–	–
GPIO10	Timer3	I2C0_SCL	–	SPI1_SSn1	–	PWM0	–	–
GPIO12	GPIO12	SPI0_SCLK	I2C1_SCL	UART1_TXD	–	PWM1	–	–
GPIO7	GPIO7	SPI0_MOSI	I2C0_SCL	UART1_CTSn	–	PWM5	–	–
GPIO13	GPIO13	SPI0_MISO	I2C1_SDA	UART1_RXD	–	PWM0	–	–

Table 3: Color code for interface identification.

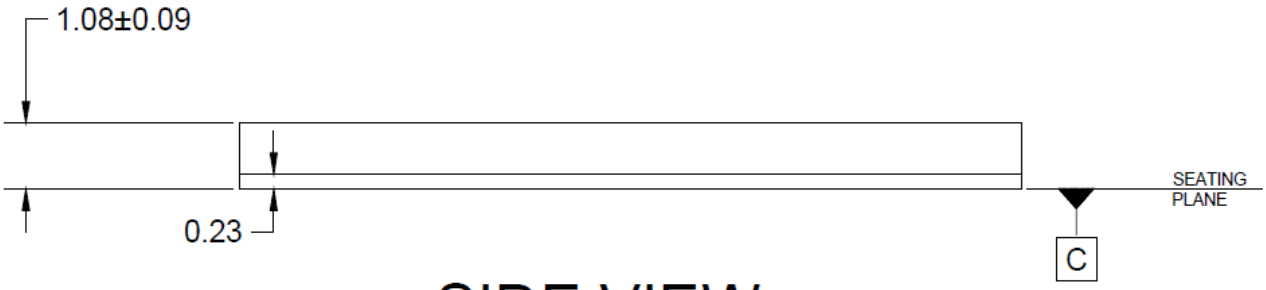
Color	Interface
	UART0
	UART1
	UART2
	SPI0
	SPI1
	I2C0
	I2C1

3. PACKAGE OUTLINE



BOTTOM VIEW

Figure 3: Package outline.



SIDE VIEW

Figure 4: Package outline side view.

4. RECOMMENDED PCB FOOTPRINT

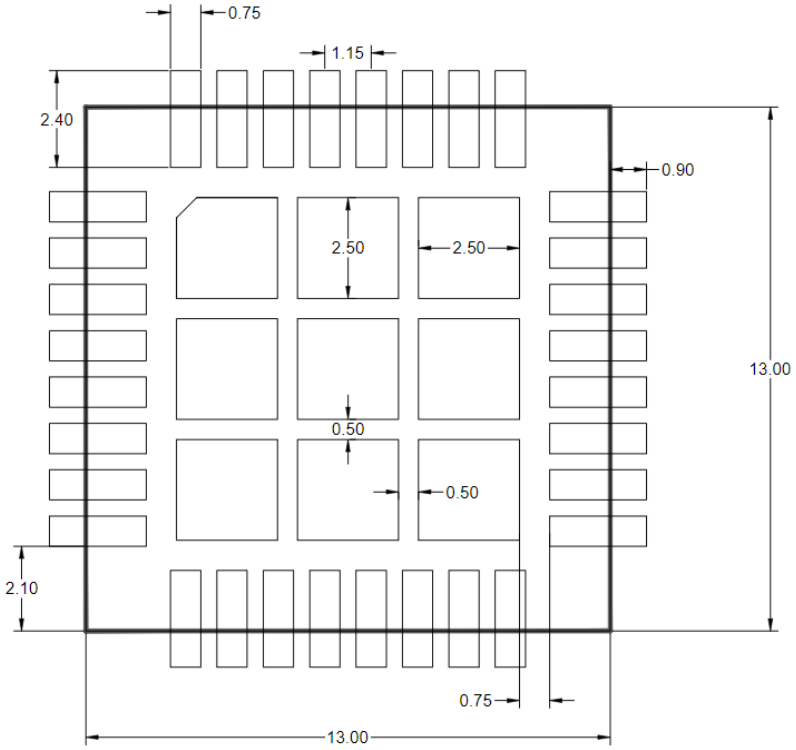


Figure 5: Recommended PCB footprint.

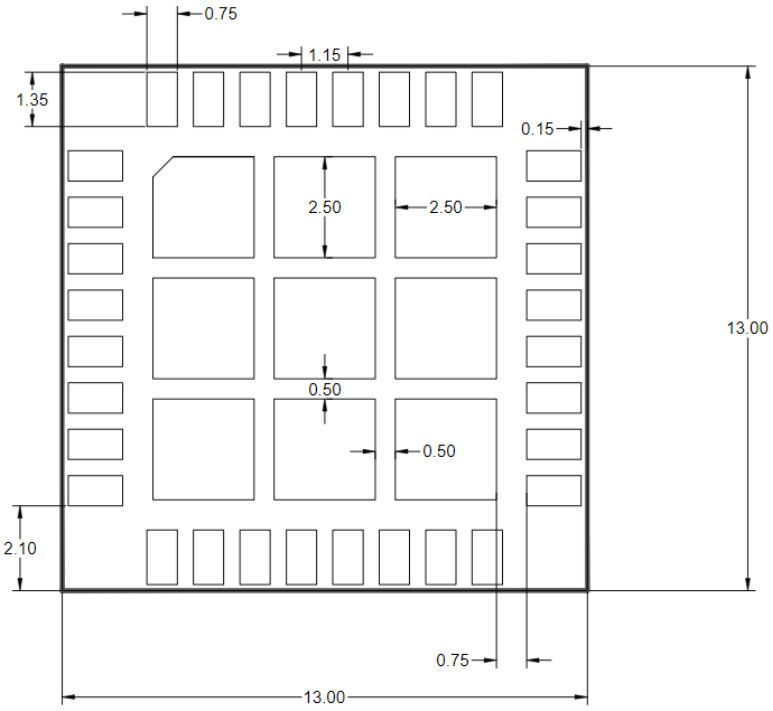


Figure 6: Recommended PCB footprint for shielded HTNB32L-XXX.

5. PART NUMBER

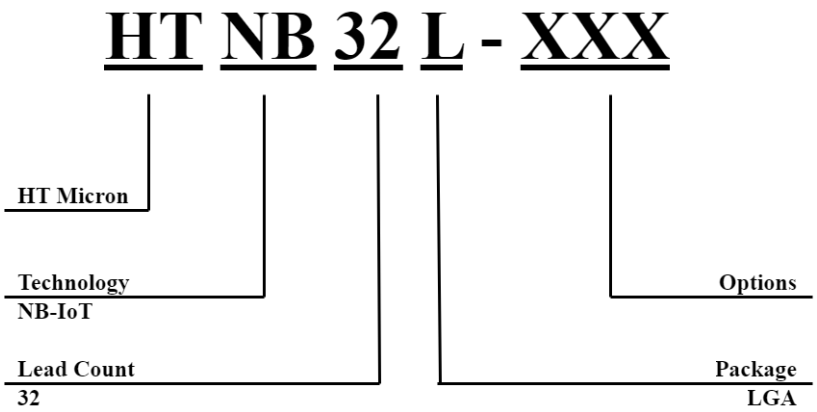


Figure 7: Part Number description.

Table 4: Option table.

Option Number	Version	Shielding	eSIM
000	BR	NO	NO
001	BR	NO	YES
010	BR	YES	NO
011	BR	YES	YES
Z00	GLOBAL	NO	NO
Z01	GLOBAL	NO	YES
Z10	GLOBAL	YES	NO
Z11	GLOBAL	YES	YES

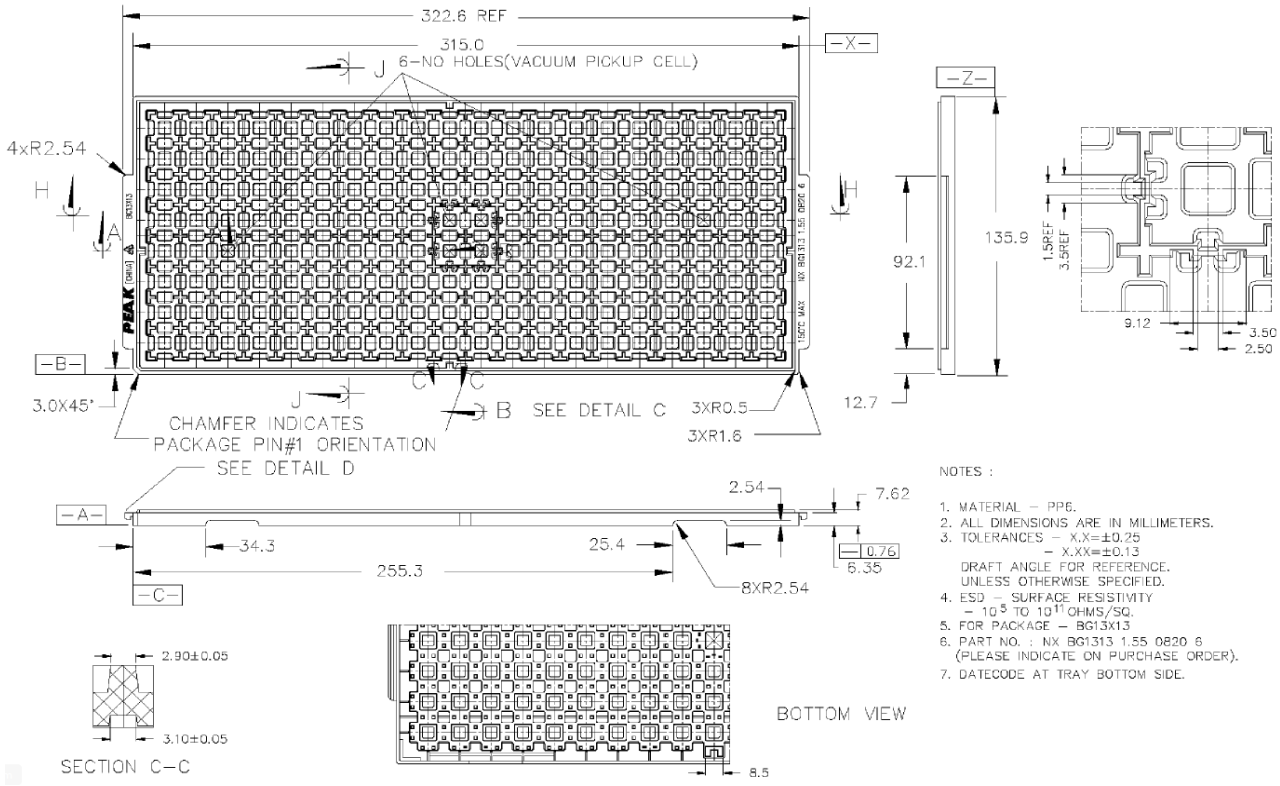
6. PACKAGING AND ORDERING INFORMATION

Table 5: Ordering Information

Part number	Package	
	Name	Description
HTNB32L-XXX	iMCP HTNB32L	SiP module in LGA package; body 13mm x 13mm

Products sold directly by HT Micron will be delivered in bagged trays, sealed in moisture-resistant bags with a desiccant pack and humidity cards. Trays are suitable for baking temperatures. Samples provided by HT Micron may be delivered in other packing methods. Please, refer to section 7 for storage, handling and moisture sensitivity information.

Figure 8: Tray Sizes



7. STORAGE AND HANDLING

CAUTION

ELECTROSTATIC and MOISTURE
SENSITIVE DEVICE

LEVEL 3

- Baking for 24 hours at 125 ±5°C is strongly recommended prior to mounting.
- Take proper precautions to avoid high-energy electrostatic discharge (ESD) as permanent damage may occur.
- For handling methods refer to the latest ESD Association standard ANSI/ESD S20.20.
- Do not expose the device to corrosive gases, extreme humidity, extensive direct sunlight.
- The device is susceptible to delamination or crack damage induced by absorbed moisture and high temperature.
- Shelf life in sealed bagged tray: 12 months at ≤40°C and ≤90% relative humidity (RH).
- This device is rated MSL 3.
- For bagged tray lots: after the bag is opened, the humidity card must read ≤20% (at 23 ±5°C), and the devices must be mounted within 168 hours at environmental conditions of ≤30°C, ≤60% RH.
- If the above condition is not met, baking for 24 hours at 125 ±5°C is mandatory prior to mounting.

- For moisture sensitivity devices precaution methods refer to the latest standard IPC/JEDEC-J-STD-033.
- For any other packing method: baking is required for 192 hours at 40°C prior to mounting.
- This device is composed of all RoHS-compliant materials. Refer to **Error! Reference source not found.** for t ypical Pb-Free reflow conditions.
- Hand soldering is not recommended for this device.
- For moisture sensitivity classification and soldering methods, refer to the latest standard IPC/JEDEC-J-STD-020.
- Do not drop, shock or apply mechanical stress.

8. SOLDERING INFORMATION

Soldering conditions depend greatly on the solder paste that is used and as such are application specific. The picture below depicts typical Pb-free soldering conditions as seen in IPC/JEDEC-J-STD-020 standard, which are commonly used in the industry. However, ultimately, we recommend that the instructions of the solder supplier are followed.

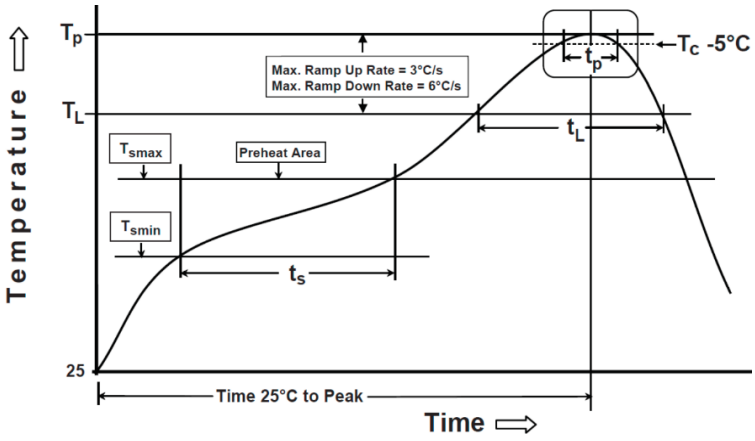


Figure 9: Typical PB-Free Reflow Conditions (IPC/JEDEC-J-STD-020).

Min preheat temperature (T_{smin}): 150 °C
Max preheat temperature (T_{smax}): 200 °C
Preheat (soaking) time (T_s): 60 to 120 s
Liquidous temperature (T_L): 217 °C
Peak temperature (T_p): 260 °C
Max ramp-up rate (T_L to T_p): 3 °C/s
Time above T_L (t_L): 60 to 150 s
Classification temperature (T_c): 260 °C
Time above Tc -5 °C (t_p): 30 s
Max ramp-down rate (T_p to T_L): 6 °C/s
Max time 25°C to T_p: 8 minutes

ABBREVIATIONS

Table 6: Abbreviations

Acronym	Description
GPIO	General Purpose Input Output
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
LPUART	Low-Power Universal Asynchronous Receiver-Transmitter
I2C	Inter-Integrated Circuit
RST	Reset
AON	Always On
ADC	Analog to Digital Converter
MQTT	Message Queuing Telemetry Transport
HTTP	Hypertext Transfer Protocol
CoAP	Constrained Application Protocol
LwM2M	Lightweight M2M
NVM	Non-volatile Memory
SDK	Software Development Kit
PWM	Pulse-Width Modulation
PSM	Power Saving Mode
TCP	Transmission Control Protocol
UDP	User Datagram Protocol

LIST OF FIGURES

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REVISION HISTORY

Version	Date	Changes	Authors
00	22/09/2023	- Initial draft	HBG

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