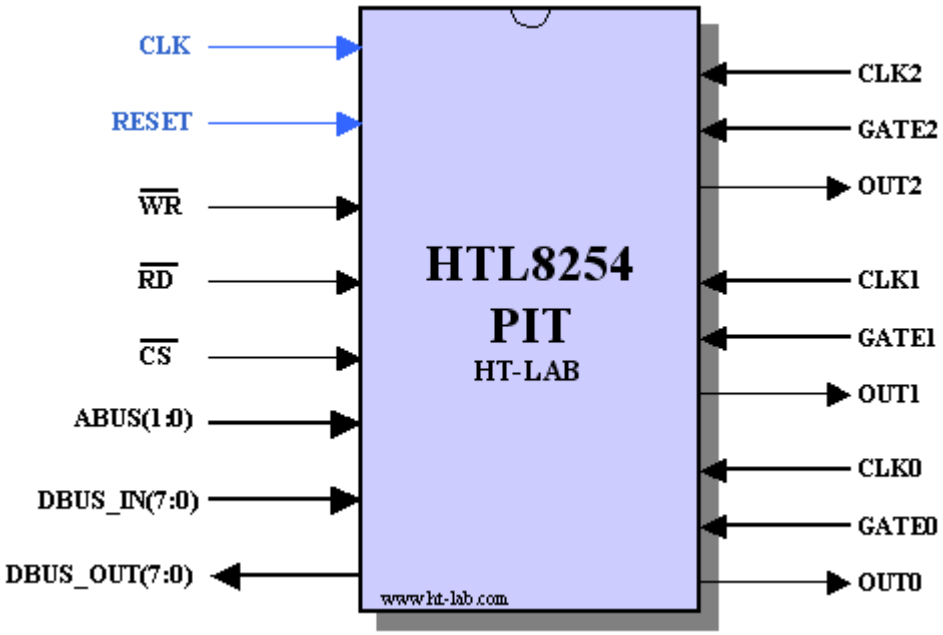
HTL8254

Programmable Interval Timer



Version 1.1
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1. Introduction

The HTL8254 is a compatible synchronous implementation of the industry standard 8254/82C54 Programmable Interval Timer (PIT). The PIT can be used for a wide range of timing functions. The HTL8254 has three independent programmable 16 bits counters each capable of timing and waveform generation capabilities. The HTL8254 is written in vendor neutral VHDL and can be synthesized for either ASIC, FPGA or CPLD implementation.

2. Directory Structure

The HTL8254 IP core is delivered in a single zip file. The directory structure after unzipping is as follows:

Directory	Contents
HTL8254\bin	Any executable files such as utilities (might be empty)
HTL8254\doc	Documentation and Datasheets
HTL8254\rtl	Synthesizable IP Core
HTL8254\testbench	Testbench files
HTL8254\Modelsim	Example script for Modelsim Simulator
HTL8254\synthesis	Synthesis script

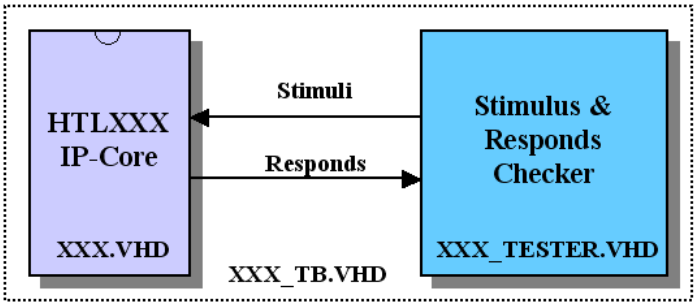
3. Filelist

The HTL8254 RTL design is contained in 7 VHDL files.

Filename	Contains
cemodule.vhd	Counter logic (CE, CR, OL modules)
ctrlword.vhd	Control Word Logic
edge3ff.vhd	Dual FF followed by edge detector
ctrlout.vhd	Finite State Machine controlling OUT signal and counter reloads
gateclk.vhd	Clock and Gate I/O module
timer.vhd	Timer containing all above modules, instantiated for each of the three counters
htl8254.vhd	Top level HTL8254

A further 4 files are used for the testbench.

Filename	Contains
htl8254_tester.vhd	Testbench generic stimulus module
htl8254_tester_wave.vhd	Testbench stimulus to create datasheet wave diagrams
htl8254_tb.vhd	Testbench, instantiates HTL8254 and Tester module
utils.vhd	Testbench support package



4. Simulation

The HTL8254 IP core is written in vendor neutral VHDL and as such can be simulated by any modern simulation tool. The testbench however uses Mentor Graphics' Modelsim *SignalSpy* in order to provide a non-intrusive Counter Element (CE) and OUT signal read.

The testbench contains 2 stimulus files, a general simulus file (*htl8254_tester.vhd*) and a waveform one (*htl8254_tester_wave.vhd*) which generates the 3 "datasheets diagrams" for each of the HTL8254 modes. Both stimulus files are executed using a DOS batch file.

To run the general simulation, execute the ***Modelsim\run.bat*** batch file from a CMD/Dosbox prompt. An equivalent Modelsim run.do file can be executed from within the Modelsim GUI.

The output should be similar to the text shown below (see *expected_output.txt* in the Modelsim directory for the full listing).

```
#  run -all
# ======= Test1 Mode0 CNT0, Status after reset =======
# Status0 : OUT=0 NULL_CNT=0 LMSB MODE0 BINARY CNT=0000
# Status1 : OUT=0 NULL_CNT=0 LMSB MODE0 BINARY CNT=FFFF
# Status2 : OUT=0 NULL_CNT=0 LMSB MODE0 BINARY CNT=FFFF
# ======= Test2 Mode0 CNT0, LSB only, Binary =======
# -- Writing 2 to Count Register LSB
# Counter Element 0 = 0002 OUT0=0
# Counter Element 0 = 0001 OUT0=0
# Counter Element 0 = 0000 OUT0=0
# Counter Element 0 = FFFF OUT0=1
# Counter Element 0 = FFFE OUT0=1
# ======= Test3 Mode0 CNT0, MSB only, Binary =======
..
..
# ======= Test25 Test Mode3 CNT0 Even Initial Value =======
# -- Writing 04 to Counter 0, expect the following sequence 4,2,4,2.....
# Counter Element 0 = 0004 OUT0=1
# Counter Element 0 = 0002 OUT0=1
# Counter Element 0 = 0004 OUT0=0
# Counter Element 0 = 0002 OUT0=1
# ======= Test26 Test Mode3 CNT0 Odd Initial Value =======
# -- Writing 05 to Counter 0, expect the following sequence
5,4,2,5,2,5,4,2,5,2.....
# Counter Element 0 = 0005 OUT0=1
# Counter Element 0 = 0004 OUT0=1
# Counter Element 0 = 0002 OUT0=1
# Counter Element 0 = 0005 OUT0=0
# Counter Element 0 = 0002 OUT0=0
# Counter Element 0 = 0005 OUT0=1
# Counter Element 0 = 0004 OUT0=1
# Counter Element 0 = 0002 OUT0=1
# ** Failure: ***** END OF TEST *****
```

Note: changing the CLKn period in the stimulus file will result in a different output and some tests might fail. For example, Test12 expect the CLKn to be slow enough to detect the *NULL Count* bit in the read-back status byte to go from 1 to 0 after writing a new counter value. If CLKn is too fast then this bit will have been cleared before it is read.

To run the waveform stimulus file, execute the ***Modelsim\runwv.bat*** batch file from a CMD/Dosbox prompt or use the equivalent *runwv.do* inside the Modelsim GUI. A Modelsim waveform screenshot of each mode can be found in *Appendix A to E*.

5. Synthesis

The HTL8254 can be synthesized using any modern synthesis tool. The area and delay figures will depends on the used synthesis tool and settings.
An example batch file for Xilinx XST 11.1 is provided. Navigate to the Synthesis directory and execute ***Synthesis\runxst.bat.*** Make sure that the **xst.exe** executable is in the search path. Part of the log file (HTL8254.syr) based on ISE11.1 is shown below.

```
=====================================================================
*                            Final Report                           *
=====================================================================
Final Results
Top Level Output File Name         : HTL8254
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : YES

Design Statistics
# IOs                              : 32
=====================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-4

 Number of Slices:                      449  out of    960    46%
 Number of Slice Flip Flops:            328  out of   1920    17%
 Number of 4 input LUTs:                794  out of   1920    41%
    Number used as logic:               788
    Number used as Shift registers:       6
 Number of IOs:                          32
 Number of bonded IOBs:                  32  out of     83    38%
 Number of GCLKs:                         1  out of     24     4%


Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 334   |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 10.898ns (Maximum Frequency: 91.760MHz)
   Minimum input arrival time before clock: 4.070ns
   Maximum output required time after clock: 10.345ns
   Maximum combinational path delay: 7.312ns
```

6. Pin Description

Symbol	Type	Function
CLK	I	Clock Input signal Note1,2
RESET	I	Active low Reset signal Note2
WRN	I	Active low Write strobe
RDN	I	Active low Read strobe
CSN	I	Active low Chip Select
ABUS(1:0)	I	Address Bus, see table below
DBUS_OUT(7:0)	O	Databus output
DBUS_IN(7:0)	I	Databus input
CLK0	I	Clock Input for Counter 0 Note3,4
GATE0	I	Gate Input for Counter 0 Note4
OUT0	O	Output of Counter 0
CLK1	I	Clock Input for Counter 1 Note3,4
GATE1	I	Gate Input for Counter 1 Note4
OUT1	O	Output of Counter 1
CLK2	I	Clock Input for Counter 2 Note3,4
GATE2	I	Gate Input for Counter 2 Note4
OUT2	O	Output of Counter 2

Note1: All actions are on the Rising Edge of the system clock.
Note2: This signal is not on the original 8254 device.
Note3: The clock should not exceed clk/6.
Note4: This signal is synchronised to the system clock CLK.

A1	A0	RD	WR	CS	Operation
0	0	0	1	0	Read Counter0
0	1	0	1	0	Read Counter1
1	0	0	1	0	Read Counter2
1	1	0	1	0	Read Control Word
0	0	1	0	0	Write Counter0
0	1	1	0	0	Write Counter1
1	0	1	0	0	Write Counter2
1	1	1	0	0	Write Control Word
x	x	x	x	1	Disabled HTL8254
x	x	1	1	0	Disabled HTL8254

7. Clocking

All internal signals are synchronised to the rising edge of the system clock CLK.

The asynchronous input signals GATEn and CLKn are synchronised to the system clock via a dual Flip-Flop(FF) synchroniser. This means that each input signal edge is delayed by at least 2 system clock periods.

All internal counters (CE) are clocked on the falling edge of the CLKn input. Due to the edge detector and dual FF synchronisers the counters are updated between 1 and 2 system clock periods later than the falling edge of the input clock CLKn.

After programming the mode register (Control Word bit D3..D1), the OUT signal is updated 4 system clock periods later.

For mode 1,2,3 and 5 the GATE input is rising edge sensitive. After the dual FF synchroniser the signal is fed into a rising edge Flip-Flop, the Flip-Flop is reset one system clock period after the rising edge of the synchronised CLKn input.

8. History

Version	Date	Changes
1.0	20/01/2002	First Version
1.0a	7/07/2002	Fixed Gate rising edge logic
1.0b	27/07/2002	Fixed Mode2/3 OUT output (immediately affected by Gate)
1.0c	25/05/09	Minor Tools update, ISE11.1 and Modelsim 6.5a
1.0d	24/10/09	Changed to stop counting on mode changes.
1.0e	13/10/09	Fixed counter gate control for mode0 and rwmode=11
1.1	30/12/09	Changed behaviour if counter is set to 0000 (measured on real device)

9. Observed differences

On some embedded 82C54 cores the counter stops counting when changing mode. The datasheets indicates that the OUT signal will go to the initial state but the counter value itself is undefined ('**N'** in the datasheet diagrams). This behaviour is implemented in version 1.0d, thus the **'N'** value in the datasheets should be considered as **counting disabled**.

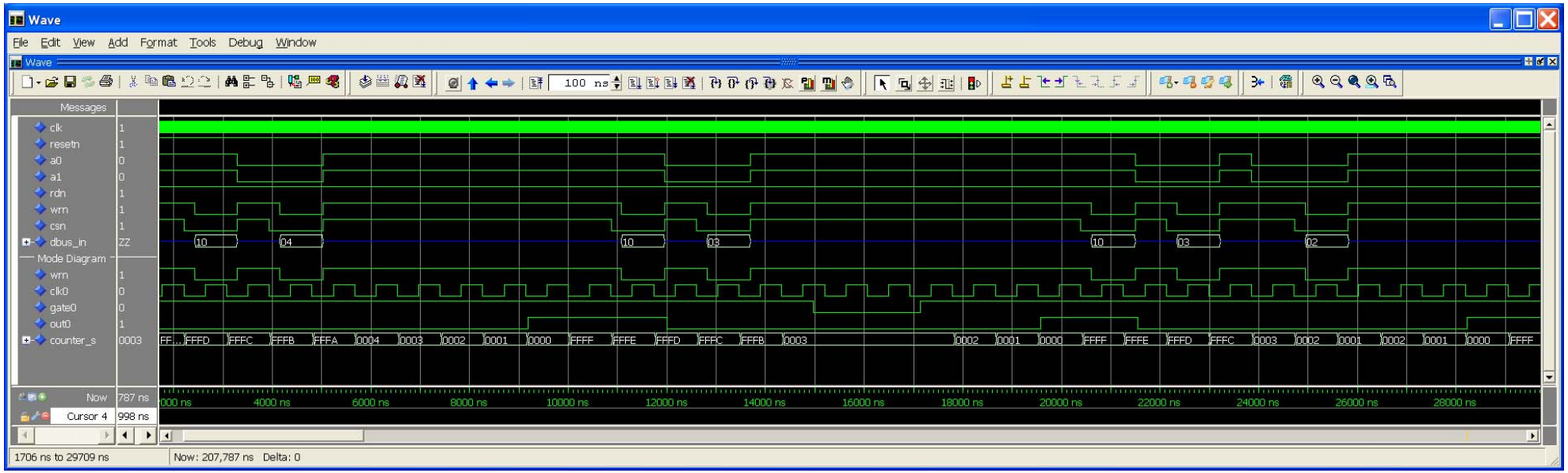
10. Support

For any support issues please use support@ht-lab.com

Trademarks

Spartan and Xilinx are the registered trademarks of Xilinx Inc, San Jose, California, US.
Modelsim is a trademark of Mentor Graphics.

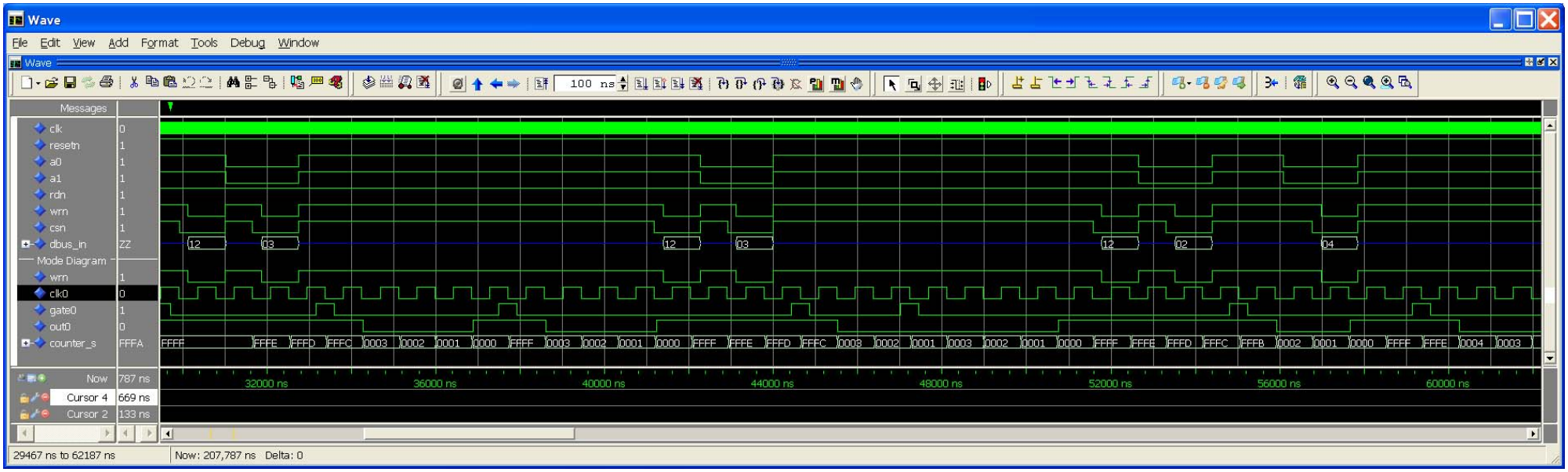
Appendix A Mode 0



Notes:

1) The testbench sets the databus input signal (dbus_in) to Z for visual effect only.
2) Counters are reloaded on the first falling edge of CLKn after the write cycle.
3) GATE=1 enables counting, GATE=0 disables counting.
4) OUT is low after setting the mode=0.
5) OUT is asserted high as soon as the counter reaches 0, it then remains high until the counter is re-initialised or a new mode is written to the control word register.

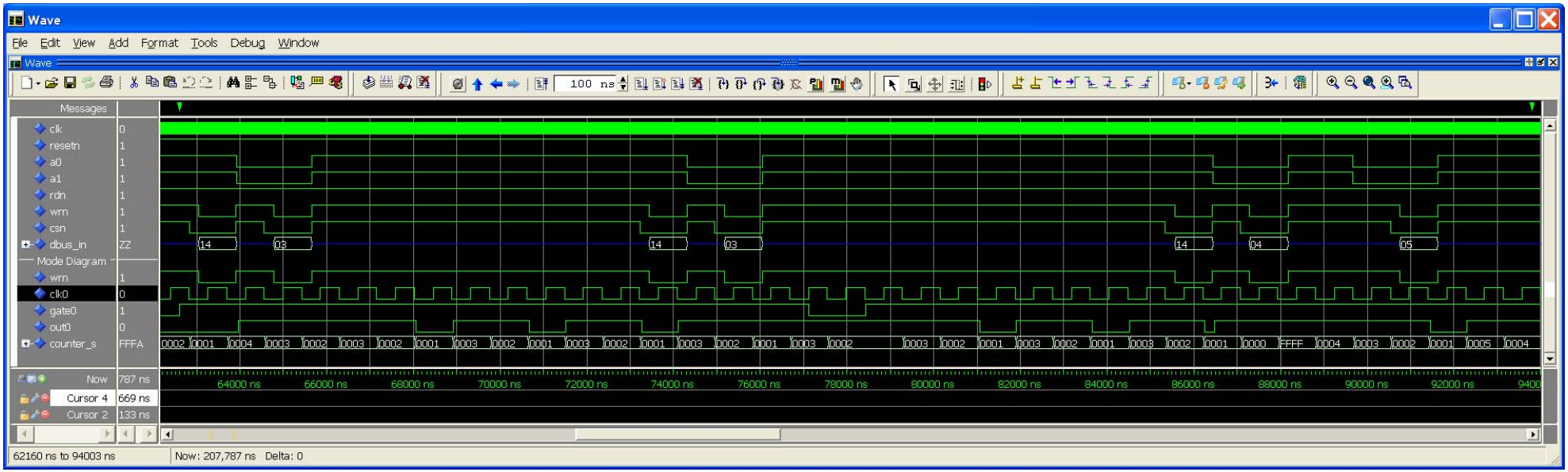
Appendix B Mode 1



Notes:

1) The testbench sets the databus input signal (dbus_in) to Z for visual effect only.
2) A rising edge on the GATE signal results in loading of the counters and negating of the OUT signal on the NEXT CLKn pulse.
3) The rising edge on Gate triggers loading of the counters and setting OUT low.
4) Note that the Gate signal is not sampled until the rising edge of CLKn, this means that a rising Gate edge which occurs before a falling CLKn edge will not be acted upon until the NEXT rising edge of CLKn. This in turn means that the counter is loaded on the following falling edge of CLKn.
5) GATE has no effect on the OUT signal
6) OUT is high after setting the mode=1
7) OUT will go low after receiving a valid GATE trigger and remains low until the counter reaches zero.

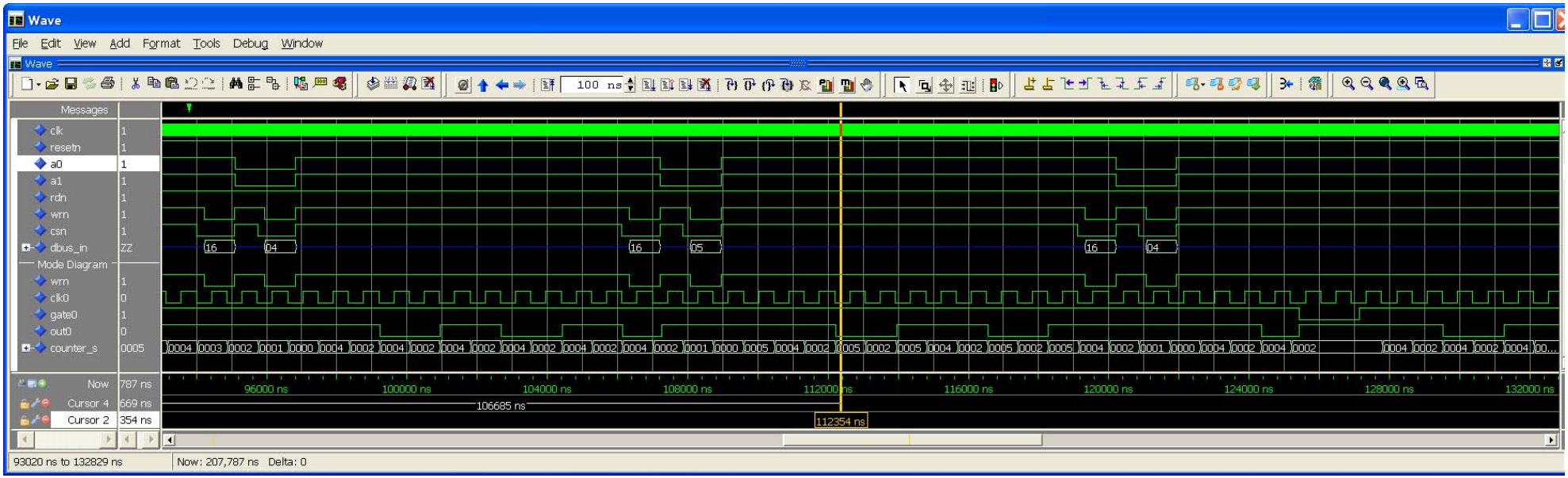
Appendix C Mode 2



Notes:

1) The testbench sets the databus input signal (dbus_in) to Z for visual effect only.
2) Counters are reloaded on the first falling edge on CLKn after the write cycle.
3) GATE=1 enables counting, GATE=0 disables counting.
4) If GATE goes low OUT goes high immediately.
5) The first falling edge on CLKn after a low to high GATE value with reload the counters.
6) OUT is high after setting the mode=2
7) OUT is low when the counter=1

Appendix D Mode 3



Notes:

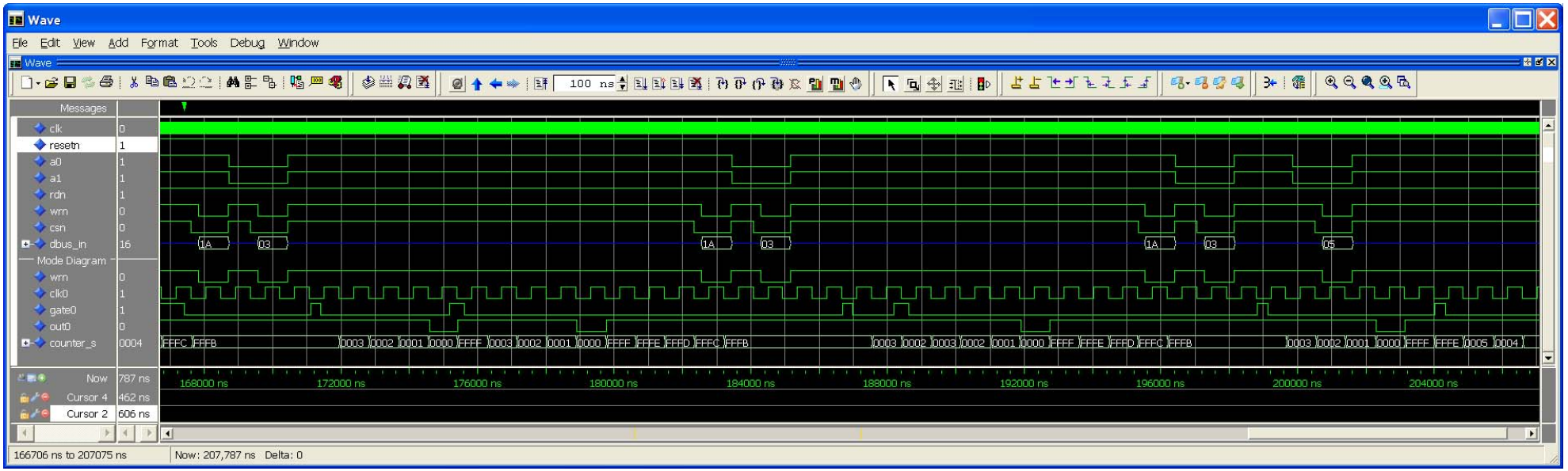
1) The testbench sets the databus input signal (dbus_in) to Z for visual effect only.
2) Counters are reloaded on the first falling edge on CLKn after the write cycle.
3) GATE=1 enables counting, GATE=0 disables counting.
4) The first falling edge on CLKn after a low to high GATE values with reload the counters.
5) OUT is high after setting the mode=3 and when GATE=0
6) OUT will be low for half the initial count. See sequence above for even and odd counter init values.

Appendix D Mode 4

Notes:

1) The testbench sets the databus input signal (dbus_in) to Z for visual effect only.
2) Counters are reloaded on the first falling edge on CLKn after the write cycle.
3) GATE=1 enables counting, GATE=0 disables counting.
4) GATE has no effect on OUT.
5) OUT is high after setting the mode=4
6) OUT is low only when the counter is equal to zero.

Appendix E Mode 5



Notes:

1) The testbench sets the databus input signal (sbus_in) to Z for visual effect only.
2) Note that the Gate signal is not sampled until the rising edge of CLKn, this means that a rising Gate edge which occurs before a falling CLKn edge will not be acted upon until the NEXT rising edge of CLKn. This in turn means that the counter is loaded on the following falling edge of CLKn.
3) OUT is high after setting the mode=5
4) OUT is low only when the counter is equal to zero.