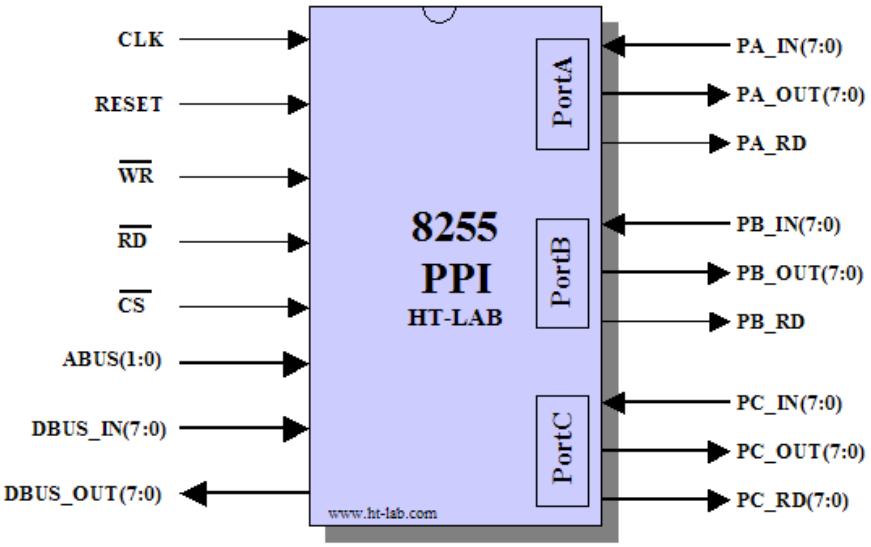
HTL8255

Programmable Parallel Interface



Version 1.0a
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1. Introduction

The HTL8255 is a synchronous implementation of the industry standard 8255/82C55 Programmable Parallel Interface (PPI) adaptor. The PPI can be used for a wide range of parallel I/O interface tasks. The HTL8255 is written in vendor neutral VHDL and can be synthesized for either ASIC or FPGA implementation.

2. Directory Structure

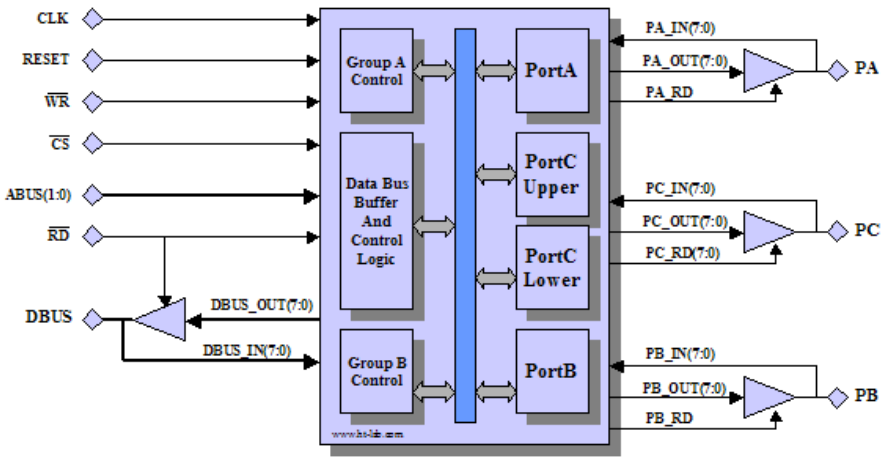
The HTL8255 IP core is delivered in a single zip file. The directory structure after unzipping is as follows:

Directory	Contents
HTL8255\bin	Any executable files such as utilities
HTL8255\doc	Documentation and Datasheets
HTL8255\rtl	Synthesizable IP Core
HTL8255\testbench	Testbench files
HTL8255\Modelsim	Example script for Modelsim Simulator
HTL8255\synthesis	Synthesis script and filelist

3. Filelist

The HTL8255 design is contained in three VHDL files and a separate top level wrapper that includes the tri-state drivers as shown in the diagram below.

Filename	Contains
intra_fsm.vhd	PortA INTRA Finite State Machine logic
intrb_fsm.vhd	PortB INTRB Finite State Machine logic
htl8255.vhd	Top level HTL8255 for instantiation
htl8255_tri.vhd	Top level HTL8255 + Tri-State drivers for single chip implementation [note1]



Standalone Implementation

Note1 : The original 82C55A device does not have a clock input and as such the HTL8255 + Enterpoint Craignell-40 board cannot be used as a replacement without additional modifications.

4. Simulation

The HTL8255 is written in vendor neutral VHDL and as such can be simulated by any modern simulation tool.

An example simulation script is provided for Mentor Graphics' Modelsim. To run the simulation execute the ***Modelsim\run.do*** file from within Modelsim. To run the simulation in command line mode execute the ***Modelsim\run.bat*** file in a Command (CMD) prompt, Cygwin shell or equivalent.
The output in both cases should be similar to the text shown below.

```
#  run 100 us
# ------- Test Mode 0 PortA/B/C Output --------
# GroupA: Mode0  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Output PortC(3:0)=Output
# ------- Test Mode 0 PortA/B/C Input --------
# GroupA: Mode0  PortA=Input  PortC(7:4)=Input   GroupB: Mode0 PortB=Input  PortC(3:0)=Input
# ------- Test Mode0 toggle portC bit --------
# GroupA: Mode0  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Output PortC(3:0)=Output
# ------- Test Mode0 split PortC I/O  --------
# GroupA: Mode0  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Output PortC(3:0)=Input
# ------- Test Mode1 Port A/B Input, PCH in, PCL out --------
# GroupA: Mode0  PortA=Output PortC(7:4)=Input   GroupB: Mode0 PortB=Input  PortC(3:0)=Output
# ------- Test Mode1 Port A/B Strobed Output --------
# GroupA: Mode1  PortA=Output PortC(7:4)=Output  GroupB: Mode1 PortB=Output PortC(3:0)=Output
# ------- Test Mode1 PortA Strobed Output + Interrupts --------
# GroupA: Mode1  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Output PortC(3:0)=Output
# ------- Test Mode1 PortB Strobed Output + Interrupts --------
# GroupA: Mode0  PortA=Input  PortC(7:4)=Input   GroupB: Mode1 PortB=Output PortC(3:0)=Output
# ------- Test Mode1 PortA Strobed Input --------
# GroupA: Mode1  PortA=Input  PortC(7:4)=Output  GroupB: Mode0 PortB=Input  PortC(3:0)=Output
# ------- Test Mode1 PortB Strobed Input --------
# GroupA: Mode0  PortA=Input  PortC(7:4)=Output  GroupB: Mode1 PortB=Input  PortC(3:0)=Output
# ------- Test Mode1 PortA Strobed Input + Interrupts --------
# GroupA: Mode1  PortA=Input  PortC(7:4)=Output  GroupB: Mode0 PortB=Input  PortC(3:0)=Output
# ------- Test Mode1 PortB Strobed Input --------
# GroupA: Mode0  PortA=Input  PortC(7:4)=Output  GroupB: Mode1 PortB=Input  PortC(3:0)=Output
# ------- Test PortA Mode1, PortB Mode0 PortC Output  --------
# GroupA: Mode1  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Output PortC(3:0)=Output
# ------- Test PortA/B Mode1, PortC Output  --------
# GroupA: Mode1  PortA=Output PortC(7:4)=Output  GroupB: Mode1 PortB=Output PortC(3:0)=Output
# ------- Test PortA/B Mode1 Input, PortC Output  --------
# GroupA: Mode1  PortA=Input  PortC(7:4)=Output  GroupB: Mode1 PortB=Input  PortC(3:0)=Output
# ------- Test Mode2 PortA Bidirectional I/O --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Input  PortC(3:0)=Output
# ------- Test PortA Mode2, PortB Mode0 Input, PortC Output --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Output  GroupB: Mode0 PortB=Input  PortC(3:0)=Output
# ------- Test PortA Mode2, PortB Mode1 Output, PortC Output --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Output  GroupB: Mode1 PortB=Output PortC(3:0)=Output
# ------- Test PortA Mode2, PortB Mode1 Input, PortC Output --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Output  GroupB: Mode1 PortB=Input  PortC(3:0)=Output
# ------- Test PortA Mode2, PortB Mode1 Input, PortC Output INTA --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Output  GroupB: Mode1 PortB=Input  PortC(3:0)=Output
# ------- Test PortC Status Read Mode 0--------
# GroupA: Mode0  PortA=Input  PortC(7:4)=Input   GroupB: Mode0 PortB=Input  PortC(3:0)=Input
# ------- Test PortC Status Read, PortA/B=Mode1 Input, PortC input --------
# GroupA: Mode1  PortA=Input  PortC(7:4)=Input   GroupB: Mode1 PortB=Input  PortC(3:0)=Input
# ------- Test PortC Status Read, PortA/B=Mode1 Output, PortC input --------
# GroupA: Mode1  PortA=Output PortC(7:4)=Input   GroupB: Mode1 PortB=Output PortC(3:0)=Input
# ------- Test PortC Status Read, PortA Mode2, PortB input Mode0 --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Input   GroupB: Mode0 PortB=Input  PortC(3:0)=Input
# ------- Test PortC Status Read, PortA Mode2, PortB input Mode1 --------
# GroupA: Mode2  PortA=Output PortC(7:4)=Input   GroupB: Mode1 PortB=Input  PortC(3:0)=Input
# ** Failure: ************ End of Test ***************
#    Time: 80843 ns  Iteration: 0  Process: /top_tristate_tb/u_1/line__57 File:
../testbench/htl8255_tri_tester.vhd
# Break in Process line__57 at ../testbench/htl8255_tri_tester.vhd line 1787
# Stopped at ../testbench/htl8255_tri_tester.vhd line 1787
#  quit
```

5. Synthesis

The HTL8255 can be synthesized using any modern synthesis tool. The area and delay figures will depends on the used synthesis tool and settings.
An example batch file for Xilinx XST 10.1 is provided. Navigate to the Synthesis directory and execute ***Synthesis\runxst.bat.*** Make sure that the **xst.exe** executable is in the search path. Part of the log file (HTL8255_Tri.syr) is shown below.

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
Top Level Output File Name         : HTL8255_Tri
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : YES

Design Statistics
# IOs                              : 39

=========================================================================
Device utilization summary:
---------------------------

Selected Device : 3s100evq100-4

 Number of Slices:                       95  out of    960     9%
 Number of Slice Flip Flops:             77  out of   1920     4%
 Number of 4 input LUTs:                167  out of   1920     8%
 Number of IOs:                          39
 Number of bonded IOBs:                  39  out of     66    59%
 Number of GCLKs:                         1  out of     24     4%

=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 77    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
reset                              | IBUF                   | 77    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 5.457ns (Maximum Frequency: 183.251MHz)
   Minimum input arrival time before clock: 8.611ns
   Maximum output required time after clock: 9.176ns
   Maximum combinational path delay: 8.106ns

Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 4.59 secs

Total memory usage is 152100 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    6 (   0 filtered)
Number of infos    :   11 (   0 filtered)
```

6. Pin Description

Symbol	Type	Function
CLK	I	Clock Input signal Note2,3
RESET	I	Active high Reset signal
WRN	I	Active low Write strobe
RDN	I	Active low Read strobe
CSN	I	Active low Chip Select
ABUS(1:0)	I	Address Bus, see table below
DBUS_OUT(7:0)	O	Databus output Note4
DBUS_IN(7:0)	I	Databus input Note4
PA_IN(7:0)	I	PortA Input Bus
PB_IN(7:0)	I	PortB Input Bus
PC_IN(7:0)	I	PortC Input Bus
PA_OUT(7:0)	O	PortA Output Bus
PB_OUT(7:0)	O	PortB Output Bus
PC_OUT(7:0)	O	PortC Output Bus
PA_RD	O	PortA Tri-State Bus control Note5
PB_RD	O	PortB Tri-State Bus control Note5
PC_RD(7:0)	O	PortC Tri-State Bus control Note5

Note2: All actions are on the Rising Edge of the clock signal.
Note3: This signal is not on the original 82C55.
Note4: The RDN & CSN strobes can be used to control a tri-state driver, see **rdn_s** signal in *htl8255_tri.vhd*.
Note5: This signal is low when driving the port, see *htl8255_tri.vhd*.

A1	A0	RD	WR	CS	Operation
0	0	0	1	0	Read PortA
0	1	0	1	0	Read PortB
1	0	0	1	0	Read PortC
1	1	0	1	0	Read Control Word
0	0	1	0	0	Write PortA
0	1	1	0	0	Write PortB
1	0	1	0	0	Write PortC
1	1	1	0	0	Write Control Word
x	x	x	x	1	Disabled HTL8255
x	x	1	1	0	Disabled HTL8255

7. Support

For any support issues please use support@ht-lab.com

Trademarks