TEST STRATEGIES FOR A FAMILY OF COMPLEX MCMs

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ABSTRACT

The development of MCM test practices from chip and board test practices is summarized. The general philosophy behind MCM test strategy selection is given. A family of complex MCMs providing computer system building blocks is described. The design features related to testability and test coverage are detailed Then, test strategies developed for each MCM are related, with emphasis on the improvements in fault coverage and diagnostic resolution provided by attention to design-for-testability.

INTRODUCTION

To provide flexible solutions to the computer design problem, Motorola is developing building block multichip modules (MCMs). Each MCM implements a computer system function (memory, processor, interface) in as general a design as possible. The user of the MCM building blocks is free to choose the amount of computer memory and the number and kind of processors through selecting the number and kind of MCMs. Computers designed in this manner could range from single processing systems with nominal memory through cache-coherent multiprocessing systems with large shared memory. MCM technology allows the combination of many integrated circuits in a single package for increased system reliability and decreased size and weight.

Design features, testability, and manufacturability were considered concurrently at the outset of this project. This paper outlines the design of this family of MCMs, concentrating on the design features related to test, and then details the test strategies developed for each MCM. Design-for-testability features include IEEE 1149.1 compatible devices and test points. For a complex MCM, the test goal is to provide high quality product without relying on full functional, at-speed test of each die mounted on the MCM. The basic test approach is assembly testing followed by limited functional test. In order to avoid discarding product that fails test, this family of MCMs is based on a repairable packaging technology. To assist the repair process, fault diagnosis methods were developed to support testing on a platform not designed to support fault diagnosis.

To set the stage for specific test strategy discussions, general philosophies on MCM test are given. First, the application of chip test strategies is compared with using board test strategies.

CHIP TEST VS BOARD TEST

MCM test strategies have developed out of board test and chip test practices [1][2] so brief descriptions of these precursors will be now given. Integrated circuits are tested by applying functional test vectors on high speed testers. Production chip testers are available with test speeds up to 100 million patterns per second. Most chips are thus tested very fast, since usually not more than several hundred thousand test vectors are used (typical tester memory is 1 million patterns). The test vectors attempt to exercise all the gates in the chip by causing the device to execute all of its functions. Test development time required for VLSI components can range from several weeks to a few years, depending on chip complexity, required fault coverage, and the ability to perform accurate simulation. The test vector development process often follows the design verification process, i.e. the simulation stimulus written by the chip design team to prove the design meets requirements is typically the starting point for manufacturing test vectors. Because of the complexities involved with developing high fault coverage test vectors, design-for-testability (DFT) practices are often used to aid the production of test vectors. The most widely used DFT methods in modern chips are internal scan design and built-in test (BIT). Internal scan design connects all chip state elements into a scan chain through which test

INTERNATIONAL TEST CONFERENCE 1994
0-7803-2102-2/94 $4.00

vectors can be applied. This practice allows automatic test pattern generation (ATPG) tools to develop tests for strictly combinational logic rather than for the much more problematic sequential logic. BIT methods are typified by the inclusion of circuitry to produce pseudorandom test vectors to apply to the rest of the chip, along with added circuitry to measure the response to the vectors.

MCMs can be tested using chip test methods, but there are key limitations. One problem is that full functional test with reasonable fault coverage is tough enough at the chip level -- at the MCM level functional test development can be an astronomical challenge [3][1]. The other problem with the chip test method is that ICs are not repaired when faulty, so there is no fault diagnosis support provided when using chip test on MCMs. MCMs which require repair in order to meet production cost goals also require automated fault diagnosis [4] so that repairs can be performed without relying on time-consuming manual troubleshooting.

To cost-effectively test MCMs, some producers are turning to board test practices [2]. Although the main drawbacks of chip test methods are avoided, board test practices have their own limitations when applied to MCMs. Table 1 compares the basics of chip test and board test. Boards are typically tested in two test steps: assembly test and system test. Assembly test is directed at finding missing components, wrong value components, and components with bad (e.g. open, shorted) connections to the board. The traditional assembly test method is in-circuit test, a practice in

Table 1: Key features of chip and board test

parameter	chip test	board test
test steps	1	2
parts pretested?	no	yes
fault coverage	full	partial
access	chip I/O	internal
fault diagnosis	none	required

which components are tested one at a time. In order to test each component, the tester must have direct access to each component. The access method which has been used for many years is a bed-of-nails test fixture contacting each circuit node with spring-loaded probes. The physical contact to the board is through device leads, edge connectors, and vias. In recent years circuit board topology has shifted toward high density, dual-sided boards with surface mount components. This has limited the applicability of in-circuit test because direct tester access to all nodes in the design is now impossible unless test points are added. Modern boards are becoming so dense that even test points are considered a limiting factor in space utilization. To answer the need for assembly test with limited access, boundary scan was developed [5]. Somewhat analogous to internal scan at the device level, boundary scan means assembly test is performed using a shift register made by connecting the individual boundary scan chains of the chips on the board. On circuit nodes that contain boundary scannable devices, direct test access is not required; test is done with the addition of only four boundary scan pins. There are a large number of ICs available today that adhere to the IEEE 1149.1 standard, so the board assembly test problem is lessened.

The second board test step commonly used is system test. This test typically places the board into a target system and runs system software. The test is excellent for demonstrating the at-speed capability of the board. System test is also good at detecting marginal ICs. But diagnosing faults is just as important as detecting them. The distinction between fault *detection* and fault *isolation* is one of the key differences between chip test and board test. Complex boards require high-quality software diagnostic routines to aid fault isolation.

The board test solution is a good match to many MCMs. The most obvious case is one in which the MCM is so complex that writing functional test vectors could prevent the design from meeting its time-to-market and quality goals. A second advantage of board test is that fault diagnosis is supported at all phases of board test, from vector development through test equipment. The two main impediments to using board test techniques on MCMs are: 1) physical access problems because MCMs are generally much smaller than boards and 2) lack of fully tested parts going into MCM assembly. The access problem is an area of active development. Substrate test points have been used for testing [6][7], but there are no commercial MCM test fixtures in widespread use. Tested parts are required because neither assembly test nor system test is efficient at detecting and diagnosing subtle components problems such as faults causing the device to fail to meet its timing specifications. A further impediment to the use of board test techniques is that much of the MCM development is coming from chip suppliers. When MCMs are treated like chips, chip design, production, and test techniques will be used. It can be a major mindset change to adopt board test practices, to say nothing of the CAD and test infrastructure changes required.

GENERAL MCM TEST PHILOSOPHY

The challenges of MCM test require that test be considered from the earliest phases of design. The architectural design process should include detailed attention to producing a testable product. For example, 1149.1 boundary scan testing can be implemented across an entire design hierarchy [8]; choosing boundary scan components and implementing compatible interfaces at all levels of the design can greatly simplify the test problem. Logic partitioning and the choice of specific integrated circuits should also be done with attention to test practices. Test vector development at the component level should consider how the component will be tested in the next level of assembly. A good example of the benefits of this practice is the inclusion of BIT at the IC level with appropriate facilities (e.g. boundary scan) to allow IC BIT to be performed and monitored at the MCM test level [9].

Once the overall system strategy is planned, specific attention can be given to test at the MCM level. The goal of MCM-level test is to assure product quality through cost-effective test. There are several characteristics of the MCM that drive which of several test strategies is the most cost effective [10][1]. Of primary importance are: 1) complexity of the MCM, 2) level of test of the dice, 3) whether the MCM is repairable, 4) amount of test access available, and 5) cost of the MCM. The MCM complexity directly affects how easy it is to generate test vectors. Secondary effects of MCM complexity include the availability of simulation models and the ease with which fault diagnosis can be achieved. The level of dice test is a critical parameter to determining the fault coverage required by MCM level test [11]. Dice cost and the MCM technology used are the main contributors to whether faulty MCMs will be repaired. Test access can be achieved in one of three ways (in order of preference): a) use 1149.1 compatible components, b) bring internal nodes out to the MCM I/O pins, c) add test pads on the substrate to allow access by test equipment. The higher the degree of test access, the simpler the test generation processes and the fault diagnosis process will be. Finally, total MCM cost will help determine the budget for test development, because very costly MCMs will almost certainly require both a repair process and very thorough test fault coverage.

Other important parameters are as follows: projected shipped volume of product; types of automatic test equipment available; availability of software tools such as logic simulators, fault simulators, and automatic test pattern generators; and the availability of system level test. High volume products can amortize over many components costly expenses such as automatic test equipment (ATE) and state-of-the-art development tools. MCM producers can usually leverage existing test equipment to some extent. For example, board test practices such as in-circuit test can be applied on VLSI testers [10]. There are a wide range of software tools available to speed both the design and test development efforts. State-of-the-art tools can be quite expensive, however, so MCM developers who already own tools being applied to board or chip design and test efforts hold an advantage over new entrants to the MCM market. A similar line of reasoning exists in discussing system level test. This is a proven method to reduce test development costs for printed circuit boards. MCM producers with access to system test capabilities can avoid the costs incurred by functional test development and functional ATE.

DESCRIPTION OF MCMs

The computer building block MCMs are 1)non-volatile memory (NVM), 2)volatile memory (VM), 3)processor (P), and 4)interface (I). Representative layouts of each MCM are shown in Figure 1. Each MCM contains some bypass capacitors and pullup and/or damping resistors. The NVM MCM contains two banks of non-volatile memory and JTAG-compatible buffers on the memory address and control lines. The VM MCM contains 10 volatile memory chips and JTAG-compatible buffers on the memory address lines. The processor MCM contains a processor chip, a cache controller chip, 8 high speed memory chips, a clock generator chip, and a programmable logic device (PLD). The interface MCM contains a communication controller chip, two application specific integrated circuits (ASICs), and volatile and non-volatile memory.

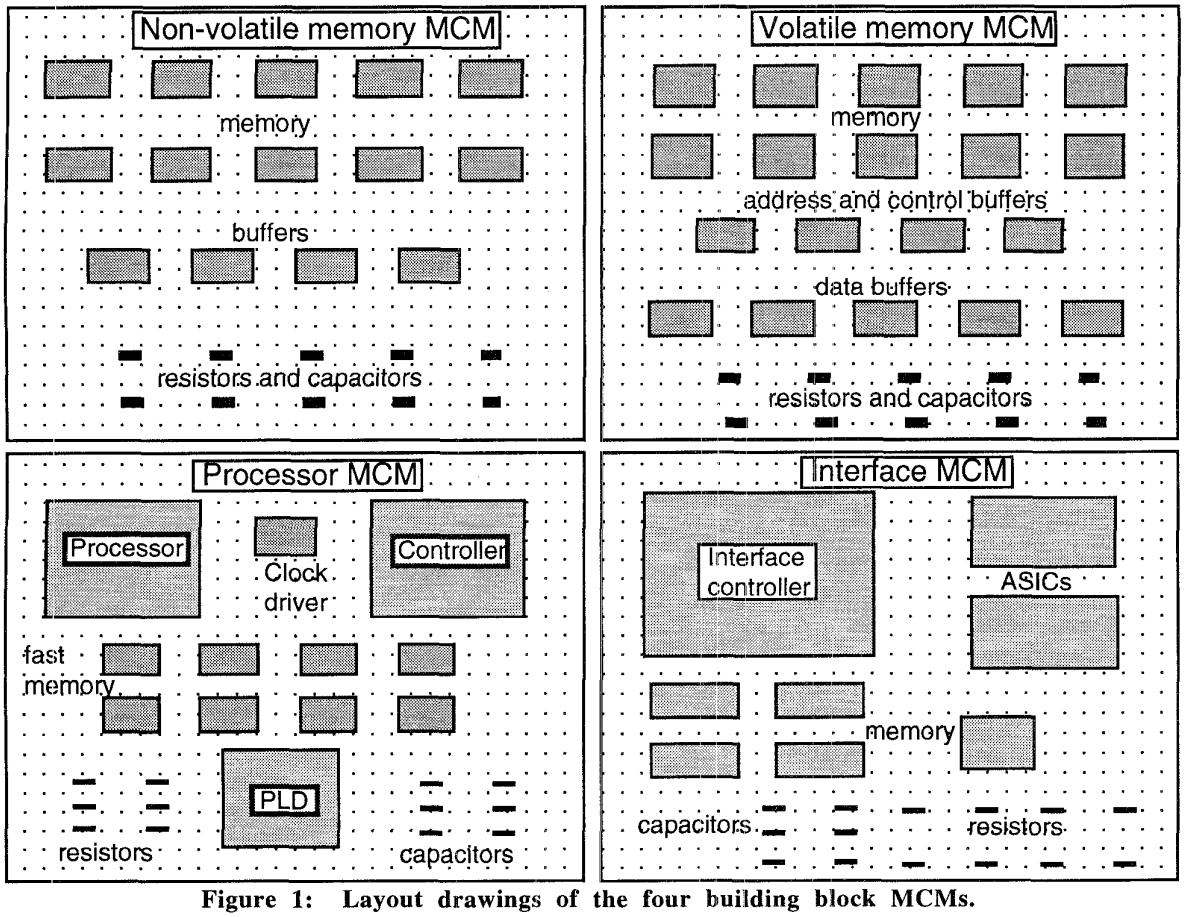

Figure 1: Layout drawings of the four building block MCMs.

DESIGN CHARACTERISTICS AFFECTING TEST REQUIREMENTS

A primary characteristic affecting the test requirements of these MCMs is that repair is required. Many of the ICs in the MCM are expensive, so throwing an assembly away because of one faulty component is very costly. Since repair is necessary, support for repair is also required. As stated earlier, complex electronic assemblies require automated assistance to prevent manual troubleshooting of failures. Fault diagnosis of failures on ATE is the means by which this assistance is given and fault dictionaries or guided probe are the traditional methods used to provide automated fault diagnosis.

Another important factor in the test analysis done at the beginning of this project was that the MCMs fit into one package type with a fixed number of leads. The number of package pins is greater than the number of MCM system pins for each design. The memory MCMs have relatively few system pins and a fairly low number of internal nodes. Only some of these internal nodes could be pinned out, however, because of pin compatibility requirements placed on the memory MCMs. Test requirements were carefully analyzed to determine which internal nodes should be pinned out. This extra observability into faults has a direct impact on the ease of generating automated fault diagnosis. For the more complex processor MCM, there were many extra pins available, so fairly large gains in testability were achieved by pinning out internal nodes.

Another factor of the design which contributed to test planning was that buffers were required in order to separate certain data paths and to provide proper DC logic levels in paths involving high fanout. Buffer parts are so common in designs and test has become so important that more than one integrated circuit manufacturer offers JTAG-compatible buffers. JTAG-compatible parts allow increased test access without using valuable package pins. JTAG-compatible MCM I/O pins also allow the MCM user to employ boundary scan testing of the connection of an MCM to a printed circuit board. Having JTAG-compatible MCM I/O provides a simple solution to a test problem that could otherwise be

extremely challenging.

A final design factor contributing to test strategy decision making is the fact that the MCMs are typified by fairly shallow levels of logic. The path from input to output generally contains 2 to 3 integrated circuits. The significance of this is that functional test generation and automated fault diagnosis is generally simpler with shallow logic levels. Additionally, lack of in-circuit test access to internal circuit nodes is less of a problem with shallow logic levels. When MCMs evolve and approach the logic depth found on printed circuit boards, then functional test generation will become extremely complicated and the loss of diagnostic resolution resulting from the lack of test access to internal nodes will be significant. A goal of this project, from a testability perspective, was to lay the groundwork for handling of such future MCMs. Consequently, the present MCMs were treated as complex subassemblies requiring some form of test access to each node. Learning how to gain and use test access on the present MCMs will be beneficial to developing adequate tests for future MCMs that are even more complex.

TESTER PLATFORM AND DIAGNOSIS SUPPORT

The determination of which tester to use for an MCM is, like much of engineering, finding a balance between functionality and cost. For these complex MCMs, a complex and expensive test strategy could have been conceived. However, with the goal of producing parts with commercial market appeal, the wish for highly sophisticated test was offset with the need for cost-effective test. The most immediately available testers for the project were moderately high speed VLSI testers used by Motorola for production testing of ASICs and microprocessors. A test strategy was developed which will utilize these testers to the limits of their functionality. That is, the chip testers will be used to support a board test strategy for these MCMs. As the MCMs migrate from low volume initial offerings to high volume production, the tester strategy will also migrate, as will be explained below.

First though, how is it possible to do board-like assembly testing on a chip tester? The answer is that it is actually quite simple; some small matters have to be taken care of, but in general a VLSI tester has at least all the required hardware capabilities. A summary of the differences between chips testers and board testers is given in Table 2. The two types of assembly test are boundary scan test and in-circuit test (ICT). Boundary scan tests for these MCMs are being developed using an in-house tool that generates vectors in a simulator format. Simulation is run to verify the vectors before translating them to tester language with another Motorola software tool. A fault dictionary is generated along with the test vectors and a lookup program has been developed which will examine the VLSI tester failure datalog and match the failures to faults in the dictionary. This diagnosis method works around the problem of lack of diagnosis support on the VLSI tester.

Table 2: Comparison of Key Features of Chip Testers and Board Testers.

parameter	board tester	chip tester
channel count	1500	256
vector depth	16K	1 Meg
speed (MHz)	5	40
backdrive (mA)	500	50
diagnosis?	yes	no
JTAG ATPG?	yes	no

For non-JTAG-compatible nodes on the MCMs, in-circuit test practices will be used. The VLSI testers provide support of ICT for all but two requirements: 1) backdrive is not possible with the relatively weak VLSI tester drivers and 2) since no diagnosis support is provided, in-circuit test failures cannot always be diagnosed to the failing node. For diagnosis purposes, the difference between ICT and boundary scan test is that in the boundary scan case there is only one output to consider. A fault dictionary for one output is much simpler than one for multiple outputs. With care, however, a fault dictionary to support ICT can be developed to provide a measure of increased fault isolation.

The second test stage for these MCMs is functional test. Design verification stimulus is converted to functional test vectors to be applied, again, on the VLSI tester. This test application is exactly what VLSI testers are designed for, except at the chip level. A limitation, still, is that no support for fault diagnosis is built in to the testers. The MCMs are much too complex to manually generate a fault dictionary. Diagnostic probing is out. The only diagnosis method remaining is manual troubleshooting. This method is supported by detailed descriptions of what is being tested in different sections of the test vectors. Knowledge of how the MCM works coupled with descriptions of precisely what is being tested in each section of vectors can make troubleshooting relatively straightforward

There is a fair chance that this family of building block MCMs will achieve relatively good market success. There are several additions to the family being

planned. To support a high volume environment, the tester strategy will be modified. The VLSI testers are costly and provide inadequate fault diagnosis support. Support for ATPG for assembly testing is also lacking. Therefore, the tester strategy will migrate toward the use of low cost testers for assembly testing. Several board tester manufacturers offer testers with all the capabilities required and at a price far below that of VLSI testers. The board testers will support the automatic generation of boundary scan and in-circuit test vectors. They will automatically setup the MCM so that other parts do not interfere with the test of one part. They will automatically generate tests for resistors and other analog components. And, finally, low cost assembly testers will support fault diagnosis.

Functional test on the VLSI testers will be replaced by system test on a hot mock-up tester. This test will basically consist of plugging the MCM into a customer system and running system software. Although potentially a costly test system, the big advantages will be very complete test coverage and fault diagnosis routines automatically run by the system when a part fails. As the family of complex MCMs grows, system test will develop into a cost effective alternative to generating functional patterns for a VLSI tester.

TEST STRATEGY FOR EACH MCM

Non-volatile Memory MCM

The NVM MCM is a relatively simple component with only two levels of logic (buffers and memory). The test strategy is assembly test followed by functional test. Assembly test consists of a combination of boundary scan tests, in-circuit tests, and cluster tests. Boundary scan components were chosen for the buffer ICs to provide better testability. The JTAG-compatible buffer on the memory control lines is tested using both boundary scan and in-circuit test, since there is access to all device pins. Standard in-circuit test vectors will exercise the chip, proving functionality while verifying good contact to the substrate. Boundary scan tests verify the JTAG circuitry on the chip so that the circuitry is tested before it is used as part of other tests. The address buffers are also JTAG-compatible. The buffer inputs are tested by applying data with the tester, capturing the data into the boundary scan chain, then shifting the data out through the chain. There is no tester access to the buffer outputs, so in-circuit test cannot be performed. Instead, cluster test is used. Cluster test is testing multiple devices simultaneously because of limited access. The buffers are tested in conjunction with the memory components. Lack of access to the buffer outputs prevents diagnostic resolution to the failing components. That is, during a cluster test, faults are detected but not diagnosed. The fact that the buffer outputs are JTAG-compatible is no help because the memories are not compatible. The other way to achieve access is through test points on the substrate. Test points are presently included as part of the substrate design, but there is no immediate plan for their use, other than for benchtop test probe points. In high volume production mode, the present plan is to fixture the test points for use in in-circuit test to achieve the fault diagnosis resolution.

The functional test of the NVM MCM simply exercises the memory enough to prove it is functional. That is, the memory die are not exhaustively tested. The MCM I/O is used to apply the vectors and monitor the results. The design verification stimulus is the source of the test vectors.

Volatile Memory MCM

This MCM is structurally similar to the NVM but has buffers on both the address and data lines. The control lines have JTAG buffers with 100% tester access. The buffers are tested using in-circuit means to verify their functionality and connections. Their boundary scan circuitry is then verified for subsequent use in testing other components. The address and data line buffers are tested for JTAG functionality and the input interconnect is tested using the boundary scan chain to capture stimulus. The buffer outputs are verified using cluster testing with the volatile memory.

The functional test for the VM MCM is derived from the simulation vectors used to verify the design. The buffers and memory are exercised to prove their operation, but, once again, the memory test is not exhaustive.

Processor MCM

The PLD on the Processor MCM is tested using in-circuit methods. Access to all device pins is obtained at the MCM I/O pins. Other devices that may affect the test of the PLD are tristated. The processor and cache controller chips are JTAG-compatible devices. MCM input connections to these devices are tested by applying vectors to the inputs and then capturing the data into the boundary scan chain for subsequent shiftout and examination. Primary outputs are tested by applying vectors using the scan chain and then reading output levels with the tester. Processor to controller connections are tested using JTAG interconnect tests. Three sets of tests are performed: 1) stuck-at-1 tests (apply 0 to interconnect drivers, capture in receivers), 2) stuck-at-0 tests (apply 1 to interconnect drivers, capture in receivers), and 3) shorts test using walking 1 (apply 0 to all interconnect except one, capture in receivers, then repeat test with the 1 data moving to each interconnect).

There are connections to the processor and controller chips which are not connected to the MCM I/O and are connected to non-JTAG chips. These connections are tested using cluster test methods. For example, the memory chips have control lines available at the MCM I/O but the data and address lines are unavailable. The processor and cache controller chips drive these memory lines. The cluster test consists of a test of the memory by applying address and data through the boundary scan chain of the other chips while the control lines are operated directly through the MCM I/O. Enough memory cycles are performed to verify all interconnects involved. For example, addresses 0, 1, 2, 4, 8, 16,... are written with different data and then read. This will prove the address lines. Data lines are tested in a similar fashion.

The functional test for this MCM has not been developed yet. Simulation models for the complex components on this MCM are not as readily obtainable as for the simpler components on the memory MCMs. Whether full logic simulation is achievable or not, the functional test will consist of loading the memory on the MCM with processor code, then running the program. The test program will execute processor instructions to move data around, respond to interrupts, etc. This is similar to built-in test, but not strictly BIT because the tester will drive and receive on the external interfaces to verify the MCM can communicate with the outside.

Interface MCM

The Interface MCM contains three large JTAG-compatible devices -- two ASICs and an advanced communication controller. These components are tested in a manner similar to the processor and cache controller chips of the processor MCM. That is, the pins connected to the MCM I/O are tested using the boundary scan chain, the pins connected between the three boundary scan compatible chips are tested using standard JTAG interconnect test techniques, and the remaining pins are tested using cluster test. The memory devices on the MCM are cluster tested along with the previously mentioned connections on the ASICs and controller.

The Interface MCM functional test will be similar to the test for the processor MCM. The communication controller chip will execute code to exercise a large percentage of the MCM logic. Simulation models for the IC's on the MCM are readily obtainable, either as gate level, behavioral, or hardware models. With these models, the functional test will be simulated to give a measure of confidence that the test will work properly on a real system.

SUMMARY OF DFT BENEFITS

This section compares the testability features designed into the four MCMs and summarizes the fault coverage provided by these features. Table 3 presents the breakdown of increased test access provided by one of three DFT practices: 1) pinning internal nodes out to the MCM I/O, 2) using boundary scan components, and 3) adding test points on the MCM substrate. The Table lists the number of nodes that are fully boundary scan compatible as well as the number of nodes with partial boundary scan. A node with partial boundary scan is **not** treated as having test access, but note that partial boundary scan does allow a measure of increased controllability and/or observability (otherwise, access would be by propagating logic states through possibly very complex intermediate logic). Through the combination of the three types of access, the memory MCMs achieve full test access. The Processor MCM, with a much larger node count, has high test access; full access could not be achieved because of limited substrate area for test points. The Interface MCM is still in the design phase, so information on access other than that provided by boundary scan components is unavailable.

Table 3: Details of test access provided by various design-for-testability features.

MCM	pinned	full BS	partial BS	test points	%access
NVM	6	0	62	62	100
VM	0	4	80	80	100
P	35	56	116	97	93
I	n/a	120	92	n/a	n/a

In previous discussions on planned test methods, the use of cluster testing was mentioned. This is a modification of strict in-circuit testing necessary when access is limited. Why use cluster testing when there is a high degree of access as shown in Table 3? The reason is that the test fixturing necessary to apply test probes to the substrate test points has yet to be developed. For the initial production runs of these MCMs, fixturing to the MCM I/O pins is performed. Fixturing to test points (refer to Figure 2) has been investigated enough to show that the technology is available to support the activity, but it was felt to be risky to develop a test strategy which depended upon test point fixturing to meet test goals.

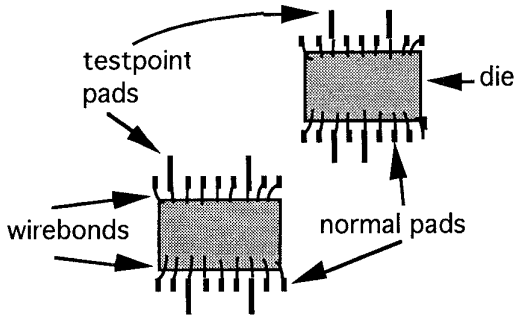

Figure 2: Section of an MCM layout showing how testpoints were created by wirebond pad enlargement. The normal bondpad length of 10 mils was doubled to provide a testpad of 10 by 15 mils. Present day fixturing technology is available to probe targets of this size.

Therefore, cluster testing is being specified in areas where test points are involved. By the time these MCMs go into volume production, proper fixtures to support full in-circuit testing will be developed and cluster testing will be eliminated, where possible. The resulting diagnostic resolution gained will provide support for MCM repair in a volume production environment.

Table 4 summarizes the assembly test methods and coverage for each MCM. Complete test coverage for all MCM interconnect is achieved through the combined test methods of JTAG, in-circuit test, and cluster test. JTAG boundary scan testing is performed on all ICs containing 1149.1 circuitry. Testing the test circuitry is done as a first step before using the test circuitry to test interconnects. MCM I/O connected directly to JTAG-components are tested using boundary scan methods. On MCMs containing full boundary scan nodes, JTAG interconnect tests verify chip to chip interconnect. In-circuit testing is performed on components with full tester access. This is presently very few components because, as mentioned above, test probe fixturing to test points on the substrate is still in the development stage. Cluster testing is used in the interim and, as the Table shows, is used heavily. There are some cases in which cluster testing will be used even after tester access is achieved. For example, on the Processor MCM, there are memory device inputs controlled by non-tristatable drivers on the processor and cache controller chips. When tester access to these nodes is achieved, the tester will be used to monitor the VLSI outputs, but the tester will not be used to apply inputs to the memories because tester overdrive of logic states would be required. Cluster testing is the only method that can be used in this case.

Table 4: Assembly test type and coverage for each MCM

MCM	Device	Test Method	Test Coverage
NVM	Address buff.	JTAG	JTAG circuit and inputs
		Cluster	Outputs
	Control buff.	JTAG	JTAG circuit and all pins
		ICT	All pins
	Memory	Cluster	All pins
VM	Buffers	JTAG	JTAG circuit and inputs
	memory	Cluster	All pins
P	Processor	JTAG	JTAG circuit and interconnects
		Cluster	Memory interconnect
	Controller	JTAG	JTAG circuit and interconnects
		Cluster	Memory interconnect
	Memory	Cluster	All pins
	PLD	ICT	All pins
I	Com. cntrlr.	JTAG	JTAG circuit, system I/O and ASIC links
		Cluster	Memory interconnect
	ASICs	JTAG	JTAG circuit, system I/O and controller links
		Cluster	Memory interconnect
	Memory	Cluster	All pins

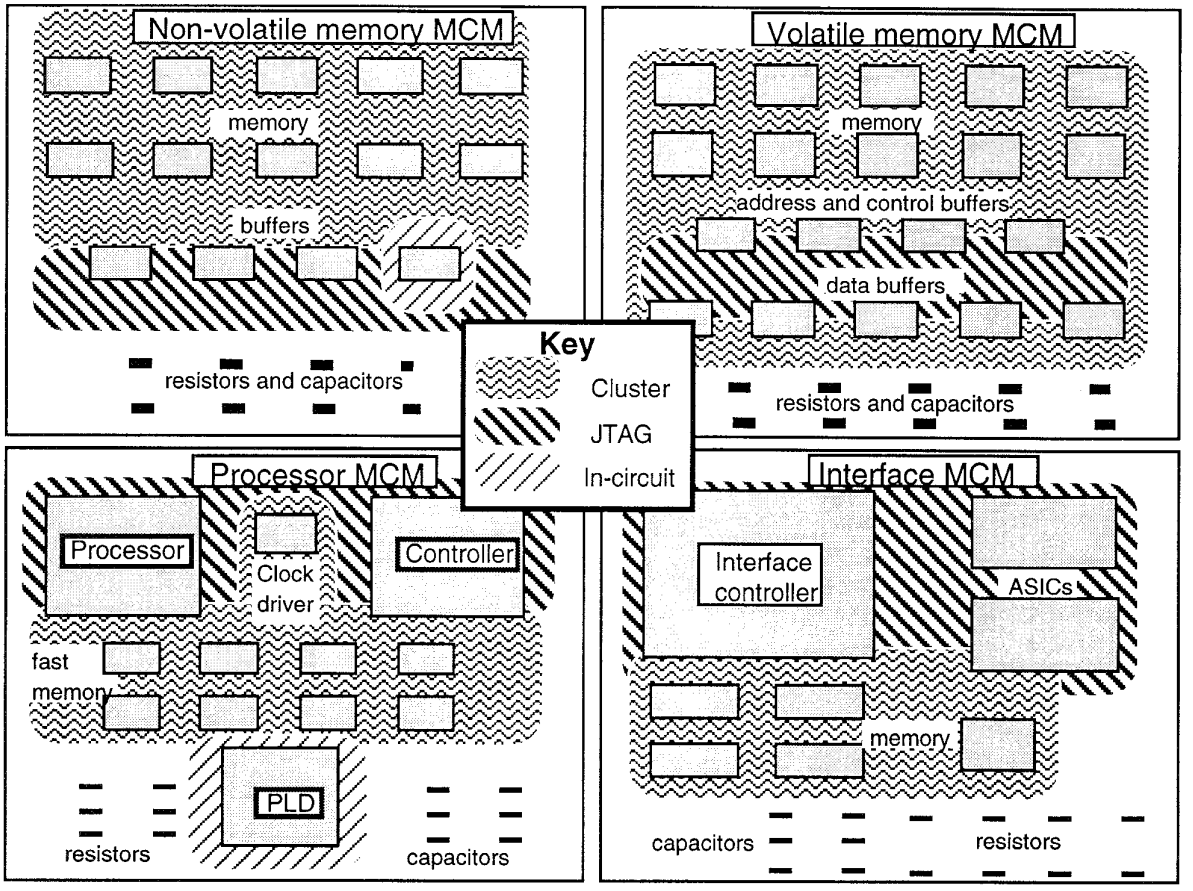

Figure 3: The assembly test coverage provided by three different test methods is shown. MCM I/O signals that are JTAG-compatible are tested using boundary scan. Interconnects between JTAG-compatible components are also tested using boundary scan. Most other connections are tested using cluster test, although the testpoints are available for more complete in-circuit testing in the future.

In Figure 3, a graphical summary of the information in Table 4 is provided. Not included in either place is a description of the testing performed on the passive analog components on the MCMs. The bypass capacitors are not tested since they are all paralleled across power and ground. The resistors are tested, though. The series damping resistors are cluster tested as part of the interconnect testing. The pullup and pulldown resistors are all available at primary I/O connections and so are tested using the VLSI tester parametric measurement unit. These tests are basically input leakage tests, with the measurement unit programmed to look for leakage current appropriate for the resistive connections.

Not apparent in Figure 3 is the fact that cluster test is applied using two quite different methods. In the first method, stimulus is applied through the normal logic (i.e. not through special test logic) of a simple chip. For example, the NVM MCM has memory chips which are cluster tested through the buffer chips. The boundary scan circuitry of the buffer chips is not used during the memory cluster test. The second cluster test method *does* use boundary scan. Vectors are applied by shifting stimulus through the scan chain of a complex device to be applied to another device. An example of this method is the cluster test of the memory on the Processor MCM.

CONCLUSIONS

A family of MCMs designed to support building block computer implementations has been described. Detailed descriptions of the test strategies for each MCM have been provided. The general practice is to test the products like small circuit boards. This involves a two-step test process. The first is assembly testing using a combination of boundary scan, in-circuit test, and cluster test. Assembly defects such as open wire bonds are detected. For JTAG-compatible nodes, diagnosis to the

failing node is guaranteed. For non-JTAG nodes, diagnosis to the failing node is not guaranteed because of the use of VLSI testers and cluster test practices, but diagnostic aids are implemented to make the process as automatic as possible. The second test step is a functional test of the MCMs based on design verification stimulus. Using the MCM system I/O pins, the functional test verifies overall MCM operation by testing much, but not all, of the logic internal to the ICs within the MCMs.

There is presently much debate as to whether MCMs can be tested like circuit boards. Proponents of chip test methods for MCMs support their methods in order to produce high quality product. If the board test strategy proves effective for this family of MCMs, then a further step in the development of practical MCM test strategies is achieved.

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