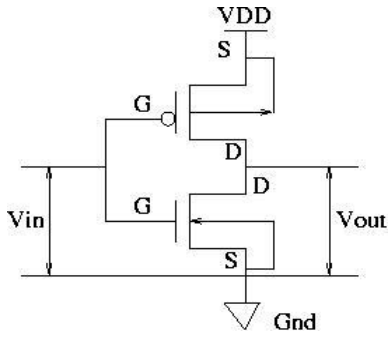
Experiment Name:

Geometric layout of the CMOS inverter using Export Microwind software.

Theory:

A complementary CMOS inverter consists of a p-type and n-type device connected in series. The transfer characteristics of the inverter are a function of the output voltage (V_{out}) with respect to the input voltage (V_{in}).



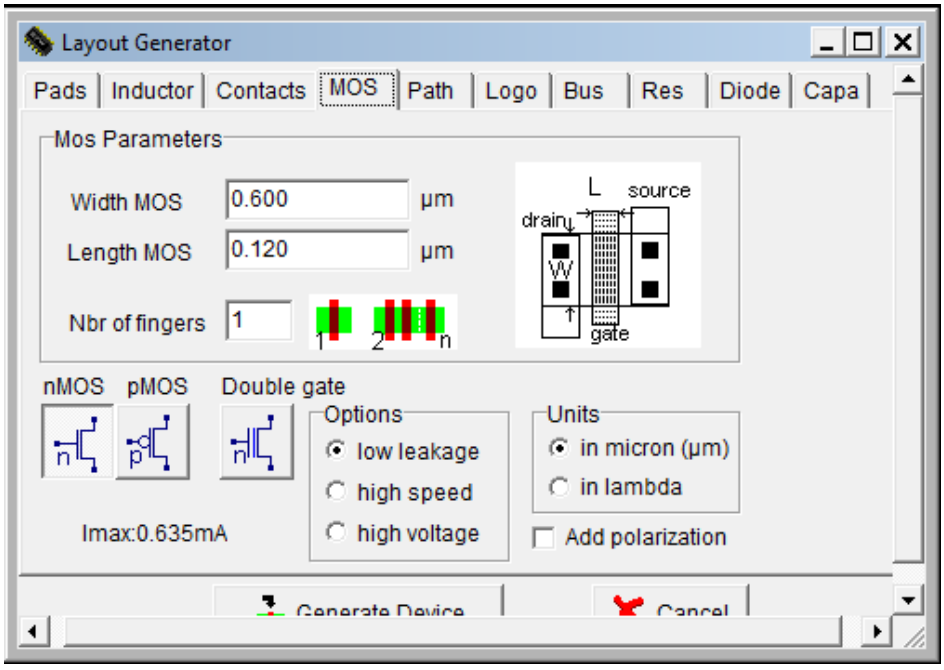
The MOS device first Shockley equations describing the transistors in cut-off, linear and saturation modes can be used to generate the transfer characteristics of a CMOS inverter. The DC transfer characteristics curve is determined by plotting the common points of Vgs intersection after taking the absolute value of the p-device IV curves, reflecting them about the x-axis and superimposing them on the n-device IV curves.

Apparatus:

- **Microwind**
- **nMOS – IRF 150, pMOS - IRF 9140, Register, Capacitor, V_{dc}, AGND, wire.**

Procedure:

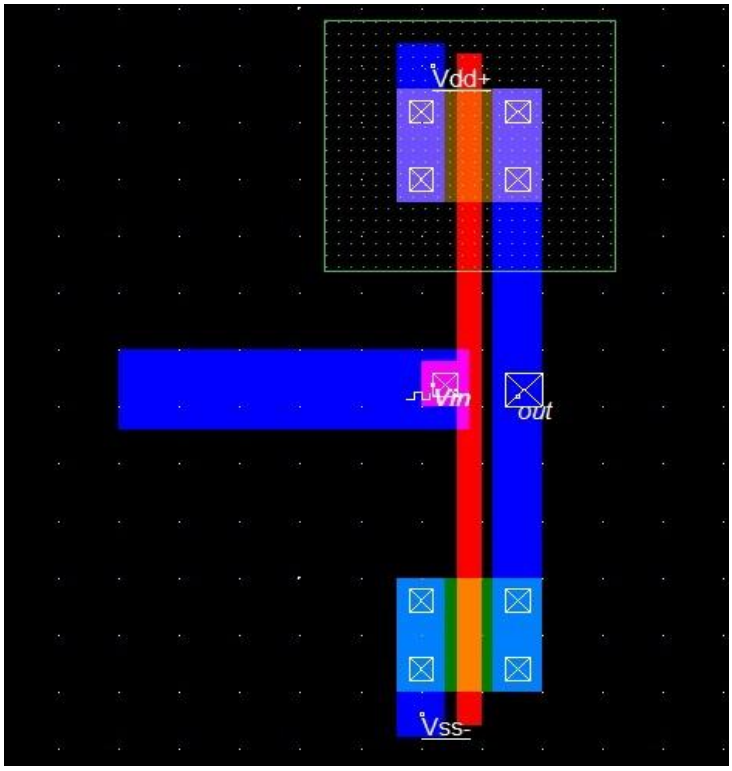
1. **At first open the Export Microwind software.**
2. **Click the 'View – Palette of Layers', then a dialog box is shown by the right side of the screen.**
3. **Click the icon 'MOS generator' of the Palette dialog box. The following window is shown on the screen.**
4. **A tick on p-channel of the box and click Generate Device. Then click on the middle of the screen to fix the MOS device.**
5. **Now click again the icon MOS generator on the palette and change the type of device by a tick on n-channel and click Generate Device. Click on the bottom of the pMOS to fix the nMOS device.**



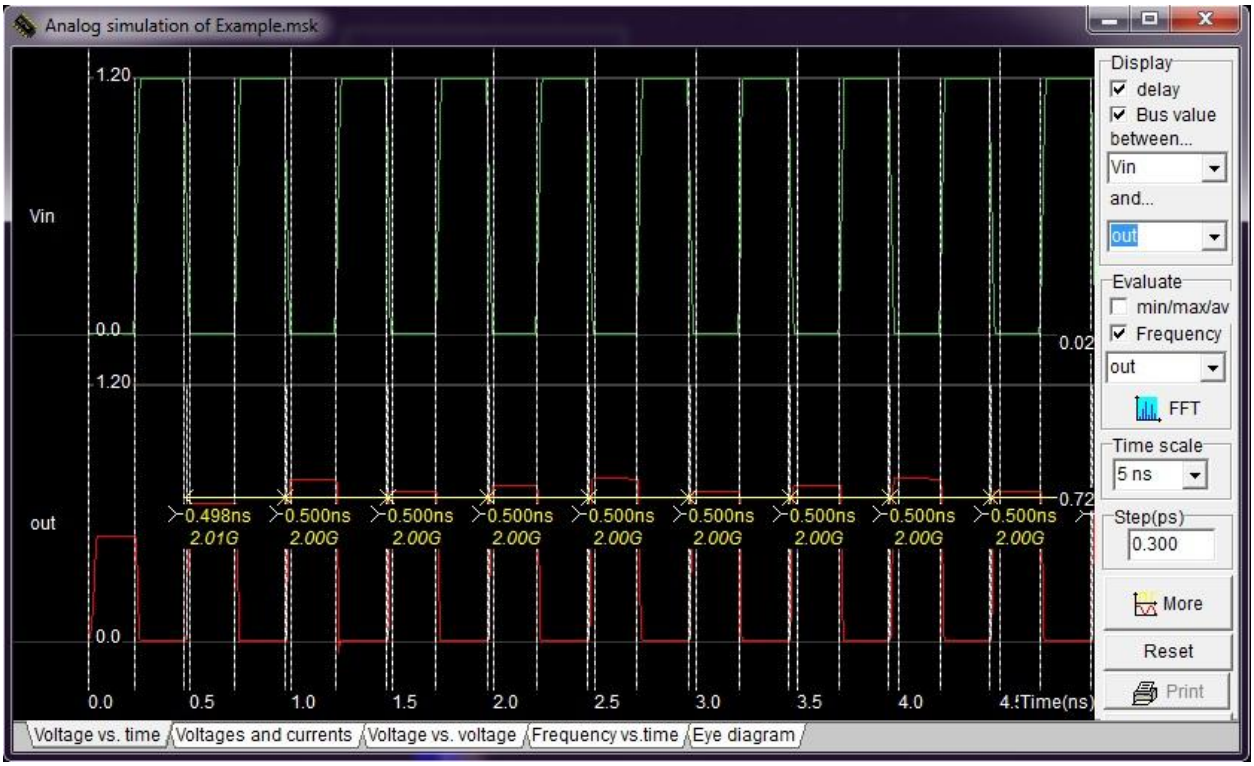
6. **Now click the Polysilicon on the palette box and connect the two polysilicon layer of the pMOS and nMOS device.**
7. **On the same way click the Metal 1 on the palette box and connect the two metal of the nMOS and pMOS.**

8. **Within CMOS cells, metal and polysilicon are used as interconnects for signal. Metal is much better conductor than polysilicon. Consequently, polysilicon is only used to interconnect gates, such as the bridge between pMOS and nMOS gates, as described in the schematic diagram.**
9. **Click the 'Contact metal/poly' on the palette box and fix in the joint of the middle metal and polysilicon.**
10. **Click the 'Vdd Supply' on the palette box and fix the metal of pMOS.**
11. **Click the 'Ground' on the palette box and fix the metal of nMOS.**
12. **Click the 'Contact' on the palette box and fix the metal.**
13. **Then click the 'Visible Node' on the palette box and fix the contact of the metal.**
14. **Now click 'Design Rule Checker' on the tool bar.**
15. **Then click 'Simulate tool – Run simulate – Voltage vs Time (Default)' and see the graphical window as output.**

Geometric Layout:



OUTPUT:



Discussion:

The output of the CMOS inverter shows on the figure. On the output figure the CMOS inverter shows the V_{in} and V_{out} where the $V_{in}$is 0 then the $V_{out}$is 1 and $V_{in}$is 1 and $V_{out}$is 0. That means when the pMOS is ON then the nMOS is OFF and when the nMOS is ON then the pMOS is OFF. The CMOS inverter works as a switch on/off.