Department of Computer Science & Engineering

University of Asia Pacific (UAP)

Program: B.Sc. in Computer Science and Engineering

Final Examination	**Spring 2020**	**3rd Year 1st Semester**
Course Code: CSE 311	**Course Title: Microprocessors & Assembly Language**	**Credits: 3**
Full Marks: 120* (Written)		**Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. **a)** Draw the internal diagram of the CPU of 8086 and describe each component with your own language. 8+7

b) What is the importance of Stack Segment while implementing procedure mechanism in 8086? What happens in the Stack segment when calling a procedure or returning from a procedure? Explain with necessary diagrams. 4+3+8

2. **a)** Suppose, CS = (Last 4 digit of your student id)H, IP = (Last 4 digit of your best friend's student id)H. Now, find out the physical address according to the given logical address. What will be the starting and ending physical address of the mentioned code segment? 7+8

b) Suppose, AX = (Last 4 digit of your student id) H. 5+5+5

(i) Write a code segment that will set both LSB and MSB bit of AX.

(iI) Write a code segment that will clear the lower byte (AL) of AX.

(iii) Write a code segment that will toggle the upper byte (AH) of AX.

3. **a)** Write an assembly code to input a character then check and response whether it is a digit, alphabet or punctuation mark and display the strings accordingly: 12

i. It is a digit
ii. It is an alphabet
iii. It is a punctuation mark.
iv. Otherwise invalid

b) Write a procedure to find out the sum of even number series up to N, where N is the counting value/ limit of the series. 10

c) Explain the multiplication and division syntax in assembly language, with example code. 8

4. a) Explain the function of data bus transceiver 8286 with the help of DT/$\overline{R}$ and $\overline{DEN}$ and address latch 8282 with the help of ALE. 10

b) Draw the block diagram of 8086 in minimum mode configuration. 10

c) Mention the different control signals that are generated by the bus controller 8288 with the help of the status signals $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ in 8086 .

OR

a) Illustrate the functions of INTR and $\overline{NMI}$. Define bus operation in 8086. 10

b) Draw the read cycle diagram of 8086 in minimum mode. Also explain the necessary signals generated in bus timing during different clock periods. What is the effect of READY pin during this phase 20