

EEE 222 (CSE)

**ELECTRICAL AND ELECTRONICS
ENGINEERING II LAB**

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University of Asia Pacific (UAP)
Dept. of Electrical and Electronic Engineering (EEE)

EEE 222: Electrical and Electronics Engineering II Lab
Experiment No- 01

Study of a Single Phase Transformer and Determination of Turn Ratio

Introduction:

A transformer is a static device comprising coils coupled through a magnetic medium connecting two ports at different or same voltage levels in an electric system allowing the interchange of electrical energy between the ports in either direction via the magnetic field. The most important tasks performed by transformer.

1. Changing voltage and current levels in electric power system.
2. Matching source and load impedance for maximum power transfer in electrical and communication system.
3. Electrical isolation, isolating one circuit from another.

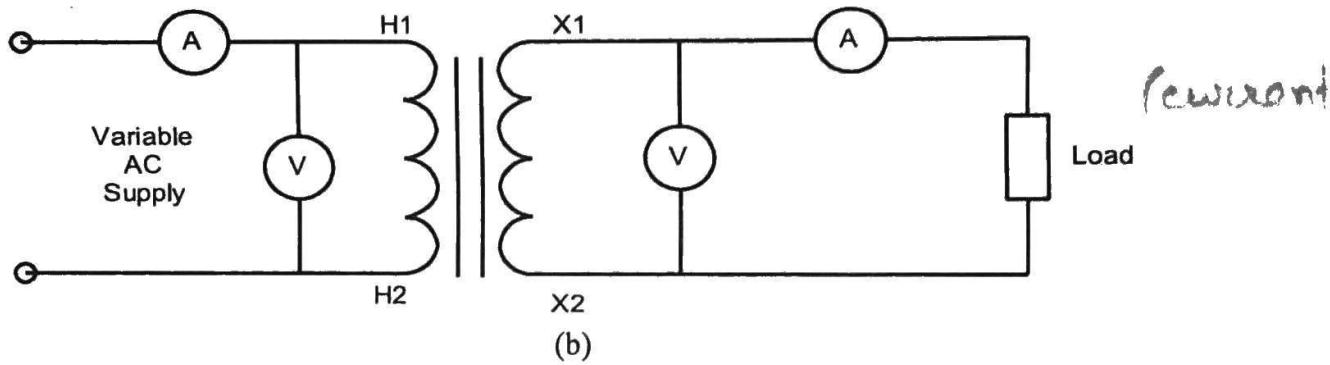
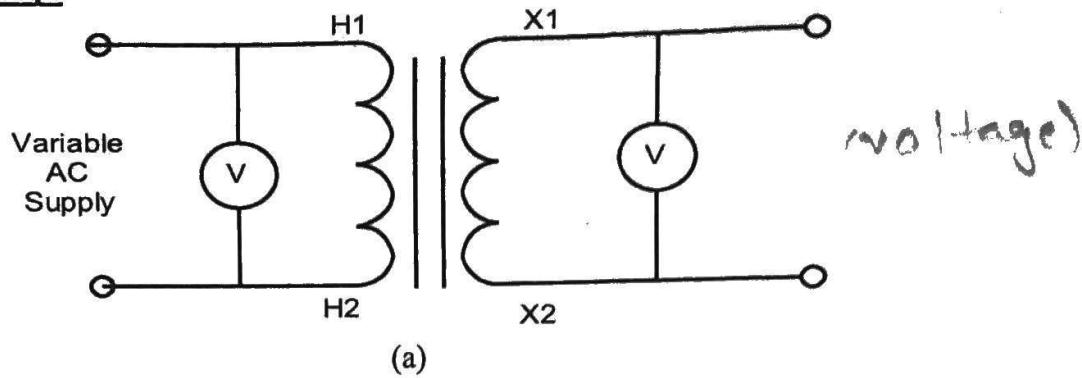
A transformer in its simple form consists essentially two insulated windings interlinked by a common or mutual magnetic field established in a core of magnetic material. When one of the windings termed the primary is connected to an alternating voltage source an alternating flux is produced in the core with amplitude depending on the primary voltage and number of primary turns. This mutual flux links the other winding called the secondary. A voltage is induced in this secondary and its magnitude will depend on the number of secondary turns if the secondary voltage is greater than the primary value the transformer is called a step up transformer. If it is less it is known as a step down transformer. If primary and secondary voltage is equal, the transformer is said to have a one to one ratio. One to one ratio transformer is used so electrically isolate two parts of a circuit. Any transformer may be used as a step up or step down depending on the way it is connected. The turn ratio of a transformer is defined as in this experiment we shall determine the turn ratio of a power transformer.

$$a = \frac{N_1}{N_2} = \frac{E_1}{E_2} = \frac{I_2}{I_1}$$

Apparatus:

1. Two AC voltmeters (0-300 V)
2. Two AC ammeters (0-10 A)
3. One single phase transformer.
4. One rheostat (current rating greater than or equal to 5 A)
5. Auto transformer (Variac)
6. Wires and cords.

Experimental Setup:



Procedure:

A. Voltage Ratio:-

1. Connect the primary ($H_1 - H_2$) terminals of the primary to 220 volt AC supply as shown in the figure- a.
2. Measure the voltage at the supply and also across secondary ($X_1 - X_2$).
3. Find the turn ratio using this formula:-

$$a = \frac{V_1(H_1 - H_2)}{V_2(X_1 - X_2)}$$

4. Repeat step-1 to step-3 for supply voltage 160 V, 180 V, 200 V, 220 V.

B. Current Ratio:-

1. Connect two ammeter in the primary and secondary circuit as shown in the figure- b.
2. Adjust the rheostat such that the reading of any ammeter does not exceed the current rating of the ammeters and the rheostat. Take three readings of both meters by adjusting the rheostat.
3. Find the turn ratio using the formula:-

$$a = \frac{I_2 (X_1 - X_2)}{I_1 (H_1 - H_2)}$$

Data sheet:

A. Voltage Ratio:-

E_1 (V)	E_2 (v)	$a = \frac{E_1}{E_2}$
160 V	79	2.025
180 V	89	2.022
200 V	99	2.020
220 V	109	2.018

B. Current Ratio:-

E_1 (V)	I_1 (A)	I_2 (A)	$a = \frac{I_2}{I_1}$
160 V	0.54	1.15	1.94
180 V	0.60	1.19	1.98
200 V	0.67	1.32	1.94
220 V	0.74	1.46	1.97

Report:

1. Show all the data in tabular form.
2. Determine the turn ratio (a) of the transformer from the voltage and current readings using the appropriate formula. Discuss the discrepancies if any.
3. Which method of determining turn ratio is more accurate and why?
4. Define the terms ideal transformer turn ratio, step up, and step down transformer.
5. Why transformers are rated in KVA instead of KW.
6. What will happen if we apply DC voltage in the primary winding?
7. Why current rating is important for rheostat?

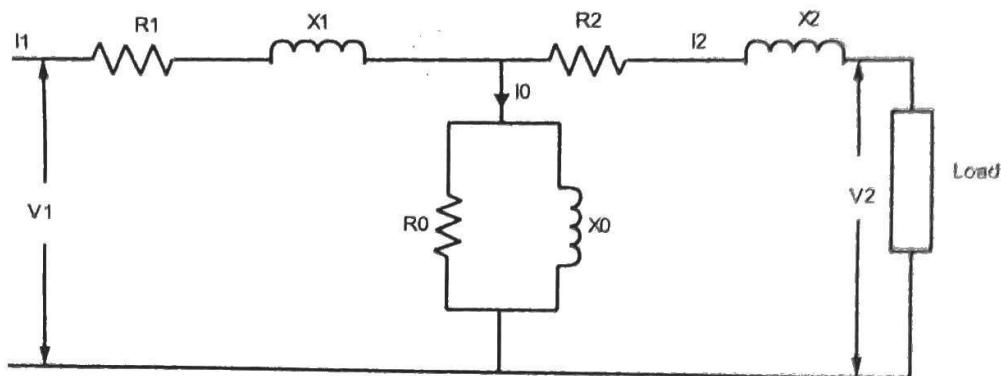
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Experiment No- 02

Open Circuit and Short Circuit Test of a Single Phase Transformer

Introduction:

A transformer is a static device by means of which electric power in one circuit is transferred into electric power in another circuit of the same frequency. It can step up or down the voltage in the circuit with a corresponding decrease or increase in current. So the volt-ampere rating of two circuits remains same. The equivalent circuit diagram of a single phase transformer is shown below.



The performances of a transformer can be calculated on the basics of its equivalent circuit contains four main parameters.

1. The equivalent resistance R_{01} referred to primary or R_{02} referred secondary side.
2. Equivalent leakage reactance X_{01} referred to primary or X_{02} referred secondary side.
3. Core loss conductance G_0 or resistance R_0
4. Magnetizing susceptance B_0 or reactance X_0

These parameters can be determined by the flowing two tests:-

1. Open circuit test.
2. Short circuit test.

At first determine the transformation ratio of the transformer: $a = \frac{E_1}{E_2}$

Apparatus:

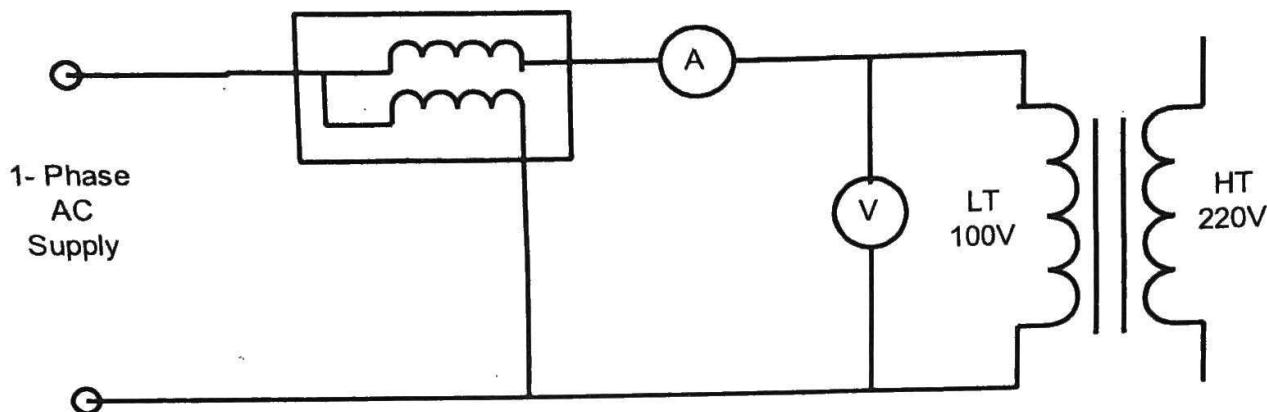
1. AC ammeter
2. AC voltmeter
3. Wattmeter
4. Single phase transformer – 220/100 V

Open circuit test:

This test determines no load loss of the transformer. The no load current I_0 helps to find X_0 and R_0 .

The circuit arrangement for this test is shown below.

Watt meter



Connect the instruments on the LT side with HT side open. Slowly apply the rated voltage on the LT side. Note down the readings of the instruments. From the wattmeter, ammeter, voltmeter.

Data sheet:

V_0 (V)	I_0 (A)	P_0 (W)	$\cos\theta_0 = \frac{P_0}{V_0 I_0}$	$I_w = I_0 \cos\theta_0$	$I_\mu = I_0 \sin\theta_0$
110	80 mA	3x2	$\frac{3}{2.5 \times 10}^4$	0.018mA	79.99 mA

$$P_0 = V_0 \times I_0 \times \cos\theta_0$$

Where $\cos\theta_0$ is called the low tension side power factor no load condition. The no load current has two components

1. Magnetizing current, $I_\mu = I_0 \sin\theta_0$
2. Working component, $I_w = I_0 \cos\theta_0$

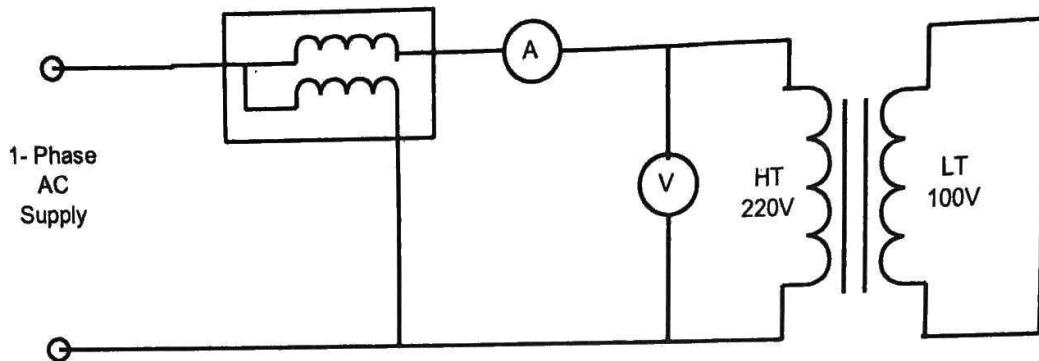
$$\text{Core resistance referred to LT side is: } R_0 = \frac{V}{I_w}$$

$$\text{Core reactance referred to LT side is: } X_0 = \frac{V}{I_\mu}$$

Short circuit test:

This test determines copper loss in the transformer. Finding this loss the regulation of the transformer can be determined. The circuit arrangement of this test is shown below.

Watt meter



Connect the ammeter, voltmeter, wattmeter in the HT side and LT side will be short circuited by pure copper wire.

Data sheet:

V_{sc} (v)	I_{sc} (A)	P_{sc} (watt)	$R_{01} = \frac{P_{sc}}{I_{sc}^2}$	$X_{01} = \sqrt{Z^2 - R_{01}^2}$
16.7	1 A	2 W	18	.

$$Z_0 = \frac{V_{sc}}{I_{sc}} = 16.7$$

$$P_{sc} = R_{01} \times I_{sc}^2$$

$$R_{01} = \frac{W_{sc}}{I_{sc}^2}$$

$$X_{01} = \sqrt{\{(V_{sc}/I_{sc})^2 - R_{01}^2\}}$$

Report:

- Find out the value of core resistance and reactance referred to the LT side from the open circuit test.
- Find out the value of copper resistance and leakage flux reactance referred to the HT side from the short circuit test.
- Why is it assumed that during open circuit all the losses are core losses?
- Why is it assumed that during sort test, all the loss is copper losses?
- Why open circuit test is performed in the LT side and short circuit test is performed in the HT side?

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Experiment No- 03

Analysis of Logic Gates using NMOS

Objective:

The objective of the experiment is to analyze the MOSFET gate circuits and to understand the internal operation of the circuit. The truth table of these gates have to be verified by giving different logic level at the input.

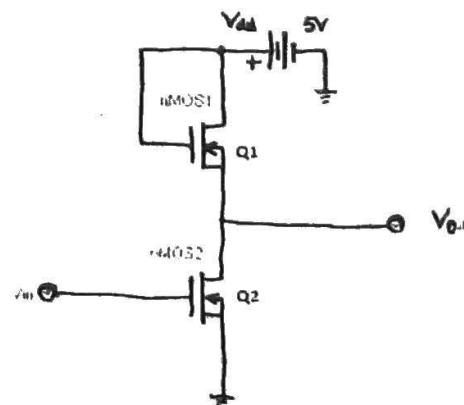
Apparatus:

1. MOSFET- 740N- 5 pieces
2. Resistor- 100 k Ω
3. Trainer board
4. Multimeter



NMOS NOT Gate:

It contains two NMOS Q1 and Q2 called switching MOS. As the gate of Q1 is permanently connected to +5V, it is always in ON state. Typically R_{ON} of Q1 is 100 k Ω . When a logic 0 (0 V) is applied at V_{in} , transistor Q2 is OFF. As a result, the output voltage is +5V. When logic 1 (5 V) is applied at V_{in} , Q2 is in ON state, as a result, output voltage will be 0 V.

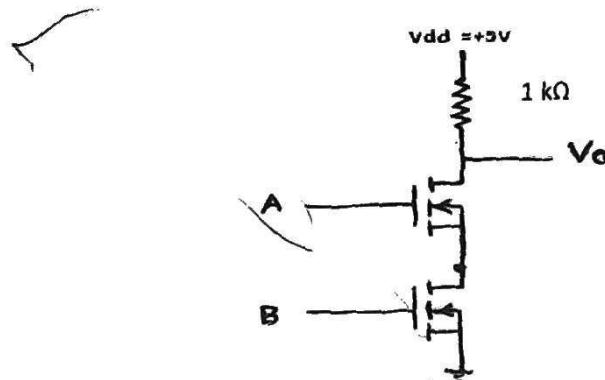


Truth Table of NOT gate:

V_{in}	V_{out}
0	1
1	0

NMOS NAND Gate:

In NMOS NAND gate two nMOS are connected in series. When logic 1 (5 V) is applied at the both input A and B, two nMOS will be at ON state. As a result, output voltage will be 0 V. In rest of the cases, the output voltage will always be logic high (5 V).



Truth Table of NAND gate:

A	B	Vout
0	0	1
0	1	1
1	0	1
1	1	0

Data Table:

a. NOT Gate:

Vin	Vout (Output Voltage)	Output Logic
0 V		
5 V		

b. NAND Gate:

A	B	Vout (Output Voltage)	Output Logic
0 V	0 V		
0 V	5 V		
5 V	0 V		
5 V	5 V		

Report:

1. Design a logic circuit of NOR and OR gate using NMOS only.
2. Design a logic circuit of 3-input NAND gate and also show the truth table.
3. Why we use nMOS instead of pMOS for designing the logic gates.

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Experiment No- 04

Study of Basic Configuration of Operational Amplifier

Objective:

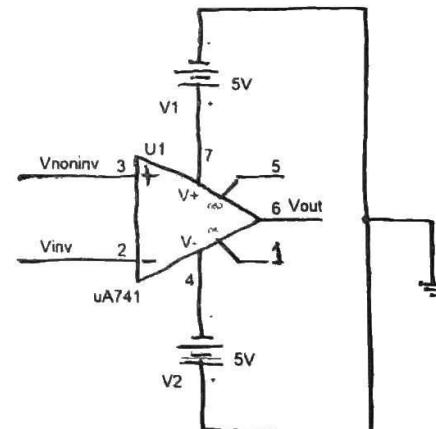
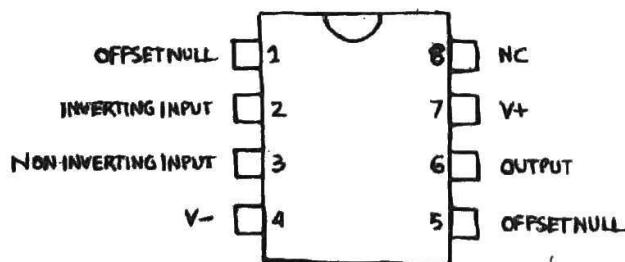
The objective of the experiment is to analyze the ac and dc performance of operational amplifier.

Apparatus:

1. Op-amp IC 741 (2)
2. Resistor- 1 kΩ (2), 2 kΩ (2), 4 kΩ (2)
3. Signal Generator
4. DC Voltage Source
5. Trainer board
6. Oscilloscope
7. Multimeter

Circuit Diagram:

The pin configuration of op-amp 741 is given below:-



1. Inverting Amplifier:

The gain of the inverting amplifier is: $\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$

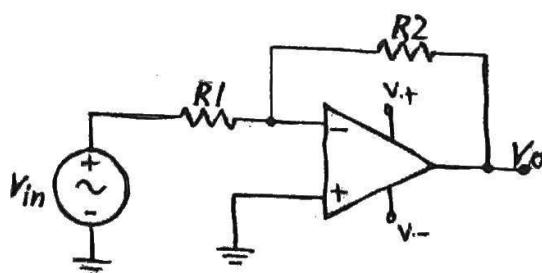


Figure- 1

2. Non-inverting Amplifier:

The gain of the non-inverting amplifier is: $\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$

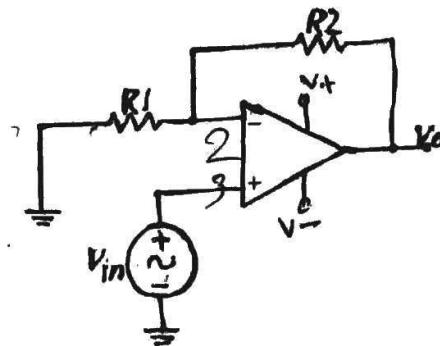


Figure- 2

3. Voltage Follower Circuit:

The gain of the voltage follower amplifier is: $\frac{V_{out}}{V_{in}} = 1$

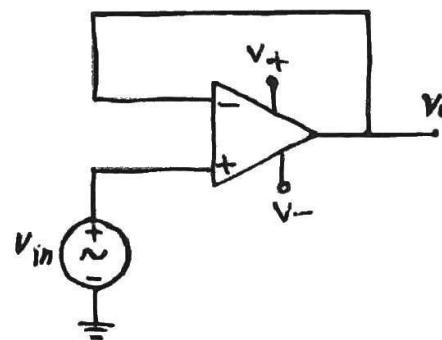


Figure- 3

4. Comparator Circuit:

Inverting terminal input < Non-inverting terminal input: $V_{out} = V_+$ (positive bias voltage)

Inverting terminal input > Non-inverting terminal input: $V_{out} = V_-$ (negative bias voltage)

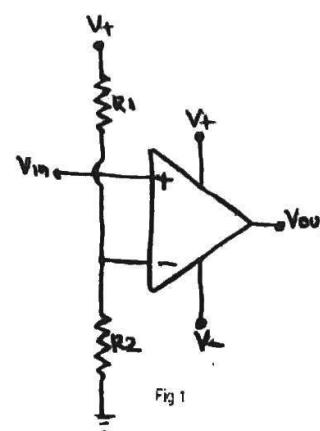


Fig 1

Figure- 4

Procedure:

1. a. Construct the circuit shown at Figure- 1 using $R_2 = 1k$ and $R_1 = 1k$.
b. Take a sinusoidal voltage of 1V p-p and 1 kHz frequency at the V_{in} .
c. Observe the V_{out} and V_{in} in dual mode.
d. Repeat steps 1c by using $R_2 = 2k$, $4k$ without changing the R_1 .
2. a. Construct the circuit shown at Figure- 2 using $R_2 = 1k$ and $R_1 = 1k$.
b. Take a sinusoidal voltage of 1V p-p and 1 kHz frequency at the V_{in} .
c. Observe the V_{out} and V_{in} in dual mode.
d. Repeat steps 1c by using $R_2 = 2k$, $4k$ without changing the R_1 .
3. a. Construct the circuit shown at Figure- 3.
b. Take a sinusoidal voltage of 1V p-p and 1 kHz frequency at the V_{in} .
c. Observe the V_{out} and V_{in} in dual mode.
4. a. Construct the circuit shown at Figure- 4 using $R_2 = 1k$ and $R_1 = 1k$.
b. Take a sinusoidal voltage of 1V p-p and 1 kHz frequency at the V_{in} .
c. Observe the V_{out} and V_{in} in dual mode.
d. Repeat steps 1c by using $R_2 = 2k$, $4k$ without changing the R_1 .

Report:

- ✓1. Draw the input output waveform for the circuit figure-1, 2, 3, and 4.
- ✓2. Also explain the effect of resistance value on the output waveform for the circuit figure-1, 2, and 4.
- 3. Design a circuit diagram that can generate a variable pulse width square wave from a sinusoidal wave. X
- ✓4. For a voltage follower circuit with ± 5 V biasing what will happen if we give a ± 6 V sine wave.

3. Design a non-amplifier gain is 5.

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Experiment No- 05

Analysis of Binary Weighted D/A Converter

Digital to Analog

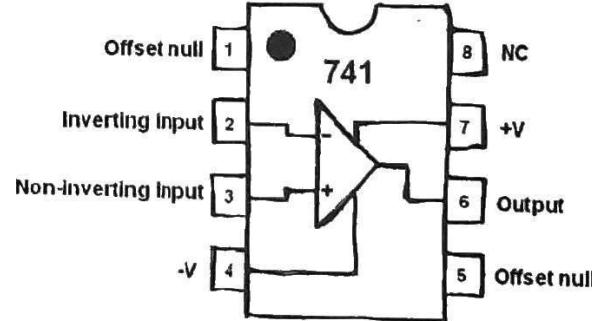
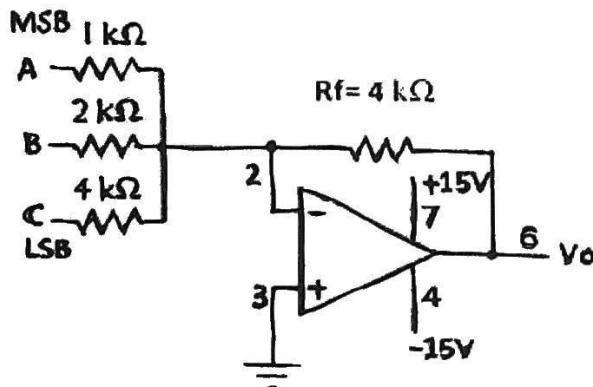
Objective:

The objective of the experiment is to construct the D/A converter and to verify that digital signal is converted to analog signal.

Apparatus:

1. Op-amp IC 741
2. Resistor- 1 kΩ (1), 2 kΩ (1), 4 kΩ (2)
3. Trainer board
4. Multimeter

Circuit Diagram:



Description:

The circuit diagram shows the basic circuit for 3 bit DAC. The input A, B, C are binary inputs which are assumed to have values either 1 (1 V) or 0 (0 V). The operational amplifier is employed as a summing amplifier, which produces the weighted sum of these input voltages. The output characteristics of inverting weighted summer is shown below:-

$$V_{out} = -R_f \left(\frac{V_a}{R_1} + \frac{V_b}{R_2} + \frac{V_c}{R_3} \right)$$

If, $R_1 = 1 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, $R_3 = 4 \text{ k}\Omega$, and $R_f = 4 \text{ k}\Omega$, then $V_{out} = -(4V_a + 2V_b + V_c)$. Here, V_c acts like LSB and V_a is the MSB.

The characteristics table of 3-bit DAC is shown below:-

V _a (V)	V _b (V)	V _c (V)	V _{out} (V)
0	0	0	0
0	0	1	-1
0	1	0	-2
0	1	1	-3
1	0	0	-4
1	0	1	-5
1	1	0	-6
1	1	1	-7

Procedure:

1. Construct the circuit according to the diagram.
2. Apply the supply voltage V_{cc} = +15 V and -15 V to Op-amp.
3. Logic High is 1 V and logic Low is 0 V.
4. Apply different input voltage level to the 3 input according to the table. Use Multimeter to observe the output voltage level and logic level and fill up the following table.

V _a (V)	V _b (V)	V _c (V)	V _{out} (V)
0	0	0	0.06
0	0	1	-0.94
0	1	0	-2.08
0	1	1	-3.08
1	0	0	-4.60
1	0	1	-5.6
1	1	0	-6.72
1	1	1	-7.71

Report:

1. Draw the circuit diagram of a 4-bit DAC and also derive the equation of 4-bit DAC.

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Experiment No- 06

Analysis of Flash ADC Converter

Objective:

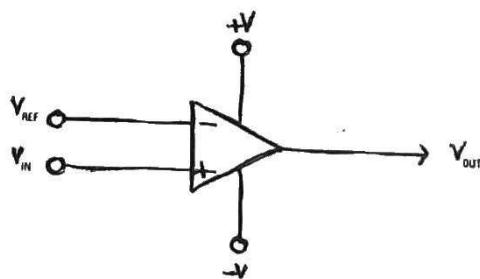
The objective of the experiment is to construct the flash ADC. In this experiment, we use comparator and priority encoder.

Apparatus:

1. Op-amp IC 741 (3)
2. Priority Encoder (IC 74148)
3. Resistor- 2 k Ω (1) ,1 k Ω (3)
4. DC Power Supply
5. Trainer board
6. Multimeter

Comparator:

In a comparator, if the + input (pin 3) is greater than the - input (pin 2), then the output will be high (+V_{SAT}). If the - input (pin 2) is greater than the + input (pin 3), then the output will be low (-V_{SAT}). The biasing is given +5V in pin 7 and 0V at pin 4.

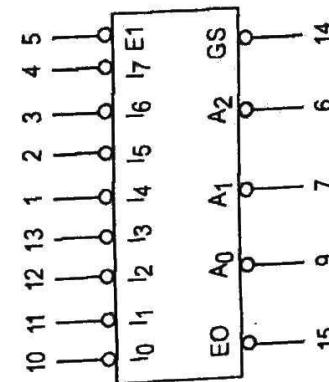


Priority Encoder:

IC 74148 is 8 input priority encoder accepts data from eight active LOW inputs (I_0-I_7) and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so represented on the output, with input line 7 having the highest priority. To activate the IC the enable pin E1 (pin 5) must be tied to ground. The functional table for IC 74148 is shown below:-

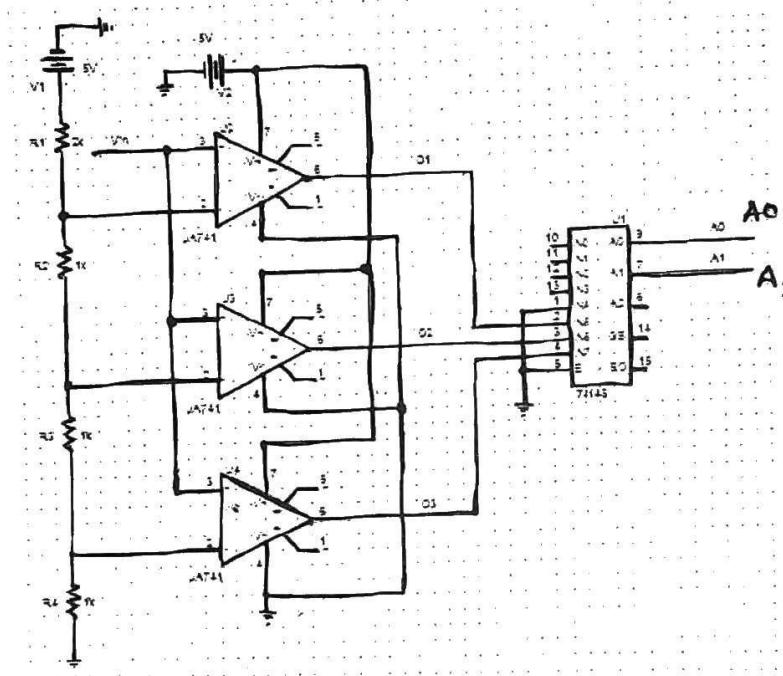
Inputs								Outputs					
E7	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	GS	A ₀	A ₁	A ₂	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care



V_{CC} = PIN 16
GND = PIN 8

Circuit Diagram:



A reference 5 V is divided by 4 series resistors (2k, 1k, 1k, 1k). As a result, the voltage at the negative terminal of comparators are 3 V, 2 V, and 1 V respectively (top to bottom). Input voltage V_{in} is given at the positive terminal of the each comparators. Whenever, V_{in} is greater than the corresponding negative terminal of the comparator output voltage will be high (5V), otherwise output voltage will be low (0 V). The output node from the three comparators (O1, O2, and O3) are connected with the IN5 (pin 2), IN6 (pin 3), and IN7 (pin 4) of IC74148 respectively. IN4 (pin 1) should be tied to the ground. The functional behavior of the 2-bit flash ADC is shown below:-

Vin	O1	O2	O3	IN4	IN5	IN6	IN7	A1	A0
0~1.0 V	0	0	0	0	0	0	0	L	L
1.0~2.0	0	0	5	0	0	0	5	L	H
2.0~3.0	0	5	5	0	0	5	5	H	L
3.0+	5	5	5	0	5	5	5	H	H

Procedure:

1. Construct the circuit shown in the diagram.
2. Check the output data bit by giving various input at the Vin.

Data Table:

Vin	O1	O2	O3	IN4	IN5	IN6	IN7	A1	A0
0~1.0 V								1	1
1.0~2.0							1		
2.0~3.0		1	1		1	1	1		1
3.0+					1	1	1	1	1

Report:

Construct a 3 bit flash ADC. Draw the circuit diagram.

Hints: It utilizes 7 comparators and 1 priority encoder. In the priority encoder, check the pin priority truth table of the IC appropriately. This circuit is similar as the 2 bit flash ADC. Construct the circuit and estimate the output voltage of the 7 comparators and the logic values of the output of the priority encoder.

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Experiment No- 07

Analysis of Astable Multivibrator using 555 timer

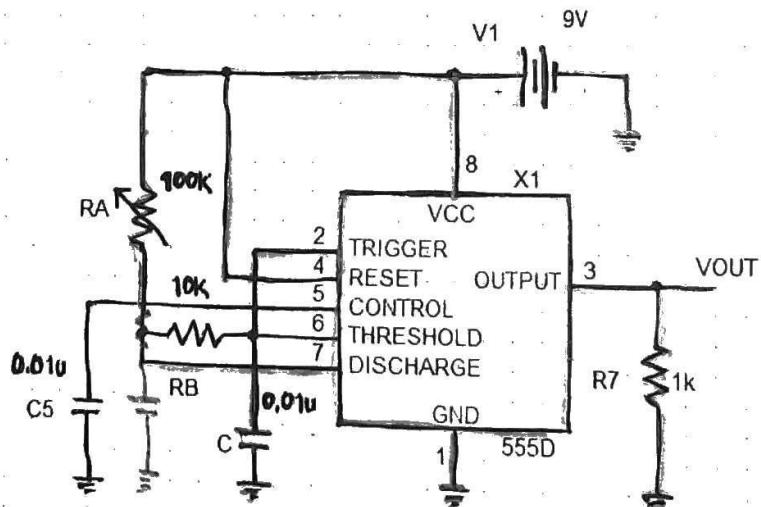
Objective:

The objective of the experiment is to analyze the astable multivibrator using 555 timer and to observe the output. To understand this first we have to understand the function of a 555 timer.

Apparatus:

1. Timer IC- 555
2. Capacitance- $0.01 \mu F$ (2)
3. Resistor- $10 k\Omega$ (2)
4. Variable Resistor- $100 k\Omega$ (1)
5. Trainer board
6. Multimeter
7. Oscilloscope

Circuit Diagram:



If the circuit is connected as shown in figure (pin- 2 and pin- 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through RA + RB and discharges through RB. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.693 (RA + RB) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (RB) C$$

Thus the total period is:

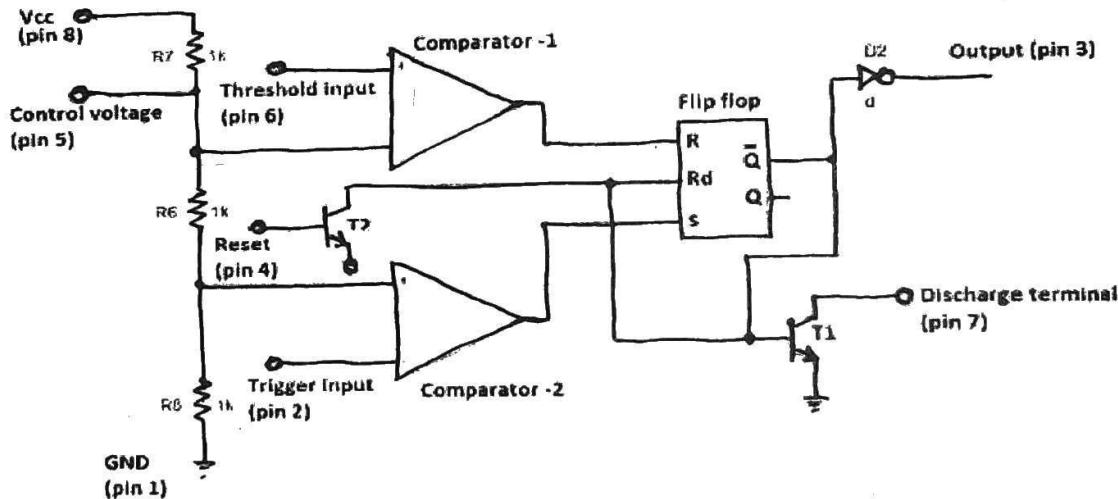
$$T = t_1 + t_2 = 0.693 (RA + 2RB) C$$

The frequency of oscillation is:

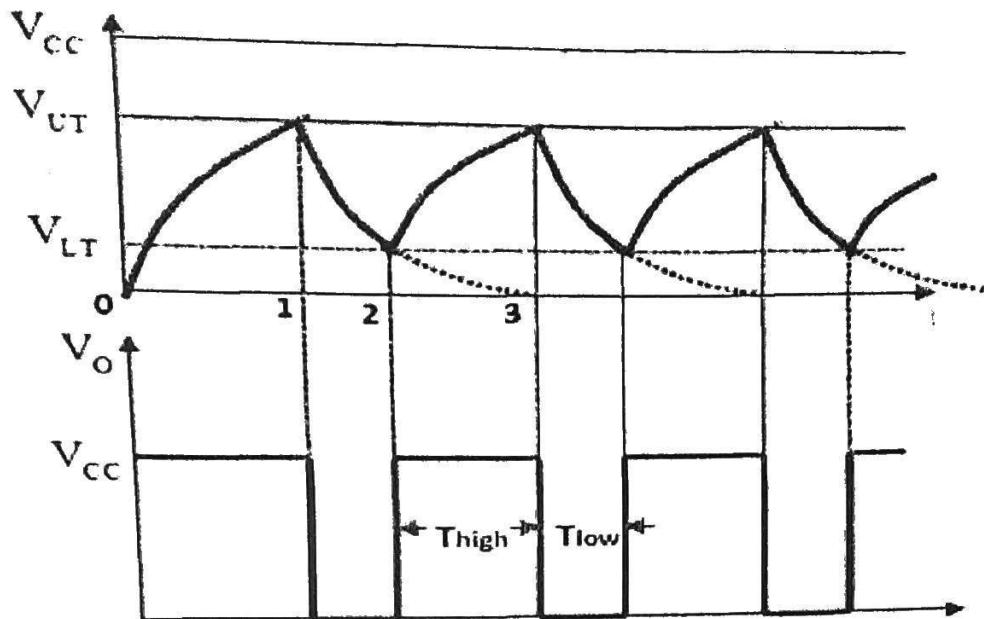
$$f = \frac{1}{T} = \frac{1.44}{(RA + 2RB)C}$$

The duty cycle is:

$$D = \frac{RB}{RA + 2RB}$$



It has two comparators, comparator 1 and 2, two transistors T1 and T2, an RS flip-flop and a output buffer stage (inverter). There are 3 resistors of equal value, which are connected between Vcc and ground. It provides the reference voltages for the two comparators. For the comparator 1, the reference voltage provided by the resistors is $2V_{cc}/3 = V_{UT}$. For comparator 2, the reference voltage provided by the resistors is $V_{cc}/3 = V_{LT}$. Transistor T1 is an npn and it provides the discharge path when the output is high. Transistor T2 facilitates the reset operation of the RS flip flop, but we have not used this transistor in this experiment, since the reset terminal is wired with Vcc.



Procedure:

1. Construct the circuit as shown in the figure.
2. Connect the trigger (pin 2) and output (pin 3) with the oscilloscope.
3. Draw the output waveform in the report portion.
4. Measure T_{high} , T_{low} , T from oscilloscope.

Report:

1. Draw the output wave shape of pin 3 from oscilloscope. Show T_{high} , T_{low} , T .
2. Draw the wave shape across the discharge capacitor (C). Show V_{LT} , V_{UT} changing time, discharging time in the wave shape.
3. Show if the charging time of capacitor is equal to T_{high} and discharging time of the capacitor is equal to T_{low} . Also check values of V_{LT} , V_{UT} .
4. Write the value of the following components:

$R_a =$

$R_b =$

$C =$

5. Measure the time of the positive going pulse at pin 3 from the oscilloscope $T_{high} =$
6. Compute T_{high} using the formula T_{high} . Is the computed value approximately same as the measured value? Discuss.