University of Asia Pacific (UAP)
Department of Computer Science

Course Outline

Program:	Computer Science and Engineering (CSE)
Course Title:	Computer Architecture
Course Code:	CSE 317
Semester:	Fall 2020
Level:	6th Semester
Credit Hour:	3.0
Name & Designation of Teacher:	Shammi Akhtar, Assistant Professor
Office/Room:	7th Floor, Teacher's Compound
Class Hours:	
Consultation Hours:	
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Rationale:	Required course and a pre-requisite for Digital System Design, Microprocessor and Operating System in the CSE program. The knowledge of this course is very important for the field of Hardware Design and Implementation.
Pre-requisite (if any)**:**	CSE 209: Digital Logic & System Design

Course Synopsis:

Introduction: Computer Architecture and Organization. Instruction set architecture: Overview of MIPS, basic instruction, high level to MIPS conversion of instruction, MIPS control and data path design. Computer arithmetic and number system: Binary review; floating point number representation; basic addition and multiplication algorithm and hardware. Advanced computer arithmetic: Booth multiplication scheme, recoding process, best and worst multiplier, average gain. Computer system performance and performance matrices: Execution time, clock rate, processor speed, CPI-clock per instruction, mathematical problems. Memory and cache hierarchy: Primary memory, secondary memory, memory hierarchy, virtual memory, caching scheme: direct addressed caching, other policies, Control design: Processor control Unit design and data path analysis, Pipelining: Pipelined data path and control, super scalar and dynamic pipelining. I/O organization: Introduction, bus control, I/O systems, programmed IO, DMA and interrupts, I/O processors, multiprocessor system: UMA, NUMA etc.

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Course Objectives: The objectives of this course are to:

1. **Explain** the layers of computer organization.
2. **Explain** terms related to computer organization.
3. **Introduce** with clock cycle, instruction cycle, performance, instruction format, addressing mode and instruction throughput of single-cycle, multi-cycle, and pipelined implementations of a simple instruction set and pipeline hazard.
4. **Provide** the knowledge **of** computer hardware, memory hierarchy, cache configurations, identification, placement, replacement Strategy and Show how cache design parameters affect cache hit rate.

Course Outcomes (CO) and their mapping with Program outcomes (PO) and Teaching-Learning Assessment methods:

CO No.	**CO Statements:** Upon successful completion of the course, students should be able to:	**Corresponding POs (Appendix-1)**	**Bloom's taxonomy domain/level (Appendix-2)**	**Delivery methods and activities**	**Assessment Tools**
CO1	**explain and apply** knowledge related to the layers of computer organization.	1	1/Apply	Lecture, multimedia.	Quiz, Presentation Class Test
CO2	**Analyze** clock cycle, instruction cycle, performance, instruction format, addressing mode and instruction throughput of single-cycle, multi-cycle, and pipelined implementations of a simple instruction**.**	2	1/Analyze	Lecture, Example from MIPS Instruction set	Class Tests, Class Works
CO3	**Design and implement** computer hardware, memory hierarchy, cache configurations, identification, placement, replacement Strategy and Show how cache design parameters affect cache hit rate.	3	1/Evaluate	Problem Exercise	Assignment, Project Planning Exercise

Weighting COs with Assessment methods:

Assessment Type	% weight	CO1	CO2	CO3
Final Exam	**50%**	15	15	20
Mid Term	**60%**	**15**	**30**	15
Class performance, Class Tests, Case study, Assignment, Project, On Spot Exercises	**30%**	6	12	12
Total	**100%**	26	34	40

Grading Policy: As per the approved grading policy of UAP (Appendix-3)

Course Content Outline and mapping with COs

Week	Topics	Course Outcome	Delivery methods and activities	Reading Materials
1-2	Topic 1: Computer Abstraction and Technology Introduction to computer architecture, processor and memory technologies, performance and power wall, switching from uniprocessor to multiprocessor.	CO1,CO2	Lecture, Multimedia	Chap: 1, Computer Organization and Design: The Hardware/Software Interface (5th Edition) and lecture slides
3-5	Topic 2: Instructions: Language of the Computer Classifying instructions set architecture, types and size of operands, operations in the instruction set, Instruction for flow control, Instructions format, Addressing modes, MIPS Assembly Language.	CO1, CO2,CO3,	Lecture, Multimedia	Chap: 2, Computer Organization and Design: The Hardware/Software Interface (5th Edition) and lecture slides
	CT-1			
6-7	Topic 3: Arithmetic for Computers Arithmetic	CO1, CO2,CO3	Lecture, Multimedia	Chap: 3, Computer Organization and Design:

	Operations (Addition, Subtraction, Multiplication and Division), Floating Point Representation, Floating Point Operations (Addition and Multiplication).			The Hardware/Software Interface (5th Edition) and lecture slides
	CT-2			
8	**Midterm Exam**			
9-10	Topic 4 : CPU Organization and Design Datapath, pipelining, pipelined datapath and control, instruction-level parallelism	CO1, CO3	Lecture, Multimedia Lecture, Example Problem	Chap: 4, Computer Organization and Design: The Hardware/Software Interface (5th Edition) and lecture slides
	CT 3			
11-12	Topic 5: Cache Hierarchies Memory hierarchies, Cache policies, Memory system, RAMs, ROMs – Speed, size and cost Performance consideration – Virtual memory	C01, CO2,CO3	Lecture, Multimedia Lecture, Example Problem	Chap: 5, Computer Organization and Design: The Hardware/Software Interface (5th Edition) and lecture slides
	CT 4			
13	Topic 6: Storage, Networks, and Other Peripherals Accessing I/O devices, Interrupts, Direct Memory Access, Buses, Interface Circuits, Standard I/O Interfaces (PCI, SCSI, USB).	CO1,CO2,CO3	Lecture, Multimedia Lecture, Example Problem	Chap: 6, Computer Organization and Design: The Hardware/Software Interface (3rd Edition) and lecture slides
14	Presentations Review			
	Final Exam	C01, CO2,CO2,CO3.		

Required References: Computer Organization and Design: The Hardware/Software Interface -David A. Patterson, John L. Hennessy (5th Edition)

Recommended References: Computer Organization & Architecture-Designing for Performance - William Stallings (6th Edition, Pearson Education, 2003 reprint)

Student's responsibilities: Students must come to the class prepared for the course material covered in the previous class (es).
They must submit their assignments on time.

No late or partial assignments will be acceptable. There will be no make-up quizzes/class tests.

Special Instructions:

- Minimum 70% attendance is required for a student to appear in the final exams
- Late presence Any student coming after 20 minutes will miss the attendance

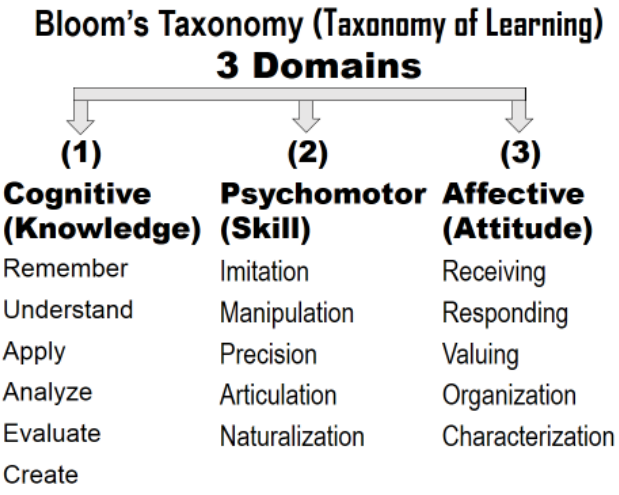
Prepared by	Checked by	Approved by
SHAMMI AKHTAR	Chairman, PSAC committee	Head of the Department

Appendix-1:

Washington Accord Program Outcomes (PO) for engineering programs:

No.	PO	Differentiating Characteristic
1	Engineering Knowledge	Breadth and depth of education and type of knowledge, both theoretical and practical
2	Problem Analysis	Complexity of analysis
3	Design/ development of solutions	Breadth and uniqueness of engineering problems i.e. the extent to which problems are original and to which solutions have previously been identified or codified
4	Investigation	Breadth and depth of investigation and experimentation
5	Modern Tool Usage	Level of understanding of the appropriateness of the tool
6	The Engineer and Society	Level of knowledge and responsibility
7	Environment and Sustainability	Type of solutions.
8	Ethics	Understanding and level of practice
9	Individual and Team work	Role in and diversity of team
10	Communication	Level of communication according to type of activities performed
11	Project Management and Finance	Level of management required for differing types of activity
12	Lifelong learning	Preparation for and depth of Continuing learning.

Appendix-2



Appendix-3

UAP Grading Policy:

Numeric Grade	Letter Grade	Grade Point