INTEL 8086 MICROPROCESSR ARCHITECTURE

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FEATURES

- *It is a 16-bit µp.*
- *8086 has a 20 bit address bus can access up to 2^{20}memory locations (1 MB).*
- *It can support up to 64K I/O ports.*
- *It provides 14, 16 -bit registers.*
- *Word size is 16 bits and double word size is 4 bytes.*
- *It has multiplexed address and data bus AD0- AD15 and A16 – A19.*

- *8086 IS DESIGNED TO OPERATE IN TWO MODES, MINIMUM AND MAXIMUM.*
- *It can prefetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution.*
- *It requires +5V power supply.*
- *A 40 pin dual in line package.*
- *Address ranges from 00000H to FFFFFH*

INTEL 8086 INTERNAL ARCHITECTURE

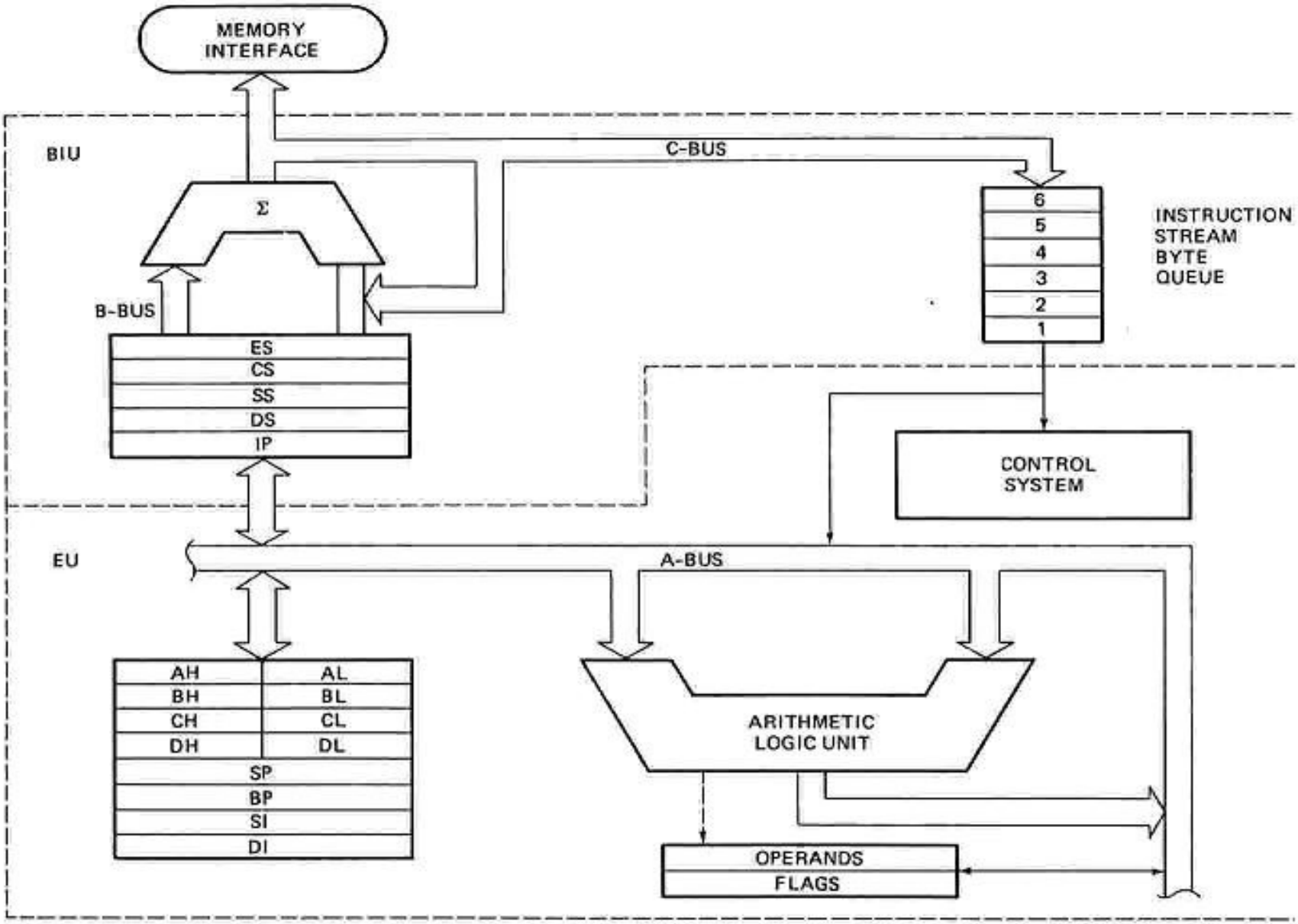

FIGURE 8086 internal block diagram. (*Intel Corp.*)

INTERNAL ARCHITECTURE OF 8086

- 8086 has two blocks BIU and EU.
- The BIU handles all transactions of data and addresses on the buses for EU.
- The BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands. The instruction bytes are transferred to the instruction queue.
- EU executes instructions from the instruction system byte queue.

- **BIU contains Instruction queue, Segment registers, Instruction pointer, Address adder.**
- **EU contains Control circuitry, Instruction decoder, ALU, Pointer and Index register, Flag register.**

EXECUTION UNIT

- Decodes instructions fetched by the BIU
- Generate control signals,
- Executes instructions.

The main parts are:

- Control Circuitry
- Instruction decoder
- ALU