University of Asia Pacific

Department of CSE

Mid-Semester Examination Fall 2020

Program: B.sc in CSE

Course Title: Computer Architecture Course No. CSE 317

Credit: 3.00 Time: 1.20 Hour. Full Mark: 60

There are **THREE** Questions. **Answer All questions.**

1. a. Draw the basic components of computer and Layer of a computer. Show the relationship among Instruction Set, Software and Hardware that define computer architecture. **[5]**

b. Define the following terms: **5**

- Response time/ execution time
- Bandwidth/ throughput
- Relative performance
- Measuring performance
- Clock cycle

c. Compiler designer is trying to decide between two code sequences for a particular machine. Based on the hardware implementation, there are three different classes of instructions: Class A, Class B, and Class C, and they require three, two, and four cycles (respectively). **10**
The first code sequence has 10 instructions:5 of A, 2 of B, and 3 of C.
The second sequence has 12 instructions: 6 of A, 4 of B, and 2 of C.

Which sequence will be faster? How much?

2. a. Briefly explain instruction classes are in MIPS architecture? In MIPS arithmetic there are exactly 3 operands, Why? **5**

b. For the following high-level statement write the MIPS machine Code. **[15]**

A[i] = C + A[i+5] ; Where i = last two digits of your registration number.

OR

a. Suppose you have an implementation of 16 bits processor. Draw the flow graph of optimized multiplication algorithm for this 16-bit processor. Also draw the hardware organization for this. **[5]**

b. i)For the following high-level statement write the MIPS machine Code. **[15]**

X[i] = Z + X[i+7]; Where i = last two digits of your registration number.

A= X[i] -Y;

ii)What is the assembly language statement corresponding to this machine Instruction?

02324020hex.

3. a. Solve the following using **Booth's** logic. **[15]**

m*(mx) using 5-bits multiplier.

Where m = multiplicand = {(last digit of your registration) mod 6} + 2.

mx = multiplier = -4 .

b. Compare all the multiplication algorithms according to hardware and flow graphs. **[5]**

Instruction	Opcode/Function
lw	100011
sw	101011
sub	100010
add	100000