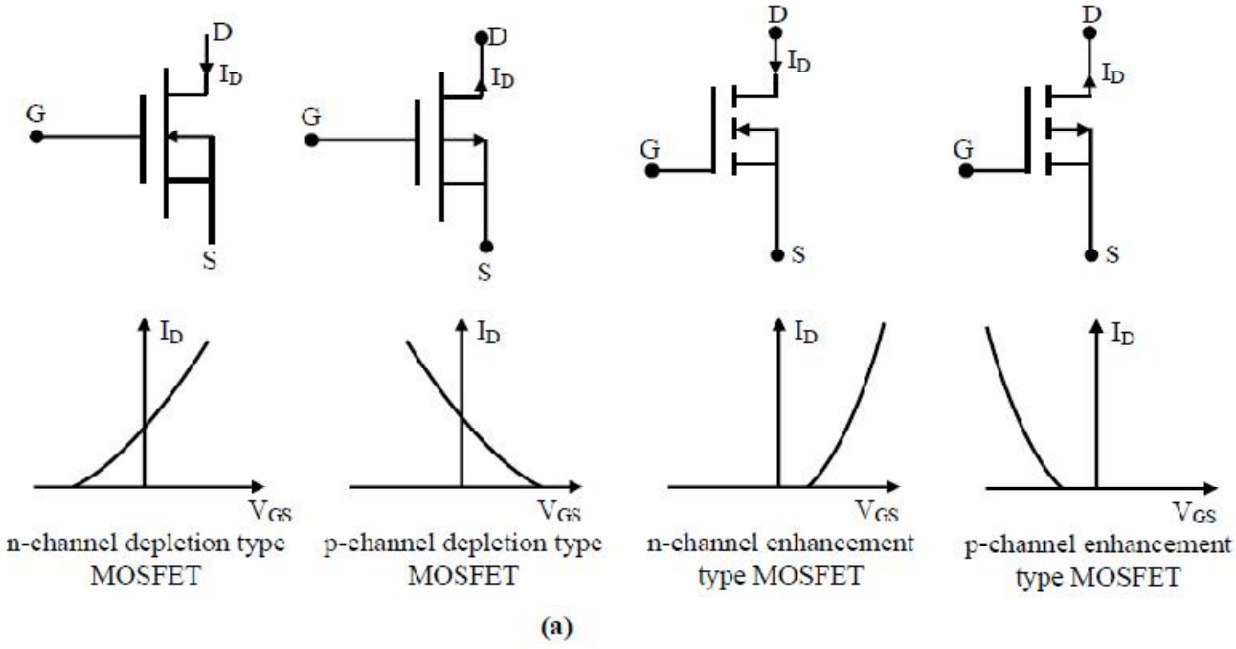
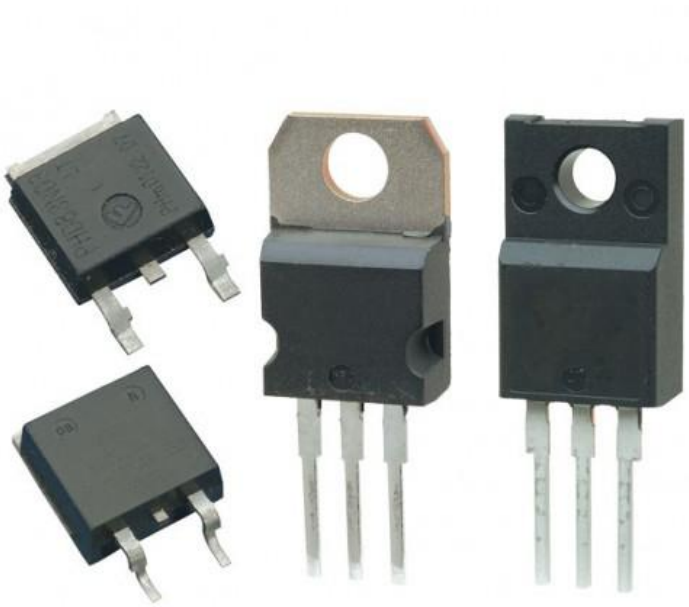
Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

From the point of view of the operating principle a MOSFET is a voltage controlled majority carrier device. As the name suggests, movement of majority carriers in a MOSFET is controlled by the voltage applied on the control electrode (called gate) which is insulated by a thin metal oxide layer from the bulk semiconductor body. The electric field produced by the gate voltage modulate the conductivity of the semiconductor material in the region between the main current carrying terminals called the Drain (D) and the Source (S). Power MOSFETs, just like their integrated circuit counterpart, can be of two types (i) depletion type and (ii) enhancement type. Both of these can be either n- channel type or p-channel type depending on the nature of the bulk semiconductor. Fig 6.1 (a) shows the circuit symbol of these four types of MOSFETs along with their drain current vs gate-source voltage characteristics (transfer characteristics).



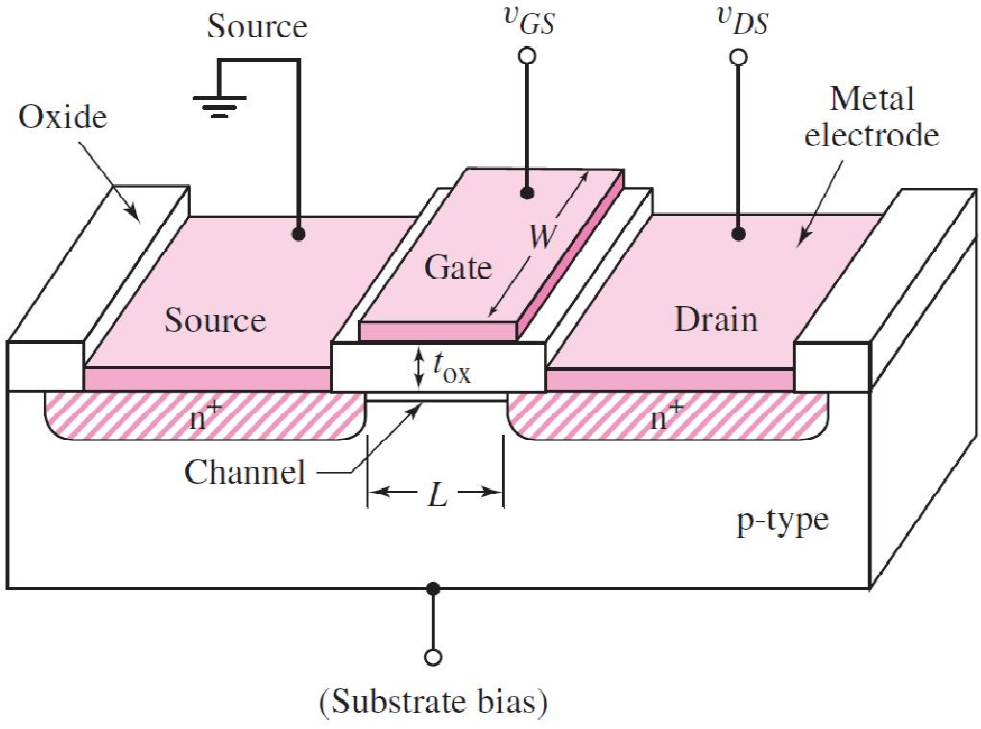
(a)

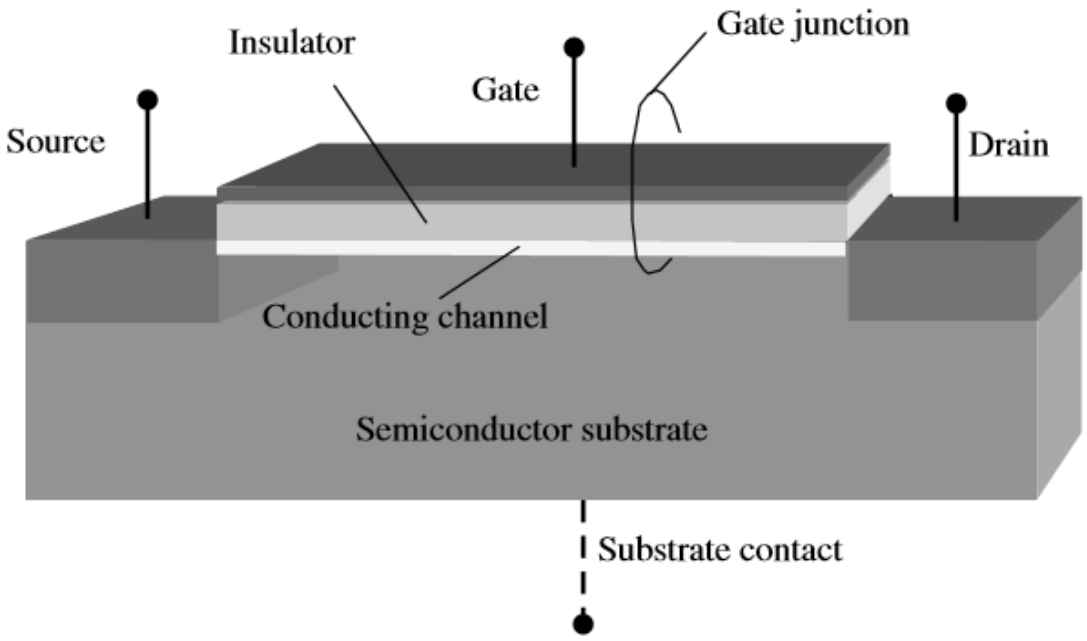
From Fig 6.1 (a) it can be concluded that depletion type MOSFETs are normally ON type switches i.e, with the gate terminal open a nonzero drain current can flow in these devices. This is not convenient in many power electronic applications. Therefore, the enhancement type MOSFETs (particularly of the n-channel variety) is more popular for power electronics applications. This is the type of MOSFET which will be discussed in this lesson. Fig 6.1 (b) shows the photograph of some commercially available n-channel enhancement type Power MOSFETs.



(b)

Almost universally, the MOS structure utilizes doped silicon as the substrate and its native oxide, silicon dioxide, as the insulator. In the silicon–silicon dioxide system, the density of surface states at the oxide–semiconductor interface is very low compared to the typical channel carrier density in a MOSFET. Also, the insulating quality of the oxide is quite good.



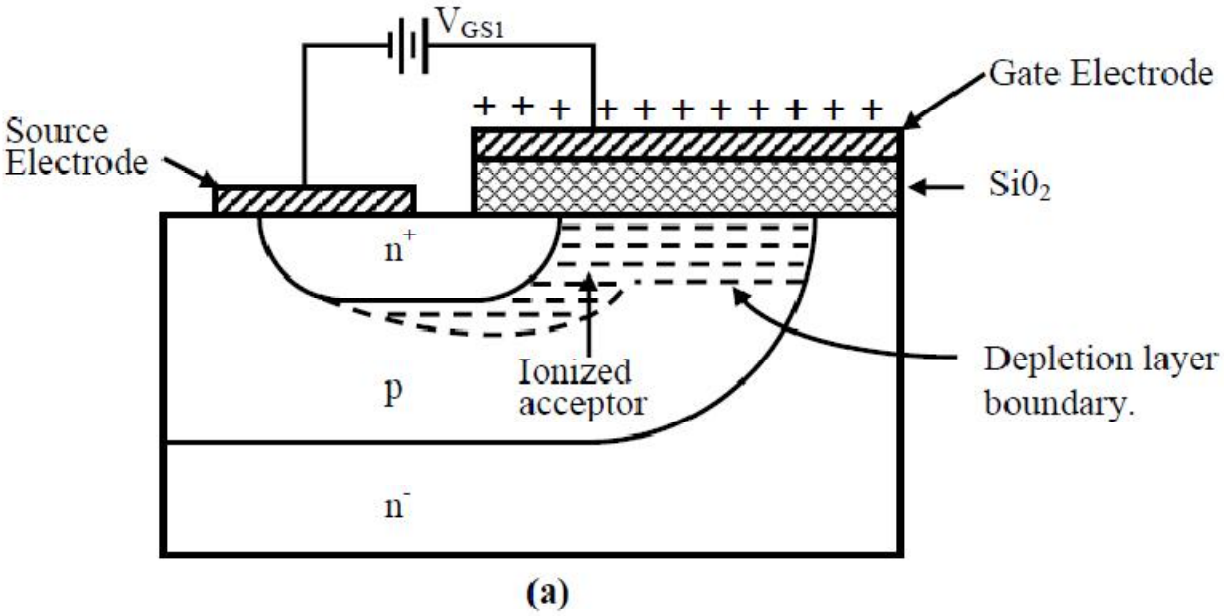


We assume that the insulator layer has infinite resistance, preventing any charge carrier transport across the dielectric layer when a bias voltage is applied between the metal and the semiconductor. Instead, the applied voltage will induce charges and counter charges in the metal and in the interface layer of the semiconductor, similar to what we expect in the metal plates of a conventional parallel plate capacitor. However, in the MOS capacitor we may use the applied voltage to control the type of interface charge we induce in the semiconductor – majority carriers, minority carriers, and depletion charge. Indeed, the ability to induce and modulate a conducting sheet of minority carriers at the semiconductor–oxide interface is the basis for the operation of the MOSFET.

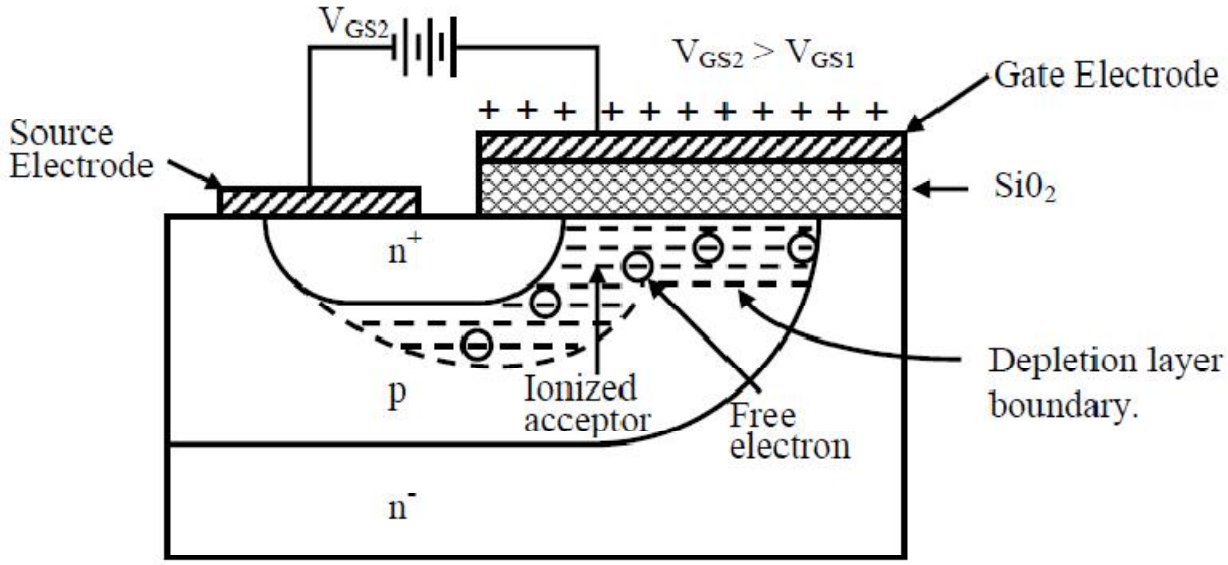
Operating principle of a MOSFET

At first glance it would appear that there is no path for any current to flow between the source and the drain terminals since at least one of the p n junctions (source – body and body-Drain) will be reverse biased for either polarity of the applied voltage between the source and the drain. There is no possibility of current injection from the gate terminal either since the gate oxide is a very good insulator. However, application of a positive voltage at the gate terminal with respect to the source will covert the silicon surface beneath the gate oxide into an n type layer or "channel", thus connecting the Source to the Drain as explained next.

The gate region of a MOSFET which is composed of the gate metallization, the gate (silicon) oxide layer and the p-body silicon forms a high quality capacitor. When a small voltage is application to this capacitor structure with gate terminal positive with respect to the source (note that body and source are shorted) a depletion region forms at the interface between the SiO_2 and the silicon as shown in Fig 6.4 (a).



(a)



(b)

The positive charge induced on the gate metallization repels the majority hole carriers from the interface region between the gate oxide and the p type body. This exposes the negatively charged acceptors and a depletion region is created.

Further increase in V_{GS} causes the depletion layer to grow in thickness. At the same time the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as shown in Fig 6.4 (b). The immediate source of electron is electron-hole generation by thermal ionization. The holes are repelled into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons from the source.

As V_{GS} increases further the density of free electrons at the interface becomes equal to the free hole density in the bulk of the body region beyond the depletion layer. The layer of free electrons at the interface is called the inversion layer and is shown in Fig 6.4 (c). The inversion layer has all the properties of an n type semiconductor and is a conductive path or "channel" between the drain and the source which permits flow of current between the drain and the source. Since current conduction in this device takes place through an n- type "channel" created by the electric field due to gate source voltage it is called "Enhancement type n-channel MOSFET".

CMOS

The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices.

One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistor consists P-channel MOS (PMOS) and N-channel MOS (NMOS).

One disadvantage of CMOS is slow speed, as compared to TTL. The input capacitances of a CMOS gate are much, much greater than that of a comparable TTL gate—owing to the use of MOSFETs rather than BJTs—and so a CMOS gate will be slower to respond to a signal transition (low-to-high or vice versa) than a TTL gate, all other factors being equal. The RC time constant formed by circuit resistances and the input capacitance of the gate tend to impede the fast rise- and fall-times of a digital logic level, thereby degrading high-frequency performance.

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of

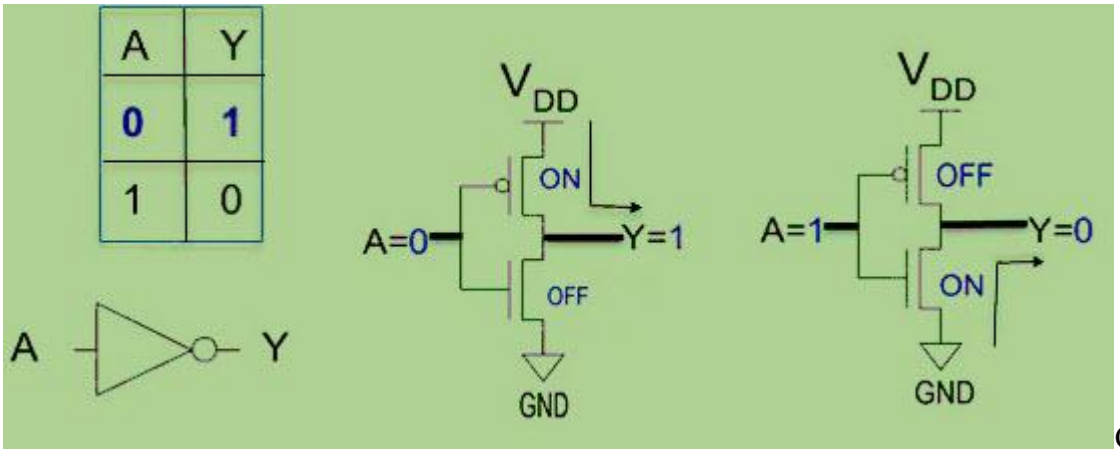
the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.

CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed). Furthermore, for the better understanding of the Complementary Metal Oxide Semiconductor working principle, we need to discuss in brief about CMOS logic gates as explained below.

CMOS Inverter

The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.



CMOS Inverter

The NMOS transistor has an input from Vss (ground) and PMOS transistor has an input from Vdd. The terminal Y is output. When a high voltage (~ Vdd) is given at input terminal (A) of the inverter, the PMOS becomes open circuit and NMOS switched OFF so the output will be pulled down to Vss.

When a low-level voltage (<Vdd, ~0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes Vdd or the circuit is pulled up to Vdd.