Department of CSE, Fall 2019

Group #3

Lecture Plan

Course Name: Digital Logic and System Design Lab.
Course Code: CSE 210, Credit Hours: 1.5
No. of Experiment: 12

Experiment No	Name of the Experiment
01	Test and verify the truth table of following gates: AND gate, OR gate, NOT gate, NAND gate, NOR gate, Exclusive-OR gate.
02	a) Simplify the given logic expression and verify the truth table. b) Design a logic circuit from a given problem.
03	a) Test and verify the Universality of NAND gate. b) Test and verify the Universality of NOR gate.
04	a) Design Half Adder and Full Adder b) Test and verify the 4-bit parallel Adder(IC # 7483) c) Design Sub tractor using IC # 7483
05	a) Design a 4 bit AU using Full Adder.
06	a) Test and verify the truth table of JK flip-flop(IC# 7476). d) Test and verify the truth table of Clocked JK flip-flop. e) Test and verify the truth table of Clocked D flip-flop.
07	a) Design and verify MOD 8 asynchronous up counter. b) Design and verify MOD 8 asynchronous down counter. c) Design and verify MOD 8 asynchronous up/down counter.
08	a) Design and verify MOD 10 asynchronous up counter. b) Design and verify MOD 10 asynchronous down counter.
09	a) Design and verify MOD 4 Ring counter. b) Design and verify MOD 8 Johnson counter. c) Using IC# 74293 design MOD 8, MOD 10, MOD 13, MOD 16, MOD60 counter.

10	a) Test and verify the 1 of 8 decoder(IC# 74138). b) Using IC# 74138 design 1 of 16 decoder. c) Test and verify the 8 input MUX(IC# 74151). d) Using IC# 74151 design 16 input MUX. e) Design and implementation of 4 bit Logic unit.
11	Using circuit maker. Design and testing 4-bit Arithmetic and Logic Unit (ALU) by combining AU and LU using MUX.
12.	Design a 4-bit register using D FFs. Testing the following transfer i. Parallel I/P- Parallel O/P ii. Parallel I/P-Serial O/P iii. Serial I/P- Parallel O/P Serial I/P and Serial O/P