

By simply drawing a line down to the horizontal axis, we can determine the diode voltage V_{D_q} , whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_q} . The current I_D is actually the current through the entire series configuration of Fig. 2.1a. The point of operation is usually called the *quiescent point* (abbreviated "Q-point") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same as would be obtained by a simultaneous mathematical solution of

$$I_D = \frac{E}{R} - \frac{V_D}{R} \quad [\text{derived from Eq. (2.1)}]$$

and

$$I_D = I_s(e^{V_D/nV_T} - 1)$$

as demonstrated later in this section in a Mathcad example. Since the curve for a diode has nonlinear characteristics, the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{D_q} and I_{D_q} were obtained. The next example demonstrates the techniques introduced above and reveals the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

- V_{D_q} and I_{D_q} .
- V_R .

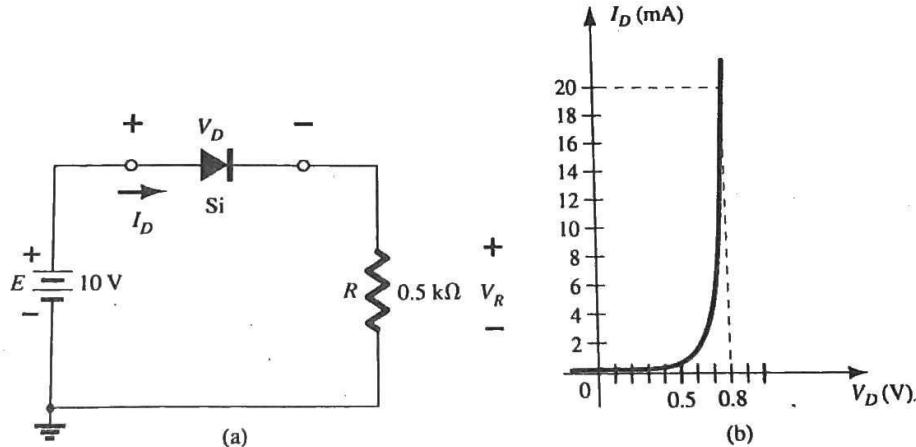


FIG. 2.3
(a) Circuit; (b) characteristics.

Solution:

a. Eq. (2.2): $I_D = \frac{E}{R} \Big|_{V_D=0\text{ V}} = \frac{10\text{ V}}{0.5\text{ k}\Omega} = 20\text{ mA}$

Eq. (2.3): $V_D = E \Big|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_q} \cong 0.78\text{ V}$$

$$I_{D_q} \cong 18.5\text{ mA}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

b. $V_R = I_R R = I_{D_q} R = (18.5\text{ mA})(1\text{ k}\Omega) = 18.5\text{ V}$

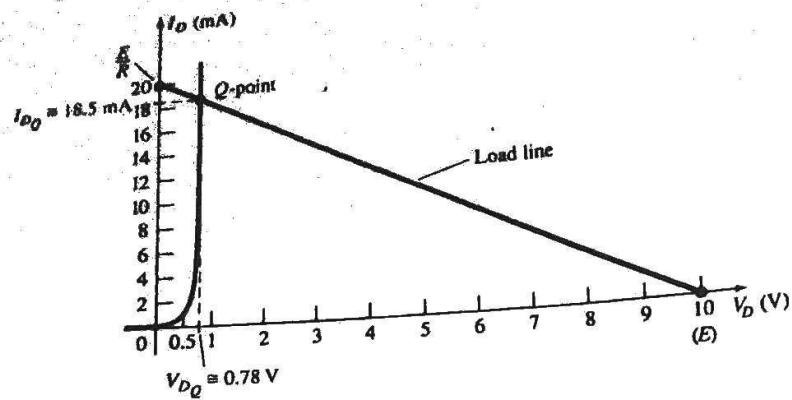


FIG. 2.4
Solution to Example 2.1.

As noted in the example above, the load line is determined solely by the applied network, whereas the characteristics are defined by the chosen device. If we turn to our approximate model for the diode and do not disturb the network, the load line will be exactly the same as obtained in the example above. In fact, the next two examples repeat the analysis of Example 2.1 using the approximate model to permit a comparison of the results.

EXAMPLE 2.2 Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

Solution: The load line is redrawn as shown in Fig. 2.5 with the same intersections as defined in Example 2.1. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting *Q*-point is

$$V_{D_0} = 0.7 \text{ V}$$

$$I_{D_0} = 18.5 \text{ mA}$$

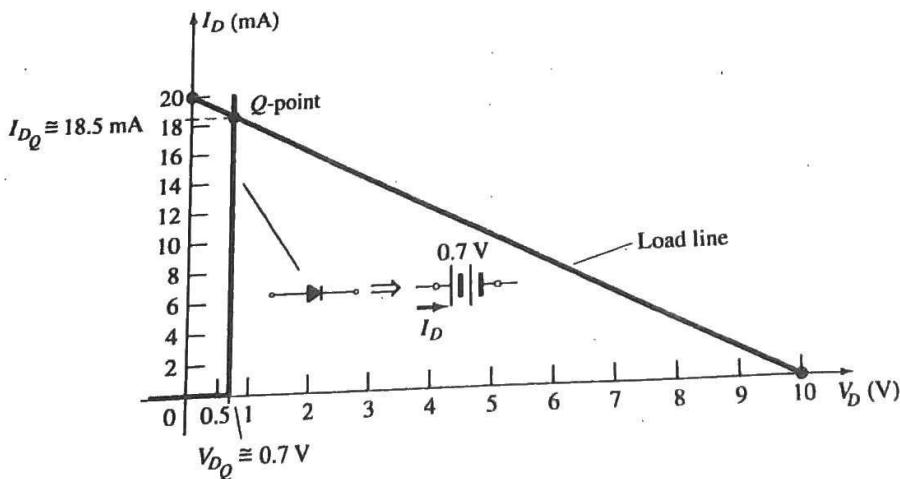


FIG. 2.5
Solution to Example 2.1 using the diode approximate model.

The results obtained in Example 2.2 are quite interesting. The level of I_{D_0} is exactly the same as obtained in Example 2.1 using a characteristic curve that is a great deal easier to draw than that appearing in Fig. 2.4. The $V_D = 0.7 \text{ V}$ here and the 0.78 V from Example 2.1 are of a different magnitude to the hundredths place, but they are certainly in the same neighborhood if we compare their magnitudes to the magnitudes of the other voltages of the network.

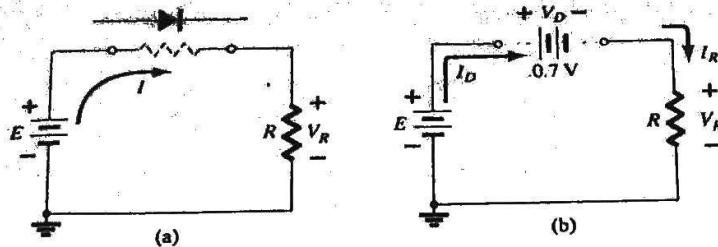


FIG. 2.9

(a) Determining the state of the diode of Fig. 2.8; (b) substituting the equivalent model for the "on" diode of Fig. 2.9a.

that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

$$V_D = V_R \quad (2.4)$$

$$V_R = E - V_K \quad (2.5)$$

$$I_D = I_R = \frac{V_R}{R} \quad (2.6)$$

In Fig. 2.10 the diode of Fig. 2.7 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.11 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.12. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0 \text{ A}) R = 0 \text{ V}$$

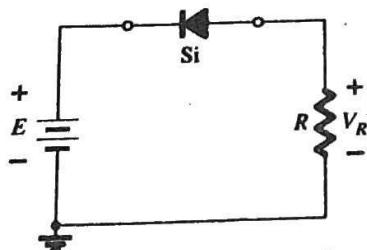


FIG. 2.10

Reversing the diode of Fig. 2.8.

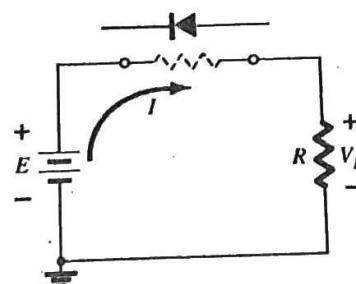


FIG. 2.11

Determining the state of the diode of Fig. 2.10.

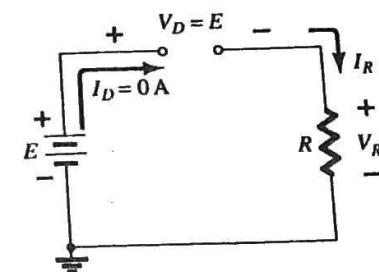


FIG. 2.12

Substituting the equivalent model for the "off" diode of Fig. 2.10.

The fact that $V_R = 0 \text{ V}$ will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13, determine V_D , V_R , and I_D .

Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = 0.7 \text{ V}$$

$$V_R = E - V_D = 8 \text{ V} - 0.7 \text{ V} = 7.3 \text{ V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3 \text{ V}}{2.2 \text{ k}\Omega} \cong 3.32 \text{ mA}$$

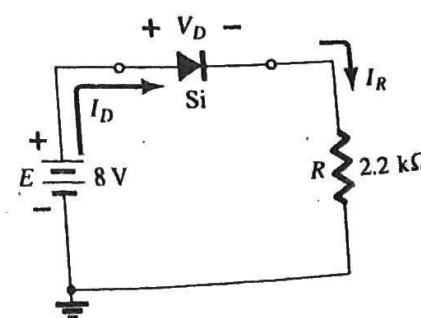


FIG. 2.13

Circuit for Example 2.4.

EXAMPLE 2.5 Repeat Example 2.4 with the diode reversed.

Solution: Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.14, where $I_D = 0\text{ A}$ due to the open circuit. Since $V_R = I_R R$, we have $V_R = (0)\text{R} = 0\text{ V}$. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = 8\text{ V}$$

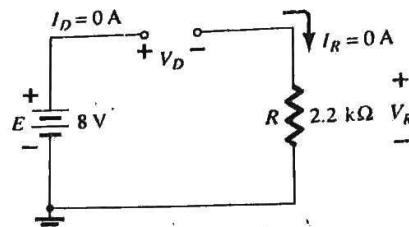


FIG. 2.14
Determining the unknown quantities for
Example 2.5.

In particular, note in Example 2.5 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

An open circuit can have any voltage across its terminals, but the current is always 0 A.
A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.15 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

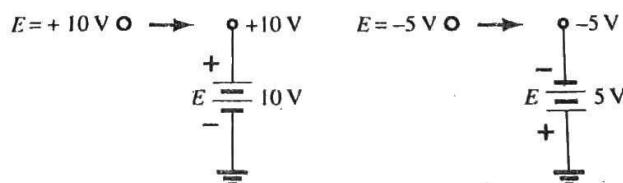


FIG. 2.15
Source notation.

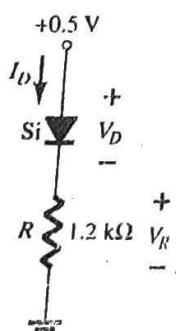


FIG. 2.16

Series diode circuit for
Example 2.6.

EXAMPLE 2.6 For the series diode configuration of Fig. 2.16, determine V_D , V_R , and I_D .

Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.17, establishing the open-circuit equivalent as the appropriate approximation, as shown in Fig. 2.18. The resulting voltage and current levels are therefore the following:

$$I_D = 0\text{ A}$$

$$V_R = I_R R = I_D R = (0\text{ A}) 1.2\text{ k}\Omega = 0\text{ V}$$

$$V_D = E = 0.5\text{ V}$$

and

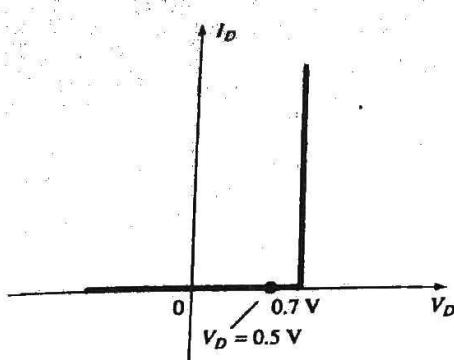


FIG. 2.17
Operating point with $E = 0.5 \text{ V}$.

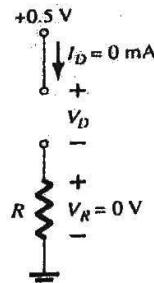


FIG. 2.18
Determining I_D , V_R , and V_D for the circuit of Fig. 2.16.

EXAMPLE 2.7 Determine V_o and I_D for the series circuit of Fig. 2.19.

Solution: An attack similar to that applied in Example 2.4 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.20 results because $E = 12 \text{ V} > (0.7 \text{ V} + 1.8 \text{ V}$ [Table 1.8]) = 2.5 V. Note the redrawn supply of 12 V and the polarity of V_o across the $680\text{-}\Omega$ resistor. The resulting voltage is

$$V_o = E - V_{K_1} - V_{K_2} = 12 \text{ V} - 2.5 \text{ V} = 9.5 \text{ V}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5 \text{ V}}{680 \Omega} = 13.97 \text{ mA}$$

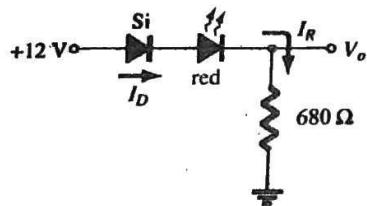


FIG. 2.19
Circuit for Example 2.7.

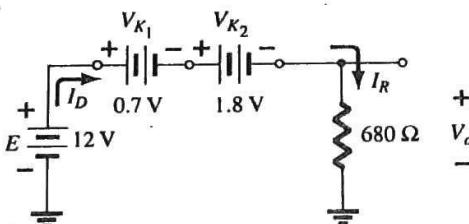


FIG. 2.20
Determining the unknown quantities for Example 2.7.

EXAMPLE 2.8 Determine I_D , V_{D_2} , and V_o for the circuit of Fig. 2.21.

Solution: Removing the diodes and determining the direction of the resulting current I result in the circuit of Fig. 2.22. There is a match in current direction for the silicon diode but not for the germanium diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = 0 \text{ A}$, as shown in Fig. 2.23.

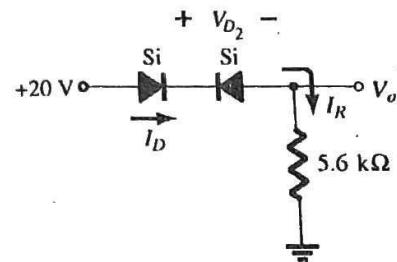


FIG. 2.21
Circuit for Example 2.8.

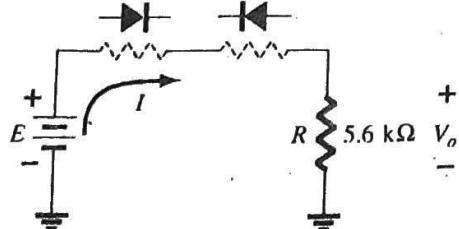


FIG. 2.22
Determining the state of the diodes of Fig. 2.21.

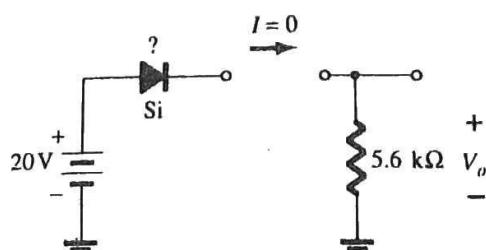


FIG. 2.23
Substituting the equivalent state for the open diode.

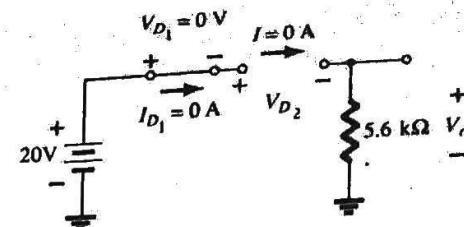


FIG. 2.24
Determining the unknown quantities for the circuit of Example 2.8.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0 \text{ A}$, $V_D = 0 \text{ V}$ (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0 \text{ A}$ and $V_{D_1} = 0 \text{ V}$ are indicated in Fig. 2.24. We have

$$V_o = I_R R = I_D R = (0 \text{ A})R = 0 \text{ V}$$

and

$$V_{D_2} = V_{\text{open circuit}} = E = 20 \text{ V}$$

Applying Kirchhoff's voltage law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and

$$\begin{aligned} V_{D_2} &= E - V_{D_1} - V_o = 20 \text{ V} - 0 - 0 \\ &= 20 \text{ V} \end{aligned}$$

with

$$V_o = 0 \text{ V}$$

EXAMPLE 2.9 Determine I , V_1 , V_2 , and V_o for the series dc configuration of Fig. 2.25.

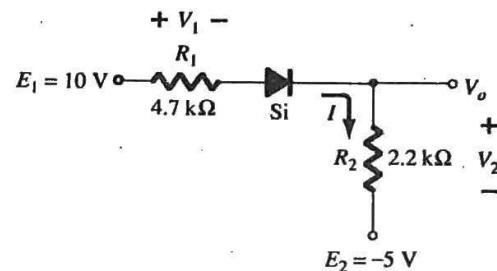


FIG. 2.25
Circuit for Example 2.9.

Solution: The sources are drawn and the current direction indicated as shown in Fig. 2.26. The diode is in the "on" state and the notation appearing in Fig. 2.27 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7 \text{ V}$ on the figure. This eliminates the need to redraw the network and avoids any confusion that may

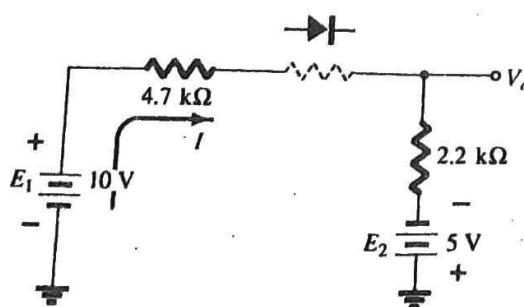


FIG. 2.26
Determining the state of the diode for the network of Fig. 2.25.

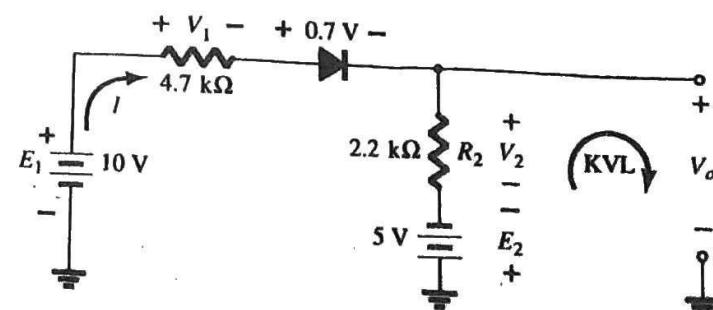


FIG. 2.27
Determining the unknown quantities for the network of Fig. 2.25. KVL, Kirchhoff voltage loop.

result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$

$$\approx 2.07\text{ mA}$$

and the voltages are

$$V_1 = IR_1 = (2.07\text{ mA})(4.7\text{ k}\Omega) = 9.73\text{ V}$$

$$V_2 = IR_2 = (2.07\text{ mA})(2.2\text{ k}\Omega) = 4.55\text{ V}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction results in

$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.55\text{ V} - 5\text{ V} = -0.45\text{ V}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.25.

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

The methods applied in Section 2.3 can be extended to the analysis of parallel and series-parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.10 Determine V_o , I_1 , I_{D_1} , and I_{D_2} for the parallel diode configuration of Fig. 2.28.

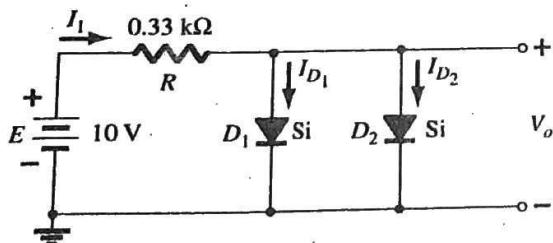


FIG. 2.28
Network for Example 2.10.

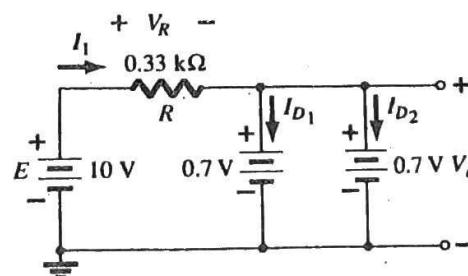


FIG. 2.29
Determining the unknown quantities for the network of Example 2.10.

Solution: For the applied voltage the "pressure" of the source acts to establish a current through each diode in the same direction as shown in Fig. 2.29. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = 0.7\text{ V}$$

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = 28.18\text{ mA}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = 14.09\text{ mA}$$

This example demonstrates one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.28 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.28. By placing two in parallel, we limit the current to a safe value of 14.09 mA with the same terminal voltage.

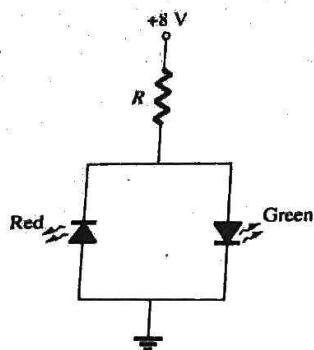


FIG. 2.30
Network for Example 2.11.

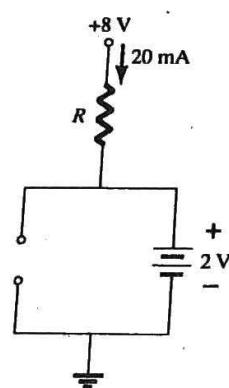


FIG. 2.31

Operating conditions for the network of Fig. 2.30.

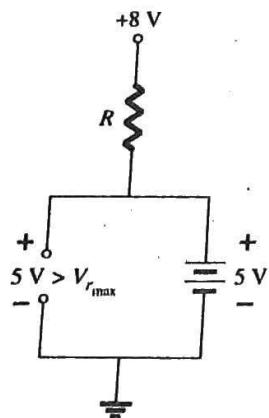


FIG. 2.32

Network of Fig. 2.31 with a blue diode.

EXAMPLE 2.11 In this example there are two LEDs that can be used as a polarity detector. Apply a positive source voltage and a green light results. Negative supplies result in a red light. Packages of such combinations are commercially available.

Find the resistor R to ensure a current of 20 mA through the "on" diode for the configuration of Fig. 2.30. Both diodes have a reverse breakdown voltage of 3 V and an average turn-on voltage of 2 V.

Solution: The application of a positive supply voltage results in a conventional current that matches the arrow of the green diode and turns it on.

The polarity of the voltage across the green diode is such that it reverse biases the red diode by the same amount. The result is the equivalent network of Fig. 2.31.

Applying Ohm's law, we obtain

$$I = 20 \text{ mA} = \frac{E - V_{\text{LED}}}{R} = \frac{8 \text{ V} - 2 \text{ V}}{R}$$

and

$$R = \frac{6 \text{ V}}{20 \text{ mA}} = 300 \Omega$$

Note that the reverse breakdown voltage across the red diode is 2 V, which is fine for an LED with a reverse breakdown voltage of 3 V.

However, if the green diode were to be replaced by a blue diode, problems would develop, as shown in Fig. 2.32. Recall that the forward bias required to turn on a blue diode is about 5 V. The result would appear to require a smaller resistor R to establish the current of 20 mA. However, note that the reverse bias voltage of the red LED is 5 V, but the reverse breakdown voltage of the diode is only 3 V. The result is the voltage across the red LED would lock in at 3 V as shown in Fig. 2.33. The voltage across R would be 5 V and the current limited to 20 mA with a 250Ω resistor but neither LED would be on.

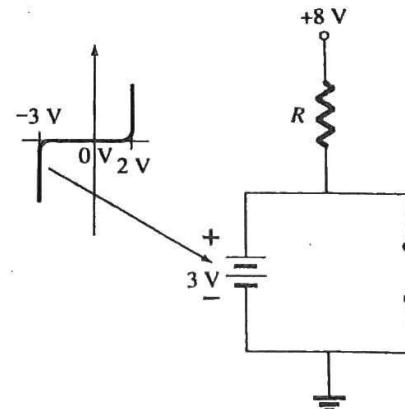
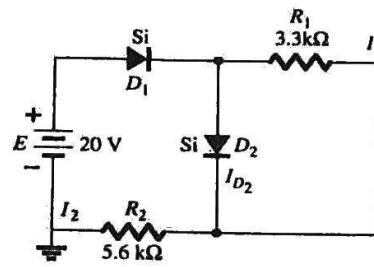


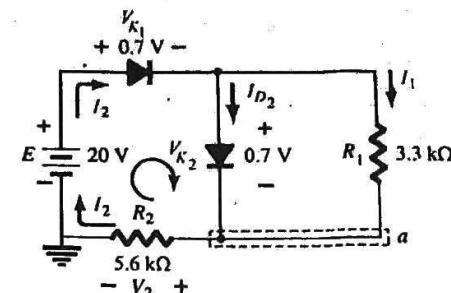
FIG. 2.33

Demonstrating damage to the red LED if the reverse breakdown voltage is exceeded.

A simple solution to the above is to simply add the appropriate resistance level in series with each diode to establish the desired 20 mA and to include another diode to add to the reverse-bias total reverse breakdown voltage rating, as shown in Fig. 2.34. When the blue LED is on, the diode in series with the blue LED will also be on, causing a total voltage drop of 5.7 V across the two series diodes and a voltage of 2.3 V across the resistor R_1 , establishing a high emission current of 19.17 mA. At the same time the red LED diode and

EXAMPLE 2.13 Determine the currents I_1 , I_2 , and I_{D_1} for the network of Fig. 2.37.**FIG. 2.37**

Network for Example 2.13.

**FIG. 2.38**

Determining the unknown quantities for Example 2.13.

Solution: The applied voltage (pressure) is such as to turn both diodes on, as indicated by the resulting current directions in the network of Fig. 2.38. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series-parallel networks. We have

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7 \text{ V}}{3.3 \text{ k}\Omega} = 0.212 \text{ mA}$$

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

and $V_2 = E - V_{K_1} - V_{K_2} = 20 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} = 18.6 \text{ V}$

with $I_2 = \frac{V_2}{R_2} = \frac{18.6 \text{ V}}{5.6 \text{ k}\Omega} = 3.32 \text{ mA}$

At the bottom node a ,

$$I_{D_1} + I_1 = I_2$$

and $I_{D_2} = I_2 - I_1 = 3.32 \text{ mA} - 0.212 \text{ mA} \approx 3.11 \text{ mA}$

2.5 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

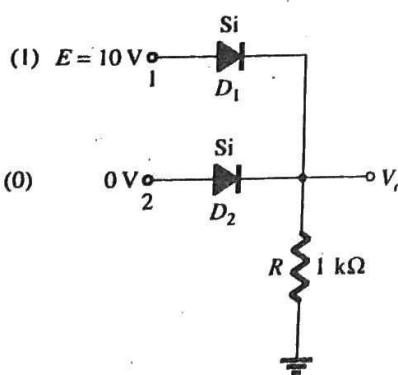
The network to be analyzed in Example 2.14 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.39 is assigned a "1" for Boolean algebra and the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either or both inputs are a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

EXAMPLE 2.14 Determine V_o for the network of Fig. 2.39.

Solution: First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of

**FIG. 2.39**

Positive logic OR gate.

level of $V_K = 0.7 \text{ V}$ and $v_o = v_i - V_K$, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where $V_m \gg V_K$, the following equation can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \approx 0.318(V_m - V_K) \quad (2.8)$$

In fact, if V_m is sufficiently greater than V_K , Eq. (2.7) is often applied as a first approximation for V_{dc} .

EXAMPLE 2.16

- Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
- Repeat part (a) if the ideal diode is replaced by a silicon diode.
- Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).

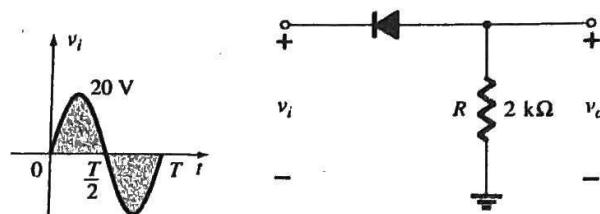


FIG. 2.49
Network for Example 2.16.

Solution:

- In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20 \text{ V}) = -6.36 \text{ V}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.49.

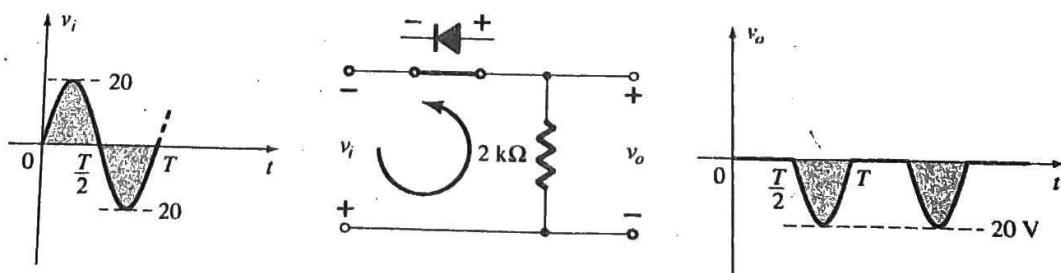


FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

- For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{dc} \approx -0.318(V_m - 0.7 \text{ V}) = -0.318(19.3 \text{ V}) \approx -6.14 \text{ V}$$

The resulting drop in dc level is 0.22 V, or about 3.5%.

- Eq. (2.7): $V_{dc} = -0.318 V_m = -0.318(200 \text{ V}) = -63.6 \text{ V}$
- Eq. (2.8): $V_{dc} = -0.318(V_m - V_K) = -0.318(200 \text{ V} - 0.7 \text{ V})$
 $= -(0.318)(199.3 \text{ V}) = -63.38 \text{ V}$

which is a difference that can certainly be ignored for most applications. For part (c) the offset and drop in amplitude due to V_K would not be discernible on a typical oscilloscope if the full pattern is displayed.

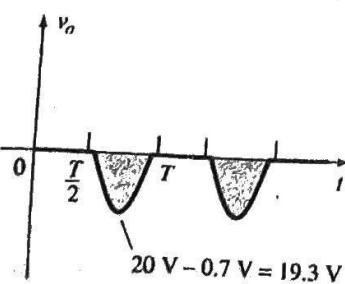


FIG. 2.51
Effect of V_K on output of Fig. 2.50.

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.52, which displays the reverse-biased diode of Fig. 2.44 with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geq V_m \quad \text{half-wave rectifier} \quad (2.9)$$

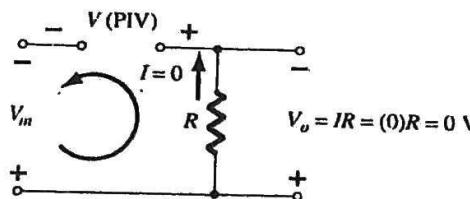


FIG. 2.52

Determining the required PIV rating for the half-wave rectifier.

2.7 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.53 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.54. The resulting polarities across the ideal diodes are also shown in Fig. 2.54 to reveal that D_2 and D_3 are conducting, whereas D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.55, with its indicated current and polarity across R . Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.

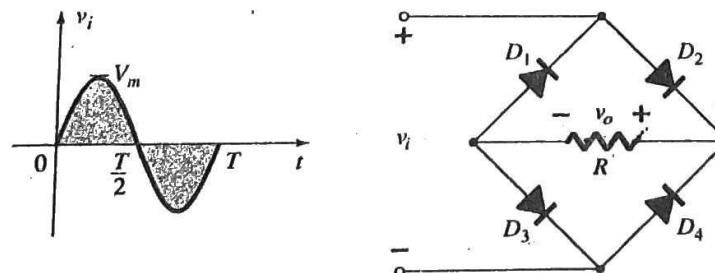


FIG. 2.53
Full-wave bridge rectifier.

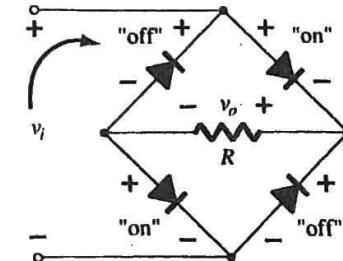


FIG. 2.54
Network of Fig. 2.53 for the period $0 \rightarrow T/2$ of the input voltage v_i .

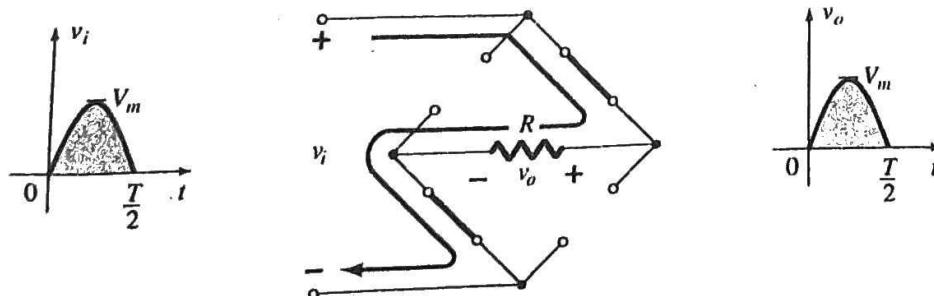


FIG. 2.55
Conduction path for the positive region of v_i .

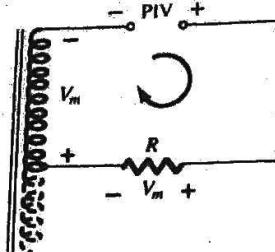


FIG. 2.63

Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

PIV The network of Fig. 2.63 will help us determine the net PIV for each diod full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as establishe by the adjoining loop results in

$$\begin{aligned} \text{PIV} &= V_{\text{secondary}} + V_R \\ &= V_m + V_m \end{aligned}$$

(2.13)

and

$$\text{PIV} \cong 2V_m \quad \text{CT transformer, full-wave rectifier}$$

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

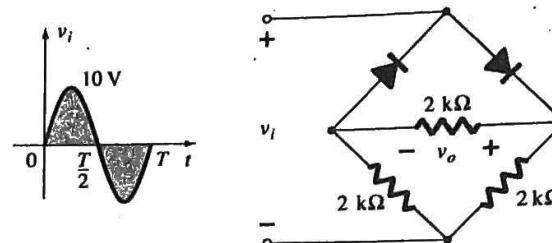


FIG. 2.64

Bridge network for Example 2.17.

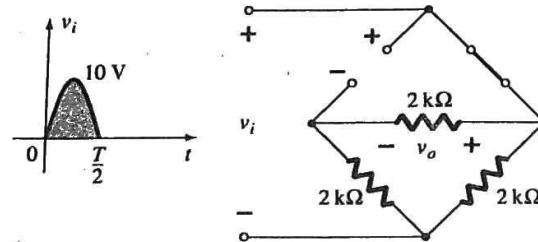


FIG. 2.65

Network of Fig. 2.64 for the positive region of v_i .

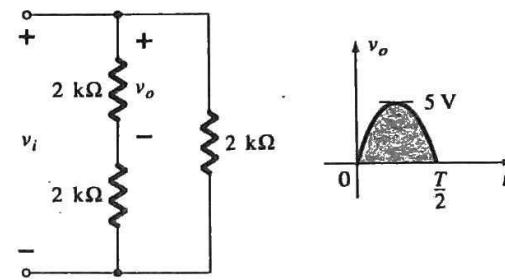


FIG. 2.66

Redrawn network of Fig. 2.65.

Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10 \text{ V}) = 5 \text{ V}$, as shown in Fig. 2.66. For the negative part of the input the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{dc} = 0.636(5 \text{ V}) = 3.18 \text{ V}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across R , which is 5 V, or half of that required for a half-wave rectifier with the same input.

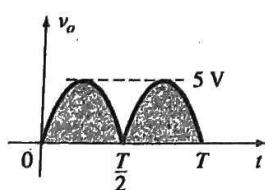


FIG. 2.67

Resulting output for Example 2.17.

2.8 CLIPPERS

The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clamps will expand on the wave-shaping abilities of diodes.

Clippers are networks that employ diodes to “clip” away a portion of an input signal without distorting the remaining part of the applied waveform.

results, placing the diode in the "off" state, and $v_o = i_R R = (0)V = 0\text{ V}$. The resulting output voltage appears in Fig. 2.80.

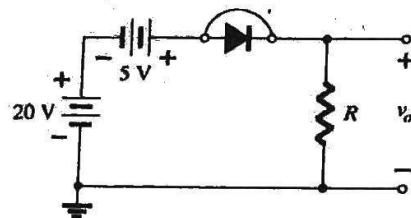


FIG. 2.78
 v_o at $v_i = +20\text{ V}$.

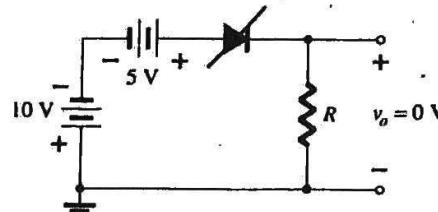


FIG. 2.79
 v_o at $v_i = -10\text{ V}$.

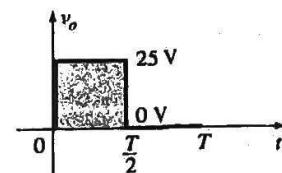


FIG. 2.80
Sketching v_o for Example 2.19.

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

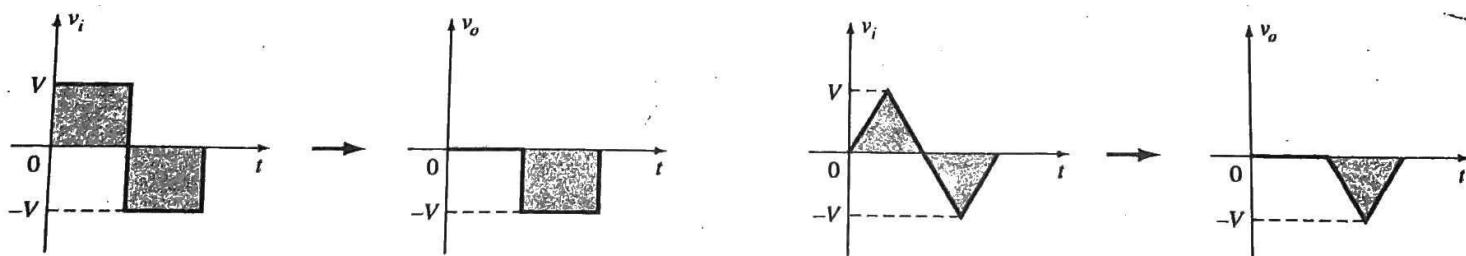
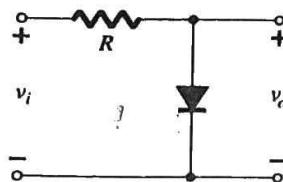


FIG. 2.81
Response to a parallel clipper.

EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor R .

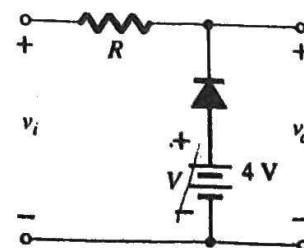
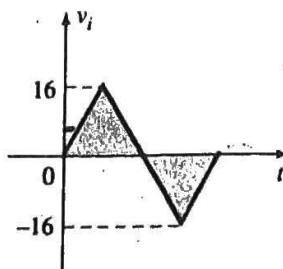


FIG. 2.82
Example 2.20.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

Step 3: The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4 \text{ V}$$

Step 4: In Fig. 2.84 the transition level is drawn along with $v_o = 4 \text{ V}$ when the diode is on. For $v_i \geq 4 \text{ V}$, $v_o = 4 \text{ V}$, and the waveform is simply repeated on the output plot.

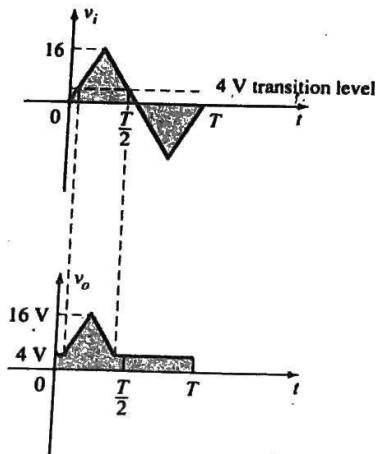


FIG. 2.84
Sketching v_o for Example 2.20.

To examine the effects of the knee voltage V_K of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

EXAMPLE 2.21 Repeat Example 2.20 using a silicon diode with $V_K = 0.7 \text{ V}$.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0 \text{ A}$ at $v_d = V_D = 0.7 \text{ V}$ and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and

$$v_i = V - V_K = 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.86 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

There is no question that including the effects of V_K will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_K , will not be that difficult.

DIODE APPLICATIONS

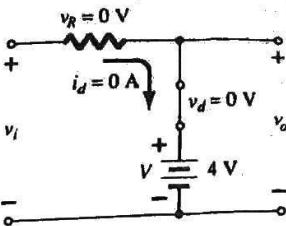


FIG. 2.83
Determining the transition level for Example 2.20.

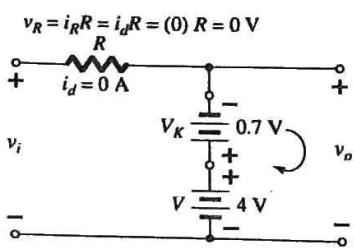


FIG. 2.85
Determining the transition level for the network of Fig. 2.82.

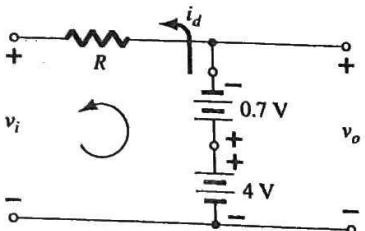


FIG. 2.86
Determining v_o for the diode of Fig. 2.82 in the "on" state.

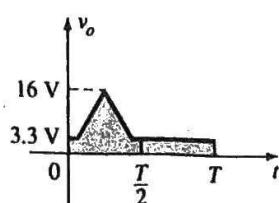
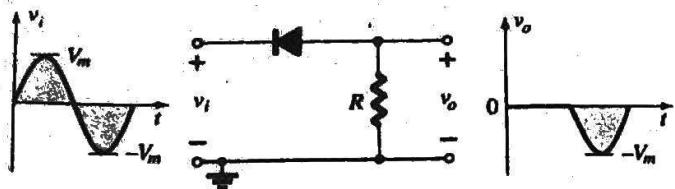


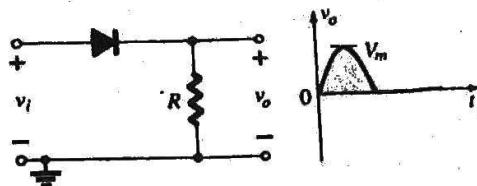
FIG. 2.87
Sketching v_o for Example 2.21.

Simple Series Clippers (Ideal Diodes)

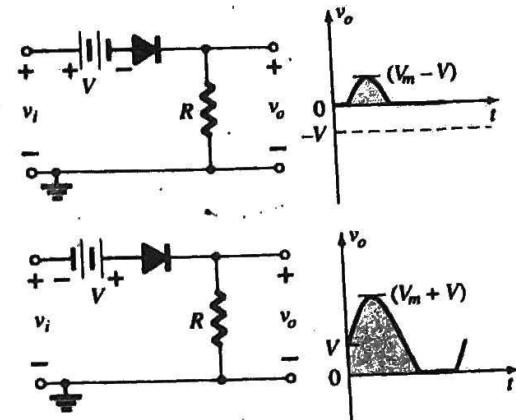
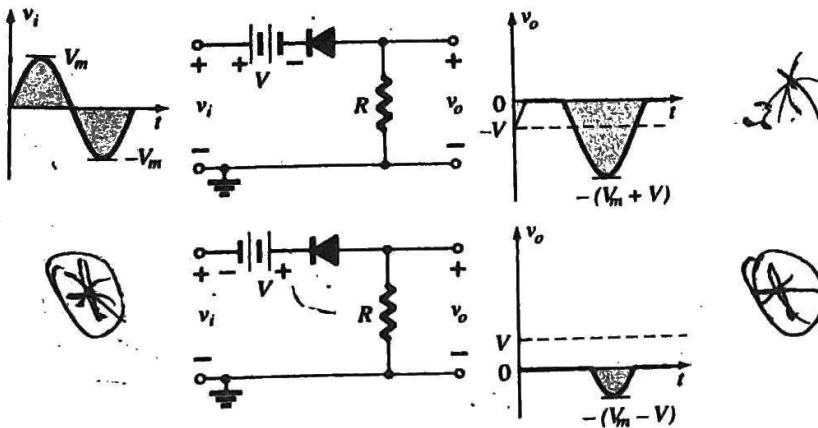
POSITIVE



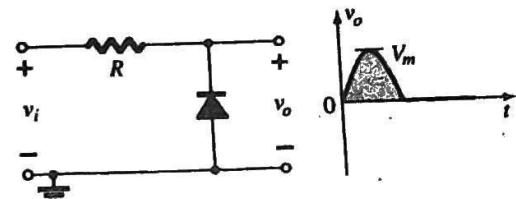
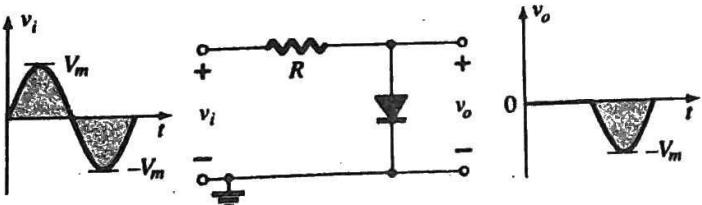
NEGATIVE



Biased Series Clippers (Ideal Diodes)



Simple Parallel Clippers (Ideal Diodes)



Biased Parallel Clippers (Ideal Diodes)

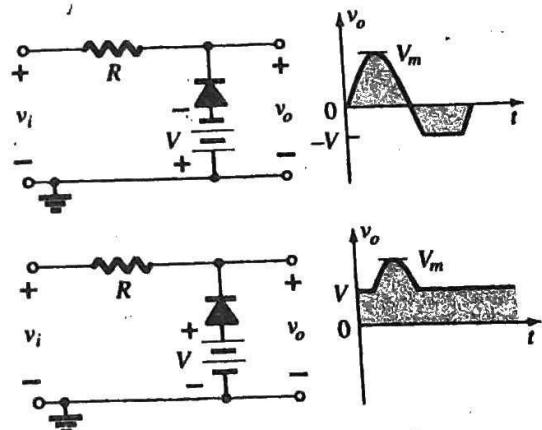
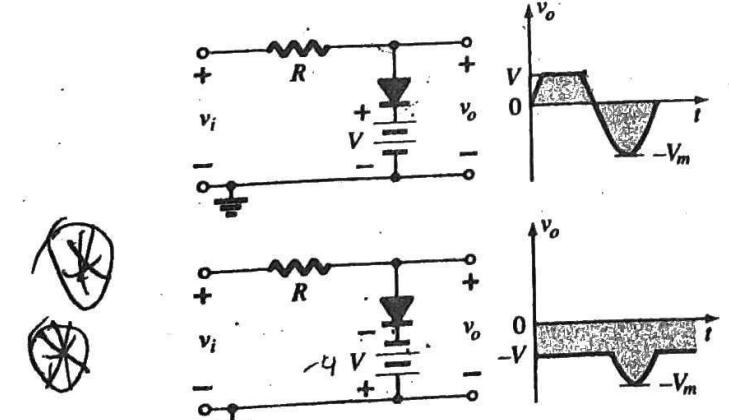


FIG. 2.88
Clipping circuits.

ELECTRONIC DEVICES AND CIRCUIT THEORY

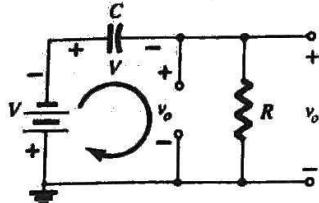


FIG. 2.91

Determining v_o with the diode "off."

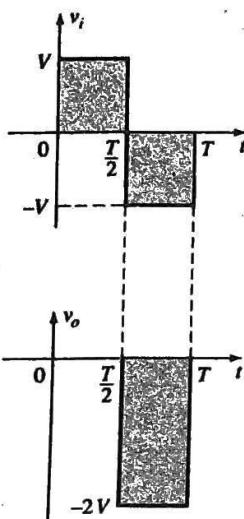


FIG. 2.92

Sketching v_o for the network of Fig. 2.91.

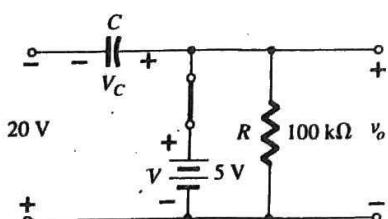


FIG. 2.94

Determining v_o and V_C with the diode in the "on" state.

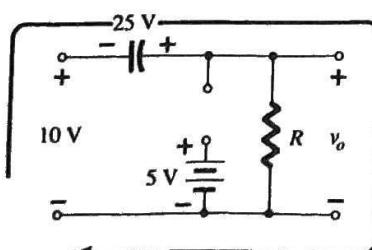


FIG. 2.95

Determining v_o with the diode in the "off" state.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ , much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign results from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o . The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

Step 5: Check that the total swing of the output matches that of the input.

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.

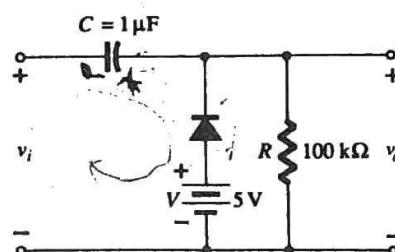
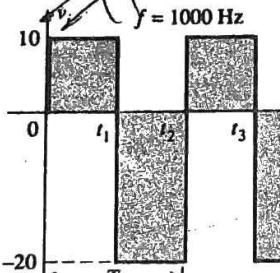


FIG. 2.93

Applied signal and network for Example 2.22.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across R , but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop results in

$$-20V + V_C - 5V = 0$$

and

$$V_C = 25V$$

The capacitor will therefore charge up to 25 V. In this case the resistor R is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0 \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.95.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on v_o , and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10V + 25V - v_o = 0$$

and

$$v_o = 35V$$

The time constant of the discharging network of Fig. 2.95 is determined by the product RC and has the magnitude

$$\tau = RC = (100 \text{ k}\Omega)(0.1 \mu\text{F}) = 0.01 \text{ s} = 10 \text{ ms}$$

The total discharge time is therefore $5\tau = 5(10 \text{ ms}) = 50 \text{ ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

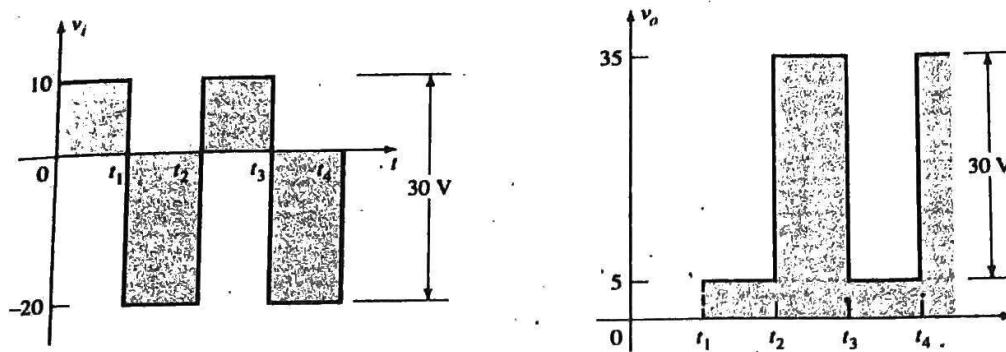


FIG. 2.96
 v_i and v_o for the clamper of Fig. 2.93.

EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7 \text{ V}$.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5 \text{ V} - 0.7 \text{ V} - v_o = 0$$

and

$$v_o = 5 \text{ V} - 0.7 \text{ V} = 4.3 \text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20 \text{ V} + V_C + 0.7 \text{ V} - 5 \text{ V} = 0$$

and

$$V_C = 25 \text{ V} - 0.7 \text{ V} = 24.3 \text{ V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10 \text{ V} + 24.3 \text{ V} - v_o = 0$$

and

$$v_o = 34.3 \text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

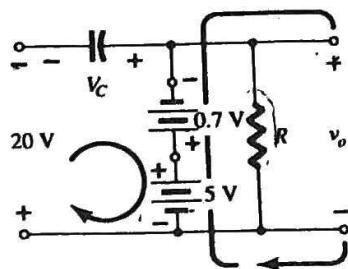
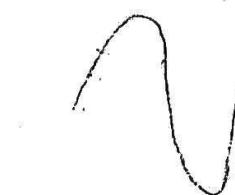


FIG. 2.97
Determining v_o and V_C with the diode in the "on" state.

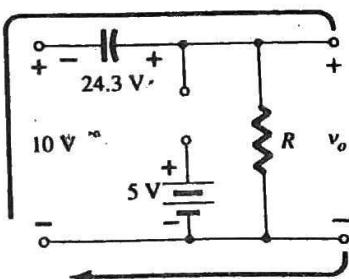


FIG. 2.98
Determining v_o with the diode in the open state.

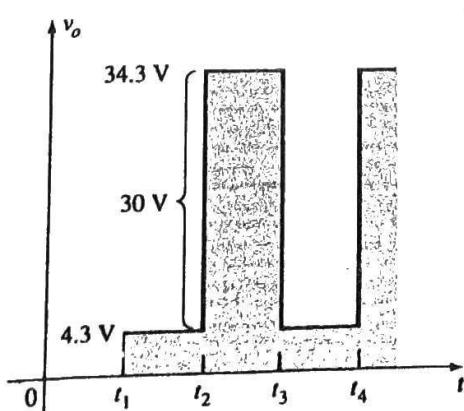


FIG. 2.99
Sketching v_o for the clamper of Fig. 2.93 with a silicon diode.

Clamping Networks

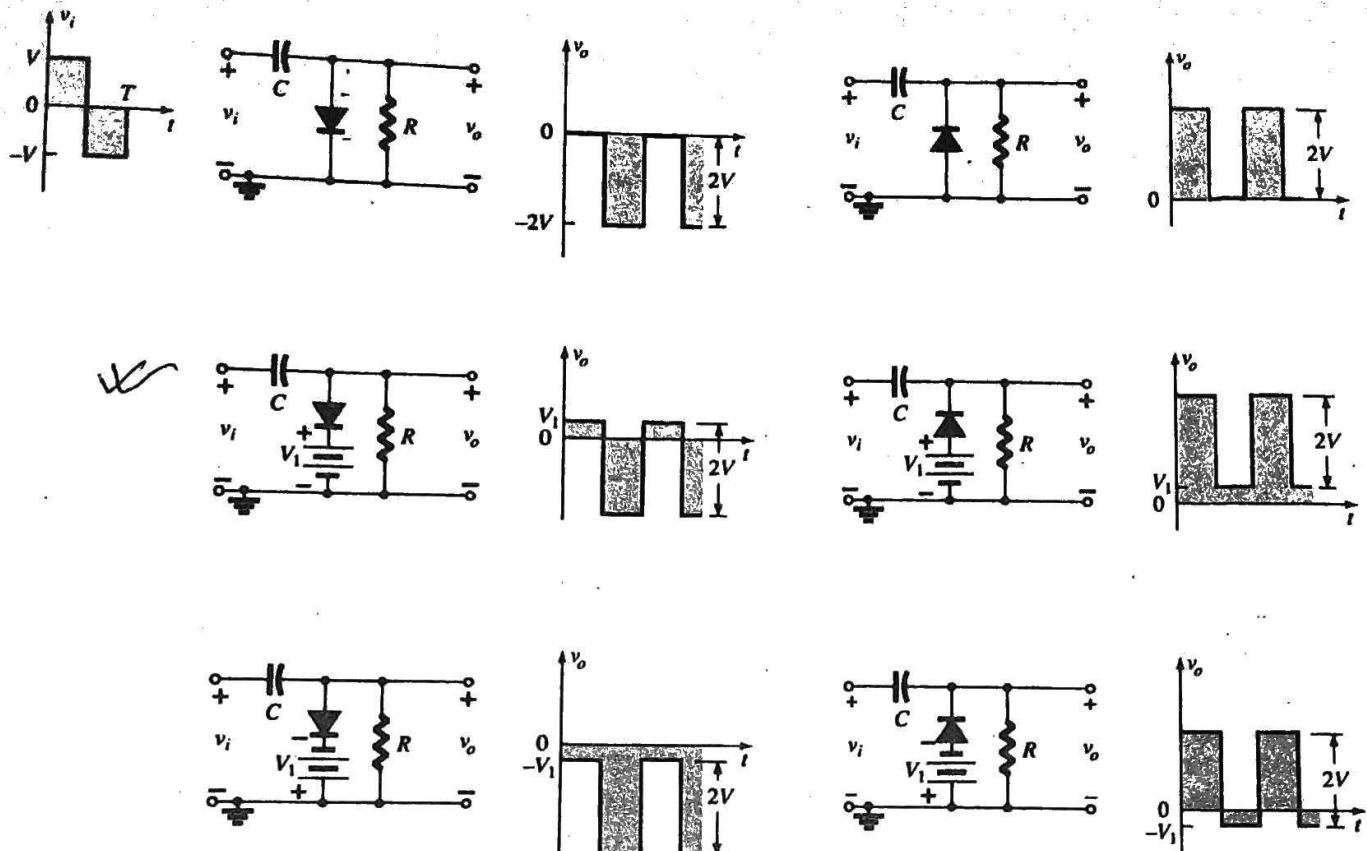


FIG. 2.100
Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

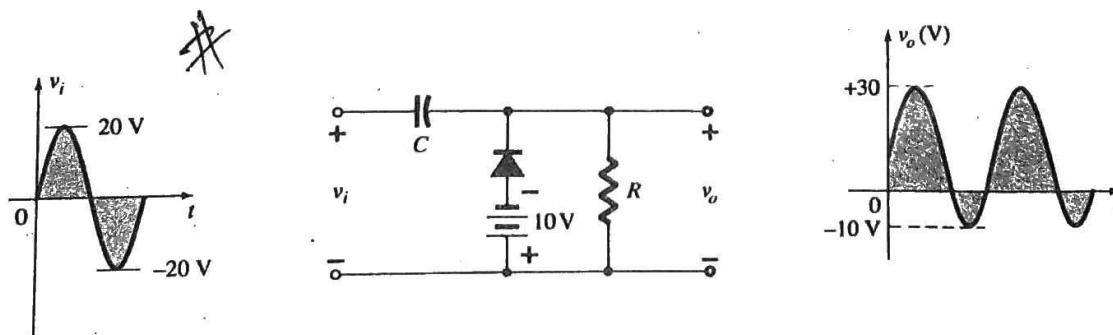


FIG. 2.101
Clamping network with a sinusoidal input.

2.10 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Figure 2.102 reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point. Note that the forward-bias region is included because occasionally an application will skip into this region also.

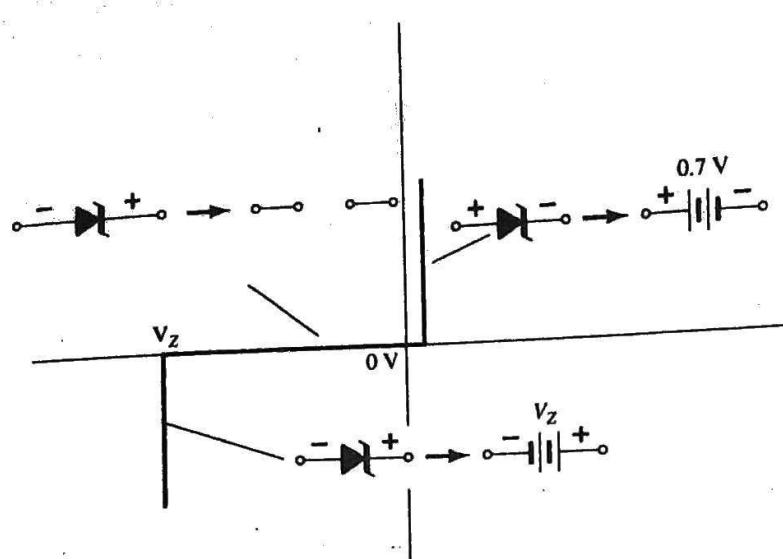


FIG. 2.102

Approximate equivalent circuits for the Zener diode in the three possible regions of application.

The first two examples will demonstrate how a Zener diode can be used to establish reference voltage levels and act as a protection device. The use of a Zener diode as a *regulator* will then be described in detail because it is one of its major areas of application. A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

EXAMPLE 2.24 Determine the reference voltages provided by the network of Fig. 2.103, which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The white LED will have a drop of about 4 V across it, the 6-V and 3.3-V Zener diodes have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V, for a total of 14 V. The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current.

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o_1} = V_{Z_1} + V_K = 3.3 \text{ V} + 0.7 \text{ V} = 4.0 \text{ V}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o_2} = V_{o_1} + V_{Z_1} = 4 \text{ V} + 6 \text{ V} = 10 \text{ V}$$

Finally, the 4 V across the white LED will leave a voltage of $40 \text{ V} - 14 \text{ V} = 26 \text{ V}$ across the resistor, and

$$I_R = I_{LED} = \frac{V_R}{R} = \frac{40 \text{ V} - V_{o_2} - V_{LED}}{1.3 \text{ k}\Omega} = \frac{40 \text{ V} - 10 \text{ V} - 4 \text{ V}}{1.3 \text{ k}\Omega} = \frac{26 \text{ V}}{1.3 \text{ k}\Omega} = 20 \text{ mA}$$

that will establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40 \text{ V})(20 \text{ mA}) = 800 \text{ mW}$$

The power absorbed by the LED is

$$P_{LED} = V_{LED} I_{LED} = (4 \text{ V})(20 \text{ mA}) = 80 \text{ mW}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_Z I_Z = (6 \text{ V})(20 \text{ mA}) = 120 \text{ mW}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

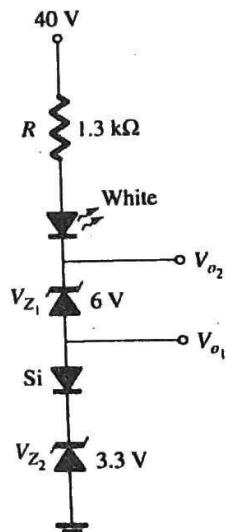


FIG. 2.103
Reference setting circuit for
Example 2.24.

EXAMPLE 2.25 The network of Fig. 2.104 is designed to limit the voltage to 20 V during the positive portion of the applied voltage and to 0 V for a negative excursion of the applied voltage. Check its operation and plot the waveform of the voltage across the system for the applied signal. Assume the system has a very high input resistance so it will not affect the behavior of the network.

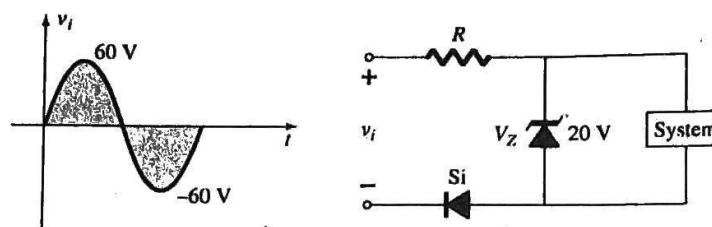


FIG. 2.104
Controlling network for Example 2.25.

Solution: For positive applied voltages less than the Zener potential of 20 V the Zener diode will be in its approximate open-circuit state, and the input signal will simply distribute itself across the elements, with the majority going to the system because it has such a high resistance level.

Once the voltage across the Zener diode reaches 20 V the Zener diode will turn on as shown in Fig. 2.105a and the voltage across the system will lock in at 20 V. Further increases in the applied voltage will simply appear across the series resistor with the voltage across the system and the forward-biased diode remaining fixed at 20 V and 0.7 V, respectively. The voltage across the system is fixed at 20 V, as shown in Fig. 2.105a, because the 0.7 V of the diode is not between the defined output terminals. The system is therefore safe from any further increases in applied voltage.

For the negative region of the applied signal the silicon diode is reverse biased and presents an open circuit to the series combination of elements. The result is that the full

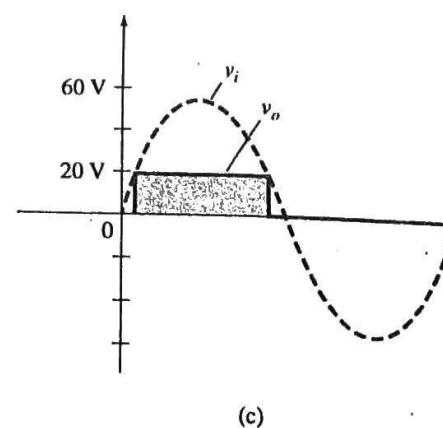
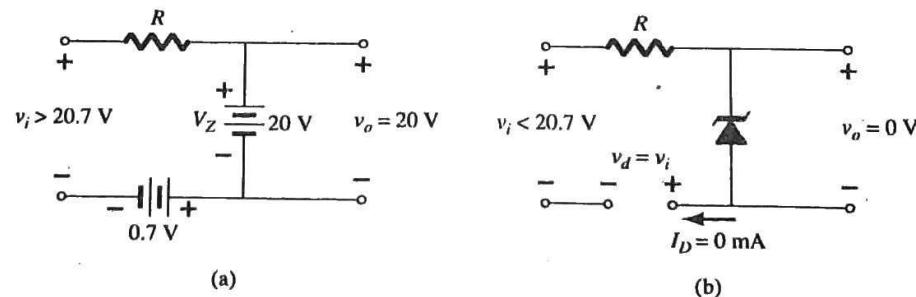


FIG. 2.105
Response of the network of Fig. 2.104 to the application of a 60-V sinusoidal signal.

negatively applied signal will appear across the open-circuited diode and the negative voltage across the system locked in at 0 V, as shown in Fig. 2.104b.
The voltage across the system will therefore appear as shown in Fig. 2.105c.

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 2.106. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

V_i and R Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.

Applying step 1 to the network of Fig. 2.106 results in the network of Fig. 2.107, where an application of the voltage divider rule results in

$$V = V_L = \frac{R_L V_i}{R + R_L} \quad (2.16)$$

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.

If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \quad (2.17)$$

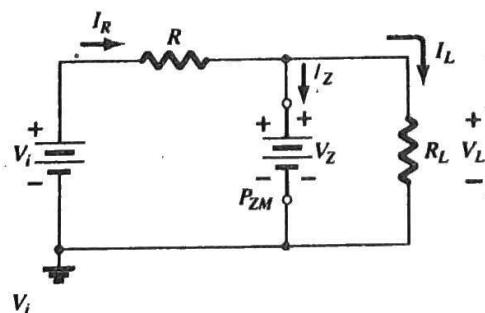


FIG. 2.108
Substituting the Zener equivalent for the
"on" situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \quad (2.18)$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

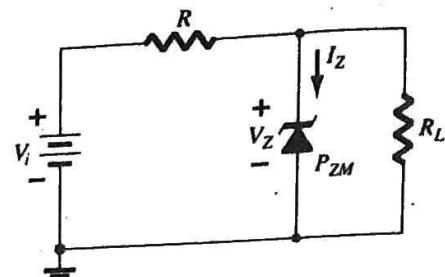


FIG. 2.106
Basic Zener regulator.

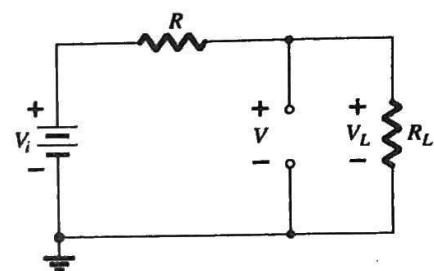


FIG. 2.107
Determining the state of the
Zener diode.

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \quad (2.19)$$

that must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the state of the Zener diode. If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn on as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

EXAMPLE 2.26

- For the Zener diode network of Fig. 2.109, determine V_L , V_R , I_Z , and P_Z .
- Repeat part (a) with $R_L = 3 \text{ k}\Omega$.

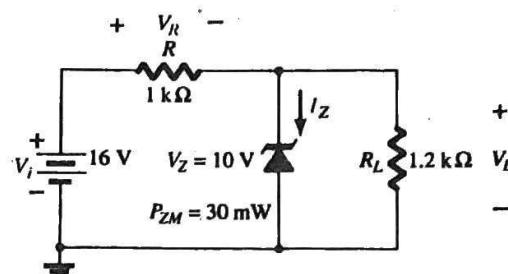


FIG. 2.109
Zener diode regulator for Example 2.26.

Solution:

- Following the suggested procedure, we redraw the network as shown in Fig. 2.110.

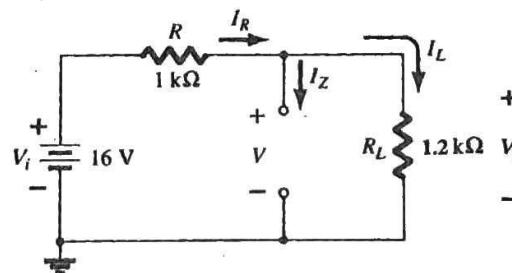


FIG. 2.110
Determining V for the regulator of Fig. 2.109.

Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2 \text{ k}\Omega (16 \text{ V})}{1 \text{ k}\Omega + 1.2 \text{ k}\Omega} = 8.73 \text{ V}$$

Since $V = 8.73 \text{ V}$ is less than $V_Z = 10 \text{ V}$, the diode is in the "off" state, as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent results in the same network as in Fig. 2.110, where we find that

$$V_L = V = 8.73 \text{ V}$$

$$V_R = V_i - V_L = 16 \text{ V} - 8.73 \text{ V} = 7.27 \text{ V}$$

$$I_Z = 0 \text{ A}$$

$$\text{and } P_Z = V_Z I_Z = V_Z (0 \text{ A}) = 0 \text{ W}$$

- Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3 \text{ k}\Omega (16 \text{ V})}{1 \text{ k}\Omega + 3 \text{ k}\Omega} = 12 \text{ V}$$

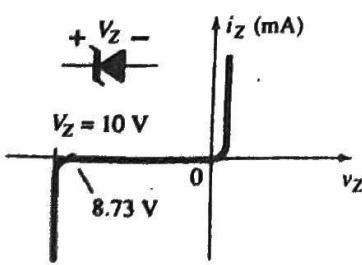


FIG. 2.111

Resulting operating point for the network of Fig. 2.109.

Once the diode is in the "on" state, the voltage across R remains fixed at

$$-V_R = V_i - V_Z$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R}$$

(2.23)

The Zener current

$$I_Z = I_R - I_L$$

(2.24)

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L . Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM}$$

(2.25)

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}}$$

(2.26)

EXAMPLE 2.27

- a. For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V.
 b. Determine the maximum wattage rating of the diode.

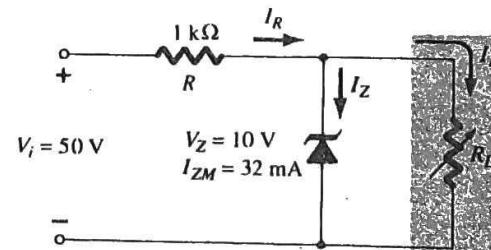


FIG. 2.113
Voltage regulator for Example 2.27.

Solution:

- a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1 \text{ k}\Omega)(10 \text{ V})}{50 \text{ V} - 10 \text{ V}} = \frac{10 \text{ k}\Omega}{40} = 250 \text{ }\Omega$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50 \text{ V} - 10 \text{ V} = 40 \text{ V}$$

and Eq. (2.23) provides the magnitude of I_R :

$$I_R = \frac{V_R}{R} = \frac{40 \text{ V}}{1 \text{ k}\Omega} = 40 \text{ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40 \text{ mA} - 32 \text{ mA} = 8 \text{ mA}$$

with Eq. (2.26) determining the maximum value of R_L :

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10 \text{ V}}{8 \text{ mA}} = 1.25 \text{ k}\Omega$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

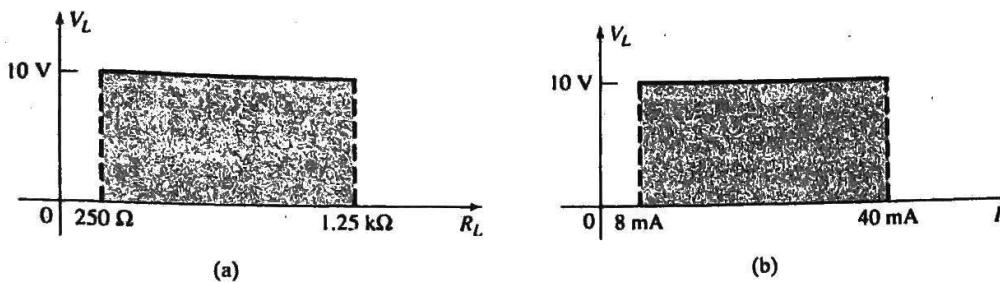


FIG. 2.114

V_L versus R_L and I_L for the regulator of Fig. 2.113.

$$\begin{aligned} \text{b. } P_{\max} &= V_Z I_{ZM} \\ &= (10 \text{ V})(32 \text{ mA}) = 320 \text{ mW} \end{aligned}$$

Circuit
character
operation
bjt
superposition

✓ Fixed R_L , Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{\min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R} \quad (2.27)$$

and

$$V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM} . Since $I_{ZM} = I_R - I_L$,

$$I_{R_{\max}} = I_{ZM} + I_L \quad (2.28)$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z , the maximum V_i is defined by

$$V_{i_{\max}} = V_{R_{\max}} + V_Z$$

$$V_{i_{\max}} = I_{R_{\max}} R + V_Z \quad (2.29)$$

EXAMPLE 2.28 Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

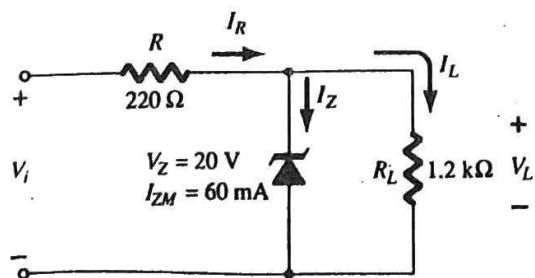


FIG. 2.115
Regulator for Example 2.28.

Collector-Emitter Loop

The collector-emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C . The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B \quad (4.5)$$

It is interesting to note that because the base current is controlled by the level of R_B and I_C is related to I_B by a constant β , the magnitude of I_C is not a function of the resistance R_C . Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE} , which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C R_C \quad (4.6)$$

which states that the voltage across the collector-emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C .

As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E \quad (4.7)$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. In this case, since $V_E = 0$ V, we have

$$V_{CE} = V_C \quad (4.8)$$

In addition, because

$$V_{BE} = V_B - V_E \quad (4.9)$$

and $V_E = 0$ V, then

$$V_{BE} = V_B \quad (4.10)$$

Keep in mind that voltage levels such as V_{CE} are determined by placing the red (positive) lead of the voltmeter at the collector terminal with the black (negative) lead at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

- I_{BQ} and I_{CQ}
- V_{CEQ}
- V_B and V_C
- V_{BC}

Solution:

a. Eq. (4.4): $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$

Eq. (4.5): $I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$

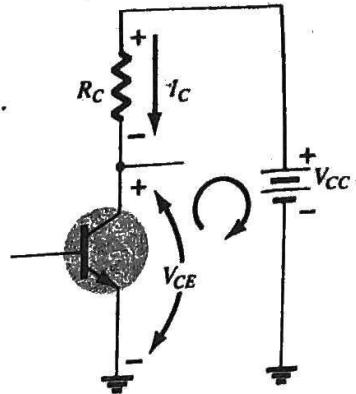


FIG. 4.5
Collector-emitter loop.

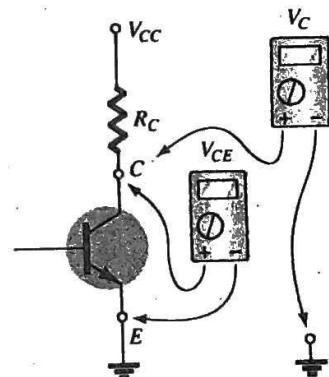


FIG. 4.6
Measuring V_{CE} and V_C .

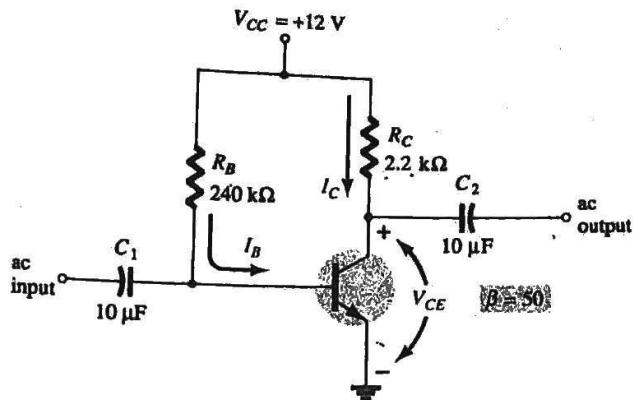


FIG. 4.7
DC fixed-bias circuit for Example 4.1.

b. Eq. (4.6): $V_{CEq} = V_{CC} - I_C R_C$
 $= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega)$
 $= 6.83 \text{ V}$

c. $V_B = V_{BE} = 0.7 \text{ V}$
 $V_C = V_{CE} = 6.83 \text{ V}$

d. Using double-subscript notation yields

$$\boxed{V_{BC}} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} \\ = -6.13 \text{ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region, the current is a maximum value *for the particular design*. Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE\text{sat}}$. In addition, the collector current is relatively high on the characteristics.

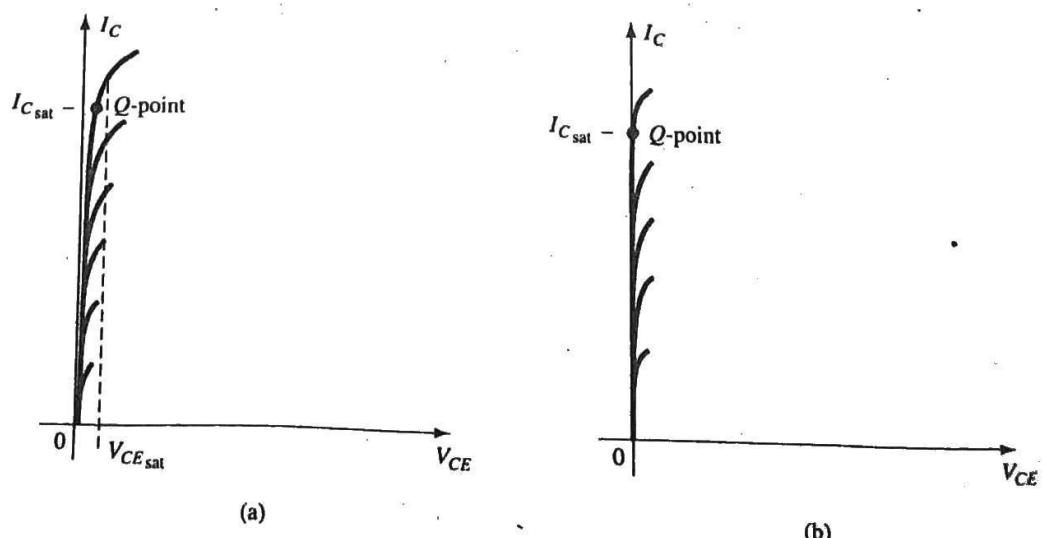


FIG. 4.8
Saturation regions: (a) actual; (b) approximate.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high, and the voltage V_{CE} is assumed to be 0 V. Applying Ohm's law, we can determine the resistance between collector and emitter terminals as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0 \text{ V}}{I_{C_{\text{sat}}}} = 0 \Omega$$

Applying the results to the network schematic results in the configuration of Fig. 4.9. For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0 \text{ V}$. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC} . The resulting saturation current for the fixed-bias configuration is

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} \quad (4.11)$$

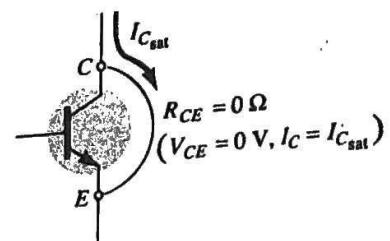


FIG. 4.9
Determining $I_{C_{\text{sat}}}$

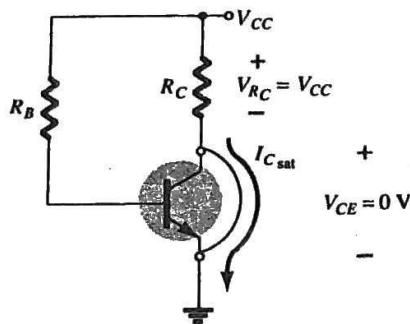


FIG. 4.10
Determining $I_{C_{\text{sat}}}$ for the fixed-bias configuration.

Once $I_{C_{\text{sat}}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2 Determine the saturation level for the network of Fig. 4.7.

Solution:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} = \frac{12 \text{ V}}{2.2 \text{ k}\Omega} = 5.45 \text{ mA}$$

The design of Example 4.1 resulted in $I_{CQ} = 2.35 \text{ mA}$, which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

Recall that the load-line solution for a diode network was found by superimposing the actual diode characteristics of the diode on a plot of the network equation involving the same network variables. The intersection of the two plots defined the actual operating conditions for the network. It is referred to as load-line analysis because the load (network resistors) of the network defined the slope of the straight line connecting the points defined by the network parameters.

The same approach can be applied to BJT networks. The characteristics of the BJT are superimposed on a plot of the network equation defined by the same axis parameters. The load resistor R_C for the fixed-bias configuration will define the slope of the network equation and the resulting intersection between the two plots. The smaller the load resistance, the steeper

Equation (4.18) will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base-emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

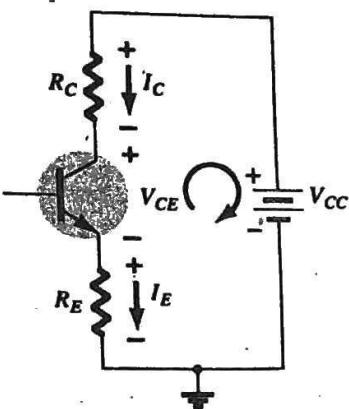


FIG. 4.22
Collector-emitter loop.

Collector-Emitter Loop

The collector-emitter loop is redrawn in Fig. 4.22. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \approx I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0 \quad (4.19)$$

and

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \quad (4.20)$$

whereas the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \quad (4.21)$$

or

$$V_C = V_{CC} - I_C R_C \quad (4.22)$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_B \quad (4.23)$$

or

$$V_B = V_{RE} + V_E \quad (4.24)$$

EXAMPLE 4.4 For the emitter-bias network of Fig. 4.23, determine:

- a. I_B .
- b. I_C .
- c. V_{CE} .
- d. V_C .
- e. V_E .
- f. V_B .
- g. V_{BC} .

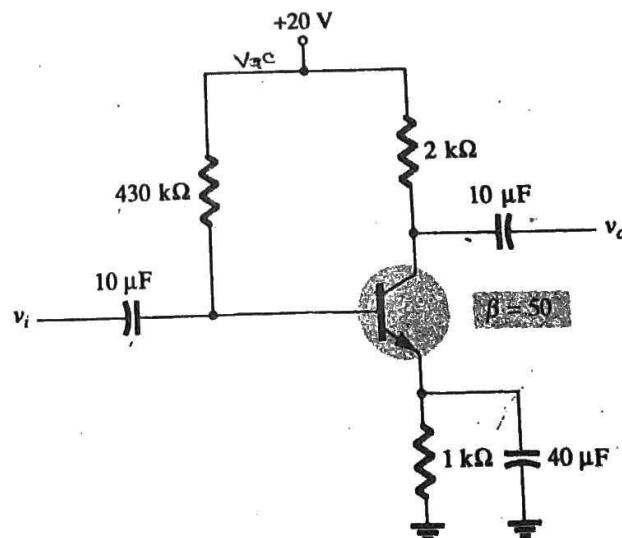


FIG. 4.23
Emitter-stabilized bias circuit for Example 4.4.

Solution:

$$\text{a. Eq. (4.17): } I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)} \\ = \frac{19.3\text{ V}}{481\text{ k}\Omega} = 40.1\text{ }\mu\text{A}$$

$$\text{b. } I_C = \beta I_B \\ = (50)(40.1\text{ }\mu\text{A}) \\ \cong 2.01\text{ mA}$$

$$\text{c. Eq. (4.19): } V_{CE} = V_{CC} - I_C(R_C + R_E) \\ = 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V} \\ = 13.97\text{ V}$$

$$\text{d. } V_C = V_{CC} - I_C R_C \\ = 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V} \\ = 15.98\text{ V}$$

$$\text{e. } V_E = V_C - V_{CE} \\ = 15.98\text{ V} - 13.97\text{ V} \\ = 2.01\text{ V}$$

~~V_E = I_ER_E ≈ I_CR_E~~

$$\text{or } V_E = I_E R_E \\ = (2.01\text{ mA})(1\text{ k}\Omega) \\ = 2.01\text{ V}$$

$$\text{f. } V_B = V_{BE} + V_E \\ = 0.7\text{ V} + 2.01\text{ V} \\ = 2.71\text{ V}$$

$$\text{g. } V_{BC} = V_B - V_C \\ = 2.71\text{ V} - 15.98\text{ V} \\ = -13.27\text{ V} \text{ (reverse-biased as required)}$$

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change. Although a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

EXAMPLE 4.5 Prepare a table and compare the bias voltage and currents of the circuits of Fig. 4.7 and Fig. 4.23 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β .

Solution: Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β . The value of I_B is the same, and V_{CE} decreased by 76%.