



University of Asia Pacific

Admit Card

Final-Term Examination of Fall, 2020

Financial Clearance	PAID
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Registration No : 17101086

Student Name : Md. Remon Hasan Apu

Program : Bachelor of Science in Computer Science and Engineering

SI.NO.	COURSE CODE	COURSE TITLE	CR.HR.	EXAM. SCHEDULE
1	CSE 425	Computer Graphics	3.00	
2	CSE 426	Computer Graphics Lab	1.50	
3	CSE 429	Compiler Design	3.00	
4	CSE 430	Compiler Design Lab	1.50	
5	BUS 401	Business and Entrepreneurship	3.00	
6	BUS 402	Business and Entrepreneurship Lab	0.75	
7	CSE 457	Design and Testing of VLSI	3.00	
8	CSE 458	Design and Testing of VLSI Lab	0.75	
9	CSE 400	Project / Thesis	3.00	

Total Credit: 19.50

1. Examinees are not allowed to enter the examination hall after 30 minutes of commencement of examination for mid semester examinations and 60 minutes for semester final examinations.
2. No examinees shall be allowed to submit their answer scripts before 50% of the allocated time of examination has elapsed.
3. No examinees would be allowed to go to washroom within the first 60 minutes of final examinations.
4. No student will be allowed to carry any books, bags, extra paper or cellular phone or objectionable items/incriminating paper in the examination hall.
Violators will be subjects to disciplinary action.

This is a system generated Admit Card. No signature is required.



University of Asia Pacific

Department of Computer Science and Engineering

SEMESTER FINAL EXAM-FALL 2020

Course Name : Design & Testing of VLSI

Course Code : CSE-457

Semester: 4th Year 2nd Semester

SUBMITTED By

Md. Remon Hasan Apu

ID: 17101086, Section: B

Date: 04.05.2021

Ans: to the Q: no - 02

a)

number of inputs = n

no of select switch = m

so,

$$m = \log_2 n$$

$$\text{so, } m = \log_2 4 = \log_2 2^2 = 2 \log_2 2 = 2 \cdot 1 = 2$$

Truth table:

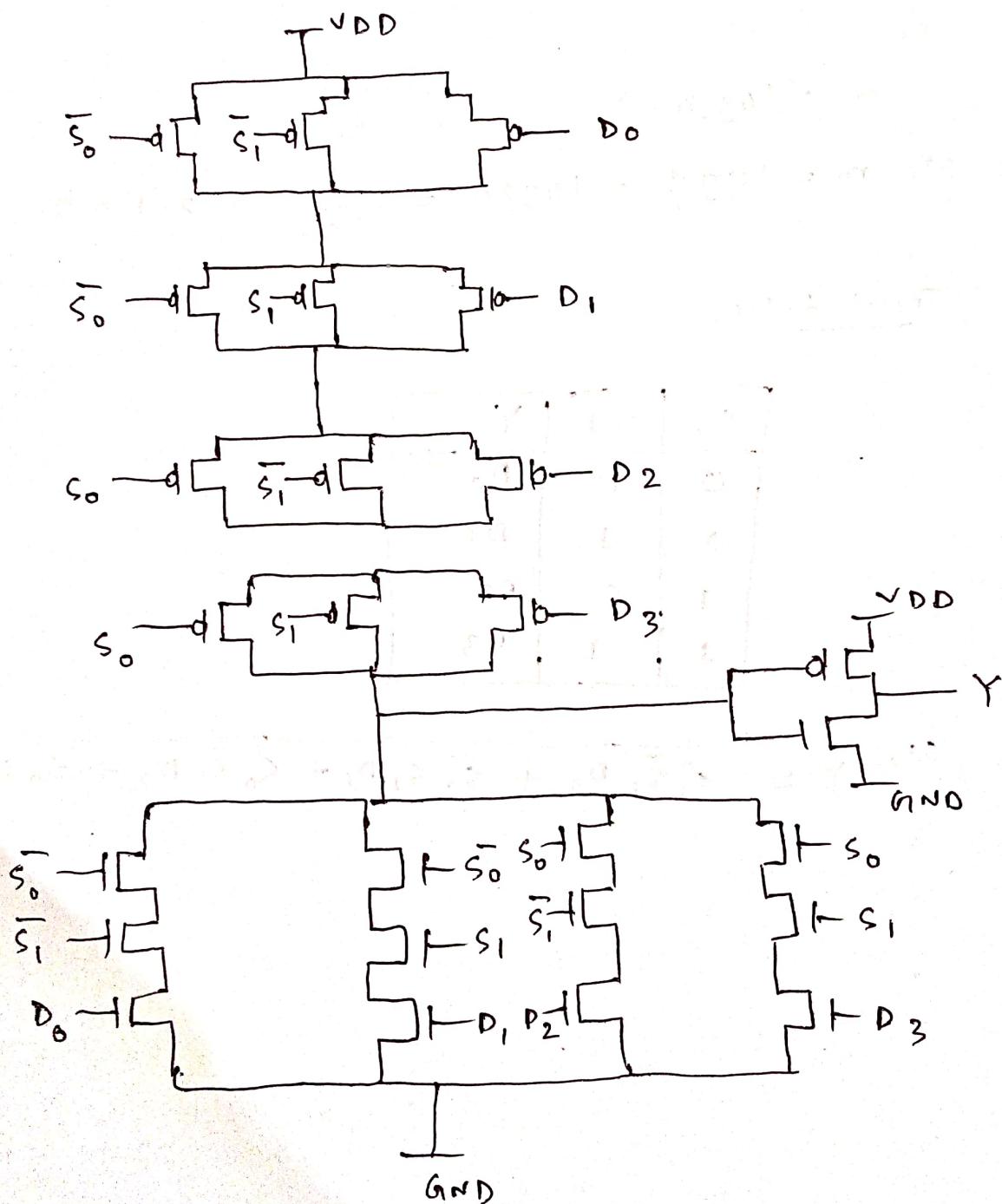
S_0	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$\text{so, } Y = \overline{S_0} \overline{S_1} D_0 + \overline{S_0} S_1 D_1 + S_0 \overline{S_1} D_2 + S_0 S_1 D_3$$

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b) CMOS equivalent circuit:

$$Y = \bar{s}_0 \bar{s}_1 D_0 + \bar{s}_0 s_1 D_1 + s_0 \bar{s}_1 D_2 + s_0 s_1 D_3$$



c)

My roll is 086

Therefore, the delay will be in $\text{ps} = 86 \text{ ps}$

Given,

No. of stages $N = 33$ stage $f = \text{frequency}$

$$\therefore \text{frequency} = \frac{1}{9 \times 33 \times 86} = 8.80 \times 10^{-5} \text{ Hz}$$

So, frequency is $8.80 \times 10^{-5} \text{ Hz}$ logical effort $g = 1$

electrical effort = 1

parasitic delay = 1

we know,
 $1 \text{ ps} = 10^{-12} \text{ s}$

$$\therefore \text{delay of each step.} = (1+1)+1 = 2$$

$$\text{Period } T = 2 \times 2^N$$

it is an N stage oscillator period of 2^N is
 is times to survive whole period.

$$\therefore f = \frac{1}{T} = \frac{1}{2 \times 2^N \times Y} = \frac{1}{2 \times 2 \times 33 \times 86 \times 10^{-12} \text{ s}}$$

 $\approx 8.8090204.37 \text{ second.}$
 $= 88.091 \text{ Hz ans.}$
 $= 88.091 \times 10^{-9} \text{ GHz}$
 $= 88.091 \times$

Ans to the Q: No - 01

a)

Lee's Algorithm is used for area Routing. This algorithm is used where the position of source and destination are through the whole entire area of chip. The goal of this algorithm is to draw a path from a source to a destination avoiding any obstacles.

Solution step:

1. At first the whole area is divided into a grid structure. There is the separation between the grid points which indicates the minimum wire width and their spacing and their spacing.

2. The routing block is modelled as obstacles.

Also the obstacles is marked as 'xy'.

3. The grid points are defined by dots and the source and destination are defined by 's' and 'd'.

Step - Wave propagation:

A path between two points is realized by propagating a waveform from the source node outwards until the destination node is reached. The method is termed as wave propagation.

The (Cont.) of step-wave propagation:

1. starting from the node 's' and the grid points are labelled.

2. The labelling is done by putting integer '1' to the grid points belonging to first wave front.

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3. The grids belonging to second wavefront are labelled by integer '2'.

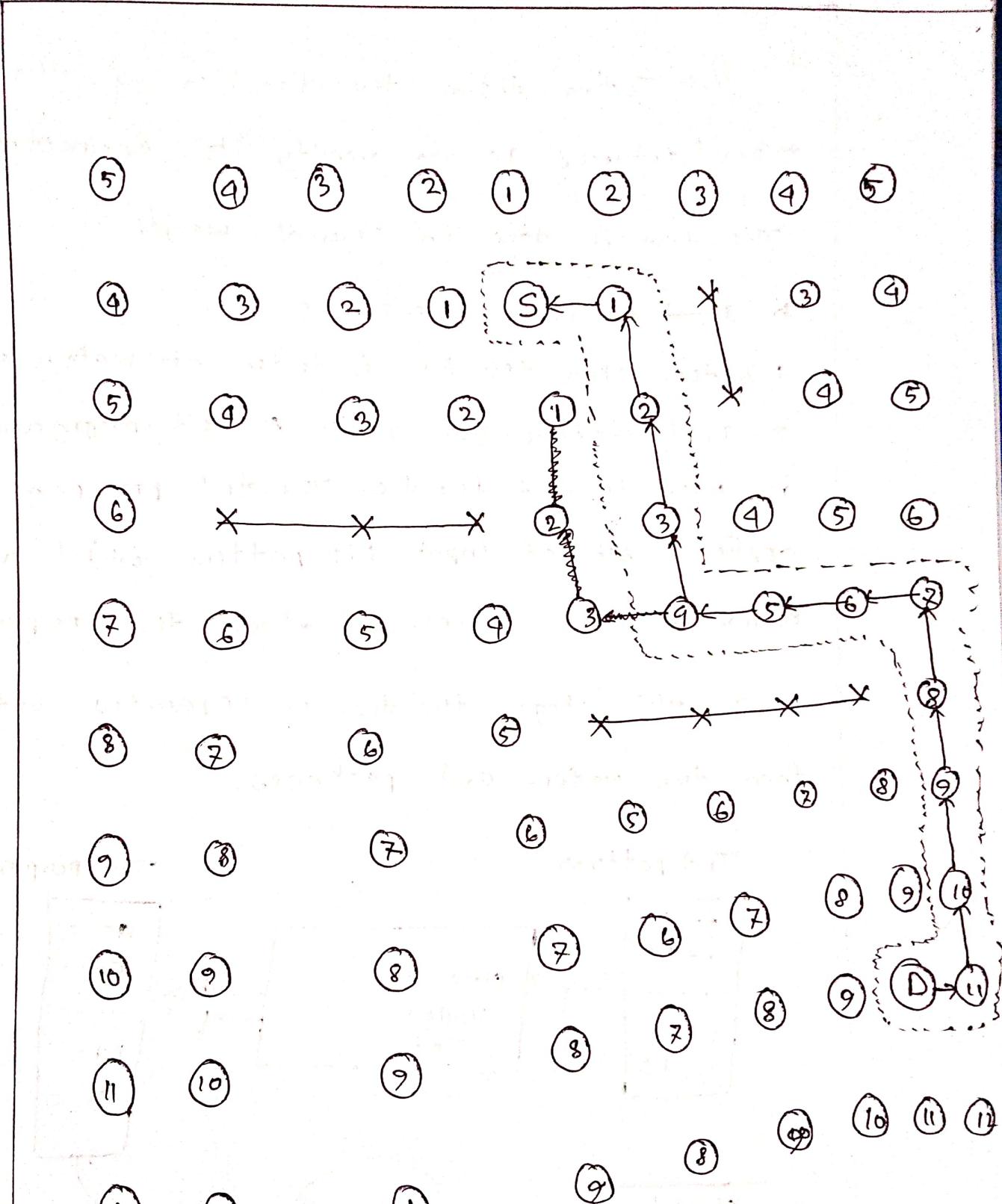
4. The process continues until the destination node '0' is reached.

step - Backtracking

Starting from the destination node '0', the shortest path is identified by backtracking the grid points with decreasing labels.

step - clean up:

The path found using the wave propagation and backtracking methods become obstacles for the next routing problem. So the labels of all the grid points are removed so that next routing task can be taken up. This is the step which is known as clean-up.



The details of the each part is following the
solution step, wave-propagation step, backtracking,
step clean up which was showed earlier.

b)

VLSI Testing defines the checking of the manufactured IC to verify its correctness.

The test is done in several ways:

~~In this stage the die is~~

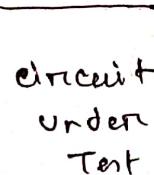
1. In this stage the die is tested at wafer level.

~~In this stage the die. A test program is used to test the die. The test program applies a set of input bit patterns which are known as test vectors. and checks the responses.~~

2. In this stage the die is separated out from the wafers and packaged.

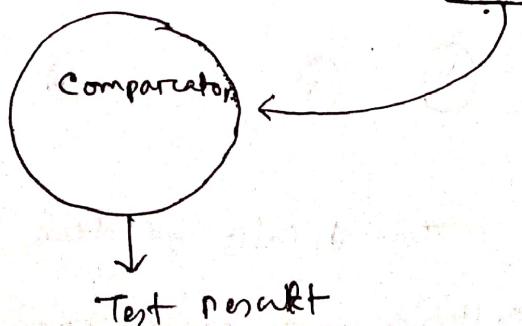
Test patterns

---	11
---	01
---	- -
---	00
---	10



Test responses

A0--
00--
- - -
01--
10--



for the circuit testing of a chip a test pattern is kept on a sample. Then the test will be applied. After test circuit under the test there is a response of Test is found. Then the test response is compared by a comparator which showed the result of testing. At last the test result is set the response as stored or correct or responses.

There are some Types of Circuit Testing :

1. Combination Circuit Testing

- ↳ Fault model
- ↳ Path sensitizing
- ↳ Random test

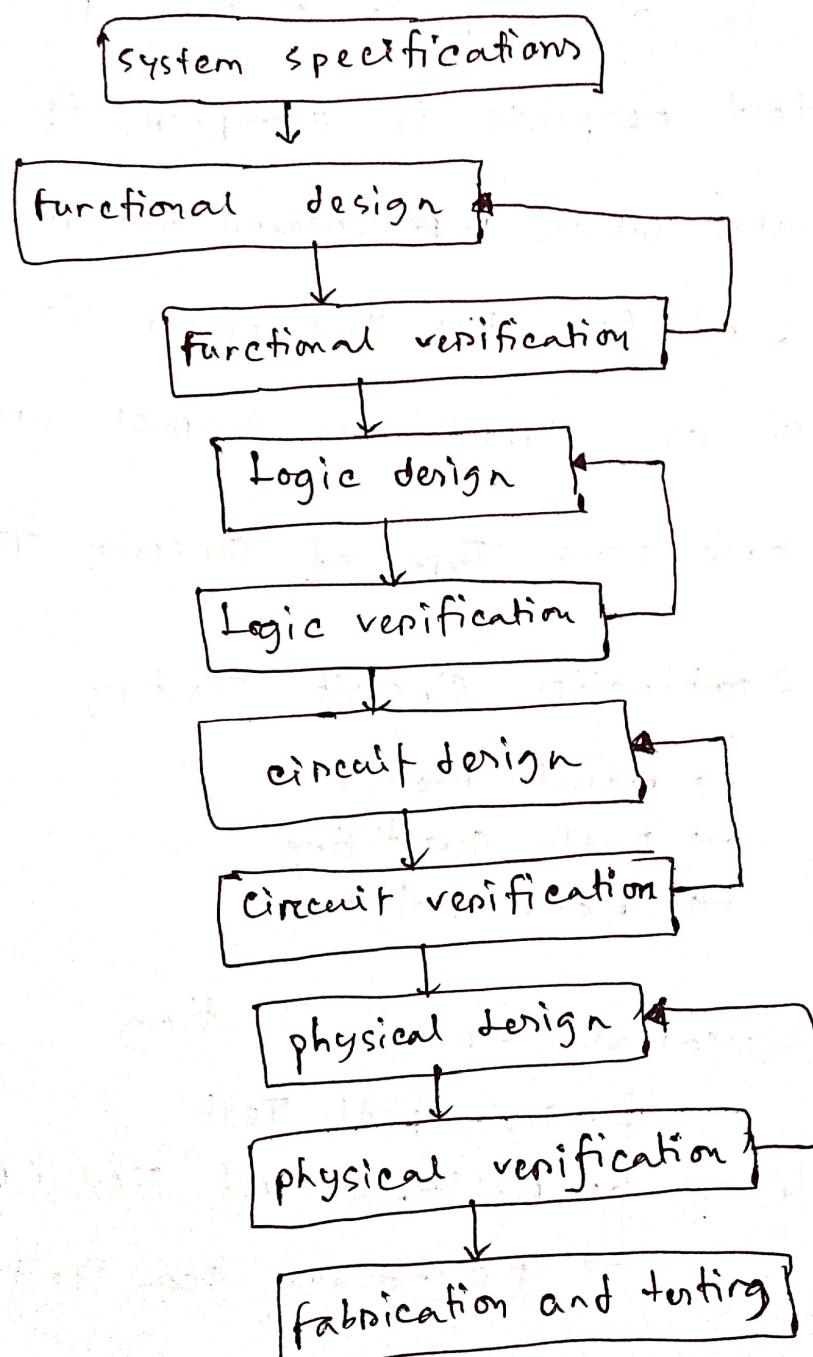
2. Sequential Circuit Testing

- ↳ Scan path Test
- ↳ Built-in self Test (BIST)
- ↳ Boundary scan Test (BST)

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Ans: to the Q: no - 09

a) VSLI Design Flow:



b)

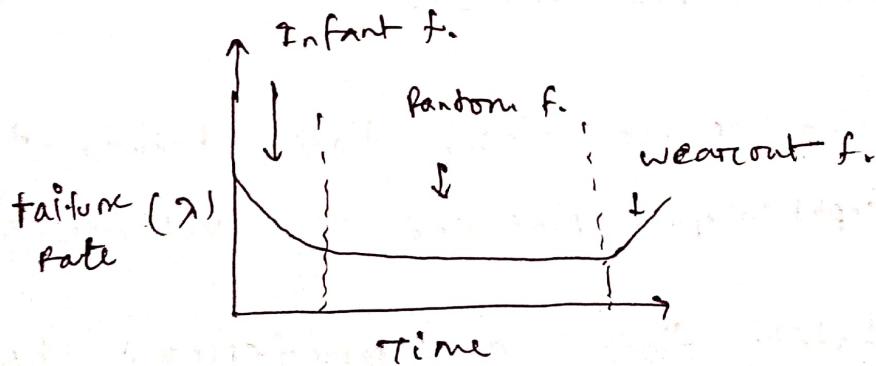
- Latch-up prevention:
1. stay belowing the absolute maximum ratings of the chip.
 2. Isolate the NMOS and PMOS devices using an oxide trench together with buried oxide layers.
 3. If we can not include an oxide trench, then we can use guarded rings around our devices. We will use guard because to add more collector terminals to the parasitic transistors in order to steer the current flow away from the desired devices.
 4. Using reverse biased diodes between the input/output pins and the voltage supplies.
 5. Schottky diodes are preferred because of their low forward resistance.
 6. Using proper grounding can avoid latch-up by using common ground point connections. Using a common ground line is not effective because in the ground line defeats the purpose.

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2. The electron-hole pairs are generated when radiation such as x-rays, cosmic etc penetrate into the chip. These carries can contribute to well currents leading to latch-up prevention for that we should avoid that.

c) The three key regions of a bathtub curve reliability testing are:

1. Infant failures
2. Random failures
3. Wearout failures



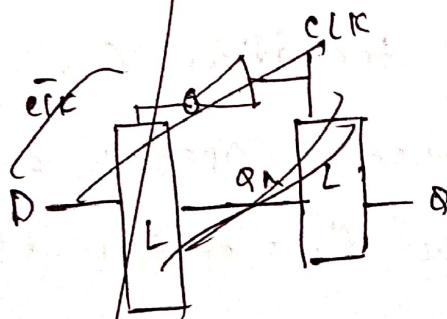
Infant early failures: λ_f is a decreasing failure rate. $\lambda_f \rightarrow 0$ as time increases.

Random failures of defines the constant failure rate. It causes due to accidental over stress or overloads, occurring randomly over the operating lifetime of the product.

Device wear-out failures of is called as aging effect. It is increasing the failure rate. Due to this the failure rate starts increasing exponentially.

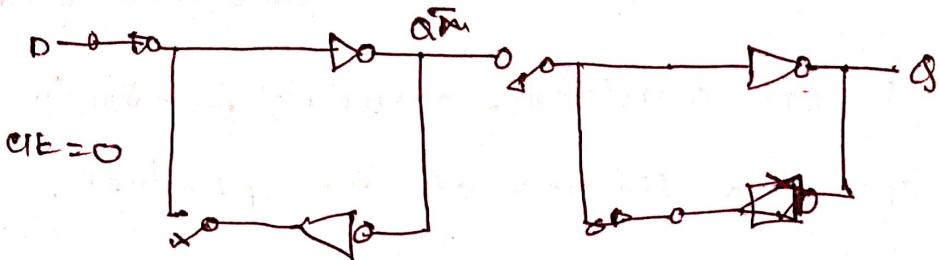
Ans: to the Q: NO - 03

- b) ~~The first latch stage is called master and the second is called the slave.~~

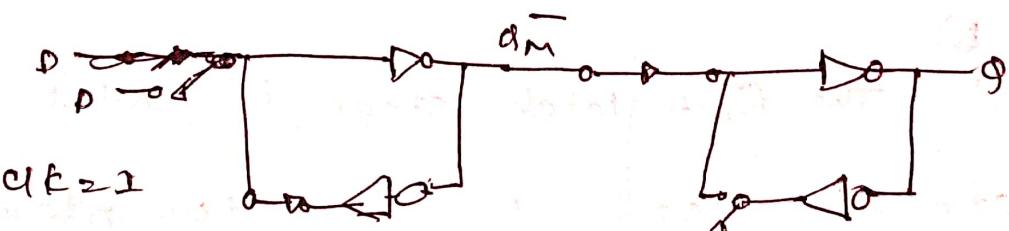


when the clock is high the D input is stored in the first latch called master but the second latch can not change state

(a) b)



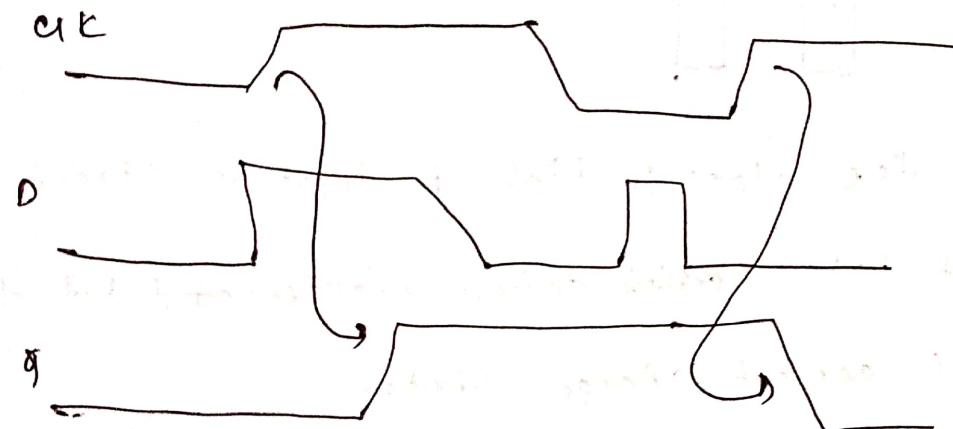
while $\text{CLK} = 0$ is low, the master negative level-sensitive latch output (α_m^-) follows the D input while the slave positive level-sensitive latch holds the previous value.



when the clock transitions from 0 to 1, the master latch becomes opaque and holds the D value at the time of the clock transition, the slave latch becomes transparent; passing the stored number master value (α_m^+) to

the output of the slave latches (a).

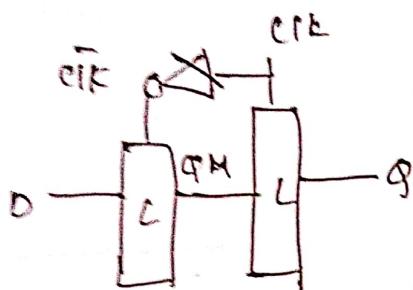
The D input is blocked from affecting the output because the master is disconnected from the D.



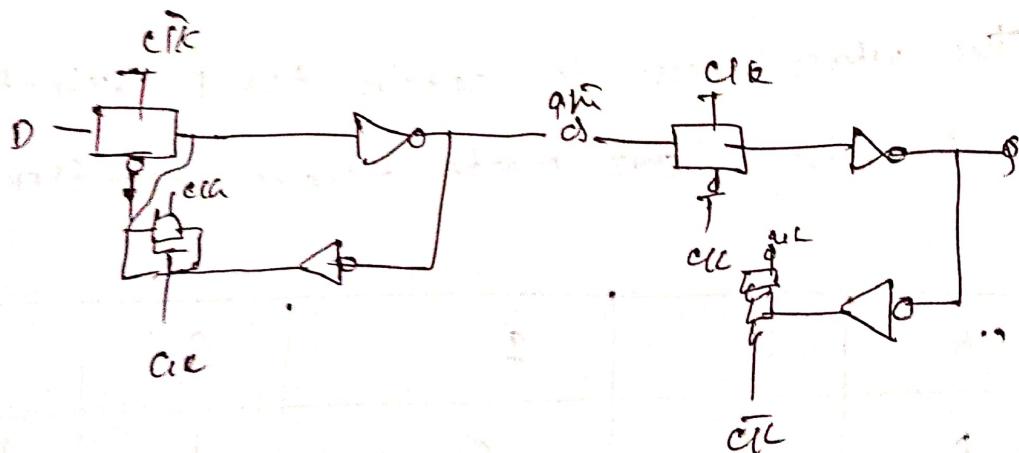
The whole process is contains the D flip-flop,
D register and master-slave flip flop.

CK	0	1	0	1
D	1	0	1	1
Q	0	1	1	1

- (ii) The first part is called master and the second part is called the slave in the diagram.



When the clock is high D input is stored in the first latch ~~and~~ called master and but the latch can not change state.



clock	0	0	1	1	0	1
D	0	1	0/1	0/1	0	0
Q	0	0	1	1	1	0