



University of Asia Pacific

Admit Card

Mid-Term Examination of Fall, 2020

Financial Clearance

PAID

Registration No : 17101086

Student Name : Md. Remon Hasan Apu

Program : Bachelor of Science in Computer Science and Engineering



SI.NO.	COURSE CODE	COURSE TITLE	CR.HR.	EXAM. SCHEDULE
1	CSE 425	Computer Graphics	3.00	
2	CSE 426	Computer Graphics Lab	1.50	
3	CSE 429	Compiler Design	3.00	
4	CSE 430	Compiler Design Lab	1.50	
5	BUS 401	Business and Entrepreneurship	3.00	
6	BUS 402	Business and Entrepreneurship Lab	0.75	
7	CSE 457	Design and Testing of VLSI	3.00	
8	CSE 458	Design and Testing of VLSI Lab	0.75	
9	CSE 400	Project / Thesis	3.00	

Total Credit: 19.50

1. Examinees are not allowed to enter the examination hall after 30 minutes of commencement of examination for mid semester examinations and 60 minutes for semester final examinations.
2. No examinees shall be allowed to submit their answer scripts before 50% of the allocated time of examination has elapsed.
3. No examinees would be allowed to go to washroom within the first 60 minutes of final examinations.
4. No student will be allowed to carry any books, bags, extra paper or cellular phone or objectionable items/incriminating paper in the examination hall.
Violators will be subjects to disciplinary action.

This is a system generated Admit Card. No signature is required.



University of Asia Pacific

Department of Computer Science and Engineering

MID SEMESTER EXAM-FALL 2020

Course Name : Design and Testing of VLSI

Course Code : CSE-457

Semester: 4th Year 2nd Semester



SUBMITTED By

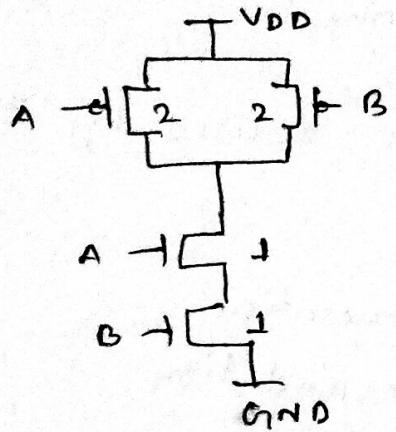
Md. Remon Hasan Apu

ID: 17101086, Section: B

Ans: to Ques Q: NO - 03

- b) N-input NAND gate has a certain logical effort:

Let, for 2 input NAND



$$\text{Here, } \text{cin} = 2+2 \\ = 4$$

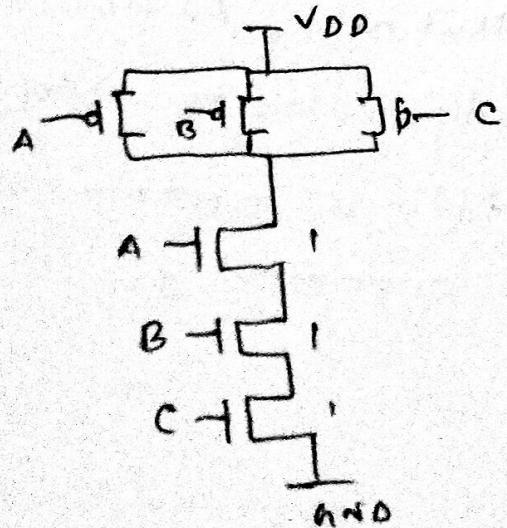
$$\text{cout} = 3$$

$$\therefore \text{Logical effort} = \frac{4}{3}$$

$$= \left(\frac{n+2}{3}\right)$$

where,
n = 2 which is 2 input

Now, for, 3 input NAND



Here,

$$\text{cin} = 1 \times 3 + 2 \\ = 5$$

$$\text{cout} = 1+2 = 3$$

$$\therefore \text{Logical Effort} = \frac{5}{3} \\ = \left(\frac{n+2}{3}\right)$$

Here, n = 3

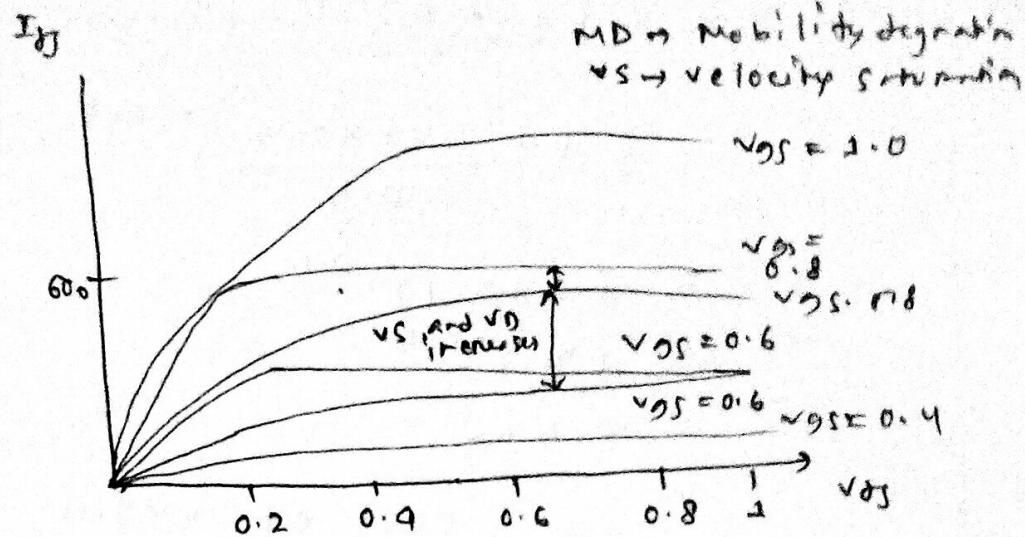
so, we found a certain logical effort for n-input NAND gate \rightarrow prove which followed $\left(\frac{n+2}{3}\right)$. (proved)

a)

Non ideal I-V characteristics:

1. When the gate voltage increases linearly, the current does not increase linearly.
2. The saturation current is always below the expected outcome.
3. This phenomenon is caused by two factors: They are:
 1. Velocity saturation
 2. Mobility Degradation

Velocity saturation is connected to voltage and lateral size. Where mobility degradation depends on vertical thickness. At the high lateral field strength, velocity stops to keep pace. And after a certain stage mobility degrades enormously.

NON IDEAL I-VAns: to the Q: NO - 02

Given,

defects density, $d = 2.5 \text{ defect/cm}^2$ clustering parameter $\alpha = 0.5$

$$\begin{aligned} \text{Area, } A &= 6\text{mm} \times 7\text{mm} \quad \text{Length width} \\ &= (7\text{mm} \times 6\text{mm}) \\ &= 42 \text{ mm} \\ &= 0.42 \text{ cm}^2 \end{aligned}$$

Total chips = 100 chips

cost of processing of a wafer = Registration ID
 $= 17,101,086$

Date

NOW,

$$\begin{aligned}
 Y &= \left(1 + \frac{A \cdot D}{\alpha} \right)^{-\alpha} \\
 &= \left(1 + \frac{0.42 \times 2.5}{0.5} \right)^{-0.5} \\
 &= (1+2.1)^{-0.5} \\
 &= (3.1)^{-0.5} \\
 &= 0.567
 \end{aligned}$$

$$\begin{aligned}
 \therefore \text{cost/clip} &= \frac{\text{cost of wafer}}{\text{Total clips} \times Y} \\
 &= \frac{17,101,086}{100 \times 0.567} \\
 &= \frac{17,101,086}{56.7} \\
 &= 301,606.455 \text{ taka}
 \end{aligned}$$

The clip size is increased by 20%, after DFT is included.

$$20\% = 1.2$$

$$\text{So, new area} = 0.42 \times 1.2 = 0.462 \text{ cm}^2$$

$$\begin{aligned}
 \therefore \text{Yield} &= \left(1 + \frac{\Delta D}{d}\right)^{-\alpha} \\
 &= \left(1 + \frac{0.462 \times 2.5}{0.5}\right)^{-0.5} \\
 &= (1 + 2.31)^{-0.5} \\
 &= (3.31)^{-0.5} \\
 &= 0.549
 \end{aligned}$$

$$\therefore \text{a wafer contain chips} = \frac{150}{1.2} = 90.91 \approx 91 \text{ chips}$$

$$\begin{aligned}
 \therefore \text{number of good chips} &= 91 \times 0.549 \\
 &= 49.95 \\
 &\approx 50 \text{ chips}
 \end{aligned}$$

$$\begin{aligned}
 \therefore \text{cost chip} &= \frac{17101086}{91 \times 0.549} \\
 &= \underline{302,302.408} \text{ taka}
 \end{aligned}$$

$$\begin{aligned}
 \text{form, } 50 \text{ chips cost will be } 17101086 \text{ taka} \\
 \therefore 1 \text{ " } 2 \text{ " } " \text{ " } " \quad \frac{17101086}{50} \\
 &= 342,021.72 \\
 &\text{taka.}
 \end{aligned}$$

Ans:

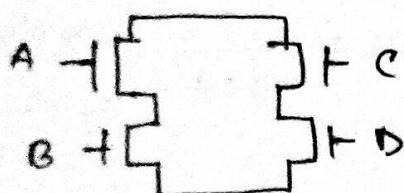
Ans: to due Q: no - 01

(b)

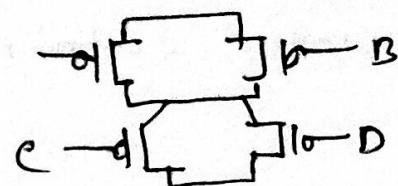
A 2021 defines,

$$\overline{A \cdot B + C \cdot D}$$

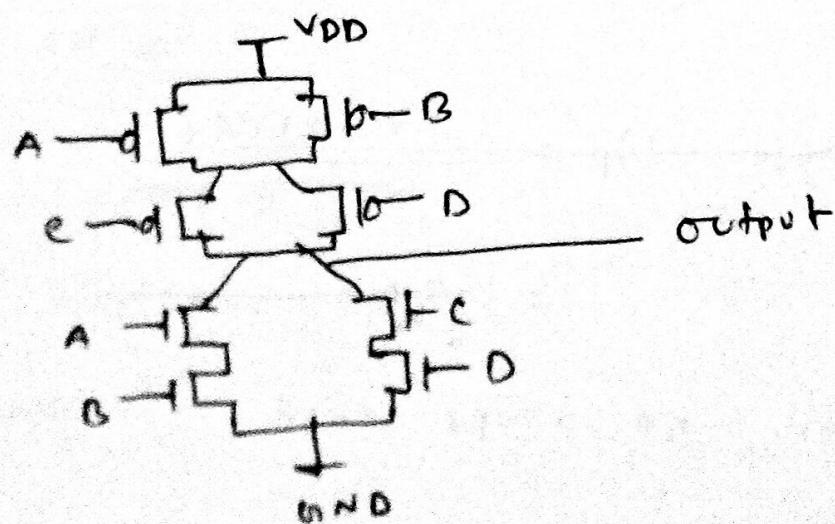
n MOS



pMOS



$$\overline{A \cdot B + C \cdot D}$$



(A)

The major impacts defines Moore's projection based on the observation that costs has decreased with increasing complexity. Moore's law impacts within the upper constraints in IC fabrication Industry.

An IC (integrated circuit) is an electronic network fabricated in a single piece of a semiconductor material.

Lithography is a process that is used to transfer patterns to each layer of the IC by containing the method's of Moore's law.

Sequences are:

1) Designer

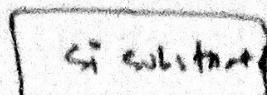
2) silicon foundry

Applicable:

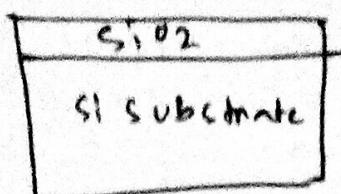
- drawing the layer patterns on a layout editor on IC designer defines.

- printing defines the mask pattern to the wafer surface for silicon foundry

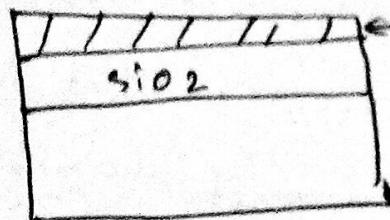
- in so, electrical power station, the components making of processes of computers.

Lithography Sequence steps

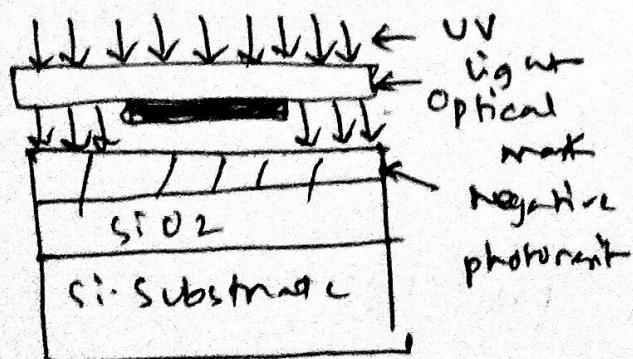
Base material



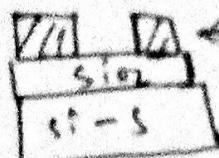
S-01: oxidation layering



S-02: photomask creating

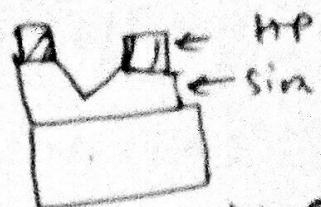


S-03: stepper exposure



← Hardening photoresist

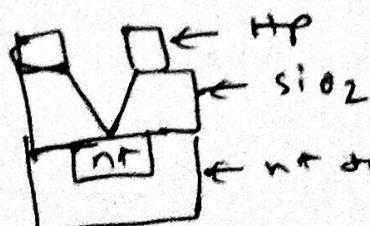
S-04: soft toning



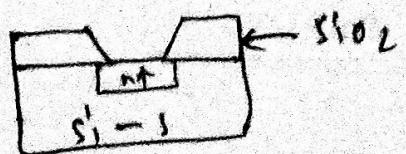
S-05: Acid etching



S-06: BFO



S-07: various steps of n+ doping



S-08: ashing