DIFFERENTIAL END CURRENT STARVED VCO IMPLEMENTED IN 28nm CMOS TECHNOLOGY

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***Abstract* – The scope of this work is to present a low power Current Starved Voltage Controlled Oscillator with Differential cross-coupled inverter as delay stages instead of regular inverter. Couple of benefits of using this Differential Cross coupled inverter is that: one, leakage power can be reduced thereby reducing overall power consumption and two, phase noise is reduced making this circuit stable; Hence can be used in space applications such as Radiation hardening of PLL. This circuit has been implemented in 28nm CMOS technology.**

***Keywords* – DIFFERENTIAL CURRENT STARVED VCO, LOW POWER CSVCO, PLL**

I. INTRODUCTION

In VLSI System Design, Phase Locked Loop (PLL) is an essential building block for many timing generator applications. It comprises of five essential blocks which are Phase Frequency detector, Charge Pump, Low pass filter, Voltage controlled oscillator and Frequency Divider.

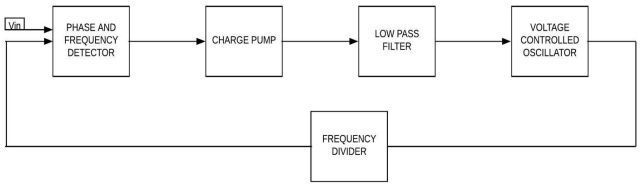

Fig. 1. Phase Locked Loop

Among many different oscillators, LC and ring oscillators are the most commonly used ones. The LC VCO occupies more area, and the tuning range is very narrow. Ring VCO provides a wide tuning range, less power consumption with less area. Among many types of Ring oscillators, Current starved VCO offers a balance between the power, area, phase noise with wide tuning range. In PLL, VCO is the most sensitive block to leakage power, and it will affect the performance of PLL to a more considerable extent.

II. VCO CIRCUIT DETAILS

By different ways the Ring oscillator can be realized. The frequency of oscillation is inversely proportional to the number of delay stages and delay time (or) propagation delay of each stage. The main disadvantage of normal ring VCO is that there is no different supply and control voltage, but supply voltage is considered as the control voltage. The current starved technique utilises the principle of current mirror. Current mirror is a technique where corresponding voltage is converted into current. As the control voltage increases, the amount of current flowing through circuit also increases, hence increasing the switching speed of delay cell, thereby increasing oscillation frequency.

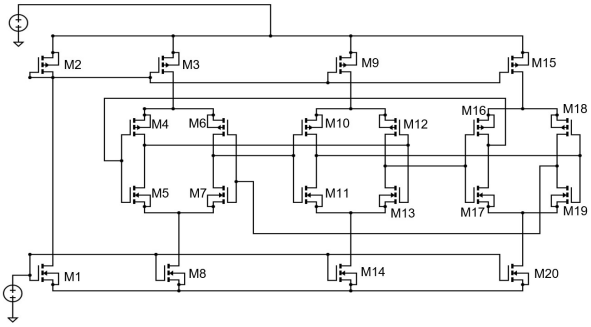

Fig. 2. Differential End Current Starved VCO

In the Differential Current Starved VCO, the delay stages are replaced by differential delay cells. The bottom two NMOS in the delay forms the pull-down network. M4, M5, M6, M7 forms one delay cell. The three delay cells are used to build a VCO to increase the oscillation frequency and gain. The advantage of using a differential delay cell is that the leakage power can be reduced a lesser Phase Noise. By increasing the number of stages of inverters from three to five the phase noise will be much better but the oscillation frequency and gain reduces.

III. Transient Analysis of the Circuit

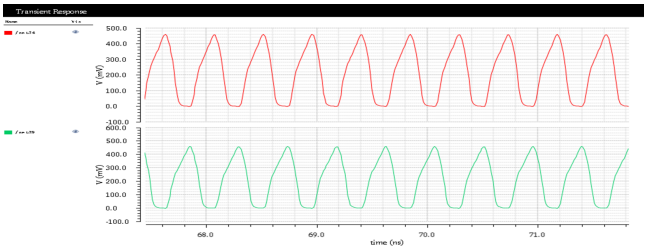

Fig. 3. Transient Analysis of Differential End Current Starved VCO

As shown in the above graph we can see that the voltage is oscillating with respect to time. Also, as expected both the outputs are out of phase.

References

[1] B. Razavi. A 2-GHz 1.6-mW phase-locked loop. IEEE Journal of Solid-State Circuits 1997; 32 (5): 730-735.

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