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Innovus™ Implementation System (Block)

Course Version 18.1

Lab Manual

Revision 1.0

cadence®

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Modules 1-4: No Labs

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Module 5: Floorplanning the Design

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Lab 5-1 Importing a Design

Objective: To start the software and import a design.

In this lab, you import a gate-level netlist and libraries into the Innovus™ Implementation System system and create a floorplan. You become familiar with the floorplanning and power planning forms and icons. You also become familiar with checking the libraries, checking the design, and using bindkeys.

Design Information

The DTMF design that you will be using in this lab contains almost 6000 instances, 57 I/Os, and about 6400 nets. The netlist is a hierarchical Verilog netlist. The DMA source clock is *DTMF_INST/clk*. The serial port interface clock is *DTMF_INST/spi_clk*. The scan clock is *scan_clk*. The process used is the 180-nanometer process technology with six layers of metal.

For more information about the DTMF design, refer to the *designDTMF.pdf* file included in the *FPR/doc* directory.

Starting the Software

1. Change to the working directory where you will run floorplanning by entering:

```
cd FPR/work
```

2. Start the Innovus Implementation System by entering:

```
innovus
```

Do not use the window where you started the software for any windowing or UNIX operations, except to communicate with the tool.

Importing a Design

1. To import a gate-level netlist, timing constraints, and libraries, choose **File – Import Design**.

The Design Import form appears.

2. Click the **Load** button.

3. Select the **dtmf.globals** file. Click **Open**.

When you load the file, it fills in the fields in the Design Import window.

Floorplanning the Design

The technology files and the *./dtmf.view* file for the labs are displayed. The *dtmf.view* file contains pointers to the timing library and the constraints files.

The I/O assignment file *dtmf.io* contains directives about how to place the I/O pads around the periphery of the core area.

4. To load the design and libraries, in the **Design Import** window, click **OK**.

The following table provides a brief description of the fields in the Design Import window.

Field	Description
Verilog files	Contains the names of gate-level Verilog netlist files.
LEF files	Library of components and physical data for the components in LEF format. Also contains routing layers and DRC rules.
IO Assignment file	This file contains the I/O pad order information to enable the software to place the pads on the periphery of the design. If this file is not provided, the tool places the I/O pads randomly around the periphery of the design.
MMMC View Definition file	Contains pointers to timing libraries and SDC constraints files.

Viewing the Design

In this section, you learn more about the objects on the screen, and how to view and interpret what you see in the design window.

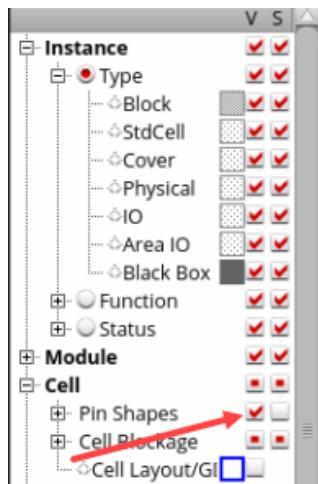
1. To enlarge the window, drag the corner of the window until you can see all the modules in your design, as well as all the Innovus menus.

2. Select the **Floorplan** view.



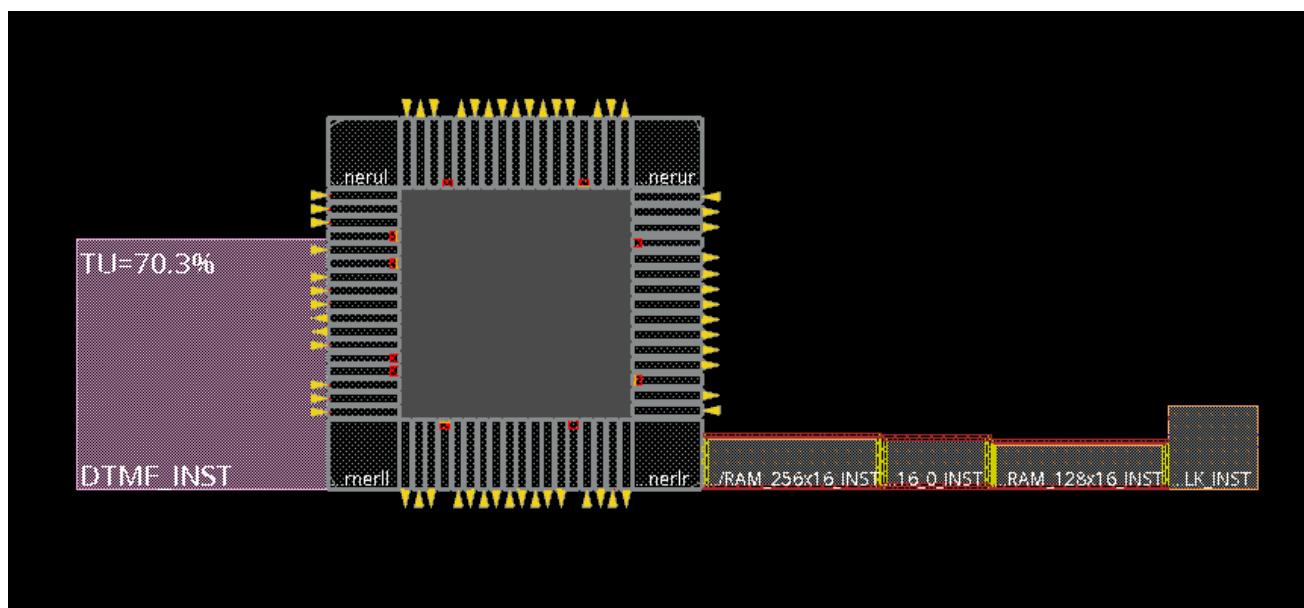
3. Fit the design to the window by pressing the **f** key.

4. Under the All colors pane, make sure that **Pin Shapes** visibility under Cell is selected.



5. Zoom out by pressing **Shift-Z** or by clicking the **Zoom Out** icon.

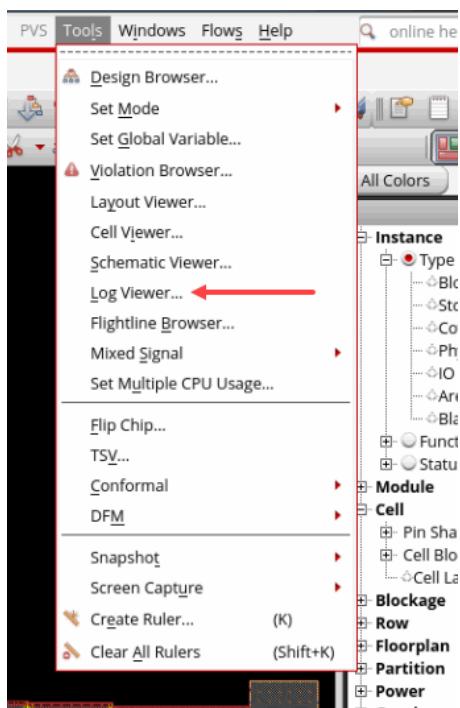
The view changes.



6. Expand the design window horizontally to display all the available pull-down menus.

Floorplanning the Design

7. Choose **Tools – Log Viewer**.



8. Select the latest Innovus log file, which corresponds to this session.

9. In the Log File form, click **Open**.

Are there any errors displayed?

Answer: _____

10. Close the Log Viewer.



11. To view more of the objects, click the **Zoom Out** icon or press **Shift-Z**.

12. Move your cursor over the icons and notice that their functions are displayed in text boxes, as shown here.



13. Select **All Colors**, which brings up the Color Preferences Menu.

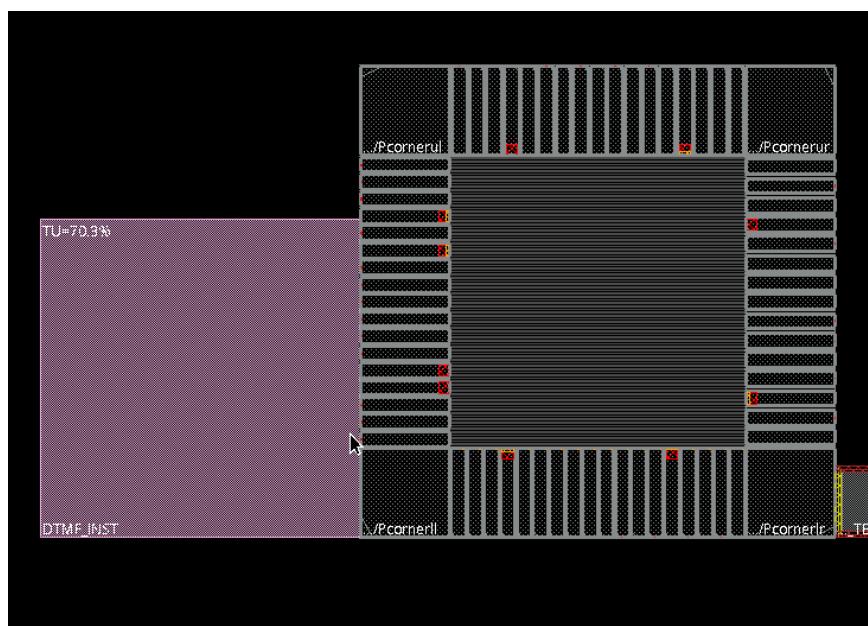
You can turn on and off the visibility and selectability of objects by clicking under **V** (for visibility) or under **S** (for selectability).

14. For example, unselect terminal visibility.

Standard Row	<input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/>
Type/StdCell	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
Pin Shapes/StdCell	<input checked="" type="checkbox"/> <input type="checkbox"/>
Cell Blockage/StdCell	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
Terminal	<input type="checkbox"/> <input checked="" type="checkbox"/>
Trim Blockage	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
Routing Blkg/Undefined	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
Status/Unplaced	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>

15. Notice that the IO terminals in the design window are no longer visible.

16. On the left of the core area, select the pink module **DTMF_INST**.

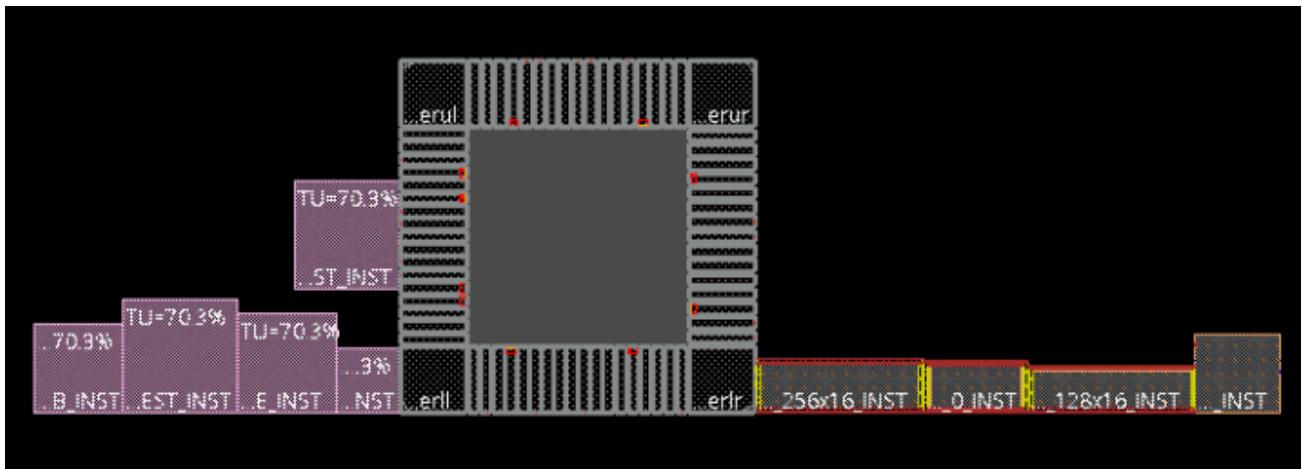


17. After selecting the **DTMF_INST** module, click the **Ungroup** icon once.



This will ungroup the module.

Do not perform this operation more than once.



18. To see names and properties of the design objects, **double-click** several objects.

The pink objects on the left of the core area is the module guide, whereas the objects to the right of the core area are all the blocks (hard macros or IP) in the design. The pink guide represents modules that were defined in the imported Verilog netlist.

The size of the module guides relates to the utilization of each module and the number of standard cells that the modules contain.

19. To zoom to a particular area, press and drag the **right** mouse button over a rectangular area.

The window zooms to that area.

20. Choose **View – Set Preferences**. Click the **Display** tab.

The Min Floorplan Module Size parameter determines the size of the module guides. Because the *Min. Floorplan Module Size* is defined as 100, if a module contains fewer than 100 instances, it will be merged into another module guide.

- a. To better understand the fields on the form, click **Help**.

Most forms have a **Help** button to display a Cadence Help window and give you more information about the form.

- b. When you are finished reviewing the fields, click **Cancel**.

21. To regroup the modules, select one of the pink guides. Click the **Group** icon.

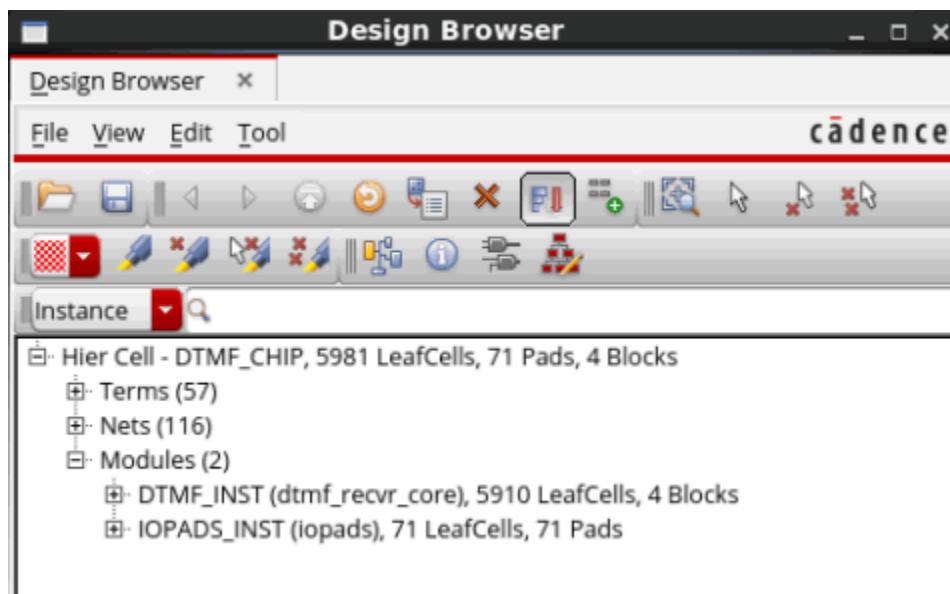


Viewing the Design Hierarchy

1. Make sure that all objects are unselected by clicking outside the design area and choosing **Tools – Design Browser**.

The Design Browser lets you explore the logical hierarchy of the netlist.

2. To expand the modules, click the plus sign (+) next to Modules.



3. To view the I/O terminals of *DTMF_INST*, click the **Terms** plus sign (+).
4. When you are finished, close the Design Browser window.

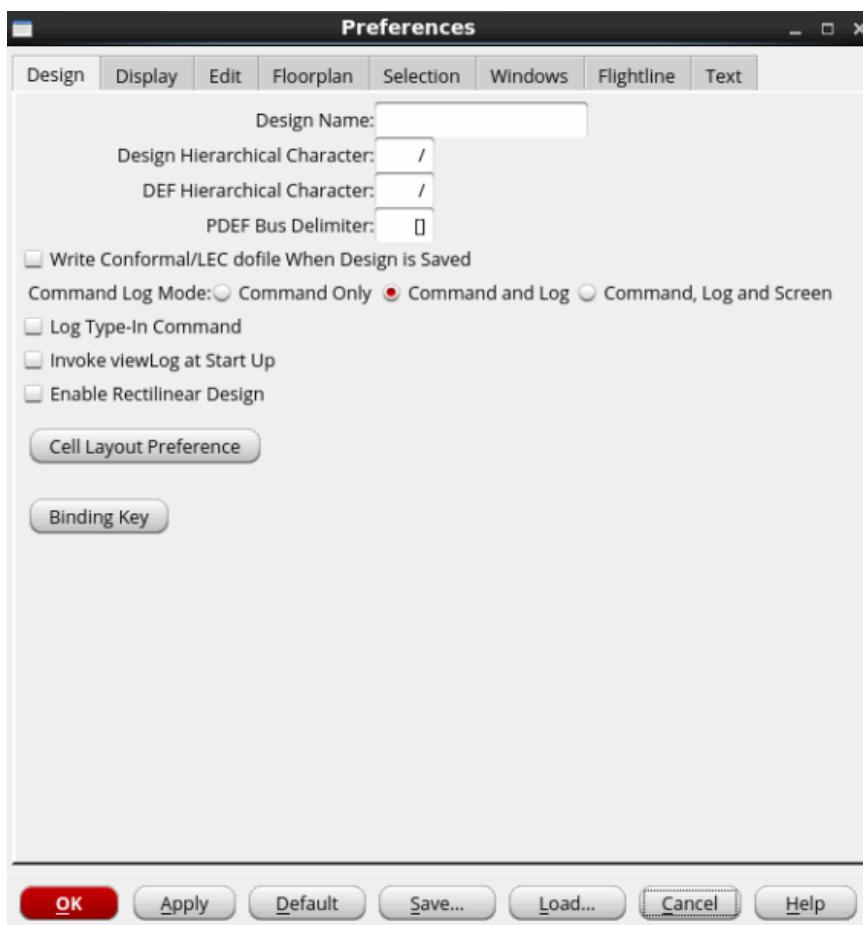


Lab 5-2 Using Bindkeys

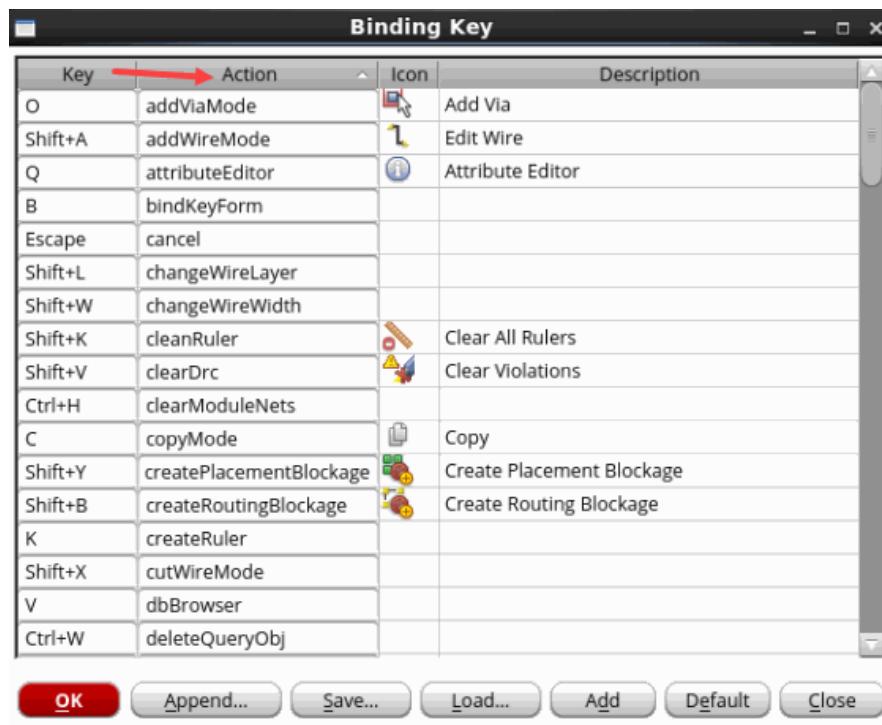
Objective: To use the bindkeys to implement floorplanning functions.

Using the Bindkey Form

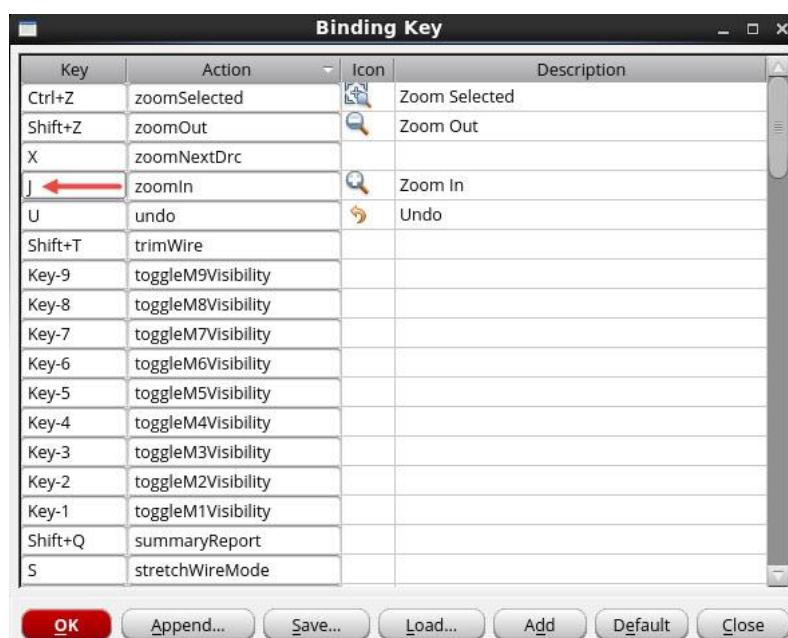
1. Make sure that you are still in the **Floorplan** view. 
2. To display the Bindkey form, choose **View – Set Preference**.
3. Select the **Design** tab, if it is not already selected.
4. To display the Binding Key definition form, click the **Binding Key** button.



5. To sort all the actions alphabetically by the action names, click **Action**.



6. To sort the bindkeys alphabetically by the binding key names, click **Key**.
7. Redefine the **Zoom In** key as *J*.



8. Click **OK**.
9. Test that the key has been redefined.

10. Reset the **Zoom In** key back to **Z**.
11. In the Preferences form, click **Cancel**.

Using Bindkeys

1. To zoom out, press **Shift-Z**.
2. To pan right, press the **right arrow** keys.
3. Click the hard macro **RAM_256x16_INST**. It is the first macro to the right of the core area.

The blue flight lines display connections between the block and the module guide that it connects to.

4. Double-click **RAM_256X16_INST**.

The Attribute Editor appears.

5. Check the orientation of the macro.

What is the orientation of the hard block?

Answer: _____

6. Close the Attribute Editor form.

7. Click the **Move** button and move the RAM inside the core area of the design.



8. Click **left** to place the RAM inside the core area.

9. Because the design has not been floorplanned, the core size has not been set.

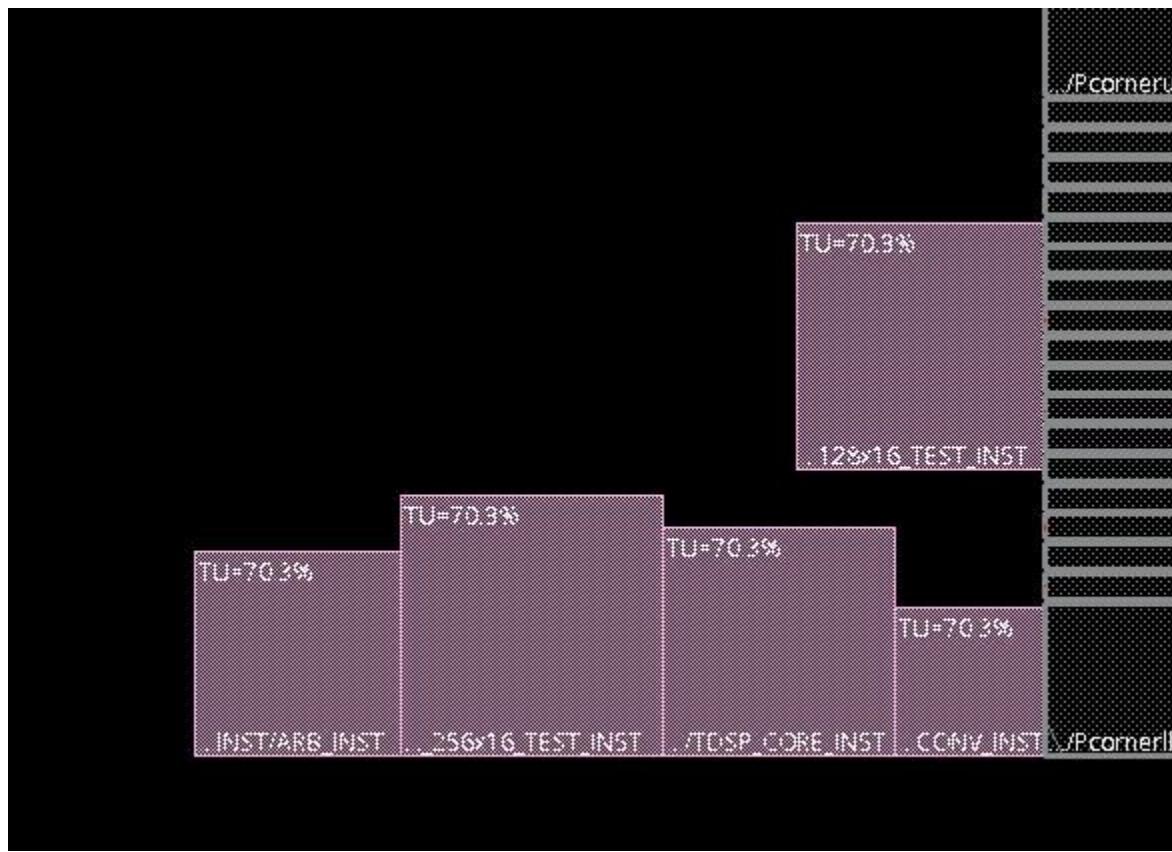
10. To display the Flip/Rotate Selected Instances form, press **r**.

11. Select **R90**. Click **OK**.

12. To close the move mode and to be in the selection mode, press the letter **a** on the keyboard.

13. Select **DTMF_INST**, the large pink module on the left of the core area.

14. To ungroup the *DTMF_INST* module, press **Shift-G** once.



You are still in select mode.

15. Select a pink module.

To select multiple objects, you would press and hold the **Shift** key down and select another module.

16. Click the **Move** button. Move the module into the core area.



17. Click **left** to place the module.

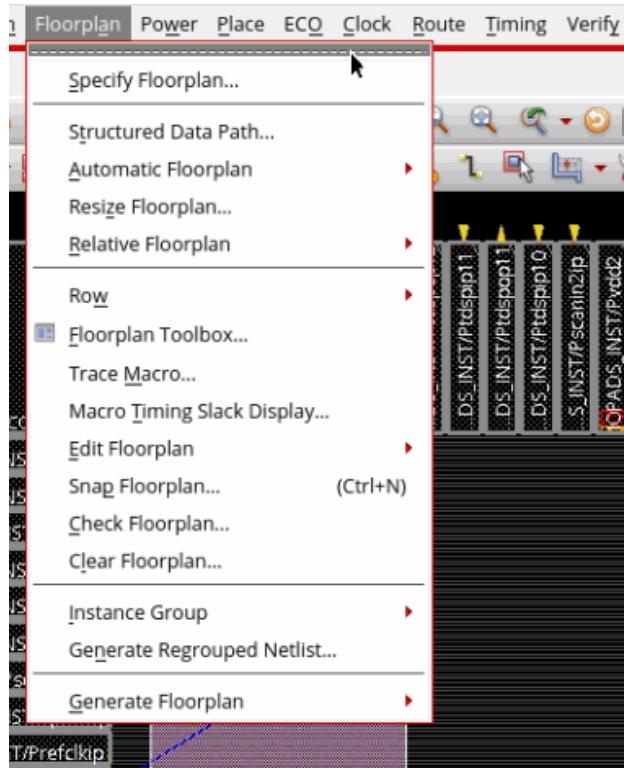
18. To get back to select mode, press **a** bindkey on the keyboard.



Lab 5-3 Tearing Off Menus

Objective: To use the tear-off menu feature when you have to repeat tasks.

1. Choose **Floorplan**.
2. To detach the menu from the main task bar, click the dashed line above the menu list.



3. Place the detached menu in a convenient location on your desktop.

 End of Lab

Lab 5-4 Clearing the Floorplan

Objective: To clear floorplanning objects from a floorplan to improve an existing floorplan or create a new one.

1. To display the Clear Floorplan form, from the **Floorplan** menu, choose **Clear Floorplan**.
2. Select **All Floorplan Objects**.



3. Click **OK**.

The module guides and the hard macro that were placed in the core area are unplaced.

- a. You can clear all floorplan objects or a subset of floorplan objects.

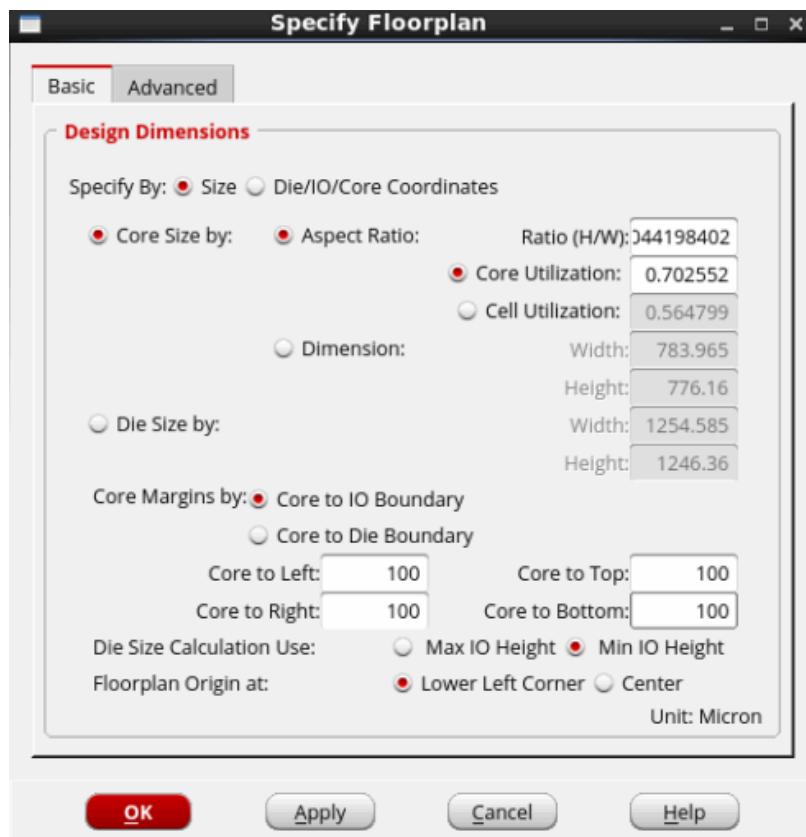


Lab 5-5 Initializing the Floorplan

Objective: To set the aspect ratio and explore the hierarchy.

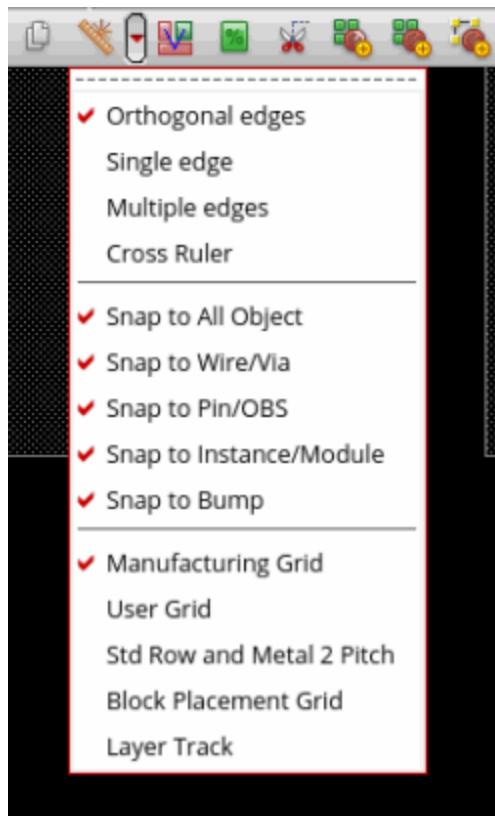
1. Choose **Specify Floorplan**.

The Specify Floorplan form appears.



2. Enter **100** for Core to Left, Core to Right, Core to Top and Core to Bottom values.
3. To display more information about the options, on the Specify Floorplan form, click **Help**.
4. To initialize the floorplan, click **OK**.
5. To measure the distance between the core area and the I/O boundary, click the **Ruler** icon or press **k**.

The ruler icon has a pull-down list which lets you select from several snapping options.



6. To delete the ruler, click the **Clear All ruler** icon or press **Shift+K**.



End of Lab

Lab 5-6 Customizing the Menus

Objective: To create a menu item and associated commands.

To add and delete menu items, use the commands *uiAdd* and *uiDelete*.

1. In the *csh* window where you started the tool, run the following command:

```
uiAdd expMenu -type menu -label NewMenu -in main
```

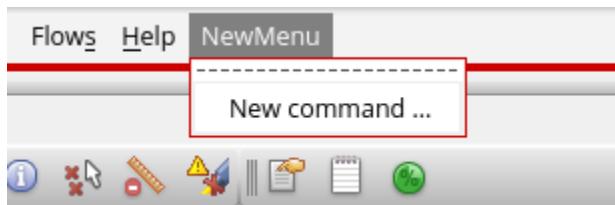
Tip: You can copy and paste all the commands in this lab section from the TCL script *menuAdd.tcl*, which has been provided in the *work* directory.

2. Notice that the new menu *NewMenu* appears in the upper-right corner of the main menu. You might have to expand the design window to see the newly created menu.



3. To add a subcommand under **NewMenu**, enter the following command:

```
uiAdd expCmd -type command -label "New command ..." \
-command [list puts "execute my command"] -in expMenu
```



You might need to expand the Innovus window to see it displayed in the toolbar.

4. To add a new toolbar, enter the following:

```
uiAdd expToolbar -type toolbar -in main -label \
"New Toolbar" -newline true
```

5. To add the new tool button **new toolbarbutton** on the New toolbar, enter the following:

```
uiAdd expToolbar -type toolbarbutton -in expToolbar \
-label "new toolbarbutton" -tooltip "new toolbarbutton" \
-icon [file join ./ \
layout-place-in-schematic.png] \
-command [list puts "New toolbarbutton ..."]
```



6. To delete NewMenu (which you created in a previous step), enter this command:

```
uiDelete expMenu
```

7. To delete the toolbar that you created, enter the following:

```
uiDelete expToolbar
```



Lab 5-7 Checking the Design

Objective: To determine if there is missing or incorrect information in the libraries or in the netlist.

In this lab, you check the design files and identify the problems to fix.

1. To check the design, run the following command:

```
checkDesign -netlist
```

The *checkDesign* command will check the following:

- The netlist after the design has been loaded.
- The physical library before floorplanning.
- Power and ground connections before routing and extraction.
- The legal placement of cells.
- Timing libraries before any timing-related operations are run such as timing-driven placement and routing, timing optimization, clock-tree synthesis, and static timing analysis.
- Tie-high and/or tie-low connections before routing and extraction.

2. View the *checkDesign/DTMF_CHIP.main.htm.ascii* file.

How many output floating nets (nets without fanout) are in the design?

You can find the answer by viewing the *checkDesign/DTMF_CHIP.main.htm* file with Mozilla® or a browser of your choice and looking for the string *Output Floating Nets*.

Alternatively, you can check for the string *Output Floating nets* in the *checkDesign/DTMF_CHIP.main.htm.ascii* file.

Answer: _____

Which cells are marked “Dont Use” in the library?

Answer: _____

3. At the prompt, enter:

```
help checkDesign
```

Running help before commands will list all the available options for the command.



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Module 6: Planning Power

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There are no labs in this module

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Module 7: Routing Power with Special Route

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Lab 7-1 Floorplanning a Design

Objective: To floorplan and explore manual floorplanning icons.

Floorplanning

This section introduces you to the floorplanning icons in the Tools area.

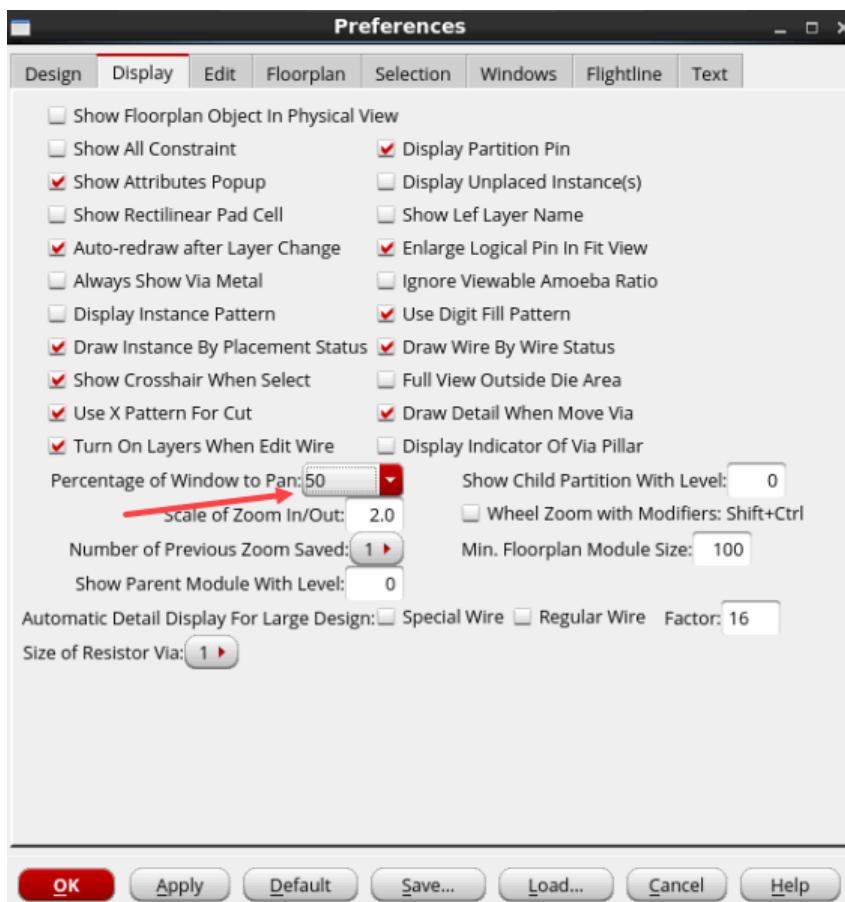
1. To display the functionality of each icon, position your cursor over each one in the **Tools** area.



2. To pan left in the design window, click the left arrow key on your keyboard.
3. To set the percentage to pan, choose **View – Set Preference**.
4. Click the **Display** tab.

Routing Power with Special Route

5. Set Percentage of Window to Pan to **50**.



6. Click **OK**.

Do you see a difference in panning with the arrows after you set the percentage to 50?

Answer: _____

7. To pan slowly up or down, press **Ctrl** while moving the scroll wheel or button forwards or backwards.

8. To pan slowly left or right, press **Shift** while moving the scroll wheel forwards or backwards.

9. If there is only one large pink guide on the left hand side, select it.



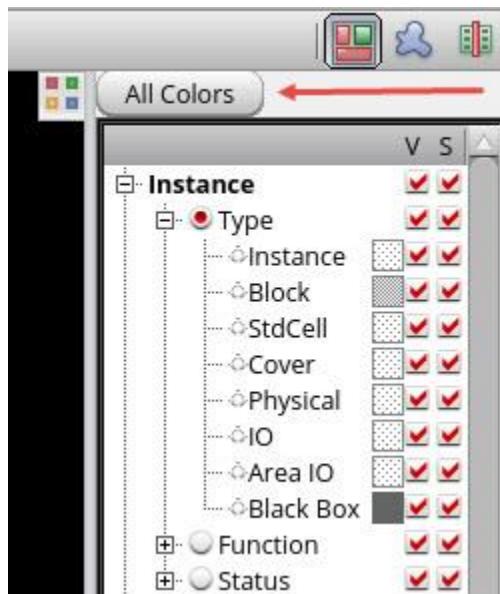
10. Click **Ungroup** once.



11. Select one of the ungrouped guides and click the **Move** button.

12. Move the selected pink module guide into the core design area.

If you do not want to display these blue flight lines, click the **All Colors** button.



The Color Preferences form is displayed.

13. Under the **View-Only** tab, deselect **Flight Line**.

FinFET Instance Grid	<input type="checkbox"/>	Pin Density	<input type="checkbox"/> <input checked="" type="checkbox"/>	Trim Grid	<input type="checkbox"/>
FinFET Manufacture Grid	<input type="checkbox"/>	Pin Text	<input checked="" type="checkbox"/>	Trim Metal	<input checked="" type="checkbox"/>
FinFET Placement Grid	<input type="checkbox"/>	Port Number	<input type="checkbox"/>	User-defined Grid	<input type="checkbox"/>
Flight Line	<input checked="" type="checkbox"/>	Power Density	<input type="checkbox"/>		
Multi-Color Layers		Flight Line Visibility			
CTD Object	<input checked="" type="checkbox"/>	Flightline Congest	<input type="checkbox"/>	Thermal	<input type="checkbox"/>
Clock Tree	<input checked="" type="checkbox"/>	GTD Object	<input checked="" type="checkbox"/>	Vertical Congest	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>

14. Close the Color Preferences form.

15. Click the **Cut Rectilinear** icon.



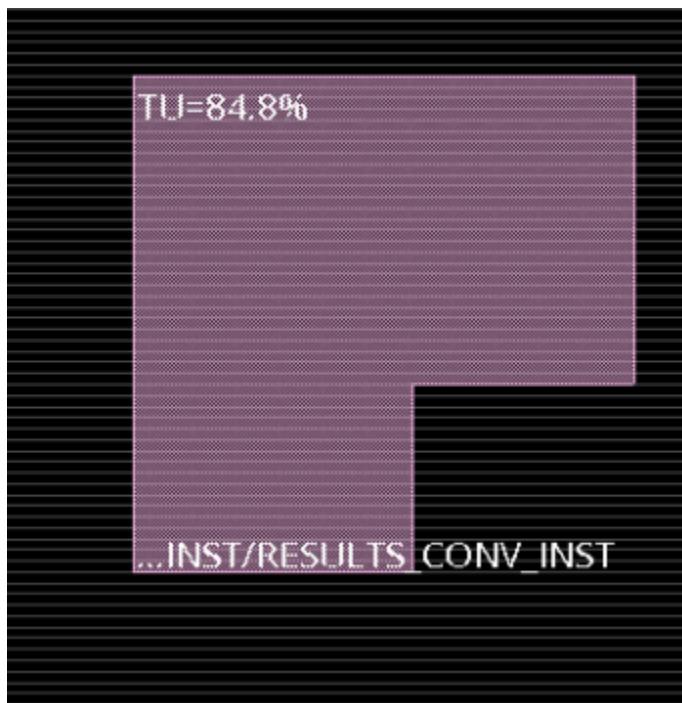
16. Grab an edge or corner of the selected module guide with the left mouse button and draw a box to represent the cutout area.

17. Click, again. The resulting rectangle is the cutout area of the originally rectangular-shaped guide.

Notice that the Target Utilization (TU) number changes. The TU value is the *target utilization percentage* for a given module area.

Routing Power with Special Route

Module constraints display a target utilization (TU=%) value to represent their physical design size. This is an estimation of module utilization for the given size of the module where only standard cell and hard macro areas are considered; floorplan constraints, such as placement blockages, are not considered. This value is calculated by the standard cells area plus the hard macros area, divided by the module area. The initial TU values are calculated during design import.



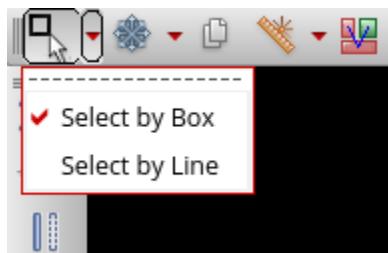
18. Click the **Select** icon.



What is the binding key that you can use instead? (The binding key is associated with the selectMode action in the Binding Key form.)

Answer: _____

Notice that the select icon has a pull-down list next to it which lets you choose the way in which you want to select single or multiple objects. You can select objects by drawing a box around objects or by drawing a line through objects.



19. To create placement blockage, click the corresponding icon. Click the **left** mouse button to create the blockage.



Make sure that the blockage that you create does not overlap a module.

20. Select the placement blockage that you created by clicking the **Select** icon. To view the properties, press **q**.

What type of placement blockage is it?

Answer: _____

21. Close the Attribute Editor.

22. To determine the difference among hard, soft, and partial, and macro-only, see the Innovus documentation.

Relative Floorplanning

In this section, you use the Relative Floorplan tool to place blocks in the core area.

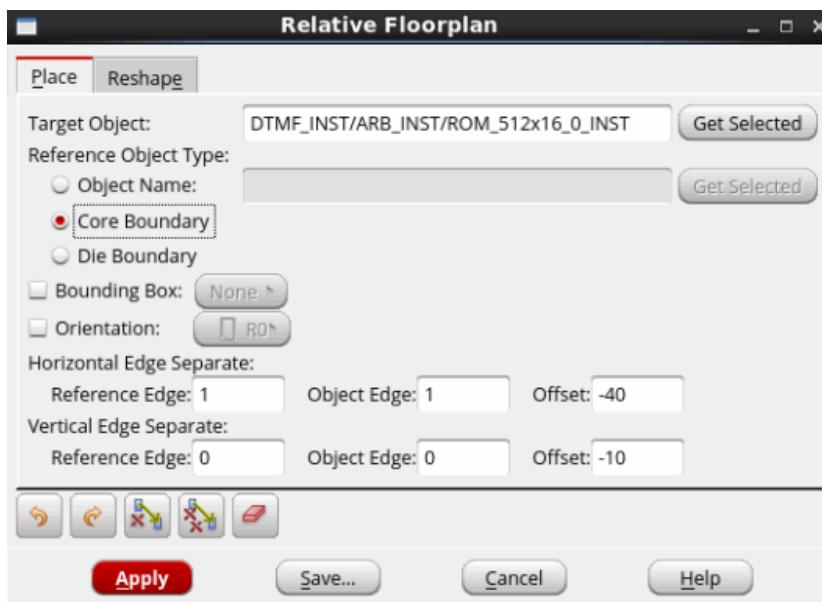
1. Clear the floorplan by selecting **Clear Floorplan** from the **Floorplan** menu and choosing **All Floorplan Objects**.
2. In the **All Colors** pane make sure that **Pin Shapes** visibility is selected.



3. Place an object relative to the core boundary by selecting **Floorplan-Relative Floorplan-Edit Constraint**.

This will bring up the Relative Floorplan form.

Routing Power with Special Route



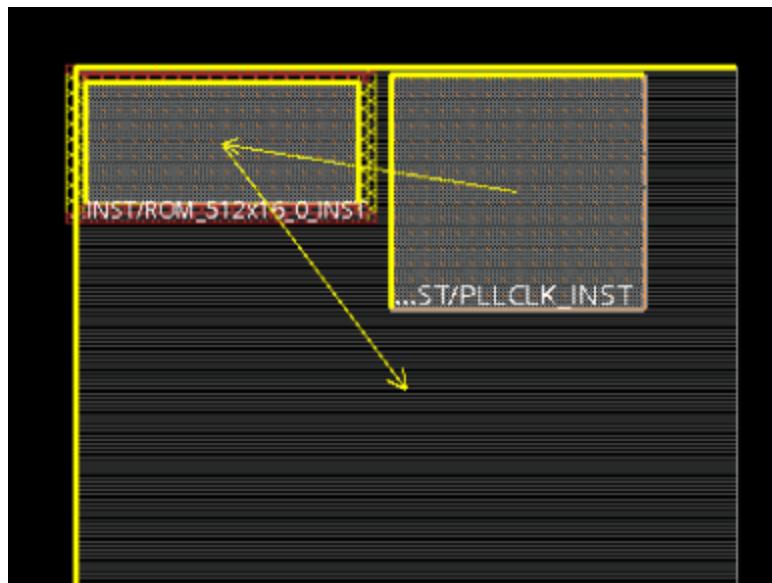
4. For the Target Object, enter **DTMF_INST/ARB_INST/ROM_512x16_0_INST**.
5. Select **Core Boundary** for the Reference Object Type.
6. For the Horizontal Edge Separate parameters, enter **1** for Reference Edge, **1** for Object Edge and **-40** for Offset.
7. For the Vertical Edge Separate, enter **0** for Reference Edge, **0** for Object Edge and **-10** for Offset.

The equivalent command is:

```
create_relative_floorplan -place DTMF_INST/ARB_INST/ROM_512x16_0_INST \
-ref_type core_boundary \
-horizontal_edge_separate {1 -40 1} \
-vertical_edge_separate {0 -10 0}
```

8. To place the *DTMF_INST/PLLCLK_INST* block relative to the previously placed block, enter the following command:

```
create_relative_floorplan -place DTMF_INST/PLLCLK_INST \
-ref_type object \
-ref DTMF_INST/ARB_INST/ROM_512x16_0_INST \
-horizontal_edge_separate {1 10 1} \
-vertical_edge_separate {2 40 0}
```



9. Delete the floorplanning constraints between the core boundary and the ROM by entering:

```
delete_relative_floorplan DTMF_INST/ARB_INST/ROM_512x16_0_INST
```

10. Click the **move** icon and move the ROM to a different location in the core area.



11. Notice that the PLL moves along with the ROM because its relative floorplanning constraints with the ROM remain even though the constraints between the ROM and core boundary have been deleted as a result of the *delete_relative_floorplan* command.

12. Press the **Select** icon or **a** key on the keyboard.



Automatic Floorplanning Synthesis for Block Placement

You can place the blocks in your design before placing the standard cells by running automatic floorplan synthesis. This Automatic Floorplan Synthesis feature is recommended for designs that have greater than 50 macros and using it for this lab, which contains only four macros, is for demonstration purposes only.

1. To undo the floorplanning that you have finished in this lab, choose **Clear Floorplan** in the detached menu.
2. Select **All Floorplan Objects**. Click **OK**.
3. In the Floorplan menu, select **Automatic Floorplan – Plan Design**.

4. Click the **Set Plan Design Mode** tab.

5. Click **Medium** under Effort Control.

6. Select **Keep Guide**.

7. Click **Apply**.

Notice that hard macros as well as the guides (modules) they belong to have been placed.

8. Now, select **High** and **Use Guide Boundary**.

9. Click **OK**.

10. Notice the placement of the macros with this combination of options.

Typically, you run block placement with various combinations of options to arrive at a desired placement to save and use as the starting point for the next implementation steps.

The blocks (hard macros) and the guides that contain the blocks are placed in the core area automatically. The guides that do not contain hard macros remain outside the core area.

Guides can overlap each other as they are not constrained by their boundaries and shapes.

11. Select **Floorplan-Clear Floorplan** and clear all the floorplan objects and block placements.

Adding a Block Halo

1. Load a floorplan by selecting **File – Load – Floorplan**.

This will bring up the Load FPlan File form.

2. Navigate and select the **dtmpf_blocks.fp** file.

3. Click **OK**.

In the physical layout of the blocks, halos had been added. You will be modifying the size of one of the block halos.

4. Measure the halo around the PLL block with the ruler.

What is the size of the halo on all sides?

Answer: _____

5. Select the **PLL block**. The instance name of the PLL block is DTMF_INST/PLLCLK_INST.

If it is too close to another macro or the edge of the core area, move it to a different location so that there is enough space around it to add a halo.

6. To add or modify a placement blockage around the block:

- a. Choose **Edit Floorplan – Edit Halo**.



- b. Select **Placement Halo**.

- c. Click **Selected Blocks/Pad**.

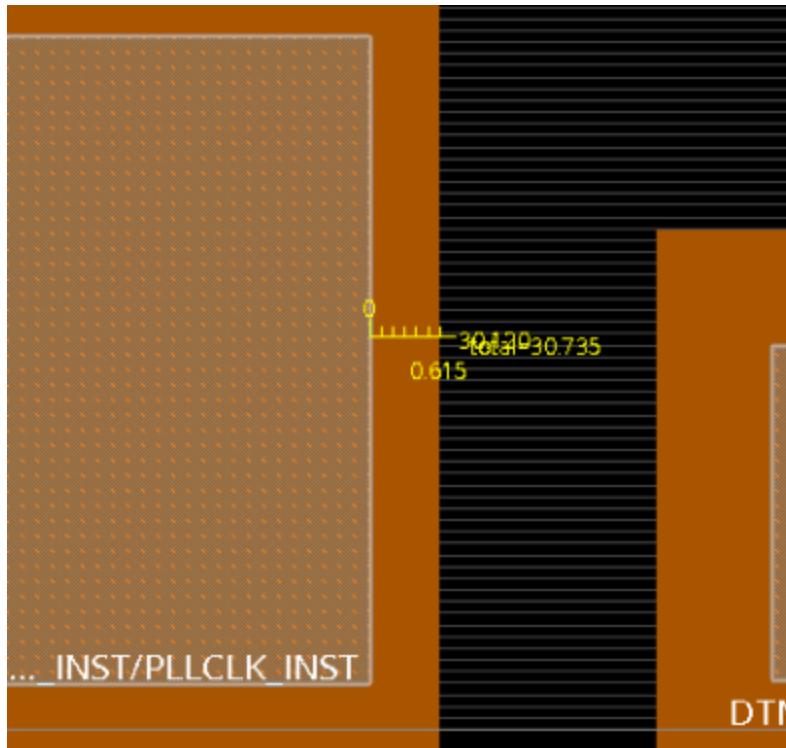
- d. For top, bottom, left, and right dimensions of the halo, enter **30 μ m**.

- e. Click **OK**.

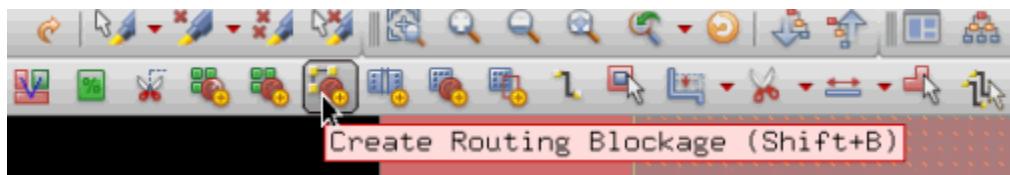
7. Redraw the view by pressing **Control-R**.

8. Measure the halo by zooming in to the area where the block is placed and by using the ruler.

Routing Power with Special Route



9. To create a routing blockage, click the corresponding icon with the left mouse button to create the blockage in a corner of the core area.



Routing blockages are added to the design to alleviate areas of possible routing congestion.

10. Select the created routing blockage. To view the properties, press **q**.

The layer that is selected is the blocked layer.

Which layer is blocked?

Answer: _____

11. Close the Attribute Editor form.

12. To save the floorplan in the FP format, choose **File – Save – Floorplan**. For the filename, enter **dtmp_fp.fp**.

13. Click **Save**.

14. View the saved floorplan file.

```
#####
# <RouteBlockages>
#   <Blockage name="blk_name" type="User|RouteGuide|PtnCut|WideWire">
#     <Attr spacing=1.2 drw=1.2 inst="name" pushdown=yes fills=yes />
#     <Layer type="route|cut|masterslice" id=layerNo />
#     <Box llx=1 lly=2 urx=3 ury=4 /> ...
#     <Poly points=nr x0=1 y0=1 x1=2 y2=2 ... />
#   </Blockage>
# </RouteBlockages>
#####
<RouteBlockages>
  <Blockage type="User">
    <Layer type="route" id=3 />
    <Box llx=355.5400 lly=629.0200 urx=381.1800 ury=649.7600 />
  </Blockage>
</RouteBlockages>
```

15. Notice that the routing blockage is saved as the RouteBlockages attribute.

16. Create a placement blockage in any area of the core.



A partial placement blockage can alleviate congestion by spreading components farther apart during placement.

17. To view its properties, select the **blockage**. Press **q**.

18. Change the Type cyclic field from Hard to **Partial**.

19. In the cyclic field, change the placement percentage to **25%**.

20. Click **OK**.

21. Close the Innovus platform.

Routing Power with Special Route

Power Planning

1. Start the Innovus platform by entering:

innovus

2. Choose **File – Import Design**.

3. Load the *dtnf.globals* file.

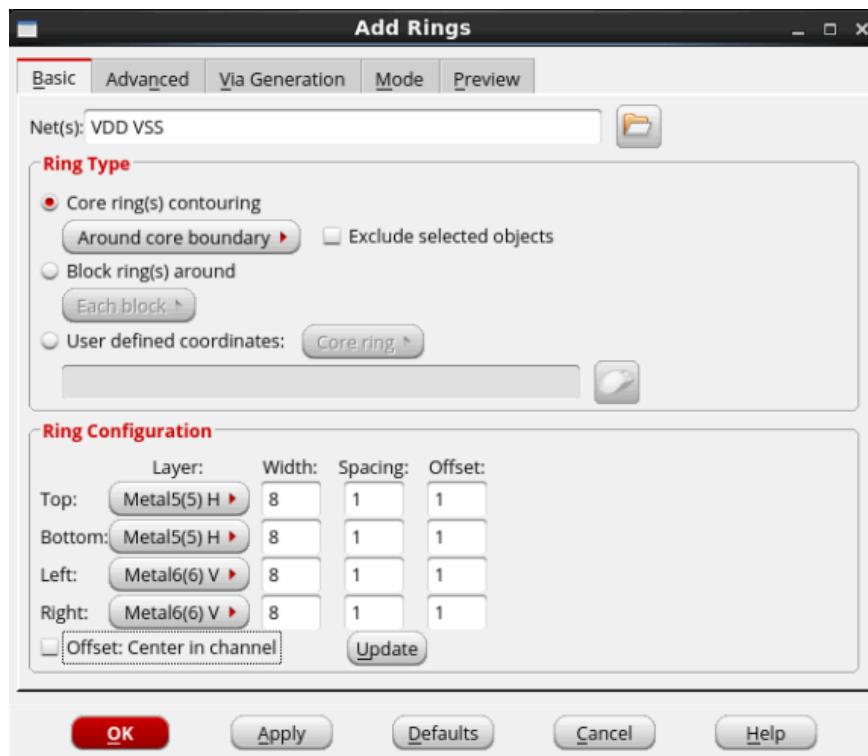
4. Click **OK**.

5. Load a floorplan by choosing **File – Load – Floorplan**.

6. Enter **dtnf_blocks.fp** for the filename.

7. Choose **Power-Power Planning – Add Ring**.

The Add Rings form is displayed.



8. To select the VDD and VSS nets, click the folder icon in the **Net(s)** field.

The Net Selection form is displayed.

9. In the Possible Nets pane, press **Shift** and **VDD** and **VSS**.

10. Click **Add**.

The selected nets appear in the Chosen Nets pane.

11. Click **OK**.

12. Make sure that the Net(s) field contains VDD and VSS.

13. Click **Core ring(s) contouring**.

14. Select **Around core boundary**.

15. In the Ring Configuration field, make sure that **METAL5(5) H** layer is selected for Top and Bottom.

16. Make sure that a width of **8** and a spacing of **1** are set.

17. Use **METAL6(6) V** as the layer for left and right. Select a width of **8** and a spacing of **1**.

18. Under Offset, in all the fields, enter **1**.

19. To generate the power rings, click **Apply**.

20. Next, you create the rings for the PLL block. It is the only block that does not have a self-contained ring.

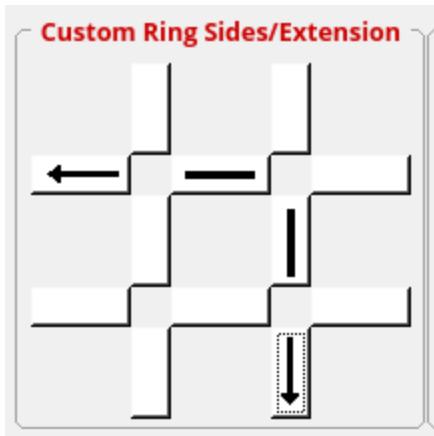
21. In the design window, select the **PLL block**.

22. In the same form, in the Ring Type section, select **Block ring(s) around**.

23. Select **Each selected block and/or group of core rows**.

24. Click the **Advanced** tab.

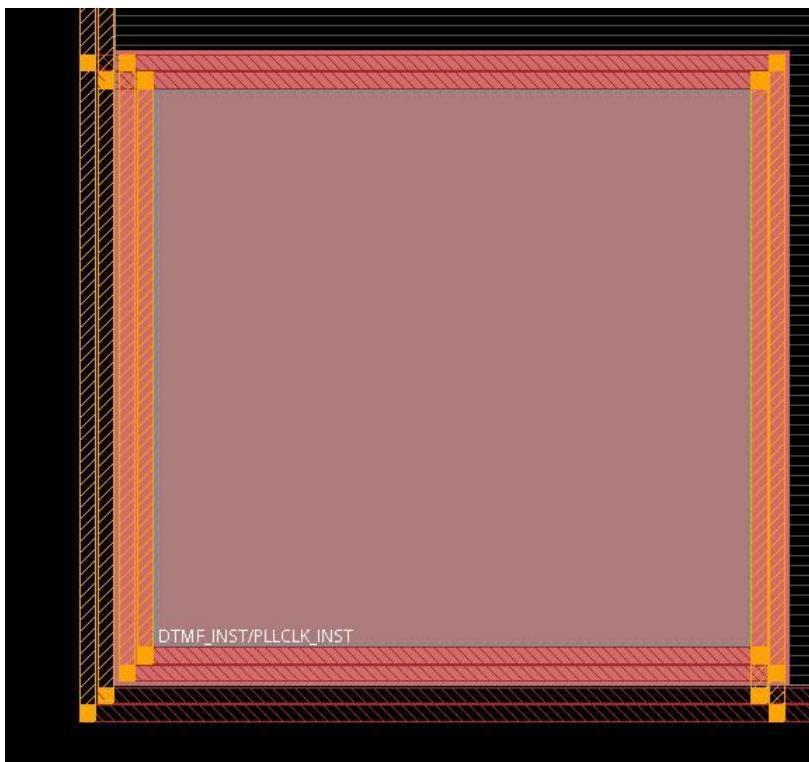
Routing Power with Special Route



25. Configure the segments, as shown above, so that the power rings around the PLL use the edges of the core rings.

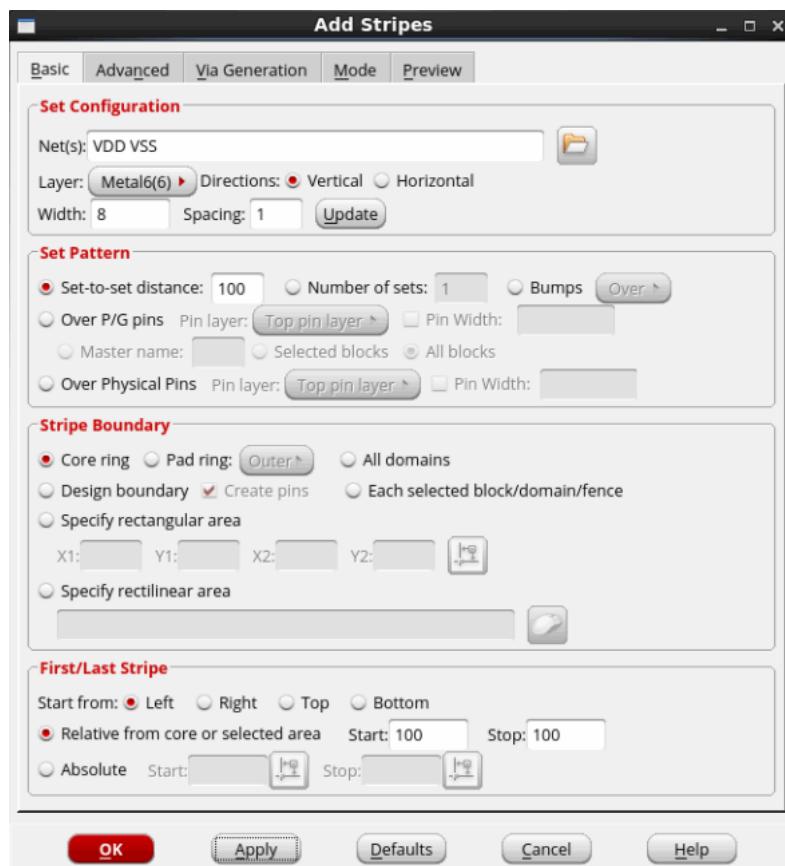
26. Maintaining all other default settings, click **OK**.

27. The following is the snapshot of the PLL.



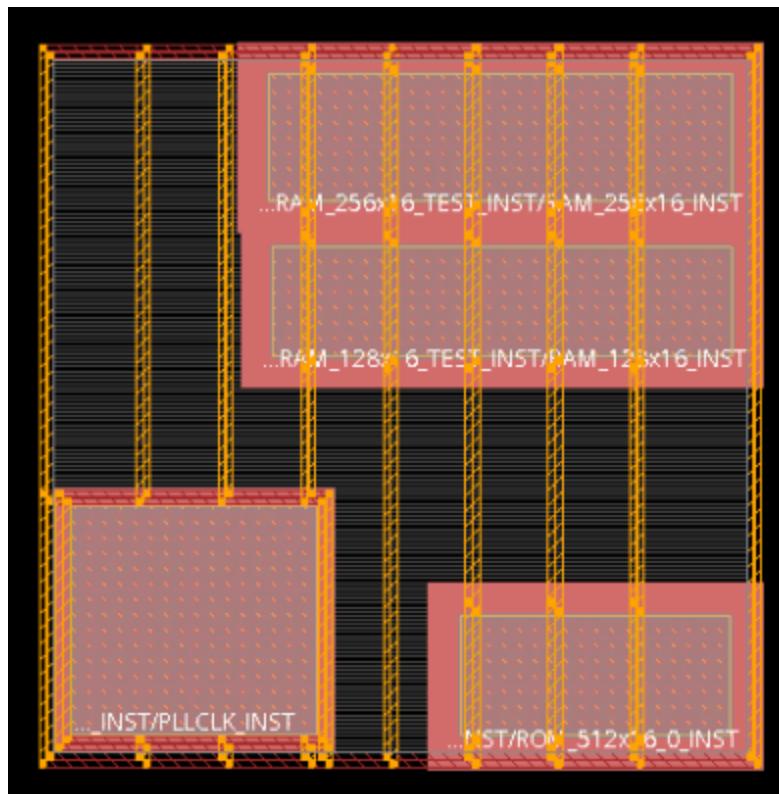
28. Choose **Power-Power Planning – Add Stripe**.

The Add Stripes form appears.



- a. Make sure that the Net(s) field contains **VDD** and **VSS**.
- b. In the cyclic field, select **Metal6**.
- c. Select **Vertical**, if it is not already selected.
- d. Set Width to **8**.
- e. Set Spacing to **1**.
- f. Set Set-to-set distance to **100**.
- g. For the Relative from core or selected area, value, enter **100** for both **Start** and **Stop**.
- h. Click **OK**.
- i. Notice the power stripes and the vias connecting the rings to the stripes are created.

Routing Power with Special Route



Replacing a Cell with the Design Browser

1. Detach the Tools menu.
2. Select **Design Browser** in the Tools menu.
3. In the Find field, enter the instance name:
`DTMF_INST/DIGIT_REG_INST/digit_out_reg_3`
4. Press **Enter**.

A standard cell of cell type *SDFFSHQX1* is displayed



5. In the Design Browser form, select the instance. To open the Attribute form for the instance, click the **Attribute Editor** icon.



The Attribute Editor for this instance is displayed.



6. Perform the following steps:

a. In the Attribute Editor in the Location section, click the **mouse** icon.

b. Move the mouse pointer in the core design area.

The pointer changes to a crosshair.

c. Click a point in the core area of the design to preplace the instance.

In the form, the coordinates in the Location field are populated by the coordinates where you click.

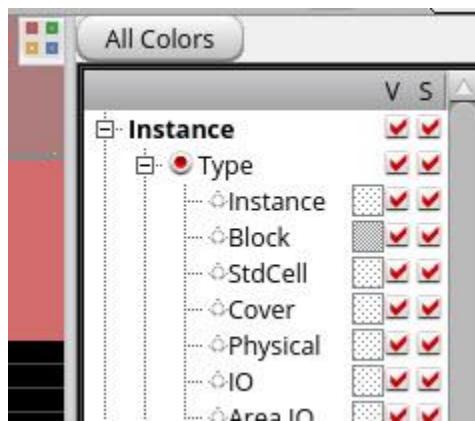
d. In the Attribute Editor, change the Status field to **Placed**. Click **OK**.

e. Select **Physical View**, if it is not already the current view.



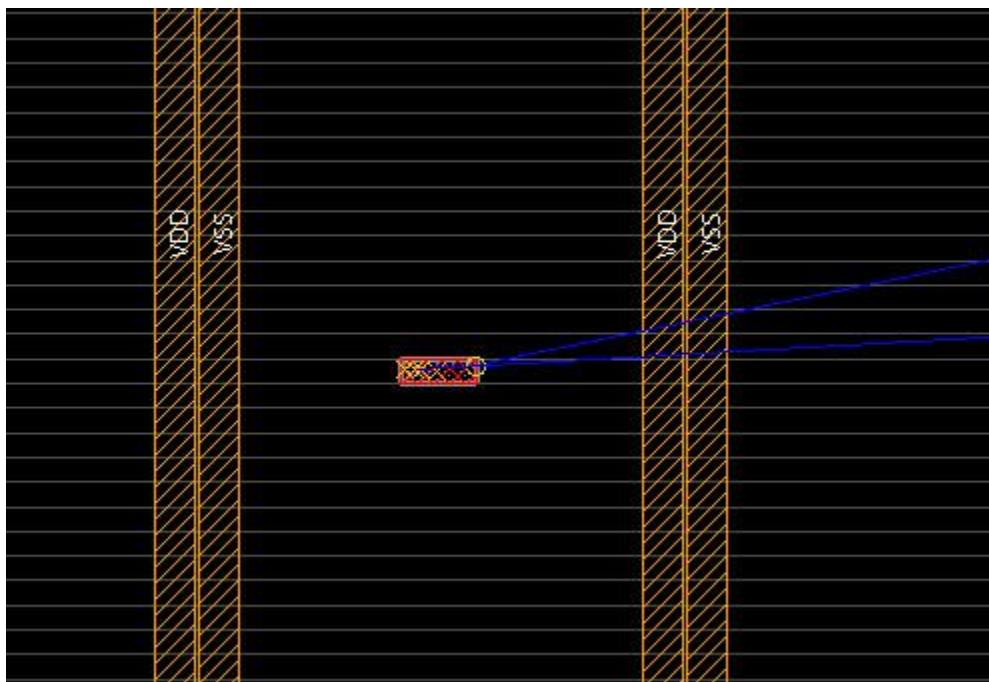
Routing Power with Special Route

- f. If you cannot see the standard cell, under the All Colors menu, set **Instance** and **StdCell** visibility.



Can you see the preplaced standard cell in your physical view?

Answer: _____



7. Close the Design Browser.

Note: You can use this method to preplace a module, block or standard cell with the Design Browser.

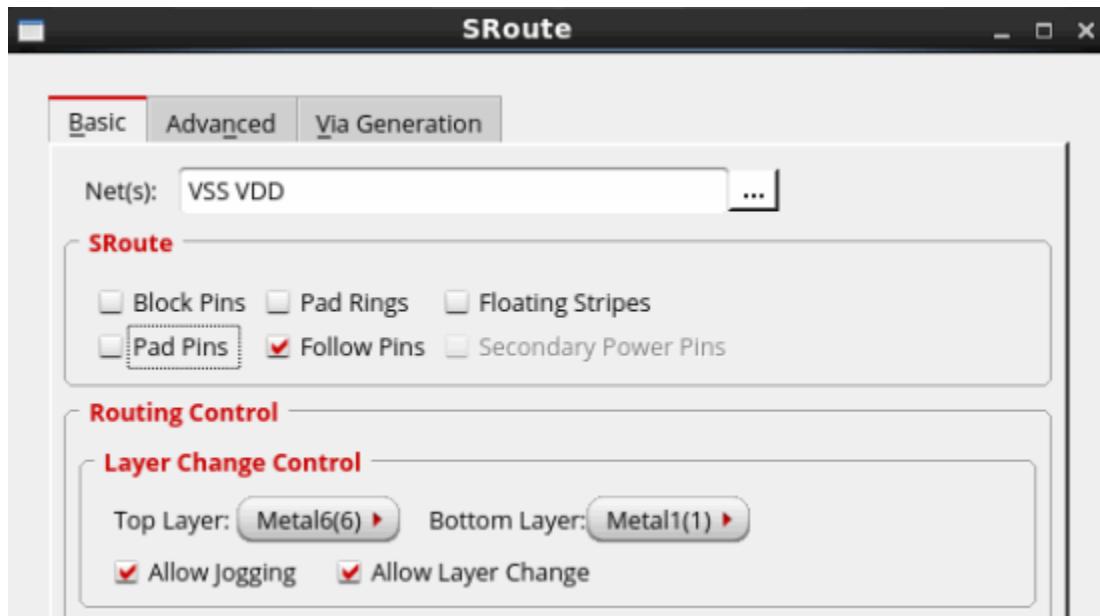
Creating Power Rails (Followpin Routing) with Special Route

1. Before creating followpin routing (also known as power rails), associate the global VDD and VSS nets names to the standard cell pin names by entering the following commands:

```
globalNetConnect VDD -type pgpin -pin VDD -inst *
globalNetConnect VSS -type pgpin -pin VSS -inst *
```

2. Choose **Route – Special Route**.

The SRoute form appears.

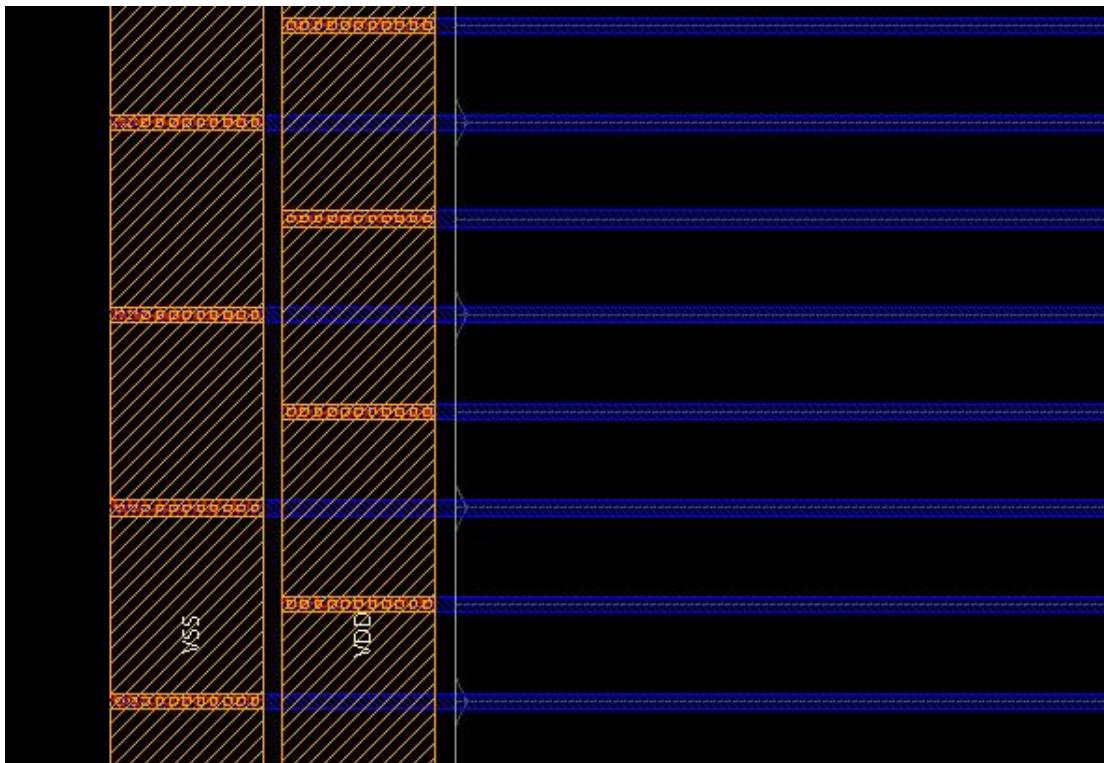


3. To populate the field with VDD and VSS, click the icon next to the **Net(s)** field. 
4. Click **Add** to add the nets to the Chosen Nets field and click **OK**.
5. Deselect all options except Follow Pins.
6. For Layer Change Control, select **Metal 6** for Top Layer and **Metal 1** for Bottom Layer.
7. Make sure that **Allow Jogging** and **Allow Layer Change** are selected.
8. Click **OK**.

The power router takes a few minutes to finish.

Routing Power with Special Route

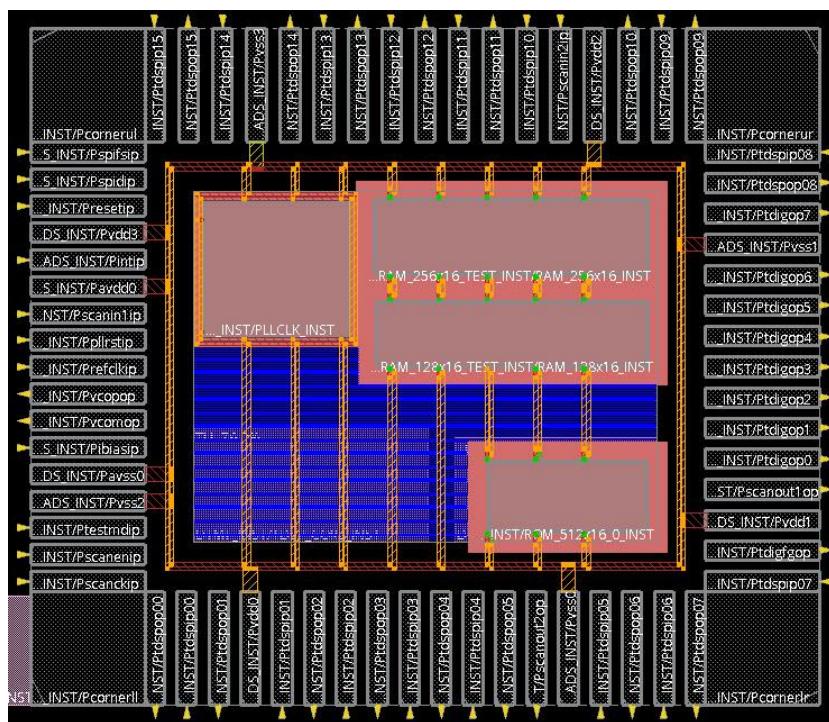
9. In the Physical view, zoom in to the followpin routes.
10. Notice that the power routes have been connected to the power planned targets with relevant vias.



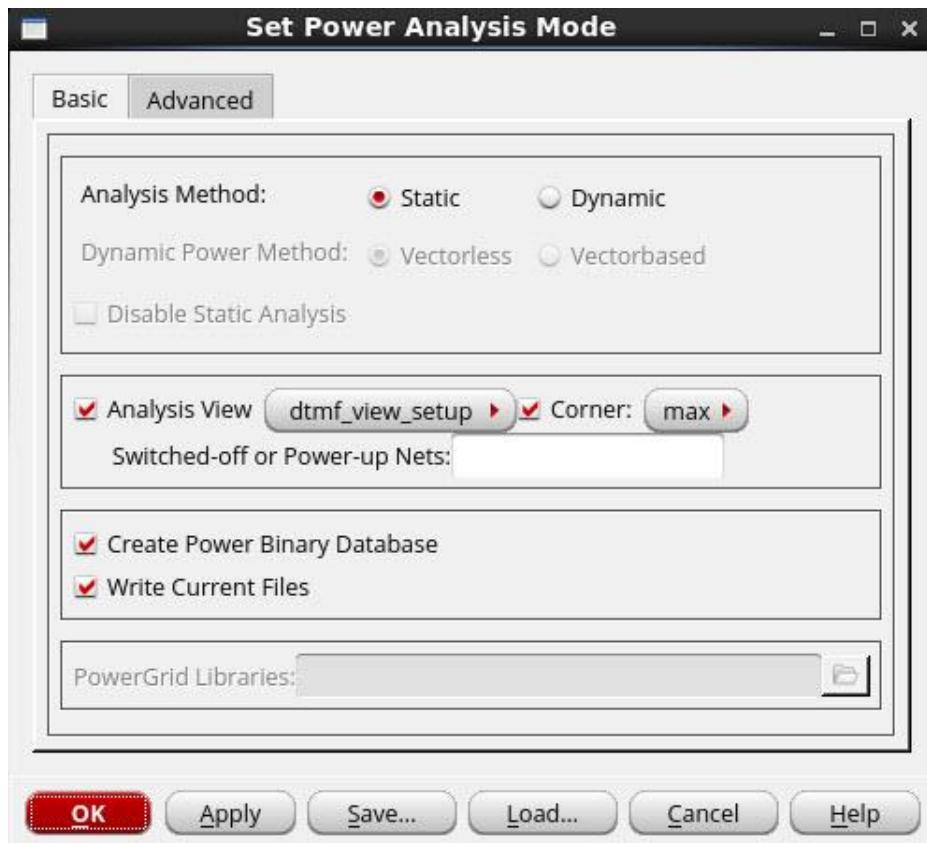
11. Exit the Innovus tool.

Running Early Rail Analysis

1. Start the Innovus tool.
2. Select **File – Import Design** and load in the *dtmpf.globals* file.
3. Select **File – Load – Floorplan**.
4. Select **dtmpf_power.fp**.
5. Click **Open**.

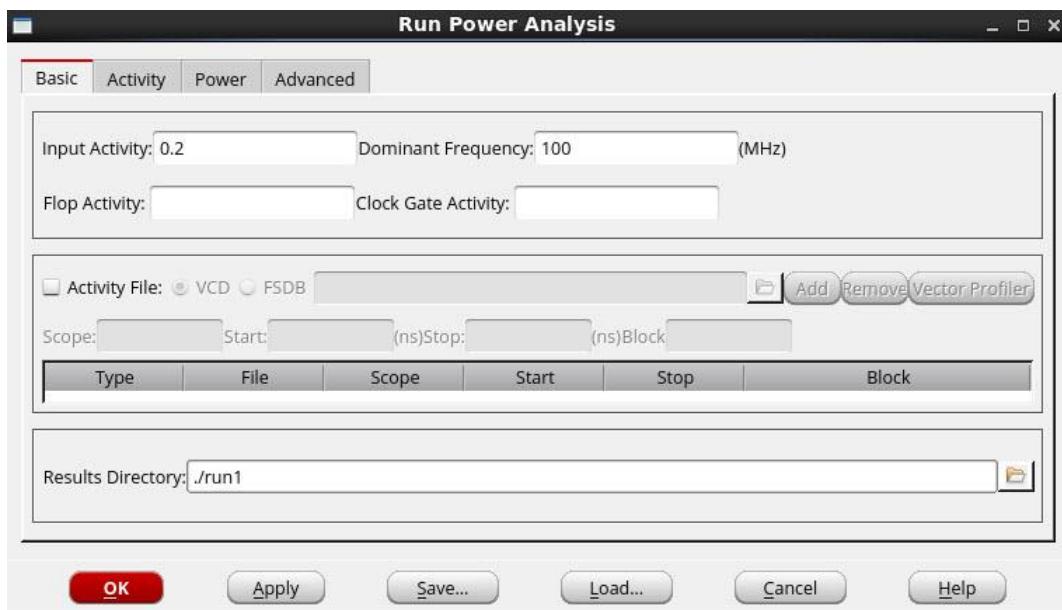


6. To display the form, choose **Power – Power Analysis – Setup**.



Routing Power with Special Route

7. In the Analysis Method, select **Static**.
8. Select **Analysis View**.
9. Select **dtmf_view_setup**
10. Select **max** for the corner.
11. Click **OK**.
12. To run power analysis, select **Power – Power Analysis – Run**.



13. Leaving all defaults as-is, enter **./run1** in the **Results Directory** field.

14. Click **OK**.

This will run power analysis and generate power consumption values.

15. From the log file for this session, determine the following:

What is the total internal power?

Answer: _____

What is the total switching power?

Answer: _____

What is the leakage power?

Answer: _____

What is the total power consumed?

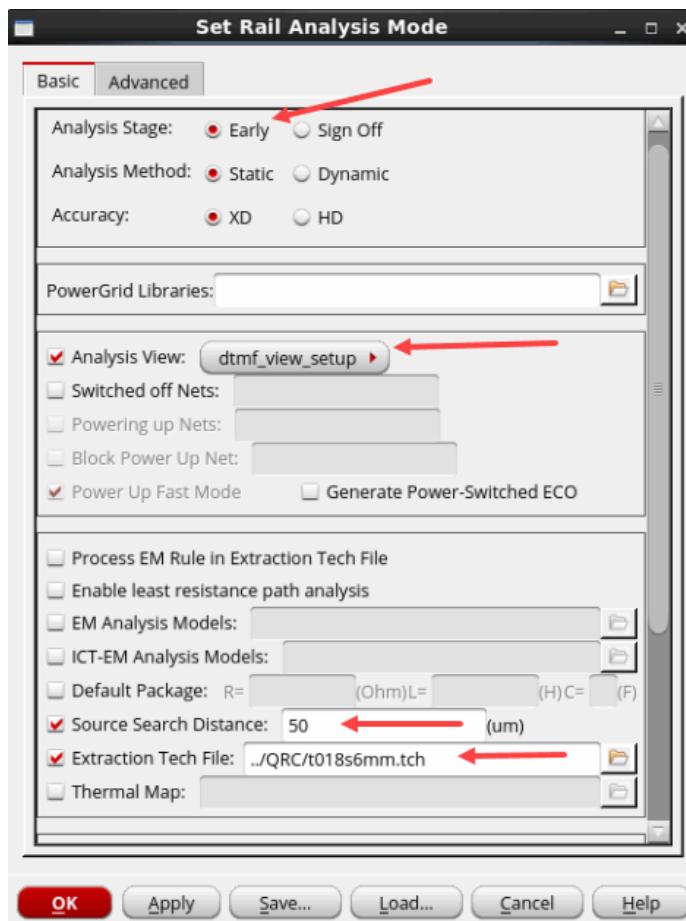
Answer: _____

16. Source the *power.tcl* file which contains the rules for global net power connections by entering the following:

```
source power.tcl
```

Setting Up Rail Analysis

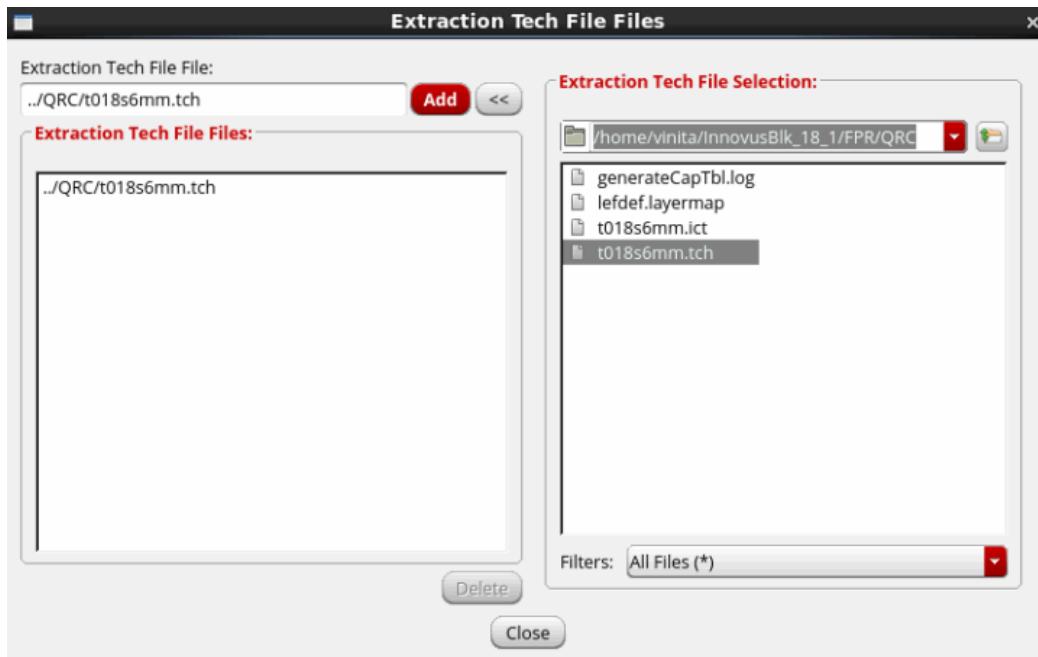
1. To run rail analysis, first, select **Power – Rail Analysis – Setup Rail Analysis**.



This will bring up the Set Rail Analysis Mode form.

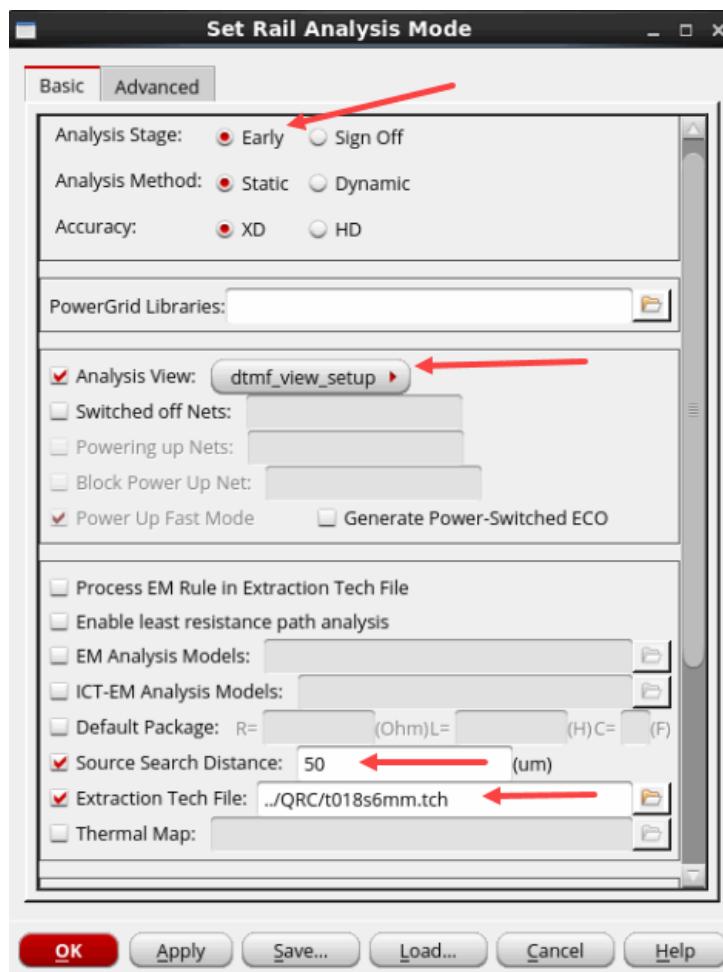
2. Select **Early** for Analysis Stage.
3. Select **Analysis View**.
4. Select **dtmf_view_setup** for worst case.

5. Select **Extraction Tech File**.
6. Click the folder icon to navigate the QRC tech file, as shown.



7. Select **All Files** to allow all files to be selectable.
8. Double-click the **t018s6mm.tch** file so that it is visible in the left hand pane.
9. Close the file navigation form.

10. Make sure that the Set Rail Analysis Mode form is filled in, as shown.

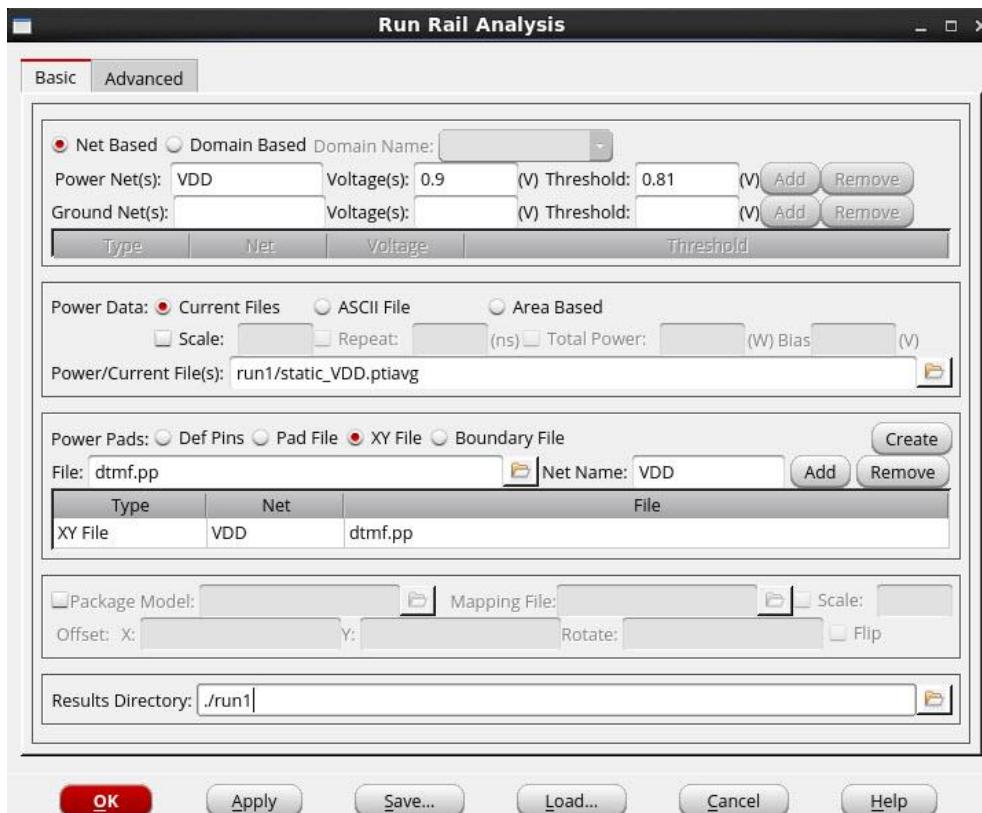


11. Click **OK**.

12. Select **Power – Rail Analysis – Run Rail Analysis**.

This will bring up the Run Rail Analysis form.

Routing Power with Special Route



13. Select **Net Based**.

14. Enter **VDD** for the Power Net.

15. Enter **0.9** in the Voltage(s) field.

16. Enter **0.81** in the Threshold field.

17. Delete **VSS** if it is in the Ground Net field.

18. Make sure that Current Files is selected.

19. For Power/Current Files, navigate to the *run1* directory, select the **static_VDD.ptiavg** file and double-click it.

20. Click **Close**.

21. To create an XY file for the power sources, select **XY File**.

22. Click **Create**.

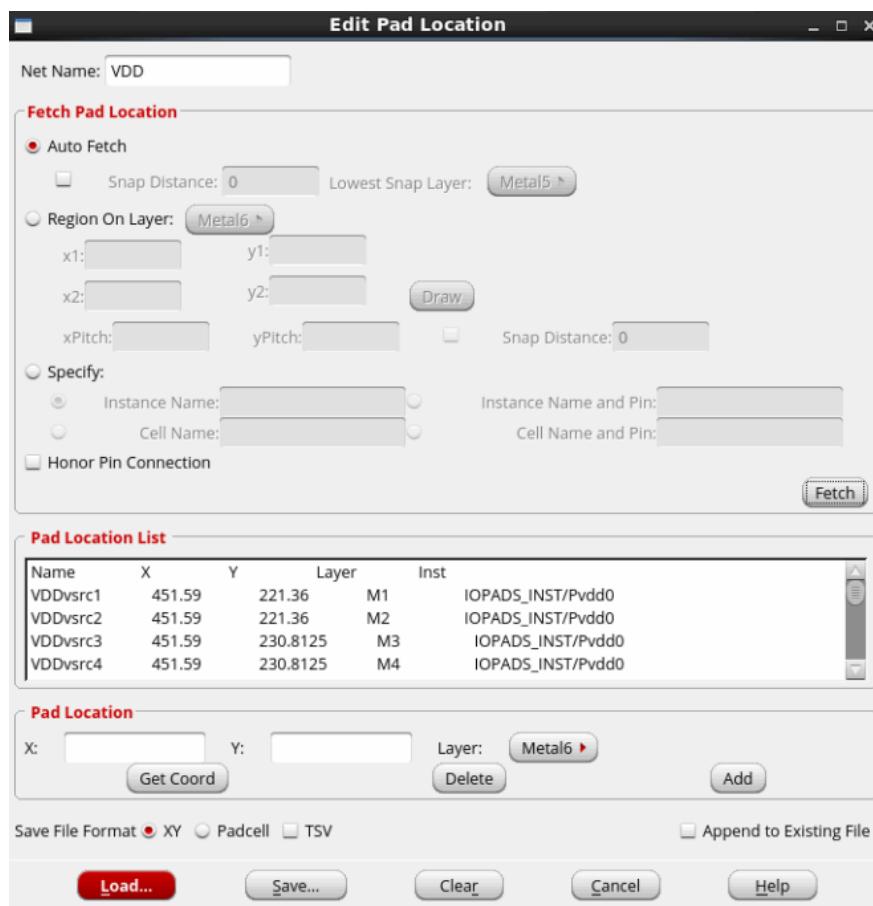
This will bring up the Edit Pad Location form

23. Enter **VDD** for the Net Name.

24. Make sure **Auto Fetch** is selected.

25. Click the **Fetch** button on the form.

26. Notice that the Pad Location List becomes populated.

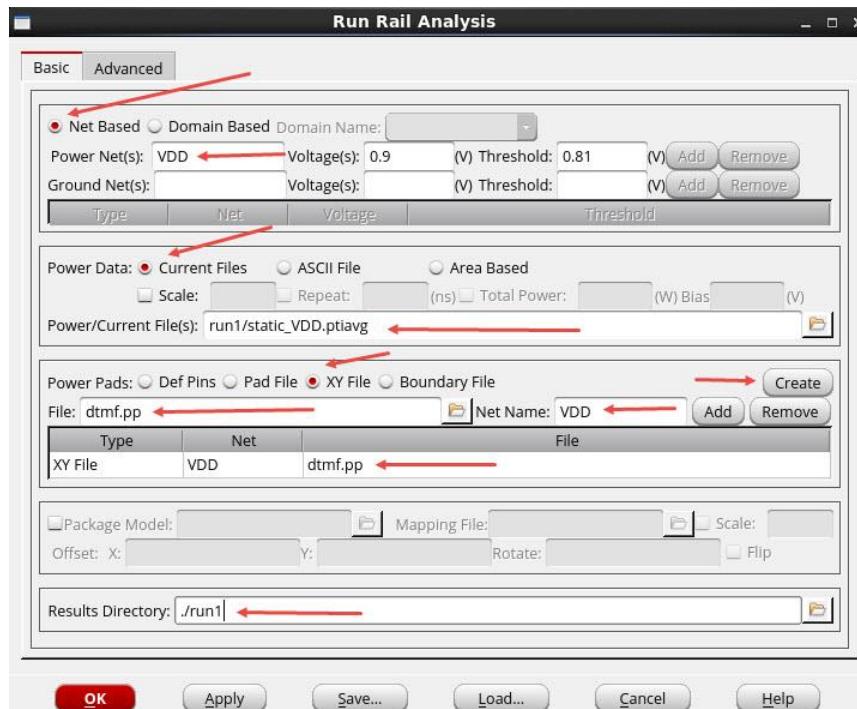


27. Click **Save**.

Routing Power with Special Route

Running Rail Analysis

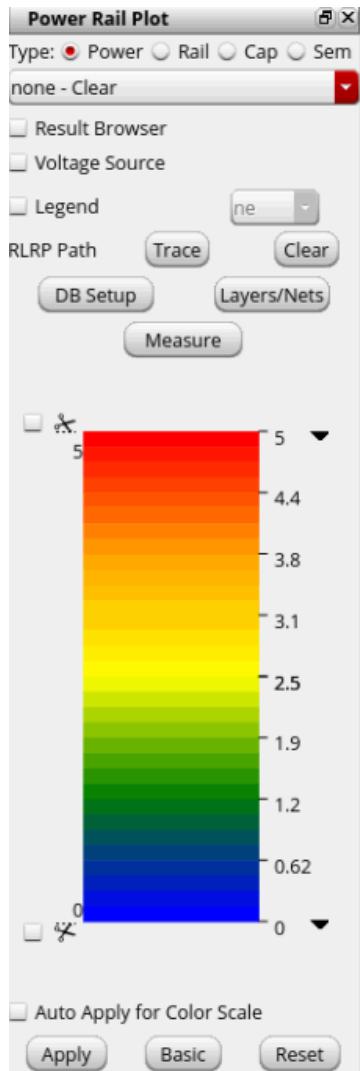
1. Enter **dtsmf.pp** for the filename.
2. Click **Save**.
3. Click **Cancel** the Edit Pad Location form.
4. In the Run Rail Analysis Form, specify the name of the XY file *dtsmf.pp* you just created in the File Field.
5. For the Net Name, specify **VDD**.
6. Click **Add** in the Run Rail Analysis form.
7. Make sure the form looks like the following screenshot.



8. Click **OK** to run rail analysis.

Viewing Rail Analysis Results

1. To display the results of rail analysis, select **Power – Report – Power & Rail Result**.
2. Notice that the pane on the left of the design window contains options to run analysis.



3. Select **Rail**.
4. Select **DB Setup**.

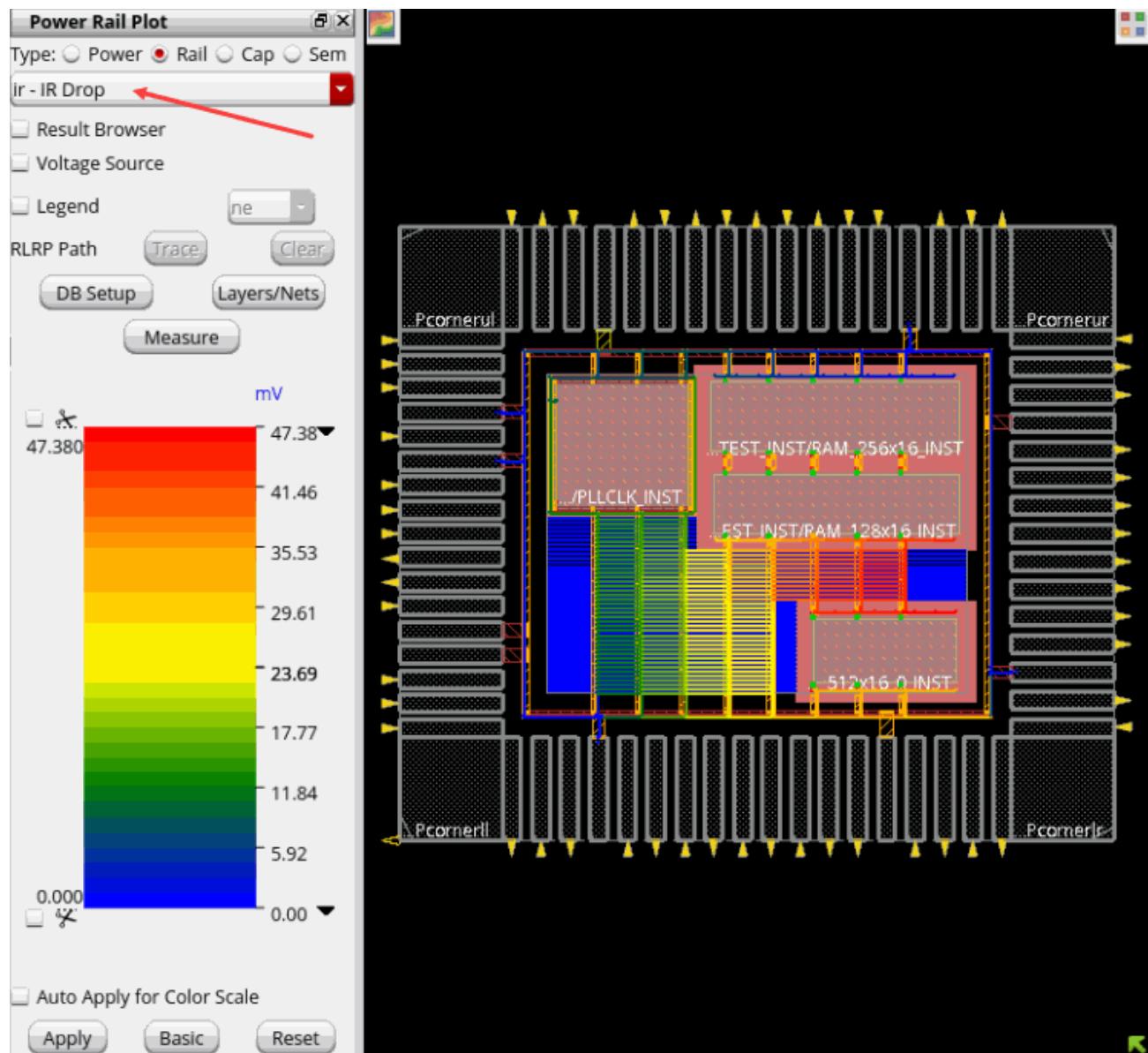
This will bring up the Power and Rail Setup form.

Routing Power with Special Route



5. Navigate and populate the Power Database field with *run1/power.db*.
6. In the Rail Database field, populate the field with the path to the directory *run1/VDD_25C_avg_** where * indicates a number which increments every time you rerun the step. For example, this directory name might be *run1/VDD_25C_avg_1*.
7. Click **OK**.
8. Select **ir – IR Drop** from the pick list.

Notice that the Innovus design window display shows the color coded voltage ranges that match the range.



Are there any red areas displayed in the main Innovus window in your lab?

Answer: _____

Saving the Session

1. To save the session, choose **File – Save Design**.
2. Select **Innovus**.

3. Enter this filename:

floorplan.inn

4. Click **OK**.

5. Close the session.

Summary

In this lab, you

- ◆ Read in a gate-level netlist
- ◆ Floorplanned the design
- ◆ Experimented with the Tools menu



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Modules 8-9: No Labs

(C) Cadence Design Systems, Inc. Do not distribute.

Module 10: Analyzing Route Feasibility with the Early Global Router

(C) Cadence Design Systems, Inc. Do not distribute.

Lab 10-1 Running Placement

Objective: To read in a floorplan file, place the standard cells in the design and run post-placement optimization.

1. To start the Innovus™ Implementation System software, enter:

```
innovus
```

2. Choose **File – Import Design**. Load the *dtsf.globals* file.

3. To load a floorplan file:

- a. Choose **File – Load – Floorplan**.
- b. Select **dtsf.fp**.
- c. Click **Open**.
- d. Click **OK**.

4. Run the following command to view the settings for the placement mode:

```
getPlaceMode
```

5. Notice that the *-place_global_timing_effort* is set to *medium* by default and *-place_global_cong_effort* is set to *auto*.

If timing or congestion are challenging these modes can be tuned.

6. Load the scan DEF file by running the following command:

```
defIn scan_input.def
```

Alternatively, you can specify the two scan chains in the design by entering the following:

```
specifyScanChain scan1 \
    -start {IOPADS_INST/Pscanin1ip/C} \
    -stop {IOPADS_INST/Pscanout1op/I}

specifyScanChain scan2 \
    -start {IOPADS_INST/Pscanin2ip/C} \
    -stop {IOPADS_INST/Pscanout2op/I}
```

Note: Instead of entering the *specifyScanChain* commands, you can source the *scan.tcl* file in the work directory.

7. Run placement optimization by running the command:

```
place_opt_design
```

The command takes a few minutes to finish.

8. View the log file in a separate xterm window.

- a. In the logfile, search for *place_opt_design* to get to the placement optimization steps and then search for the strings *Begin* and *End*.

The *Begin* and *End* strings delimit the start and end of major placement steps.

- b. Find the *Begin Area Optimization* step.

- c. In the *Density* column under area optimization is the density increasing or remaining stable?

A stable density convergence is important for not encountering downstream congestion during routing.

9. Notice that the status of the design on the lower-right corner has changed.

After the placement optimization run completes, what is the status of the design that is displayed?

Answer: _____

This field is a convenient way to check where you are in the flow.

What is the Worst Negative Slack (WNS) at this stage?

Answer: _____

Is it a positive or a negative number?

Answer: _____

A positive number indicates the design has met the timing constraints specified in the *.sdc* file whereas a negative number indicates that the timing is not met.

10. In a separate xterm window, view the log file for this session.

11. To save the scan DEF files, enter the following:

```
defOutBySection -noNets -noComps -scanChains scan.def
```

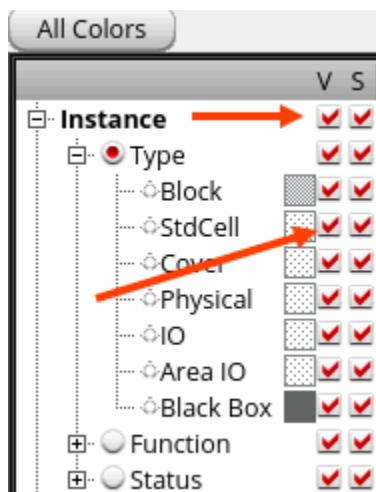
12. To display the Physical view, click the **Physical View** button.



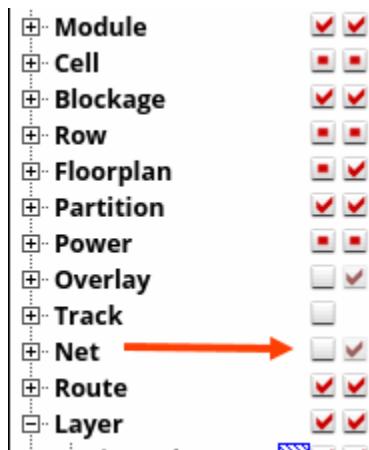
13. Display the scan chain **scan1**'s flightline connectivity by selecting **Place – Display – Scan Chain**.

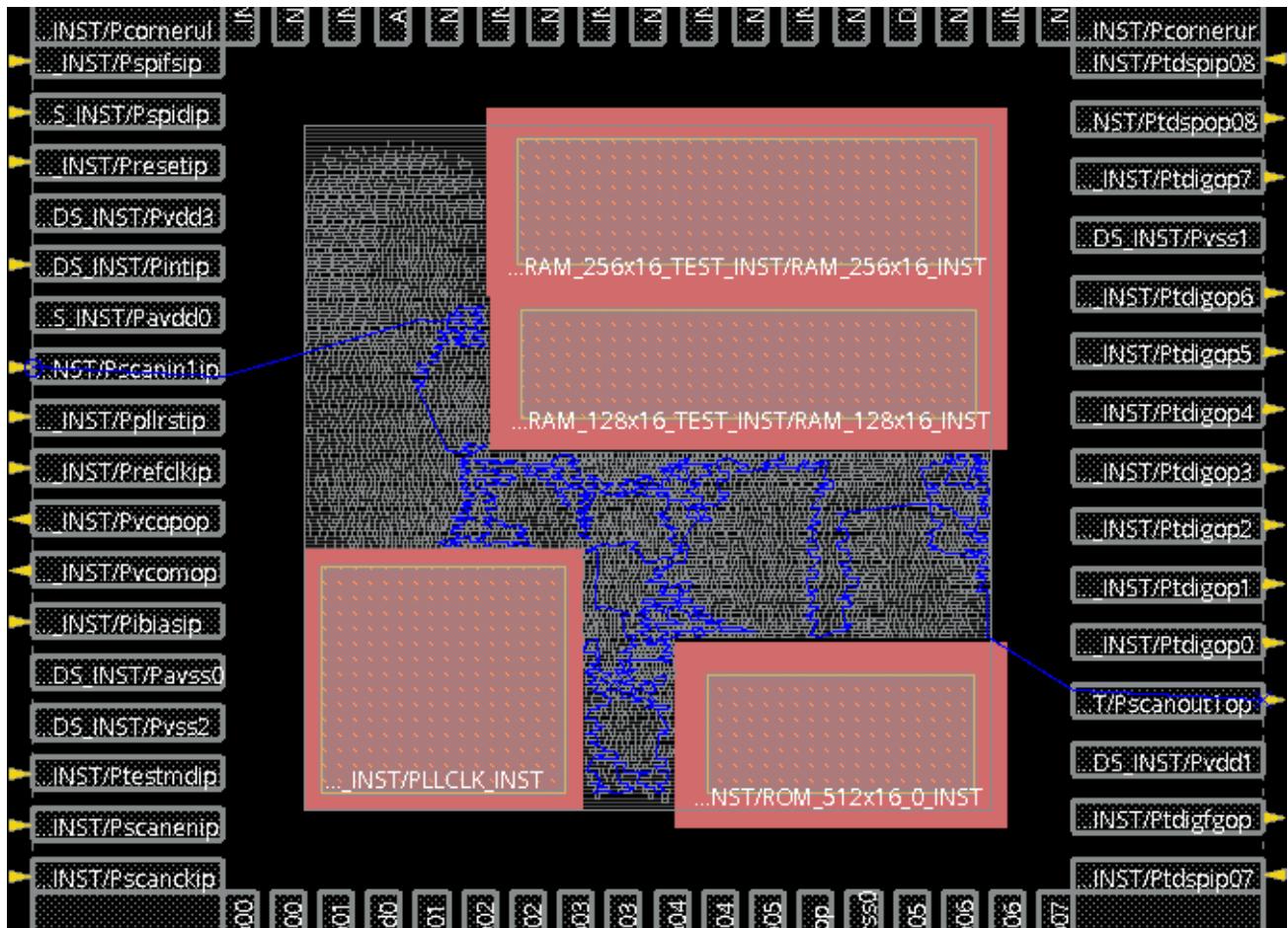
- a. Select **Selected Scan Group**.

- b. Enter **scan1** in the field.
 - c. Click **Display**.
14. Under All Colors, make sure that *Instance* and *StdCell* are set to **Visible**.

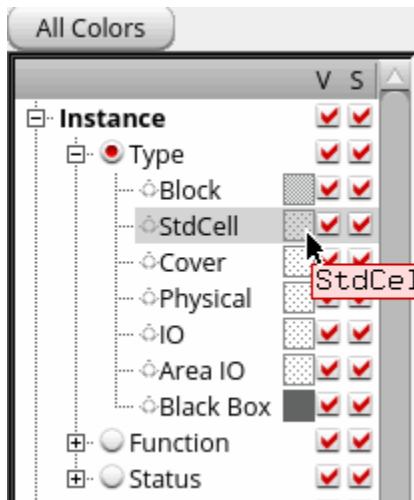


15. Under All Colors, make sure that **Net** visibility is not selected.





Alternatively, you can also select a different color for the standard cells so that you can see the scan chain clearly.



16. Clear the scan display of all the chains or of a specific chain.



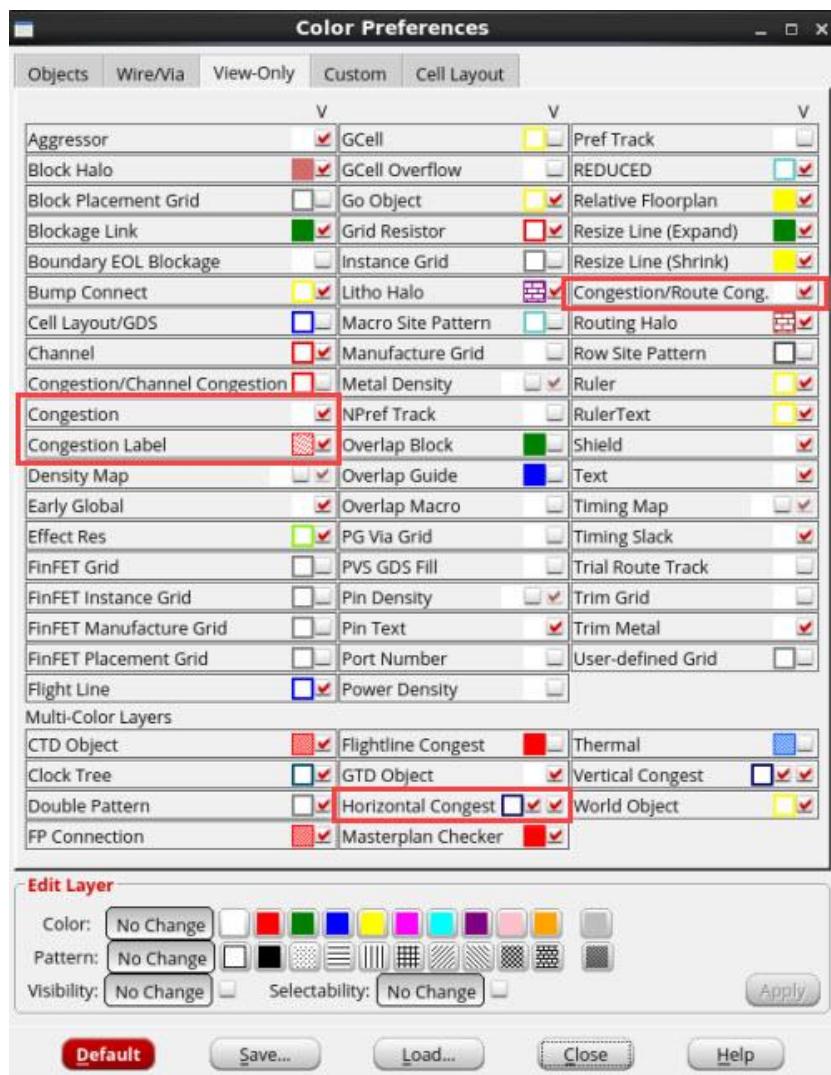
17. Click **Clear**.

18. Turn **Net** visibility back on.

19. Zoom in to see the standard cell placements.

20. Notice that in addition to cell placement, the Early Global Router has been run on the design.

21. Click the **All Colors** button.

22. Click the **View Only** tab.23. Select the **Vertical Congest**, **Horizontal Congest**, **Congestion**, **Congestion/Route Cong.**, and **Congestion Label** options, if they are not already selected.

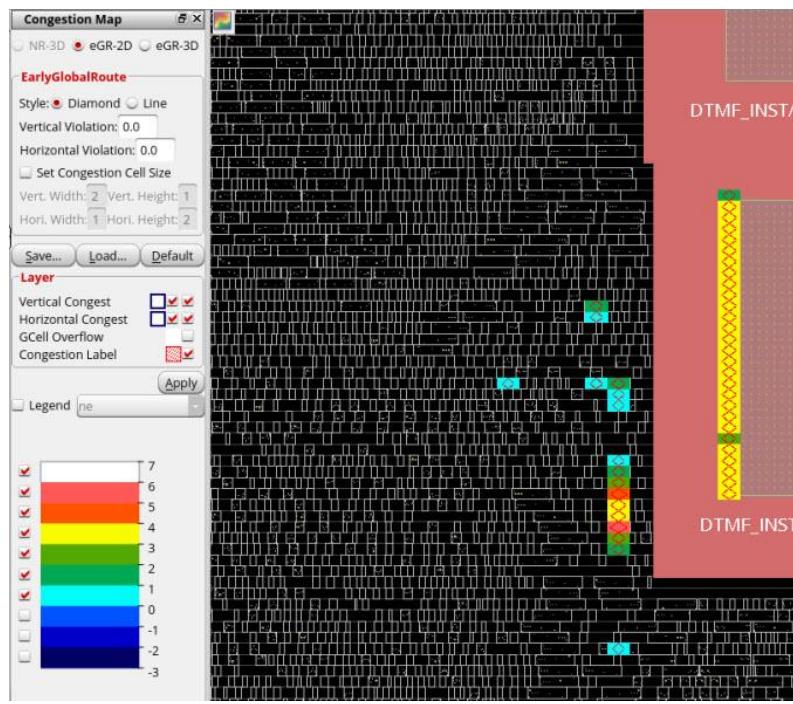
24. Turn off net visibility, if it is on.

25. Zoom in to areas where there are diamond shapes.

Is there any congestion in the vertical or in the horizontal direction?

Answer: _____

Note: Because this is a small design and not one that is hard to route, you may not see a lot of congestion markers.



26. To save the design, enter:

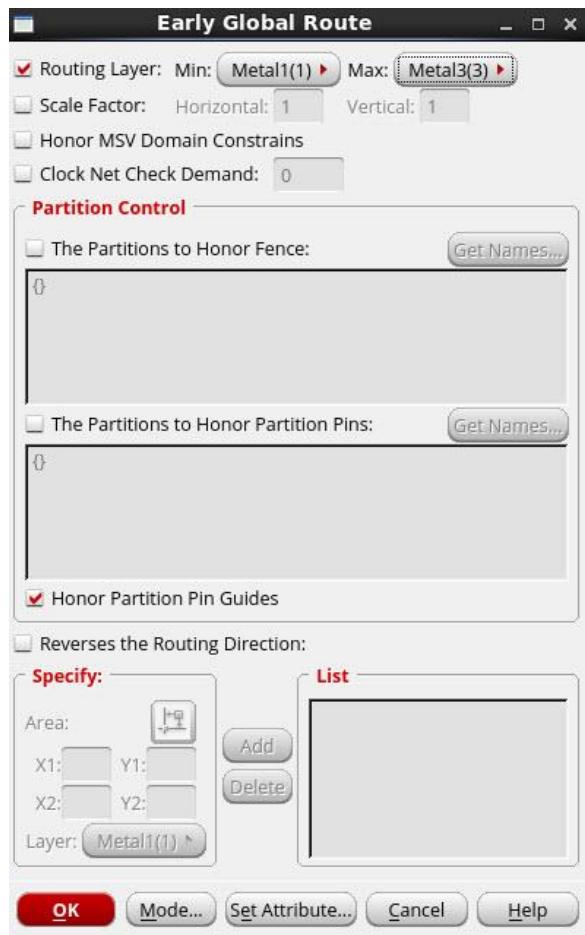
```
saveDesign placeOpt.inn
```



Lab 10-2 Running the Early Global Router

Objective: To restrict the layers for the Early Global Router and to analyze routing congestion.

1. Select **Route – Early Global Route** to bring up the form.



2. Select **Routing Layer**.
3. Set **Min:** to **Metal1(1)** and **Max:** to **Metal3(3)**.

The command to set route layers is:

```
setRouteMode -earlyGlobalMaxRouteLayer 3 -earlyGlobalMinRouteLayer 1
```

4. Click **OK**.

This will run Early Global Route.

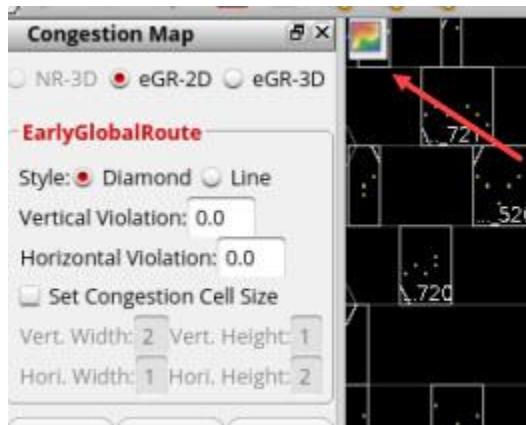
The equivalent command to run Early Global Route is:

```
earlyGlobalRoute
```

5. Refresh the design window by clicking the **redraw** icon for the Physical view.



6. The Congestion Map display pane can be displayed or minimized by clicking the icon.



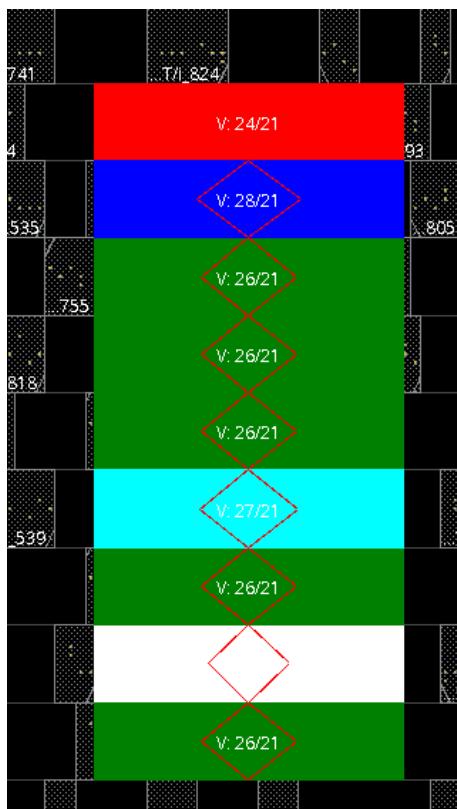
The pane on the left labeled Congestion Map lets you select the display to be either Diamond style or Line style.



7. Alternately click **Line** and **Diamond** followed by **Apply**.
8. The colors associated with the diamond shapes and lines are shown in the legend which maps the colors to the number showing the difference between available and required tracks for routing.
9. Also displayed are horizontal or vertical congestion with numbers: $V = \# / \#$ or $H = \# / \#$. Without zooming in, the congestion numbers might be difficult to see.

The V and H apply to vertical and horizontal routing tracks. The first number indicates the required tracks; the second number indicates the total available tracks.

The degree of congestion is displayed with different color coding. The colors in increasing order of congestion are *blue, green, yellow, red, magenta, grey and white*. These diamond-shaped congestion locators represent an average in the area.



What is the direction of most of the congestion?

Answer: _____

10. To turn off the markers, click **All Colors**.
11. Click the **View Only** tab.
12. Deselect Congestion, Congestion Label, Horizontal Congest, Congestion/Route Cong, and Vertical Congest.

13. Close the Color Preferences form.

Saving the Design

1. To save the session, choose **File – Save Design**.
2. Select **Innovus**.
3. In the filename field, enter **earlyGlobalrouted.inn**.
4. Click **OK**.

To restore your work in a future session, choose **File – Restore Design**. For the filename, enter **earlyGlobalRouted.inn**.

Viewing a Design After an Early Global Route

1. Make sure that you are in the Physical view.
2. Set Net visibility to ON, if it is off.
3. Zoom in to see the routes.
4. Deselect Std. Cell selectability.
5. Select a net.
6. To dim the background so that you can see the net better, press **F12**.
7. To display the Attribute Editor and view its properties, **double-click** the net.



What is the name of the net?

Answer: _____

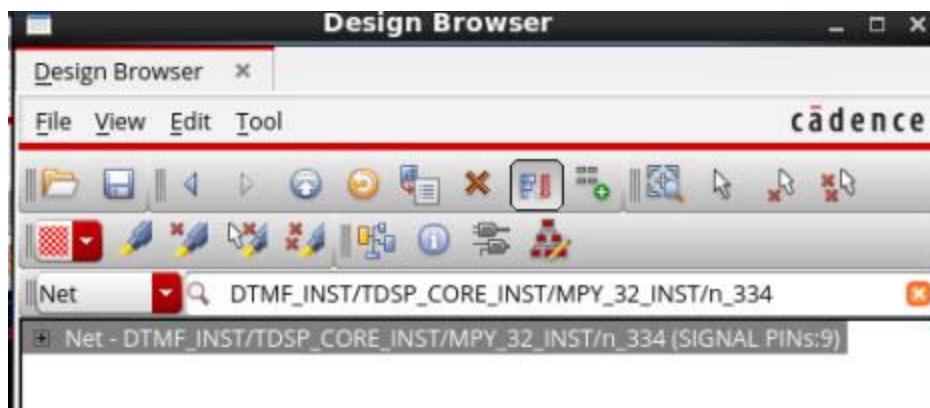
Which layer is the selected net on?

Answer: _____

The Wire Status field helps distinguish between the routes generated for the Early Global Router and the detail router that you will be running in a later step. If the Wire Status is **Unknown** instead of Routed or Fixed, the net has been routed by the Early Global Router.



8. Close the Attribute Editor.
9. To deselect the net, click in any empty space.
10. To reset the visibility, press **F12** twice.
11. Choose **Tools – Design Browser**.
12. Change the Find cyclic field from Instance to **Net**.
13. In the Design Browser, enter the net name:
DTMF_INST/TDSP_CORE_INST/MPY_32_INST/n_334
14. Press **Enter**.
15. In the Design Browser, select the net.



16. Click the **Select** button in the Design Browser. This choice selects the net in the Physical view.



17. To verify that the net is selected, look at the SelNum value in the lower-right corner of the design window.

18. To see this net, in the Design Browser form, click the **Zoom Selected** button.

You might have to zoom in further to this area to see this net.



19. To display the net better, dim the background and press **F12**. To return to the original display, press **F12** again.



20. Save the design. For the filename enter **pr.inn**.

21. Do **not** close the software.

Note: If you do close the software, you can restore the design from the *pr.inn* file that you saved in a previous step.

Summary

In this lab, you ran placement and the Early Global Router. You also analyzed the congestion after early global routing and determined the ability to route the design.



Module 11: Multi-Mode Multi-Corner Analysis

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There are no labs in this module

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Module 12: Extracting Parasitics and Running Timing Analysis

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Lab 12-1 Extracting RC Data

Objective: To extract parasitics based on Early Global Route.

Extracting RCs

1. In this lab, you extract RCs (resistance and capacitance). They are a prerequisite for running timing analysis.
2. (Skip the following steps if you did **not** close the Innovus™ Implementation System.) If you **did** close the software before starting this lab, restart the software.
 - a. Restore your design by choosing **File – Restore Design**.
 - b. Enter your previously saved *pr.inn* file.
3. (Skip these steps if you completed the previous lab.)
 - a. If you did not complete the previous lab, change to the *work* directory.
`cd work`
 - b. Restore the *pr* file by entering the following:
`innovus -init ../saved/pr.inv`
 - c. At the prompt, type the following to bring up the GUI:
`innovus> win`
4. To run extraction, choose **Timing – Extract RC**.
5. Click **OK**.

Note: For the purposes of this lab, do *not* save any files, because the generated files will be very large. The extracted RC information is annotated in the design database.

Notice that the status of the design in the lower-right corner changes to *RC Extracted*.

Calculating Delays

For the next step, delays are calculated for the interconnect wires and include instance delays.

1. Choose **Timing – Write SDF**.
2. Because you have not yet run clock tree synthesis on the design, select **Ideal Clock**, if it is not selected.
3. Select the Active View as *dtsf_view_setup*.
4. Leave the SDF output filename as-is.
5. Click **OK**.

The command creates a file in SDF format.



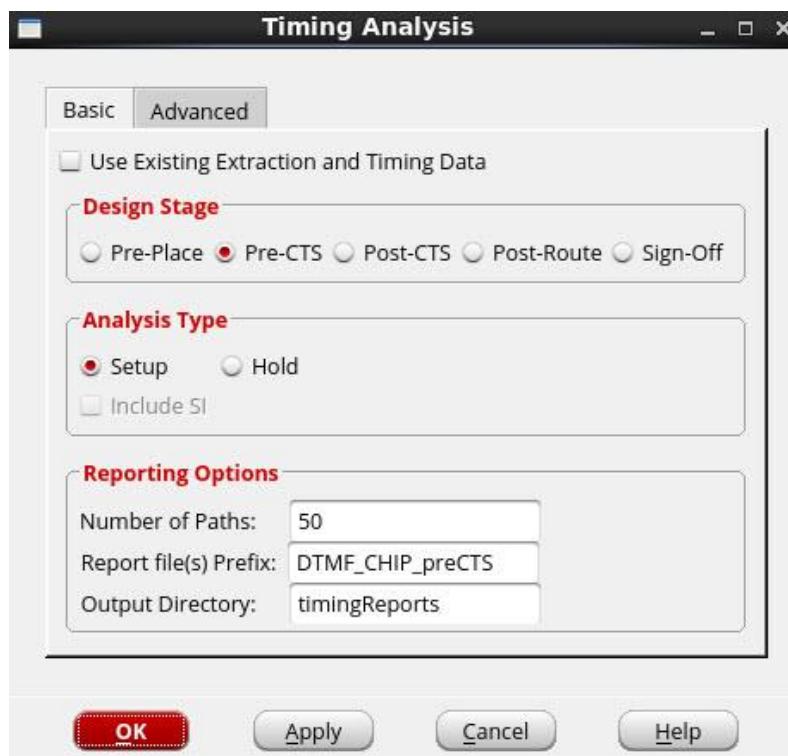
Lab 12-2 Running Timing Analysis and Generating a Slack Report

Objective: To analyze timing and display violating paths.

After extracting parasitics, run timing analysis to generate timing reports.

1. Choose **Timing – Report Timing**.

The Timing Analysis form is displayed.



2. Because you have not yet created a clock tree for the design, in the Timing Analysis form, make sure that the **Pre-CTS** option is selected.

Because we are interested in generating reports for setup under worst-case conditions, the **Setup** option is selected (default).

The timing reports are saved to the directory specified in the **Output Directory** field.

Note: The Pre-Place option considers a zero wire-load model while ignoring high-fanout nets. This option is useful to check if there are any errors in your constraints file prior to running placement for the first time.

3. To run timing analysis for setup, click **OK**.

4. Select **Timing – Debug Timing**.

This will bring up the Display/Generate Timing Report form.

5. With defaults selections, click **OK**.

The Timing Debug window is displayed.

Do you have any failing paths?

Answer: _____

What is the Worst Negative Slack (WNS) and the Total Negative Slack (TNS)?

Answer: _____

6. To run the timing analysis for both setup and hold, run the following commands:

```
set_analysis_view -setup { dtmf_view_setup } \
-hold { dtmf_view_hold }
timeDesign -preCTS
timeDesign -preCTS -hold
```

What is the WNS for dtmf_view_setup?

Answer: _____

What is the WNS for dtmf_view_hold?

Answer: _____

7. After running the analysis, view the slack report, and choose **Timing – Debug Timing**.

The Display/Generate Timing Report form is displayed.

8. Click the folder icon next to Report File(s)



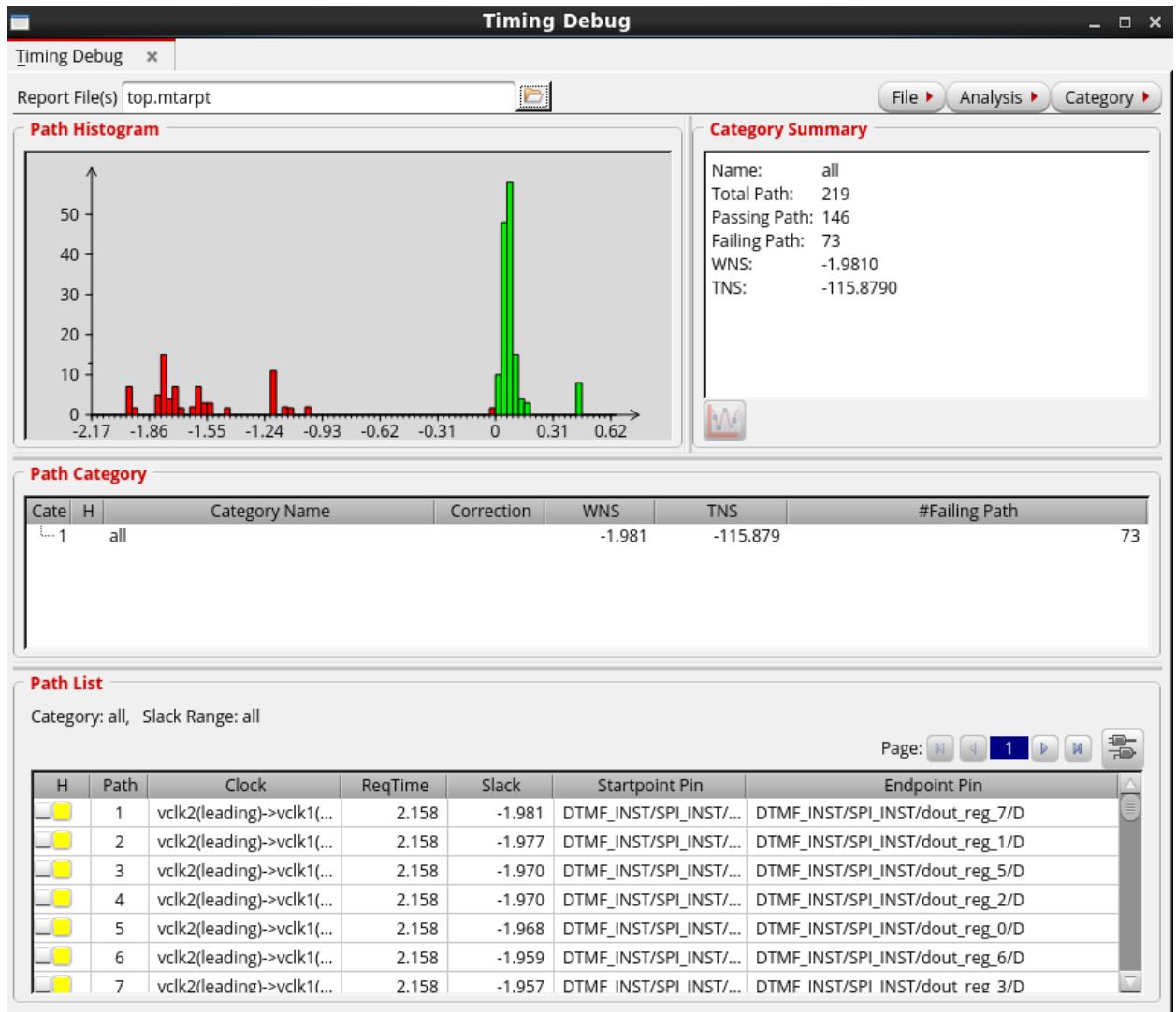
This will bring up the Display/Generate Timing Report form.

9. Select **Generate**.

10. Set Check Type to **hold**.

11. Click **OK**.

The histogram will show negative paths.



12. In the *Path List* pane of the Timing Debug window, **double-click** one of the paths.

The selected path is highlighted in the Design window.



13. Click **F12** to dim the background.

The Timing Path Analyzer with more details in the path is also displayed.

Do you see a pattern in the type of paths that have a negative slack?

Answer: _____

14. To close the Timing Path Analyzer window, click the **X** in the top-right corner of the window.

15. To close the Timing Debug form, close the window.

16. Save the design.

- a. Make sure that you save the file in the *work* directory and not in the *timingReports* directory.
- b. Choose **File – Save Design**.
- c. For the filename, enter **preCTSopt.inn**.



Module 13: Power Performance and Area Optimization

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There are no labs in this module

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Module 14: Implementing the Clock Tree

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Lab 14-1 Running Clock Tree Synthesis

Objective: To run clock tree synthesis.

After running placement or pre-CTS optimization, you run clock tree synthesis with constraints on what buffers to use and the type of clock routing to implement.

Running CTS

1. If you exited the Innovus™ software, read in the saved *pr.inv* files from the *saved* directory to the current *work* directory by entering the following commands:

```
cd work  
innovus -init ../saved/pr.inv  
innovus> win
```

Properties other than what can be derived from the *.sdc* file for running CTS have been saved in the *dtsf.ccopt* file.

2. View the *dtsf.ccopt* file and notice that *set_ccopt_property buffer_cells* and *set_ccopt_property inverter_cells* commands in the file specify the clock buffers and inverters to use.
3. To save typing, source the *dtsf.ccopt* file:

```
source dtsf.ccopt
```

4. To see all possible options for this command, run the following:

```
set_ccopt_property * -help
```

5. Generate the remaining clock tree spec file constraints from the *.sdc* file by running the command:

```
create_ccopt_clock_tree_spec
```

6. Create a clock tree by running the command:

```
ccopt_design
```

7. View the *.log* file for this session.

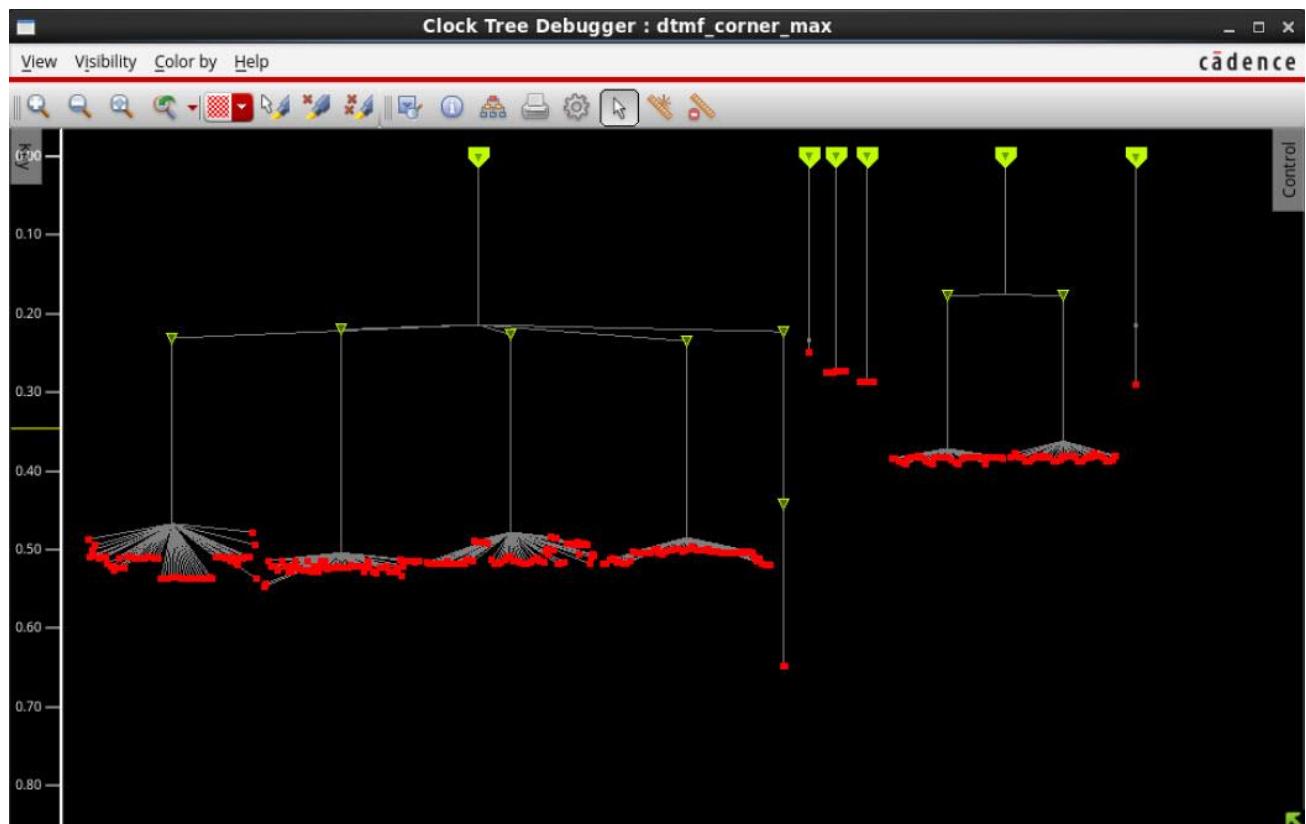
Were there any clock constraints violations?

Answer: _____

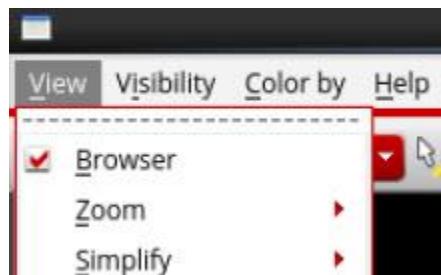
Viewing Clock Tree Results

1. Make sure you are in the Physical view.
2. Select **Clock – CCOpt Clock Tree Debugger**.
3. With defaults selected, in the **CTD Configuration** window, click **OK**.
4. Press **f** on the keyboard to fit the clock trees to the debugger window.

This will bring up the Clock Tree Debugger for the view *dtnf_corner_max*.



5. Select **View – Browser**



This will append the browser to the clock tree debugger window.

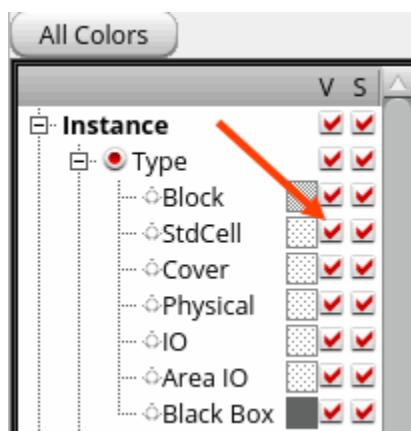
6. Zoom in by clicking and dragging the right mouse button over an area that contains leaf cells or clock buffers.

The mouse functions and bind key presets for Innovus also apply to the clock tree debugger window.

7. Click **Q** in the Innovus window.

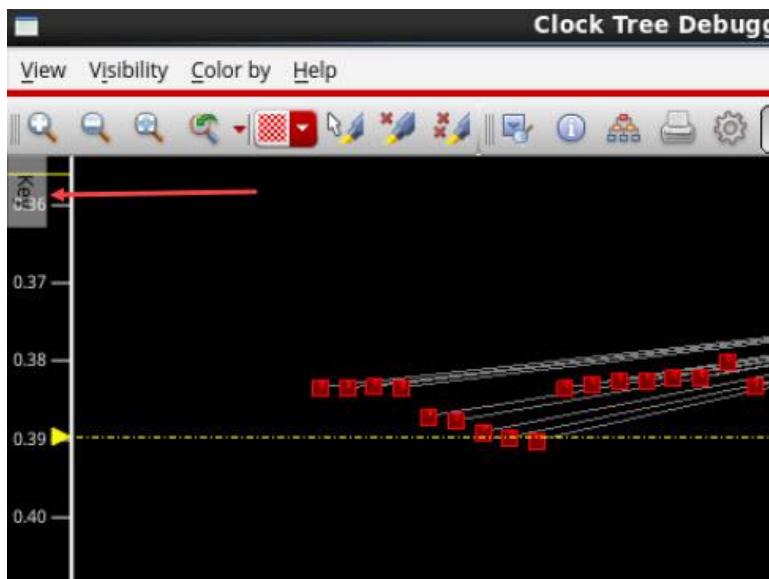


8. Hover over the objects with the cursor in the clock tree debugger window to see the cell properties.
9. Click to select a leaf cell (flop) or a clock buffer in the clock tree debugger window and notice the Innovus physical view zooms to that cell. Make sure the standard cell visibility is selected.



10. Select the Innovus window and press **F12** to dim the background to see the cell more clearly.
11. Click the **Key** tab on the left of the clock tree debugger window.

Implementing the Clock Tree



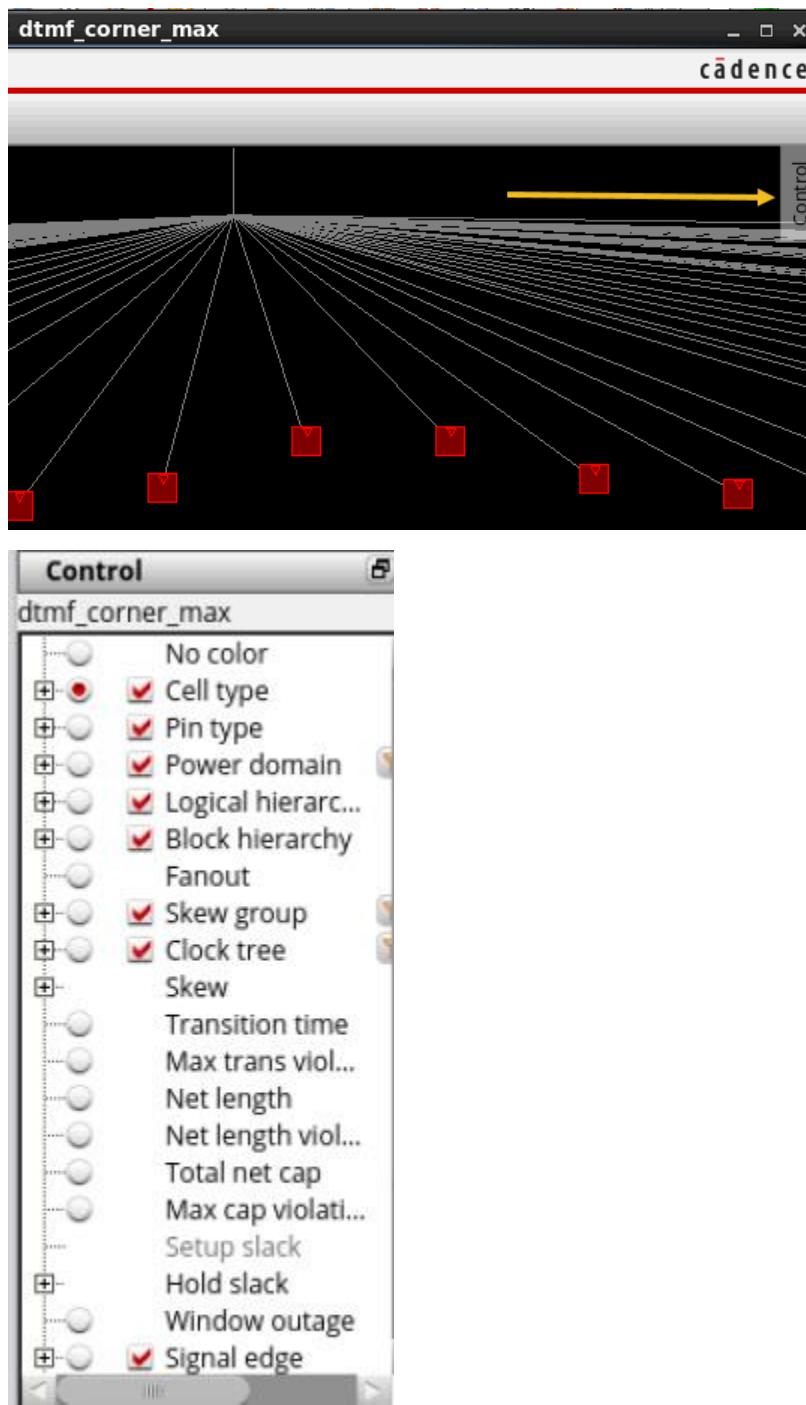
12. This will bring up the Key panel which contains the color keys and the objects that the colors represent.



13. Drag the side of the Key panel to make it wider.

14. Fit the clock tree to the window by pressing **f** on the keyboard.

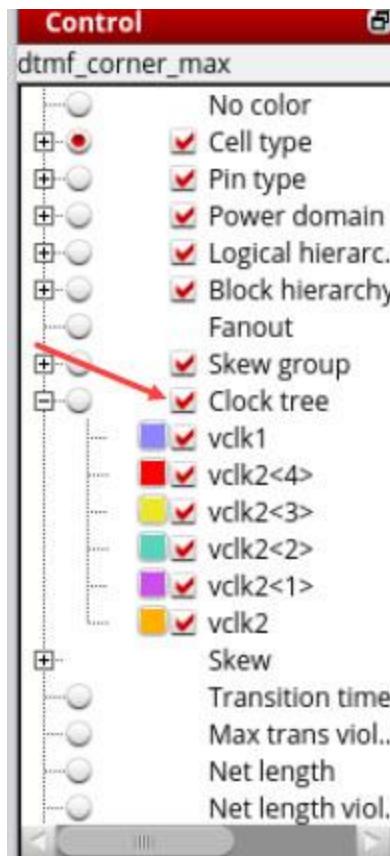
15. Click the **Control** tab on the right of the debugger window to display the **Control** panel.



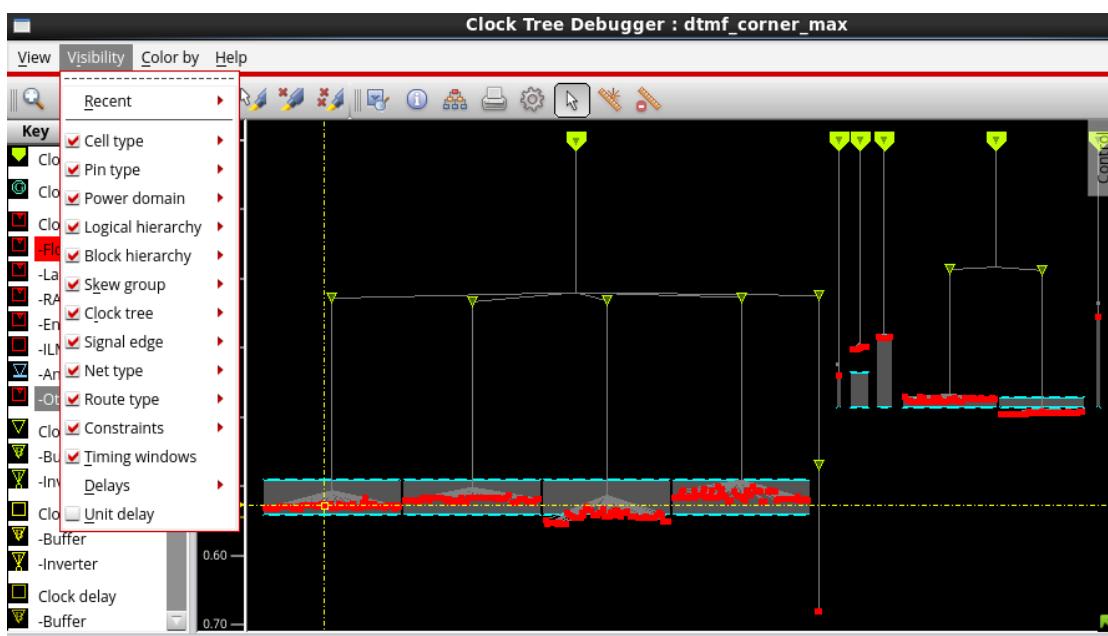
16. Expand the Clock trees by clicking the + next to Clock tree in the Control pane.

You can change the color of the clock tree in the debugger window by changing the color in the pane that is associated with the tree.

Implementing the Clock Tree

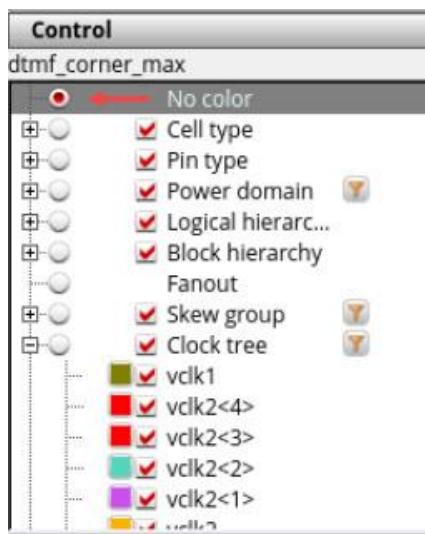


17. Select **Visibility** and **Timing window** in the pane to view the target delays for CTS.



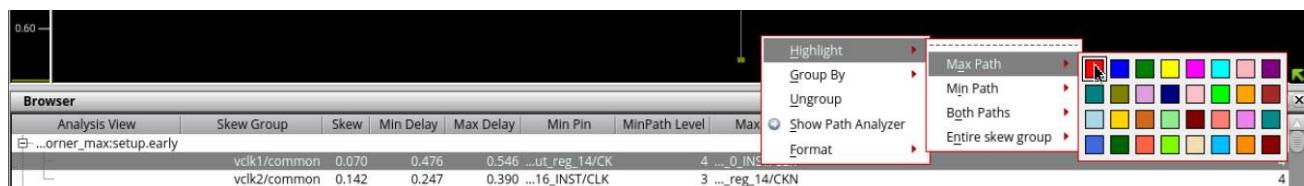
18. Unselect the **Timing window** button in the Control panel.

19. Select **No color** in the Control panel.

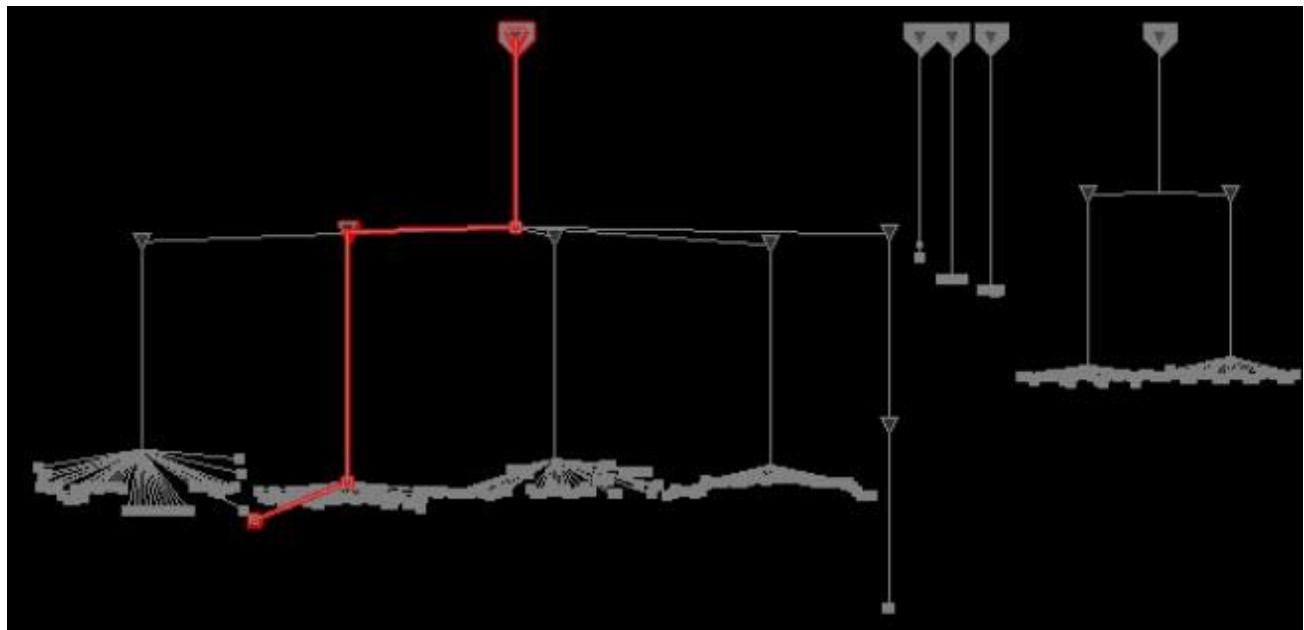


20. Select a skew group in the Browser pane.

21. Highlight the path by right-clicking on the selected path selecting **Highlight – Max Path** and select the highlight color.



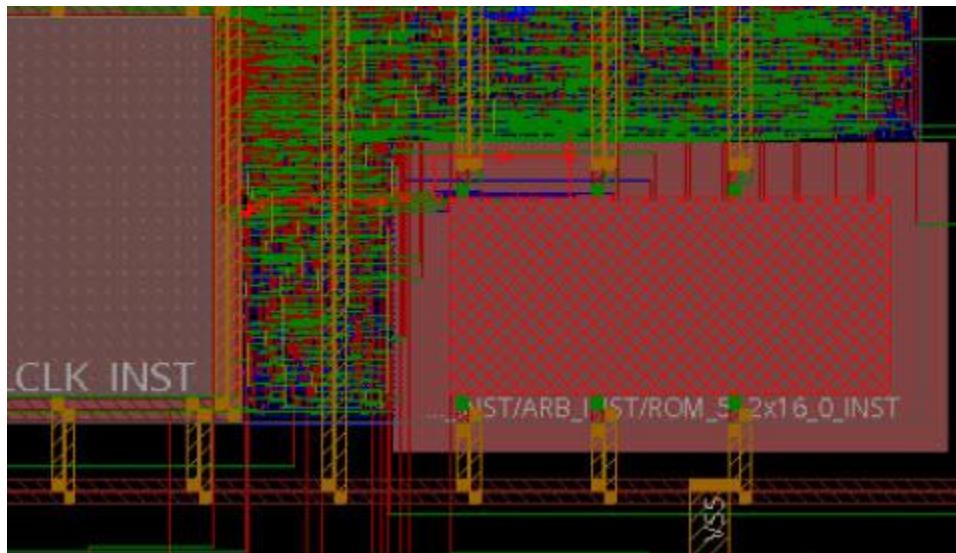
22. Notice that the path is highlighted in the debugger window.



23. Select the main Innovus window and press **f** on the keyboard.

24. Notice that the same path is also highlighted in the Innovus design window.

25. Press **F12** to see the path better in the Innovus physical view.



26. Close the clock tree debugger window.

27. Clear the highlight by selecting **View – Clear Highlight – Clear All**.

28. Run timing analysis for setup by entering:

timeDesign -postCTS

Is your slack negative?

Answer: _____

29. To run hold time analysis, enter:

timeDesign -postCTS -hold

Is your slack negative or positive?

Answer: _____

What is the slack in your design?

Answer: _____

30. If you have hold violations (negative slack), run optimization for hold by entering:

optDesign -postCTS -hold

What is the slack after optimization?

Answer: _____

31. Save your design as **postCTSopt.inv**.

32. Close the session.

Summary

In this lab, you ran clock tree synthesis and viewed the tree in the clock tree debugger.



Lab 14-2 Extracting and Generating Scale Factors

Objective: To extract the RCs in the design with both the signoff and built-in extractors and generate scale factors.

Generate scaling factors by running the *generateRCFactor* command on a routed design for better correlation between the built-in extractor and a signoff extractor.

Loading the Design

1. Verify that your working directory is set to the following:

FPR/work

2. To start the software, enter this command in a *csh* window:

innovus

After a short time, the software starts.

3. To load the design that has been detail routed, in the graphical interface, choose **File – Restore Design**.

4. Select **Innovus** for Data Type.

5. Specify this file:

routedExtracted.inv

6. To load the design, click **OK**.

Generating Scale Factors with External SPEF File

1. To run the *generateRCFactor* command to generate the scale factors for *preRoute* and *postRoute* scale factors, run the following command:

```
generateRCFactor -preroute true -postroute medium \
-referenc externalSpef -spefMapFile spef.map
```

What are the scale factors that were generated for:

Preroute Cap scale factor _____

Preroute Res scale factor _____

Postroute Cap scale factor (medium)_____

Postroute Res scale factor (medium)_____

Postroute XCap scale factor (medium)_____

Note: To set the scale factors, you would modify the *create_rc_corner* defaults in the *dtnf.view* file.

2. Close the Innovus software.

Summary

In this lab, you ran the *generateRCFactor* command to generate scale factors for better correlation of native extraction with signoff extraction.



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Module 15: Detail Routing for Signal Integrity, Timing, Power and Design for Yield

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Lab 15-1 Routing Critical Nets with Shielding and Spacing

Objective: To specify critical nets for shielding, and to route and optimize the design to meet timing and signal integrity.

Certain critical or high-speed nets require shielding or spacing from other nets. In this lab, you specify attributes to shield those nets and to assign the nets used for shielding. You also set up extra spacing for a particular net. Typically, you want to route these nets and shields *before* routing any other nets.

Loading the Design

1. Verify that your working directory is set to:

```
FPR/work
```

2. If you did not save your design *postCTSoft.inv* at the end of an earlier lab, use a saved design that has been placed and in which the clock tree has been synthesized:

```
cd work  
%innovus -init ../saved/postCTSoft.inv  
innovus> win
```

Setting Shielded and Spacing Net Attributes

1. In the *csh* Innovus™ window, where you started the software, enter this command at the *Innovus* prompt:

```
setAttribute \  
-net DTMF_INST/TDSP_CORE_INST/read_data \  
-shield_net VDD
```

The actual shielding happens in a later step.

2. To check the attributes that you set for the *read_data* net, in the same *csh* window, enter the following:

```
getAttribute -net DTMF_INST/TDSP_CORE_INST/read_data
```

Is the read_data net going to be shielded?

Answer: _____

If so, with what net will be used for shielding?

Answer: _____

3. To set the net attributes to add space around a critical net (*clk*), enter this command:

```
setAttribute -net DTMF_INST/clk -preferred_extra_space 2
```

If the design is not overly congested, the router adds extra tracks of spacing around the net.

Routing the Nets

You route the shielded net first. After routing the shielded net, you route the spaced net along with the remaining nets. The power nets are connected with default width wires to other prerouted power nets.

1. To select the net for routing, choose **Tools – Design Browser**.

Make sure that you are in the Physical view.

The Design Browser form is displayed.

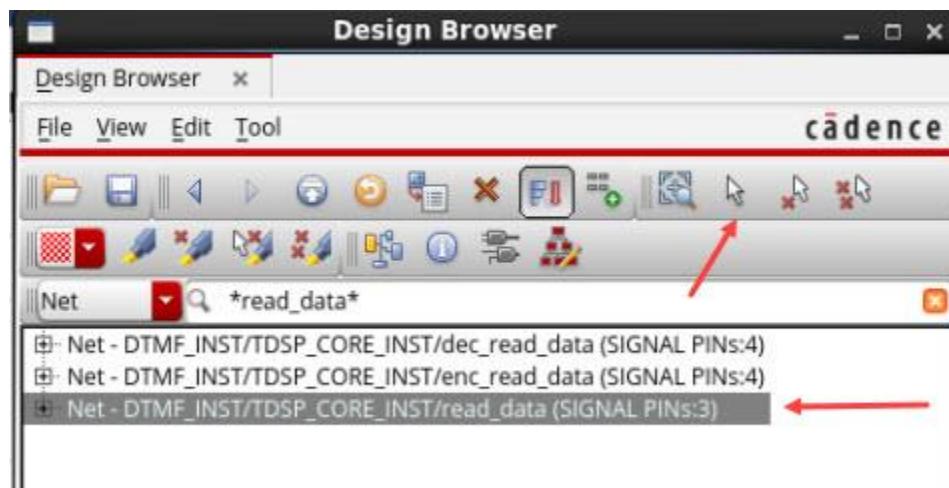
- a. In the form, change the object from Instance to Net.

- b. In the field, enter ***read_data*** and press **Enter**.

This will bring up the three nets that fit this criterion.

- c. Select the **read_data** net.

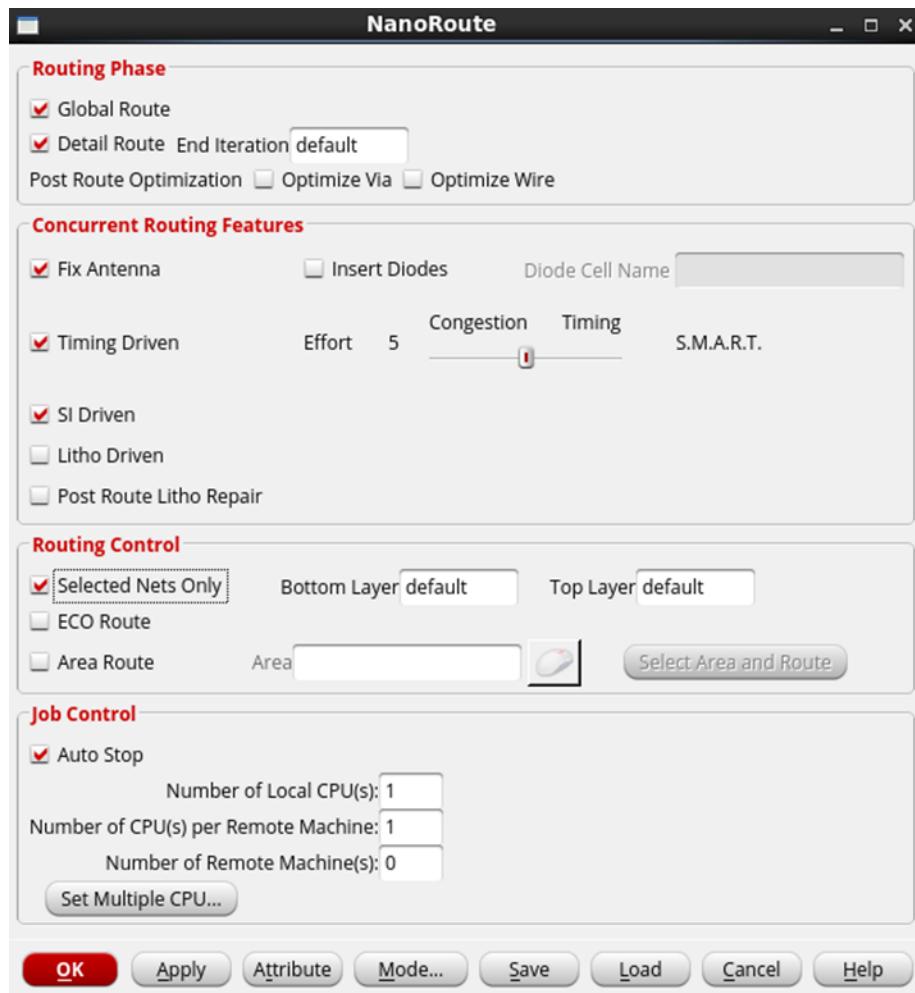
- d. Click the **Select** button.



- e. Make sure that the *SelNum* field number is set to **1** in the main design window.

2. To route the selected net, choose **Route – NanoRoute – Route**.

The NanoRoute™ form is displayed.



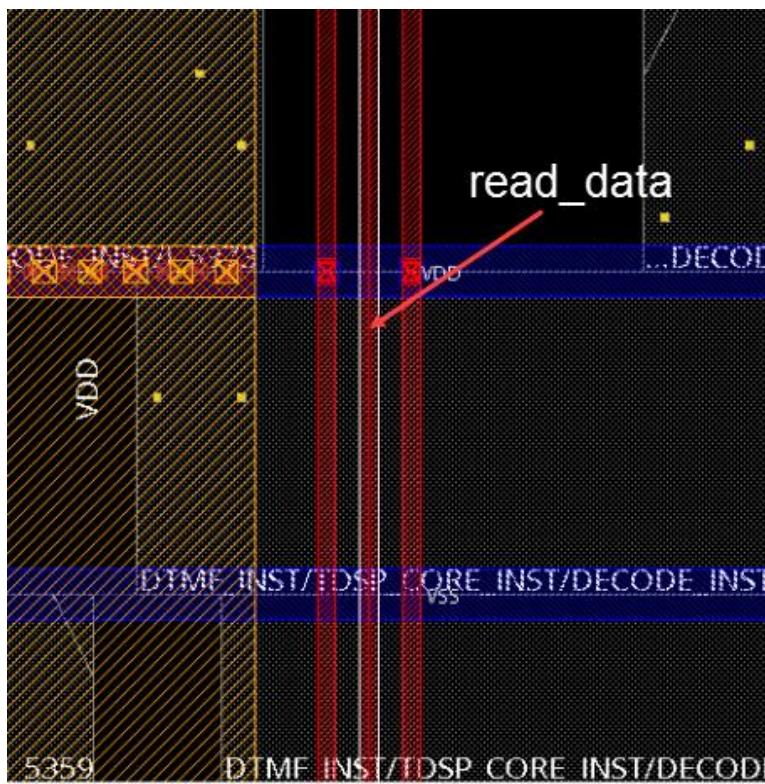
- In the Concurrent Routing Features section, turn on **Timing Driven** and **SI Driven**.
- In the Routing Control section, turn on **Selected Nets Only**.
- Click **OK**.

Make sure that you are still in the Physical view.

3. Select **Route** visibility in the All Colors pane.



4. If the *read_data* net is selected in the Physical view, zoom in to examine the shielding that is connected to VDD. If the *read_data* net is *not* selected, the next step describes how you can select and zoom in.



In your case, is the VDD shielding on one side or on both sides of the *read_data* net?

Answer: _____

5. If the *read_data* net is **not already** selected, choose **Tools – Design Browser**.

The Design Browser form is displayed.

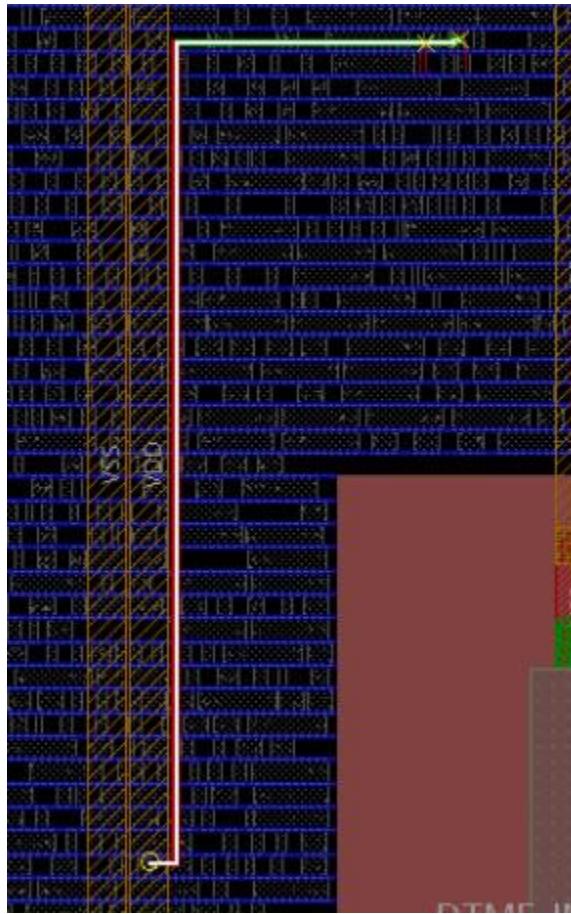
- In the form, change the object from Instance to **Net**.
- In the field, enter ***read_data***.
- Press **Enter**.

- d. In the Design Browser, click the net, the select icon, and the zoom selected icon.



- e. Zoom in further to examine the net for routing and for shielding that is connected to VDD.

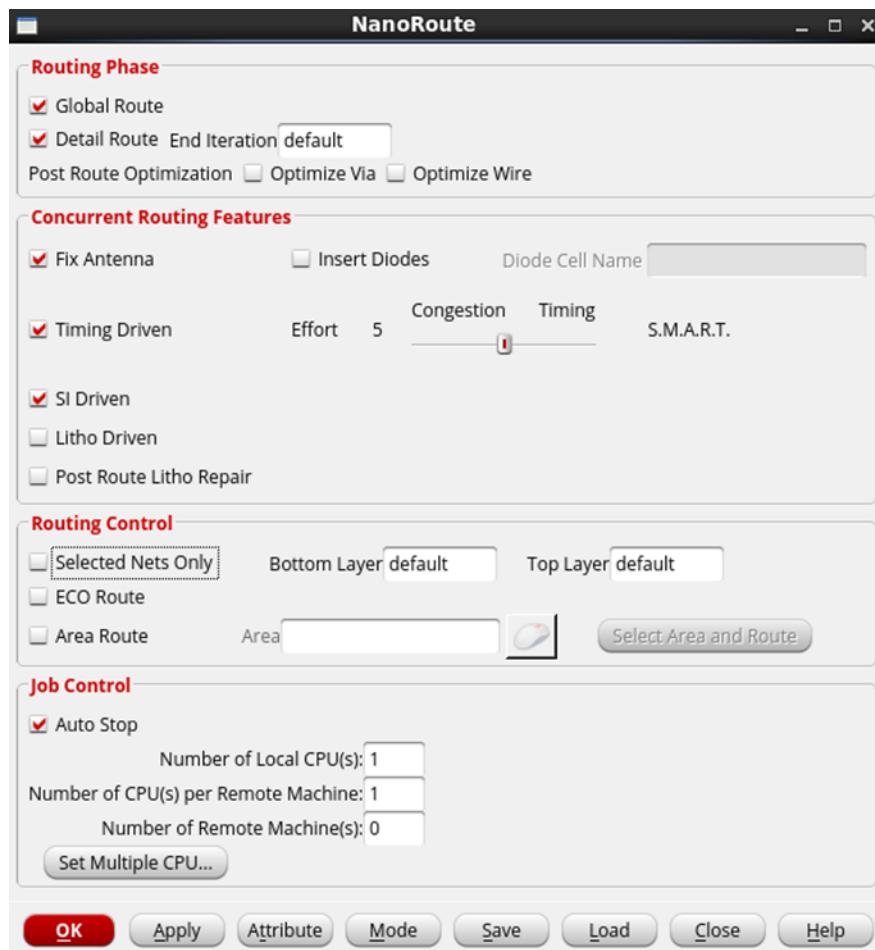
Tip: For better visibility, you can dim the background. Press **F12**.



6. To get back to the original visibility, continue to press **F12**.

7. To route the remaining nets, choose **Route – NanoRoute – Route**.

The NanoRoute form is displayed.



- Click **Mode** in the NanoRoute™ form.
This will bring up the Mode Setup form.
- In the left-hand pane of the Mode Setup form, make sure that **NanoRoute** is selected.
- In the Mode Setup form click the **DFM** tab.
- Set Concurrent Via Optimization Effort to **Medium**.
- Click **OK** in the Mode Setup form.
- Before starting the router, in the *Routing Control* section, turn **off Selected Nets Only**.
- Make sure that **Timing Driven** is selected.
- Select **SI Driven**.

- i. Make sure that Selected Nets Only is turned **off**.
 - j. Click **OK** in the NanoRoute form.
8. View the log file for the current session to determine if there were antenna violations that have been fixed during the search-and-repair operation.
9. Set the timing analysis mode by running the following commands:

```
setAnalysisMode -analysisType onChipVariation
```

10. Run setup and hold timing analysis by running the following commands:

```
timeDesign -postRoute  
timeDesign -postRoute -hold
```

What is the setup and hold TNS and WNS?

Answer: _____

Are there any setup or hold violations?

Answer: _____

11. If there are setup and hold violations, run optimization:

```
optDesign -postRoute -setup -hold
```

What is the setup and hold TNS and WNS after optimization?

Answer: _____

Is the slack improved or met for setup and hold?

Answer: _____

12. To save the design, choose **File – Save Design**. Enter this filename:

DTMF_detailrouted.inv

13. Close the Innovus software.

Summary

In this lab, you

- ◆ Set options to shield and space critical nets in a design
- ◆ Routed, timed, and optimized the entire design
- ◆ Ran concurrent SI, timing and via optimization and recorded the results



Module 16: Wire Editing

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Lab 16-1 Using the Interactive Wire Editor

Objective: To manually route a net between two points.

In this lab, you load a design, and manually route a net. You set up wire snapping to pins and tracks, and route with both default and nondefault widths.

Loading the Design

1. Change the working directory to:

```
FPR/work/EDIT_ROUTE
```

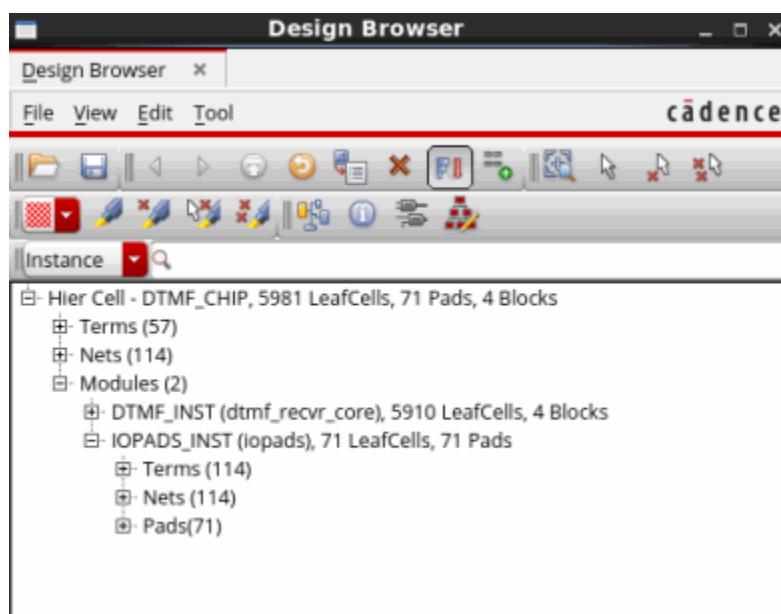
2. To start the software, in a *csh* window, enter this command:

```
innovus
```

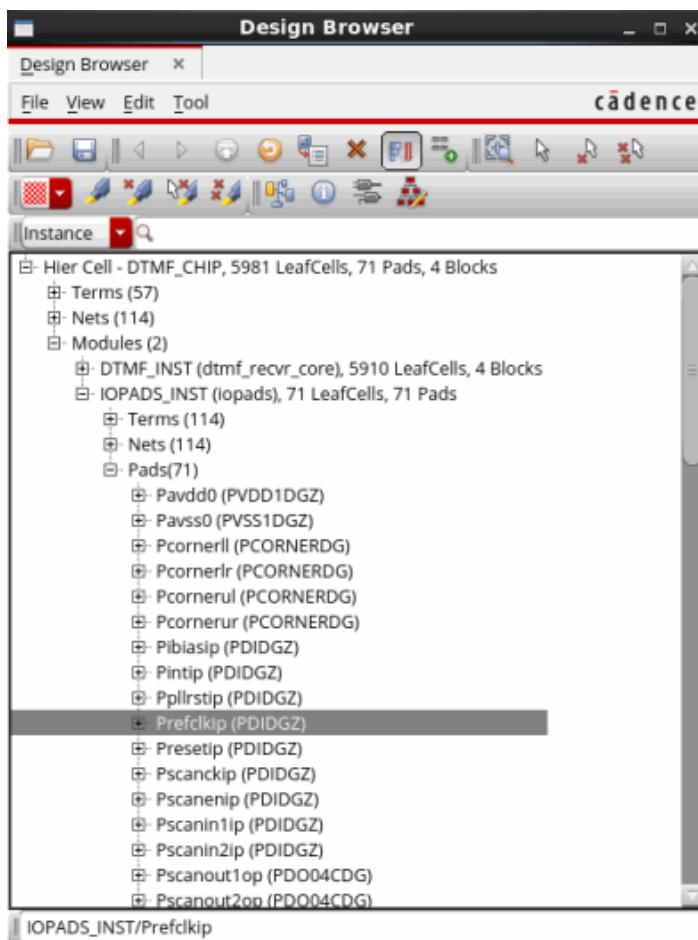
3. Load the saved design *EditRoute* by selecting **File – Restore Design**.

Locating the Net for Manual Routing

1. To make the Tools menu visible, widen the Innovus™ window.
2. To find the net to hand-route, choose **Tools – Design Browser**.
3. In the Design Browser, click the plus sign (+) next to *Modules*. Expand *IOPADS_INST*.



4. To see the list of I/O pads, expand *Pads*.
5. To select the *Prefclkip* instance, click *Prefclkip (PDIDGZ)*. To view the instance, in the Design Browser window, click the **Zoom Selected** icon.

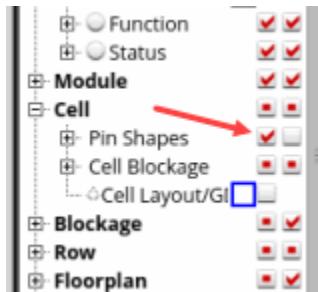


The cell is highlighted in red.



The net that you route connects the pin in the lower-right corner of the I/O instance to the *PLLCLK_INST* block.

6. Make sure that the pins are visible by expanding **Cell** in the All Colors pane and making sure that the **Pin Shapes** visibility is selected.



7. With the **left** mouse button, draw a box around the *Prefclip* pad so that you can see a blue flight line between the pad and the pin on the PLL.

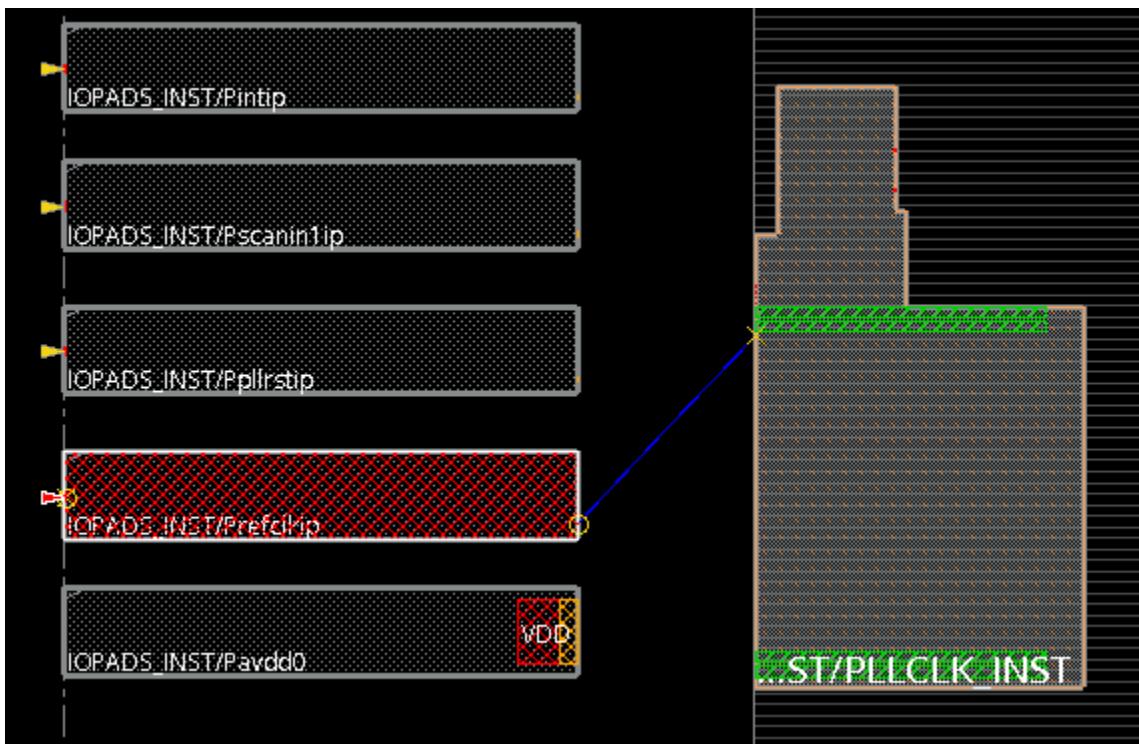
8. Make sure you are in the Physical View.



9. With the **right** mouse button, click and drag to zoom to the point where you can see both the pad pin and the PLL pin for this net.



With this view, you can determine an optimal route for the net.



The connectivity of the pin on the pad to the pin on the PLL is displayed.

10. With the **right** mouse button, click and drag, again, to zoom to an area near the PLL.

Using the Wire Editor

The following table defines the bindkeys for the Wire Editor.

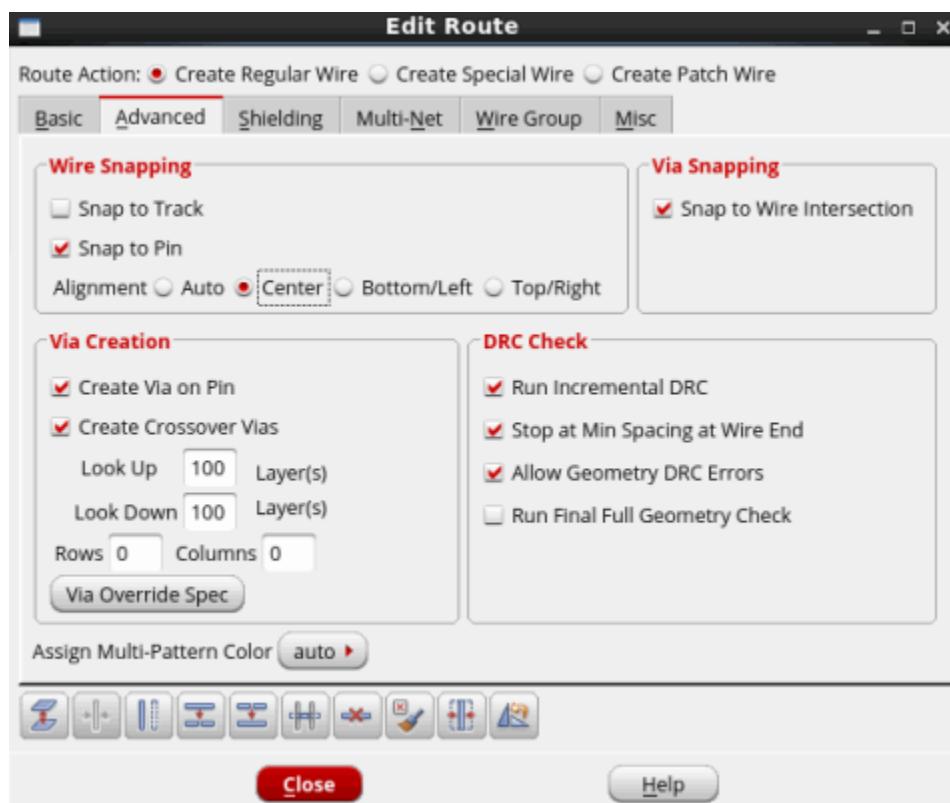
Bindkey	Description
A	Starts the Add Wire mode. The cursor turns into a pencil. Left -click to add wires if the Nets field has a net in it.
d	Opens the Select/Delete Route form.
e	Brings up Edit Route form.
n	Selects the Next Auto Query object (in Query mode only).
p	Selects the Previous Auto Query object (in Query mode only).
S	Selects the current Auto Query object and seeds the Nets tab's Nets field and the Route tab's Layer and Width fields in the Edit Route form (in Query mode only).
u	Changes wire to next higher layer (in Add Wire mode).
d	Changes wire to next lower layer (in Add Wire mode).
Control-w	Deletes the last wire segment created (Query mode only).
R	Enters nonconnectivity move mode.
N (next) or P (previous)	Displays or replaces a via that has the same LEF rule as the selected via.
Click	Ends the current wire segment.
Double-click	Enters current point and stops wire creation.

Note: For a list of all bindkeys and how to add bindkeys, choose **View – Set Preferences**, and then click **Binding Key**.

1. Make sure that you are still in the Physical view. 
2. Zoom in to the pin that you are routing.
3. To display the Edit Route form, with the Innovus window active, press **e**.
4. To set wire snapping options, click the **Advanced** tab.
5. Turn off Snap to Track.

Wire Editing

6. Leave **on** Snap to Pin. Set Alignment to **Center**.

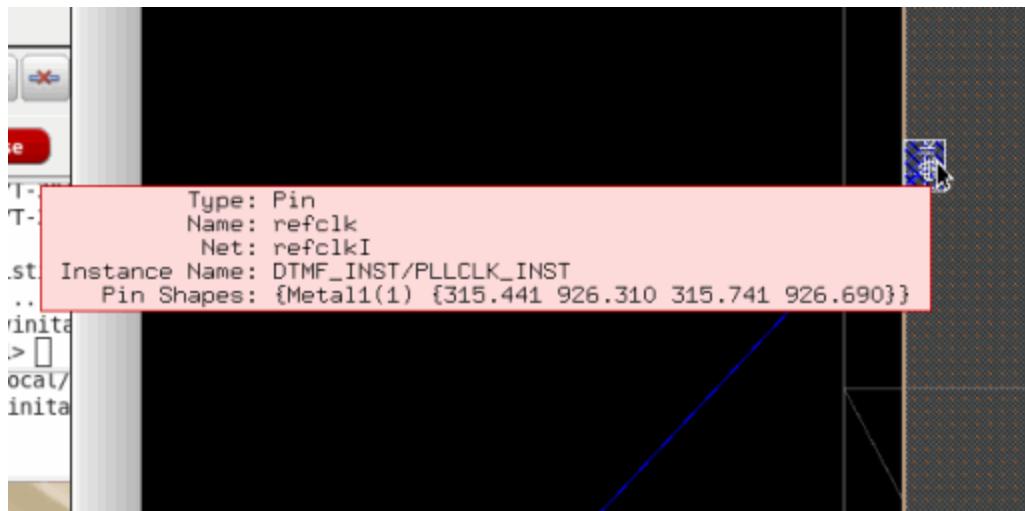


7. On the Edit Route form, click the **Basic** tab.
8. To set the selection of objects to 0, click an area where there is empty space.
9. To turn on the autoquery function, at the bottom of the Innovus graphical interface, click the **Q** button.

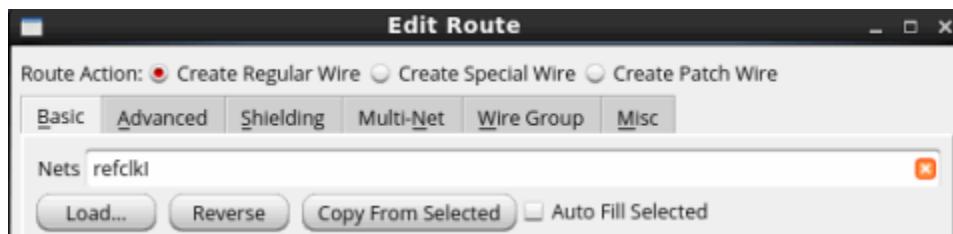


To add the net name in the **Net** field, use the autoquery feature.

10. Make sure that the Innovus window is the active window.
11. Move the pointer over the *refclkI* net (connecting to the *refclk* pin on the *PLL* block).



12. Press **Shift+S** to populate the *Nets* field in the Edit Route form with *refclkI*.



13. To change the cursor to a *pencil* for wire editing, make sure that the cursor is in the Innovus window. Press **Shift+A**, or click the **Edit Wire** icon.



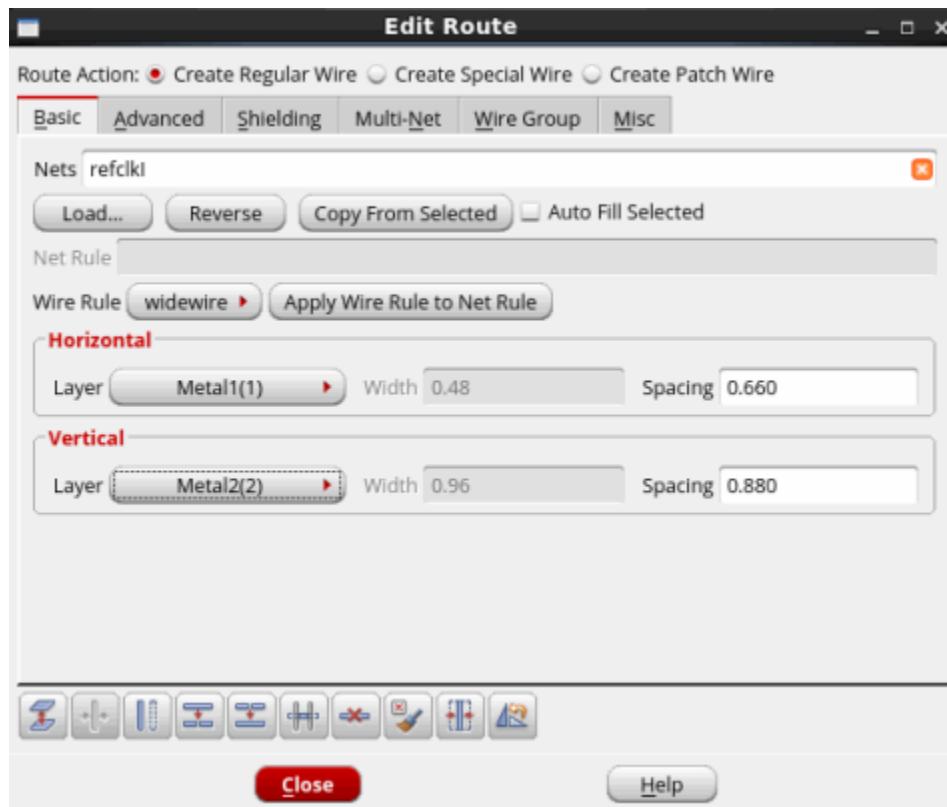
14. On the *refclk* block pin, click **left**.

The wire snaps to the center of the pin and follows the cursor.

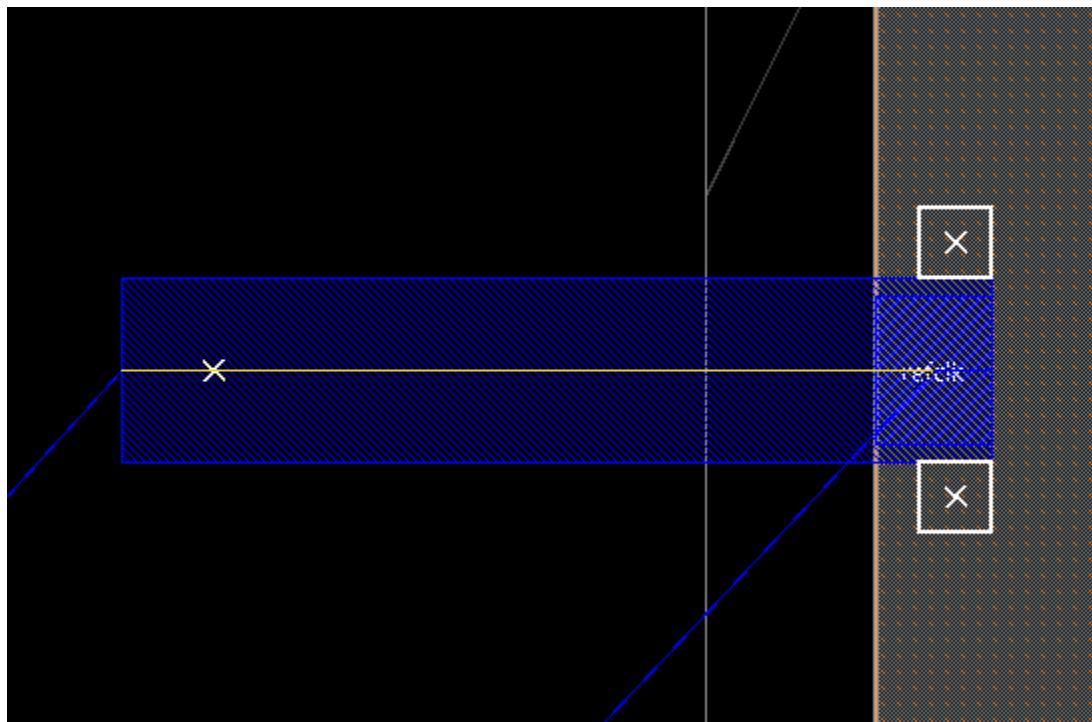
The LEF file has the *widewire* rule defined for layers and vias. To use this rule, on the Net tab in the Rule field, click the **widewire** option as shown in the next step.

Wire Editing

15. In the Edit Route form, under the **Basic** tab, change the Wire Rule field from Default to **widewire**.



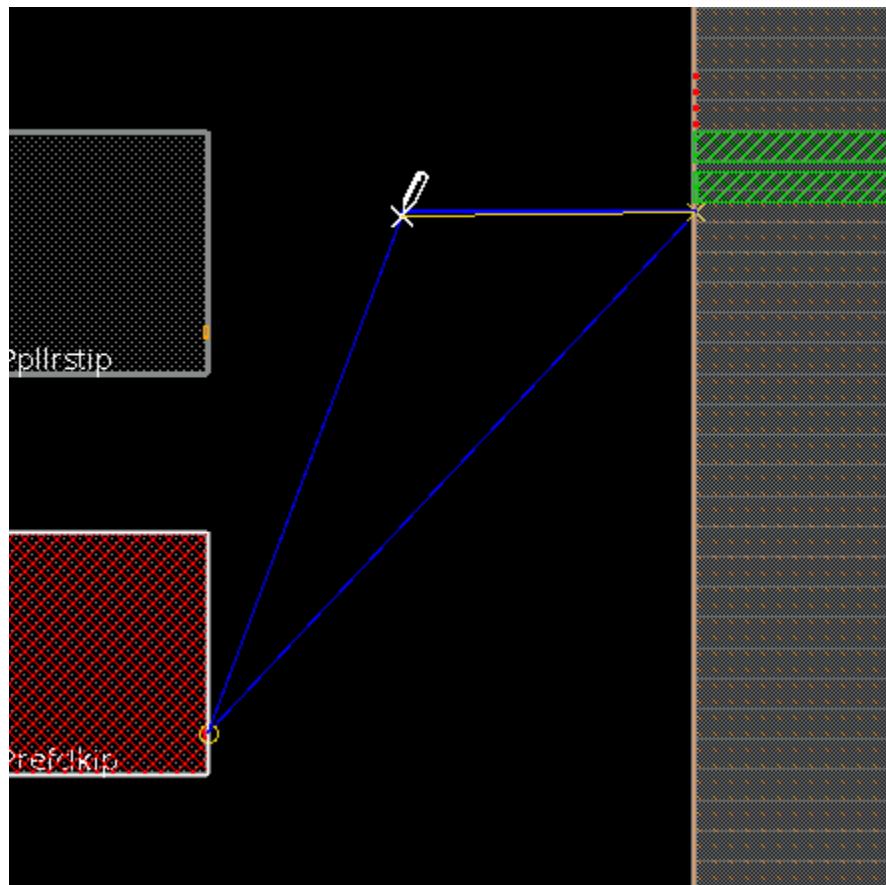
A wider wire (defined in the LEF file) coming from the pin is displayed, *but you also see violations*. The width of the wire is greater than the pin size and violates the obstructions that surround it.



16. Click the **Default** rule.

Notice that the wire width changes back from wide to the default width.

17. To move the cursor left about half way from the *refclk* pin to the destination pin, drag the wire.



18. To start drawing the wire on M1, press **1** on the keyboard.

19. To complete this segment of the route, click the left mouse button.



20. Create a vertical wire on M4 by pressing **4**.

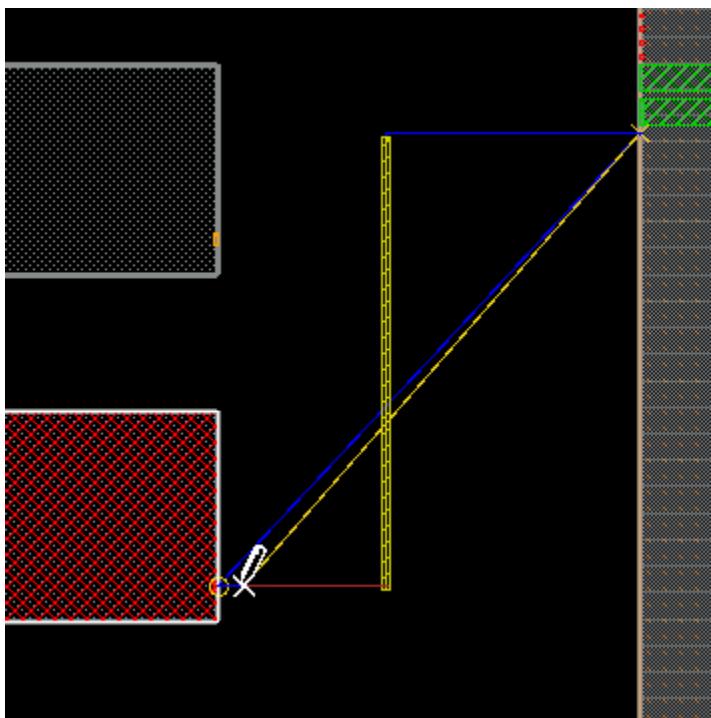
21. To route with a wide wire in M4, change Rule to **widewire**.

22. To end the *M4* vertical route when the flight line is horizontally even with the I/O pin, click the **left** mouse button.

With this action, you can change to a horizontal routing direction.

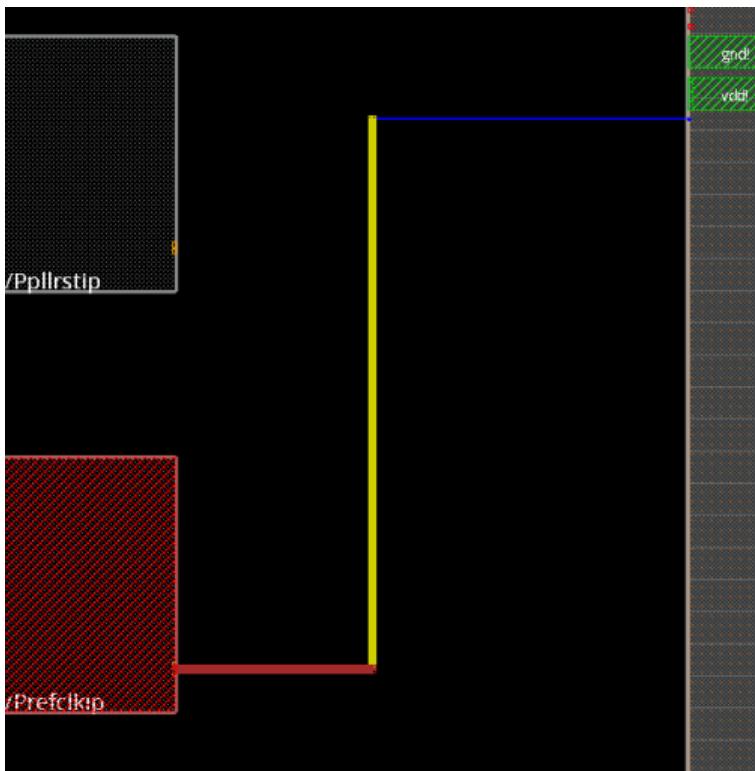
23. To change the layer for the horizontal route to M5, press **5**.

24. Change the Rule from widewire to **default**.



25. To finish the route to the I/O pin, **double-click the left mouse button** near the I/O pin.

Because you set the *Snap to Pin* value to *Center*, the tool automatically snaps to pin C.



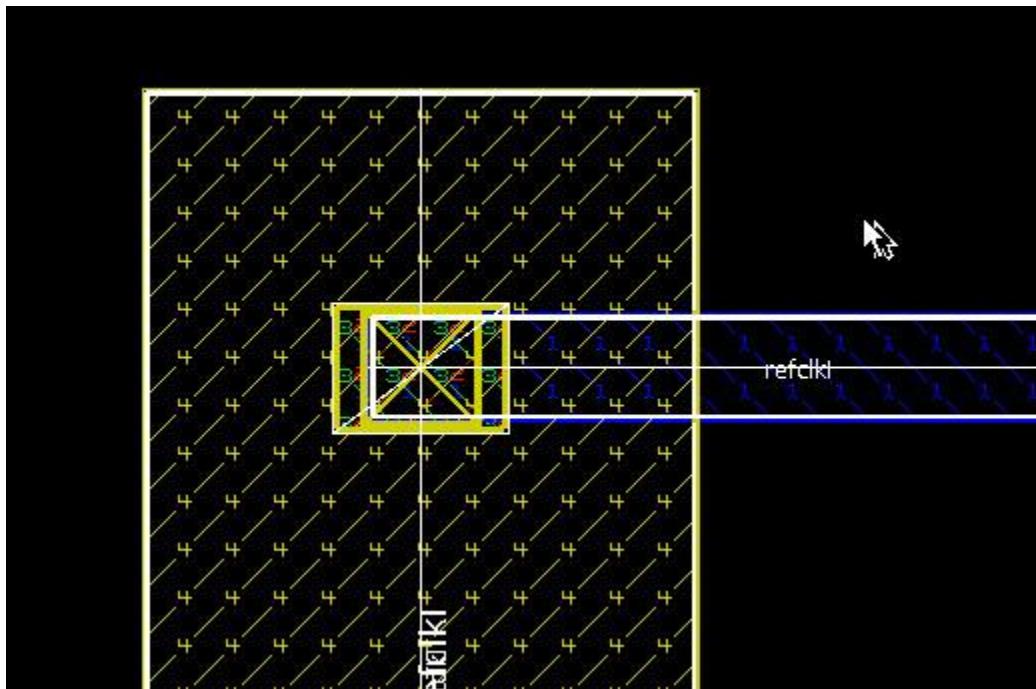
26. To close the wire edit mode and enter select mode, press **a**.

27. If you want to delete and reroute the net, press **d**.

Replacing a Via in a Design

You can replace a selected via with another, provided they both have the same LEF rule.

1. Zoom in to see the area where the stacked vias connecting M1 to M4 were placed on the refclkI net that you routed previously.
2. If it is off, turn **on** the autoquery function; at the bottom of the Innovus window, click the **Q** button.
3. To select the via to change, while pressing the **left** mouse button, draw a box around the vias.



4. To display the Attribute Editor, press **q**. Confirm that the selected object is the via.
5. If multiple objects have been selected, to search for the via, click **Next**.
6. Close the Attribute Editor.

7. Without moving the mouse, use the **Shift-n** (next) or **Shift-p** (previous) bindkey to display a via that has the same LEF rule as the selected via.

When you press the bindkey, if a via is available, the display is updated with the new via. However, if another via is not available, then you hear a warning beep when you press the bindkey. This can occur when the following happens:

- Only one via is defined in the LEF file.
- The currently queried object is not a via.
- No object is currently queried.

In the LEF file used for this lab, there are two each of the default vias.

Note: The Edit Route form does not provide access to this feature. You can change only one via at a time with the bindkeys.

8. To choose select mode, press **a**.

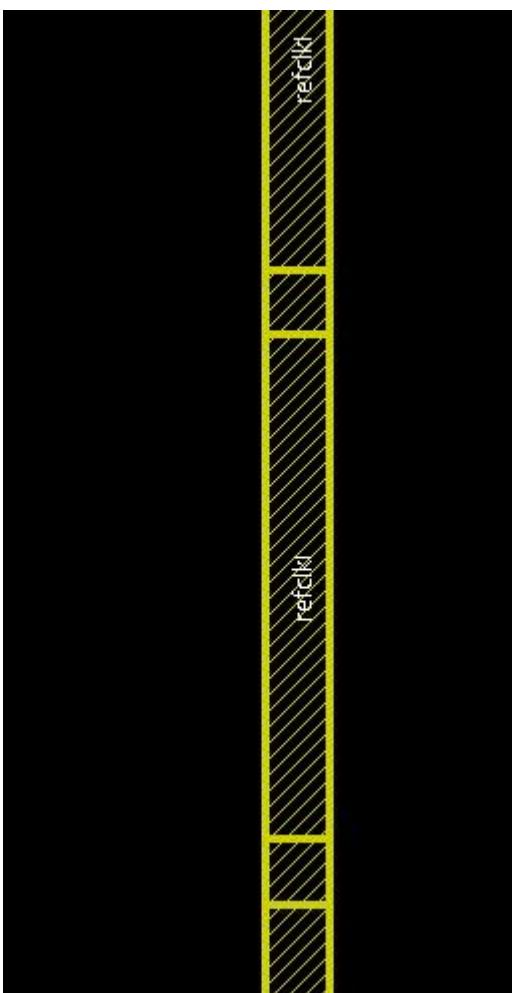
Reshaping a Wire

1. Zoom in to an area to see the vertical Metal4 route you completed.
2. Click the **Cut Wires** scissor icon with defaults in the pull-down selected.



3. Click and drag at two different places on *Metal4* horizontally where you want to create a jog.

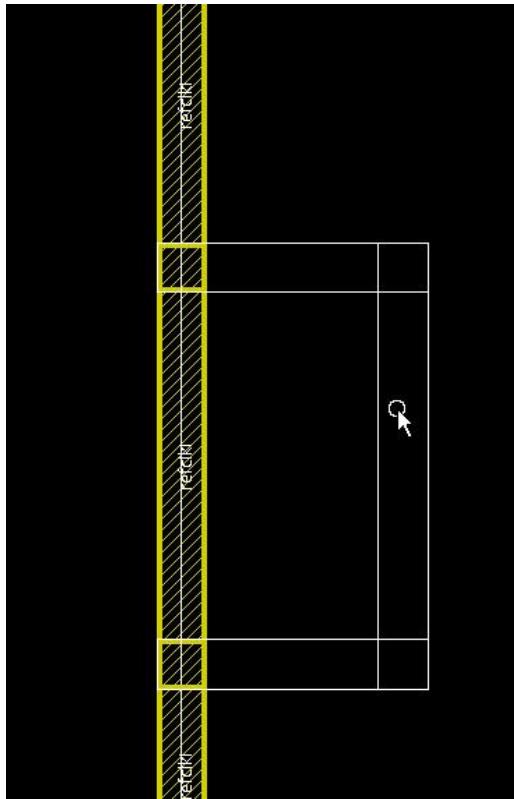
Overlapping wire segments that are based on where you made the cuts are displayed.



4. To set the select mode, press **a**.
5. Select the cut wire segment.
6. Click the **Move Wires** icon. 

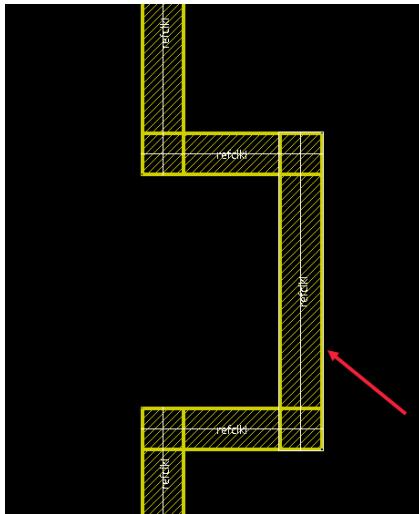
The cursor changes from an arrow to a circle.

7. To create a jog, click and drag the *metal4* segment to where you previously created the cuts. Click where you want to place the segment.

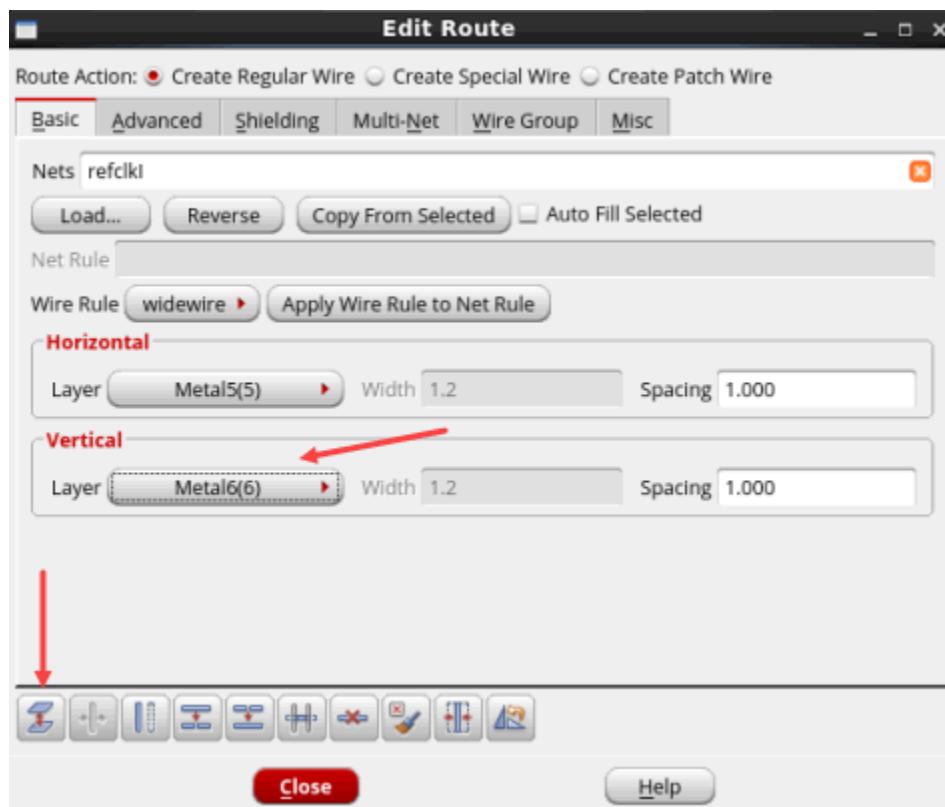


The segment and connecting wires are moved while keeping the route intact.

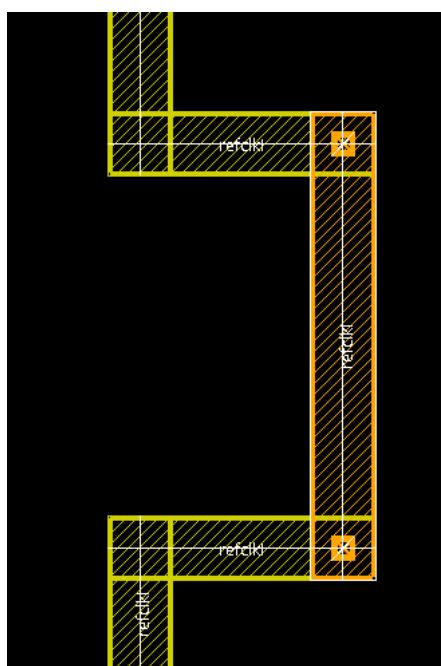
8. To change the layer of a jog segment, select the **vertical segment**.



9. Bring up the Edit Route form, if it is not already.



- In the Edit Route form, change the Vertical layer to **Metal 6**.
- Click the **Change Layer** icon.



- Notice that the layer changes and vias are inserted.

Forcing the Width of a Signal Wire

In addition to routing a nondefault wire with a wide-wire rule defined in the LEF file, you can also use the Wire Editor to force the width of a wire by making it a special wire. With this procedure, you can specify any width for the wire.

In this section, assume that you have just learned that the nondefault width used for the *refclkI* net is too small. You need to make the width of the *wire* the same as the width of the *I/O pad pin*.

1. Make sure that you are in Physical view.
2. To delete the *refclkI* wires, select the **segments**.
3. To display the Select/Delete/Deselect Routes form, press **d**.
4. Change Action to *Delete*.
5. Set Objects to **Selected**, if it is not already.
6. Deselect *Type*, if it is selected.
7. Click **Apply**.
8. Close the Select/Delete/Deselect Routes form.
9. To display the Edit Route form, press **e**.
10. On the Edit Route form, select the **Basic** tab.
11. To populate the Net field and select layers for horizontal and vertical routing, on the I/O pad, place the cursor over Pin C and press **Shift-s**.
12. Under the Edit Route form, select **Create Special Wire**.
13. In the Edit Route form, under the Basic tab, set Vertical Layer to **Metal4** and Width to **2.0**.
14. Click the **Advanced** tab.
15. Select **Snap to Pin** and set to **Auto**, if it is not already.

16. Make sure that the net name in the Nets field is *refclkI*.

17. To change the cursor to a *pencil* icon for wire editing, press **Shift-a** or click the **Edit Wire** icon.



18. To start the horizontal route, **left**-click the I/O pin.



19. **Left**-click to change directions to vertical.

20. Notice that the vertical segment's width is your specified width for M4.

21. **Left**-click to change the direction to horizontal.

22. Complete the horizontal route to the PLL block pin with default *metall* widths.

Tip: Select **Layer M1** and click **Create Regular Wire**.



23. When you get to the pin, **double**-click left to end the route.

24. To select the layers for routing, click the numeric keys (1, 2, 3, and so on).

25. When you finish, save the design and close the software.

Summary

In this lab, you

- ◆ Loaded a design
- ◆ Manually routed a net
- ◆ Swapped vias
- ◆ Modified signal wires
- ◆ Forced the width of a wire to a nondefault width



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Modules 17-18: No Labs

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Module 19: Verification

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Lab 19-1 Using the Verify Commands in a Design

Objective: To use and understand the verify commands to check design rules.

In this lab, you run different verification options in the Innovus™ system.

Loading the Design

1. Make sure that your working directory is the following:

FPR/work/VERIFY

2. To start the software, in an Innovus *csh* window, enter this command:

innovus

3. To load the design for power routing in the *csh* Innovus window, choose **File – Import Design**.

4. At the bottom of the Design Import form, click the **Load** button.

5. Select the **verify.globals** file. Click **Open**.

6. In the Design Import form, click **OK**.

7. Choose **File – Load – DEF**. Select the **tdsp_core_routed.def** file. Click **Open**.

Some errors were created in the DEF file for this lab.

8. To see the detailed routes, change your view to **Physical View**.

Using Verify Connectivity

1. Choose **Verify – Verify Connectivity**.

The Verify Connectivity form is displayed.

2. Make sure you are in **Physical view**. Turn on the **Geometry Loop** option. Click **OK**.

You can also run this option from the command line. Enter the following:

```
verifyConnectivity -geomLoop
```

Several problems including loop problems are reported.

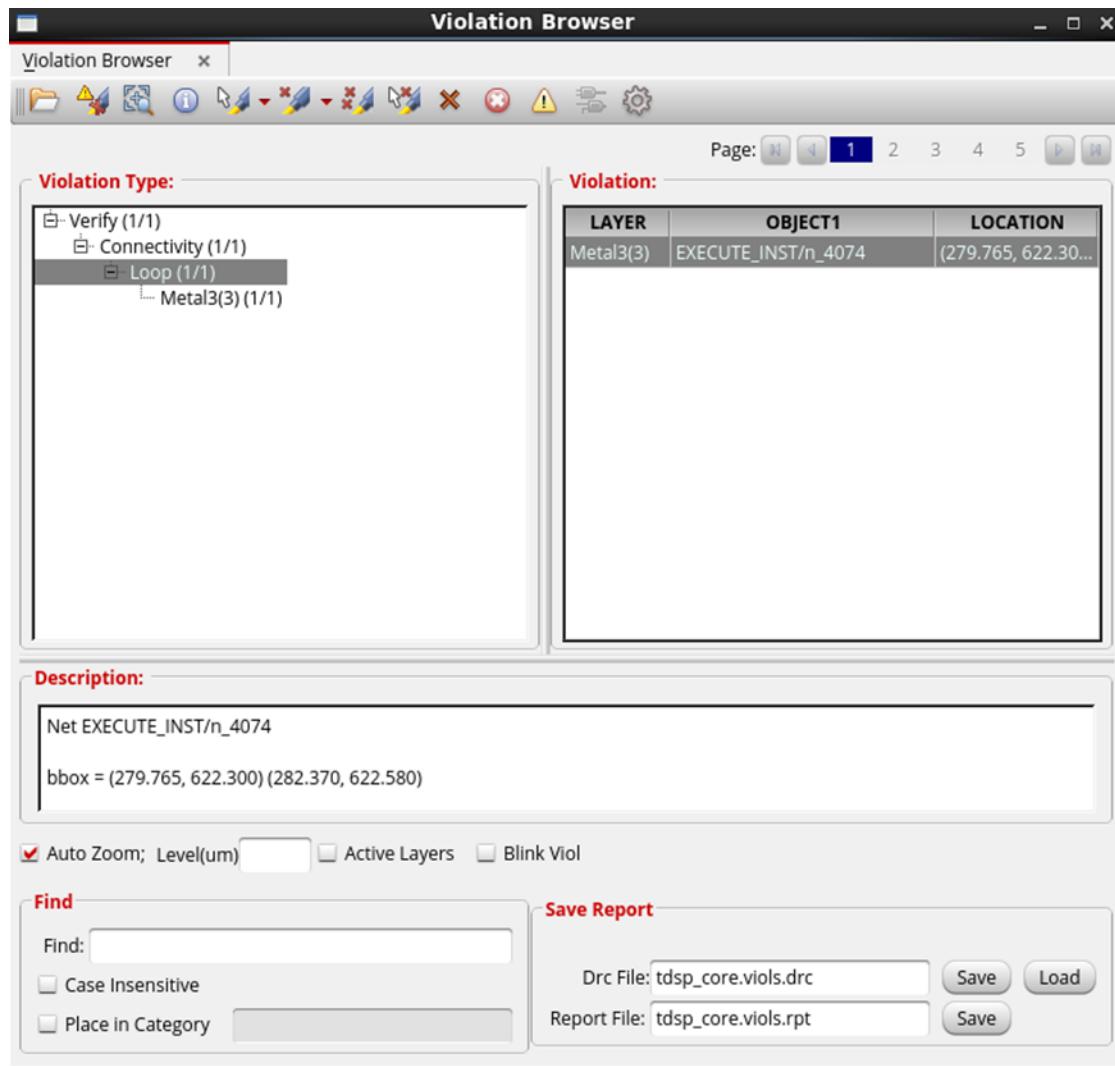
Verification

3. To locate the loop, choose **Tools – Violation Browser**.

The Violation Browser form is displayed.

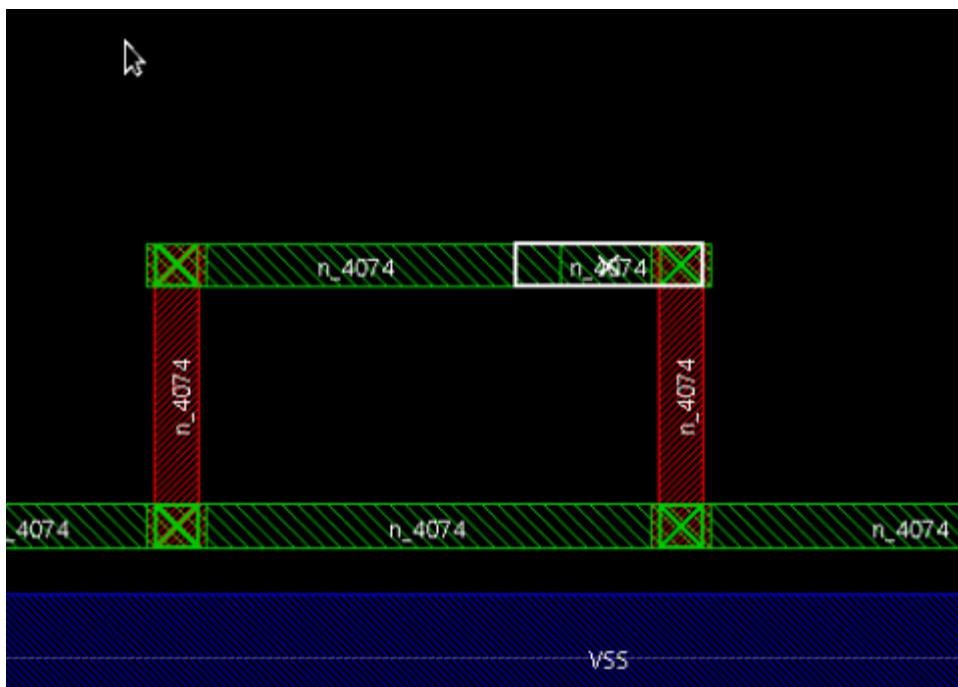
4. To zoom to the violation, select **Loop** under Violation Type.

5. Click the violation on net *n_4074*.

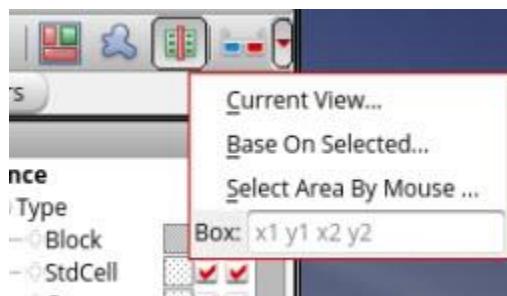


6. Notice the violation displayed.

7. Zoom out to see the entire loop.



8. (Optional) To view the violation using the 3-D, click the **Layout 3-D View** icon and select **Current View**.

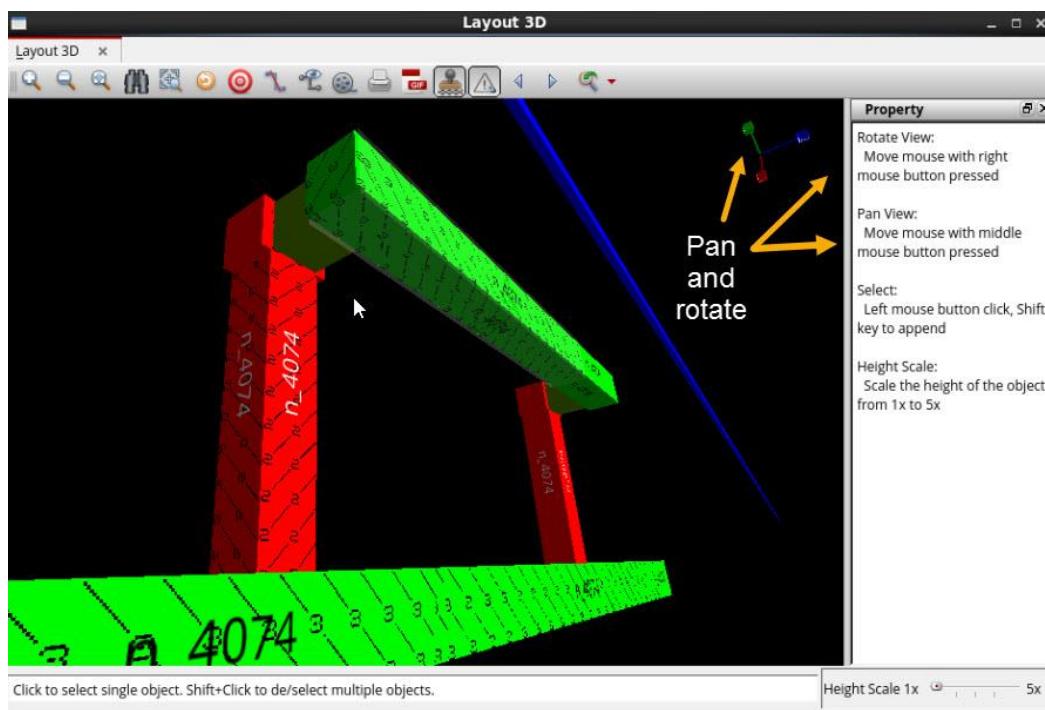


- a. If this step generates a warning about the version of OpenGL that's installed, click **Cancel**. You will not be able to view the 3D view without OpenGL 1.2 or later versions.

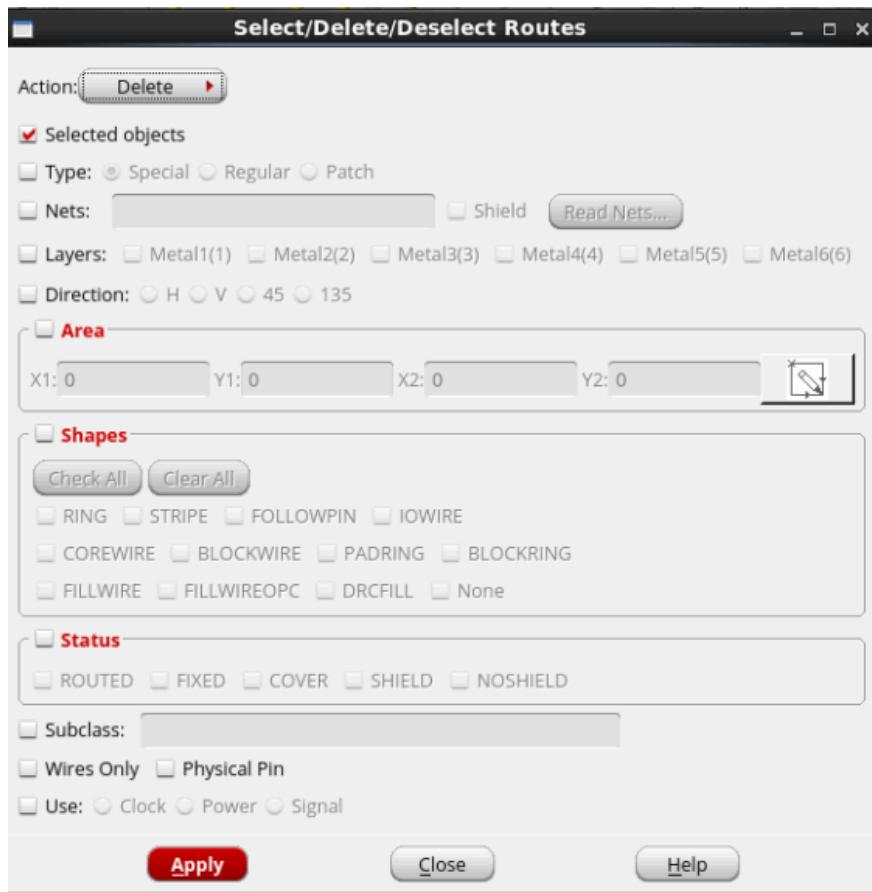


If the above warning is not generated, you will see a new Layout 3D window.

- b. Rotate and pan the loop by using the mouse buttons described in the pane shown along with the 3-D shape.



- c. Close the Layout 3D window.
9. In the Innovus design window, clear the violation marker by pressing **Shift-v**.
10. Select the loop segment.
11. To remove the loop, press **d** to display the Select/Delete/Deselect Routes form.



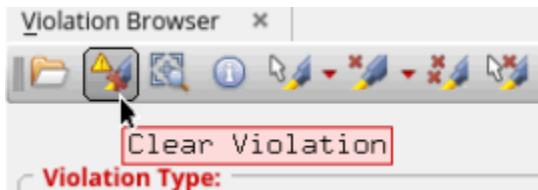
12. In the Action field, select **Delete**.
13. In the Objects field, select **Selected objects**.
14. Click **Apply**.
15. The selected segment is deleted.
16. Repeat the Select and Apply steps until all loop segments are deleted.
17. After you have deleted the loop segments, in the Select/Delete/Deselect form, click **Close**.
18. Rerun the following command to verify if the deleted loop's error has disappeared:
`verifyConnectivity -geomLoop`
There are other unrelated loop errors that remain.

Using Verify Geometry and the Influence Rule

1. From the Innovus *csh* command line, enter the following:

```
zoomBox 330 610 360 640
```

2. Clear all previously flagged violations in the violation browser by clicking the **Clear Violation** icon.



3. Run the command:

```
verify_drc -view_window
```

How many drc violations are flagged?

Answer: _____

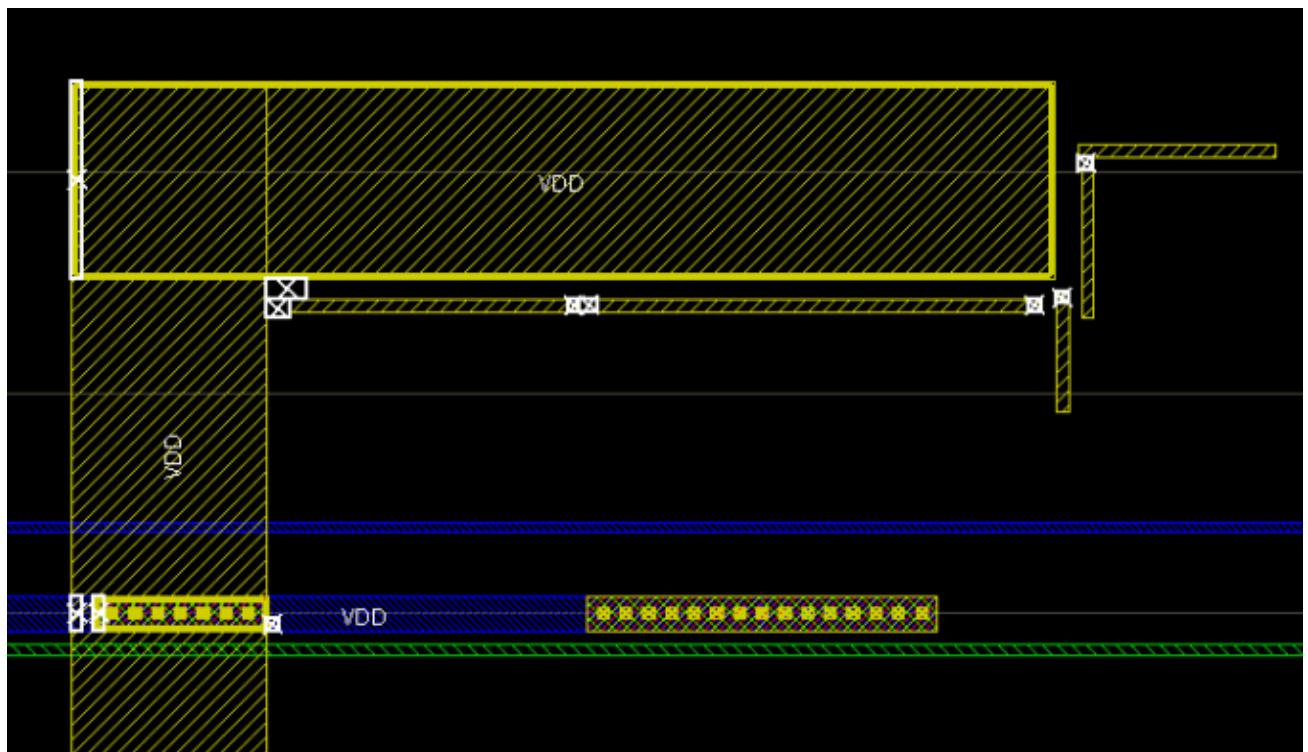
In the violation browser, what are the categories of violations?

Answer: _____

Notice the spacing violations. The corresponding LEF influence spacing rule for METAL 4 is:

```
WIDTH 3.0 WITHIN 0.90 SPACING 0.90 ;
```

If a wire is $3.0\mu\text{m}$ wide or wider, perpendicular wires in a $0.9\mu\text{m}$ halo area around the wide wire need to be spaced by at least $0.9\mu\text{m}$.



4. Close the Verify Geometry form and then the Innovus window.

Summary

In this lab, you

- ◆ Loaded a design with design rule violations
- ◆ Used the Verify flow to find and fix violations
- ◆ Observed how the LEF influence spacing rule is checked in verification



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Module 20: Engineering Change Orders

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Lab 20-1 Loading a Design for ECO Routing

Objective: To start the Innovus™ software, input the required files, and implement an ECO using a Verilog file.

Getting Started

1. Make sure that your working directory is set to the following:

```
FPR/work/ECO
```

2. Compare the *tdsp_core.v* and *tdsp_core_eco.v* files.

The *tdsp_core.v* file is the original netlist. In the *tdsp_core_eco.v* file, the instances connected to the *p_data_out[15]* and *p_data_out[14]* nets have been swapped. To find the nets, search for instances *i_5324* and *i_5331*.

Implementing an ECO in the New Netlist with a Design

1. To start the Innovus software, enter the following:

```
innovus
```

2. In the Innovus **csh** window, run the *ecoDesign* command to read in the original design, read the new Verilog file and implement the ECO:

```
ecoDesign tdsp_core.dat tdsp_core tdsp_core_eco.v
```

The *tdsp_core.dat* is the design corresponding to the original *tdsp_core.v* netlist. The *tdsp_core_eco.v* file contains the required ECO that is implemented. The *ecoDesign* command routes the changes in the netlist.

3. Select **File – Save – DEF** and with defaults selected in the form, write a new DEF file *tdsp_core_routed_eco.def*.

4. Run the following command to compare the original DEF file *tdsp_core.def* (which corresponds to the original Verilog netlist) to the current, changed Innovus ECO database:

```
ecoCompareNetlist -def tdsp_core.def -outfile ecoFile
```

5. View the *ecoFile* and verify the connections have been changed.

If this was a production design, you would continue with the postroute flow if you want, including timing and signal integrity analysis, repair, metal fill and verification.

6. To close the software, choose **File – Exit**.

Summary

In this lab, you ran an ECO and generated a routed design.



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Modules 21-22: No Labs

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Module 23: Innovus Database Access Commands

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Lab 23-1 Using the **dbGet** and **dbSet** Commands

Objective: To report and change the Innovus™ database with the **dbGet** and **dbSet** commands.

1. Make sure that your working directory is set to the following:

FPR/work

2. To start the Innovus software, enter the following:

innovus

3. From your current directory, restore the previously stored design *preCTSopt.inn*. Alternatively, you can restore any other saved design.

4. To return to the command line options of the command, in the Innovus **csh** window, enter the following:

help dbGet

5. Select **head** from the attributes that are available at this level. To return the attributes that are available at this level, enter the following:

dbGet head.?

Some useful attributes at this level are *dbUnits* and *mfgGrid*.

6. To report the values, enter the following command:

dbGet head.dbUnits

What is the value that is returned?

Answer: _____

7. Enter the following command:

dbGet head.mfgGrid

What is the value that's returned?

Answer: _____

8. To list all the attributes and their values, enter the following:

dbGet head.??

The results might not always be readable text, as in this example.

9. To list the layers, enter the following command:

```
dbGet head.layers
```

However, this command returns a hex representation of the layer names.

10. To display text, enter the following command:

```
dbGet head.layers.?
```

The name attribute displays the text.

11. Enter the following command:

```
dbGet head.layers.name
```

What does this command return?

Answer: _____

12. To get to the top level of the hierarchy, enter the following command:

```
dbGet top.?
```

This lists all the attributes that you can query.

13. Try out different attributes. Think of examples of how you can use the results in scripts or how to query only the attributes of your design to check, for example, the instances connected to a selected net.

14. In the design window, select **ROM_512x16_0_INST**.

15. Enter the following command:

```
dbGet selected.?
```

16. To change the size if the halo around the block, enter the following:

```
dbSet selected.pHaloRight 5
```

17. To view the change, refresh the Innovus design window.

18. To query some of the properties of the selected instances, enter this command:

```
dbGet selected.pgTermNets.?
```

19. Explore the attributes and properties that are returned and change them.

20. Save the design as *preCTSopt_db.inn*.

21. Close the Innovus software.

Summary

In this lab, you ran the *db* commands to report and modify the attributes of the design and its objects.



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Module 24: Foundation Flow Scripts

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Lab 24-1 Generating and Running the Foundation Flow Scripts

Objective: To start the Innovus™ platform, generate foundations flow scripts, and run a design through a part of the flow.

Getting Started

1. Make sure that your working directory is set to the following:

FPR/work/FF

2. To start the Innovus software, enter the following:

innovus

Running the Foundation Flow Wizard

1. To see all pull-down menus, widen the design window.

Instead of starting from scratch with the Foundation Flow, you will read in a previously created configuration file to save time.

2. Select **File – Import Design**.

3. Click **Load**.

4. Select **dtsf.globals**.

5. Click **Open**.

6. Click **OK** in the Design Import form.

7. Fit the design to the window by pressing **f** on the keyboard.

- To start the Foundation Flow Wizard, choose **Flows – Foundation Flow Wizard**.



- Select **Load the design setup from memory**.

- Click **Load**.

- Click **Continue**.

- Enter the process node as **130nm**.

In this example, the technology part of the LEF file and the physical LEF models for the standard cells and macros are contained in one file. The LEF file field has automatically been filled in because you have read in the *.globals* file in an earlier step.

- Click **Continue**.

14. Review the setup and click **Continue**. This will bring up the Specify Verilog Netlist and Floorplan form.

15. Make sure the Verilog field and Design Name fields are populated.

16. In the Use the floorplan file field, enter **../dtmf.fp**.



17. In the Power Net Name field, make sure that **VDD is specified**.

18. In the Ground Net Name field, make sure that **VSS is specified**.

19. Click **Continue**. If you cannot click **Continue**, click **Back** and **Continue** again.

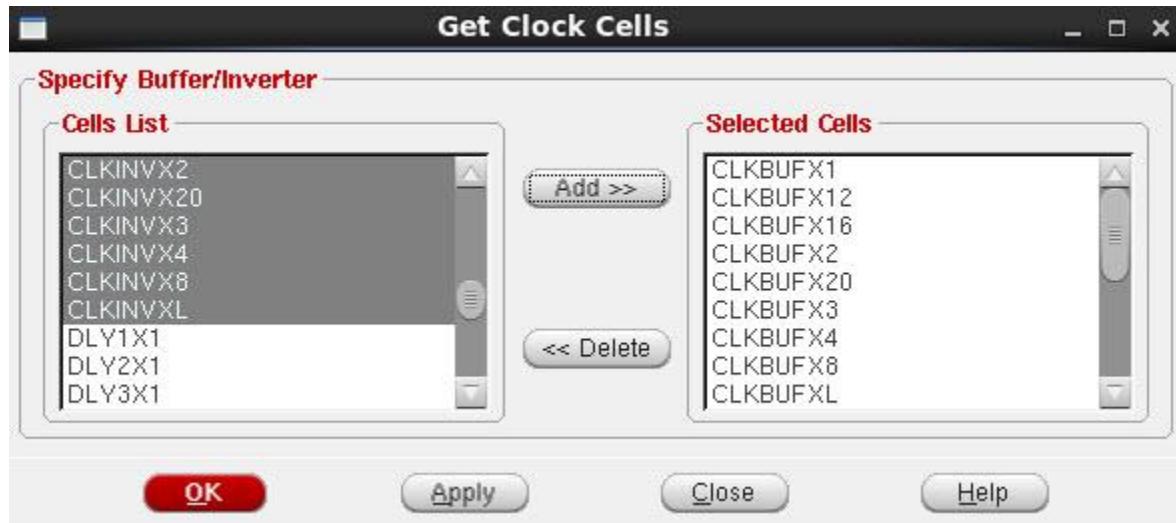
This will display the Setup Your Clock Tree Synthesis Constraints form.

20. Select **Automatically by Innovus using the following clock cells:**

21. Click **Select**.

22. Select **CLKBUFX1** under the Cells List and press and hold the **Shift** key to select all the cells that begin with a CLK.

23. Press **Add** so that the cells appear under Selected Cells.



24. Click **OK**.

25. Click **Continue**.

When the form is displayed, review your design setup. Make sure that the information that you see is correct.

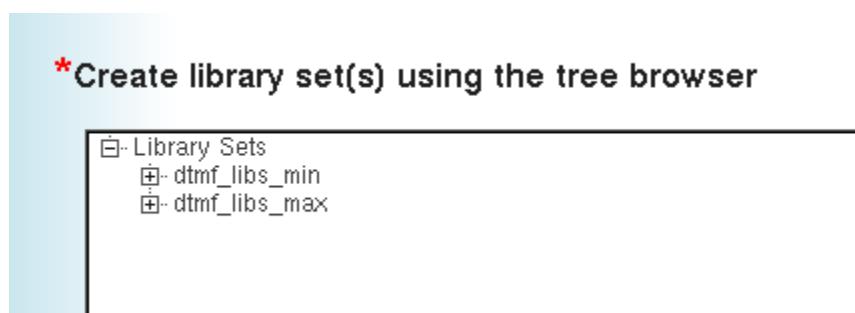
26. Click **Continue**.

27. Click **Continue**.

The Setup Your Design for Timing-Driven Place and Route form is displayed.

28. With default selections, click **Continue**. This will display the Create Timing Library Sets form.

29. The library sets have been created because you read in the globals file which pointed to the *dtsf.view* file containing the MMMC setup information.



30. Click **Continue**.

This will display the Create RC Extraction Corners form.

31. Click **Continue**. This will display the Create Delay Corner Sets form.

32. Notice that there are two corners that have been created: *dtsf_corner_min* and *dtsf_corner_max*.

33. If the pane is greyed out, press **Back** and then the **Continue** button.

34. To display the Create Constraint Modes form, click **Continue**.

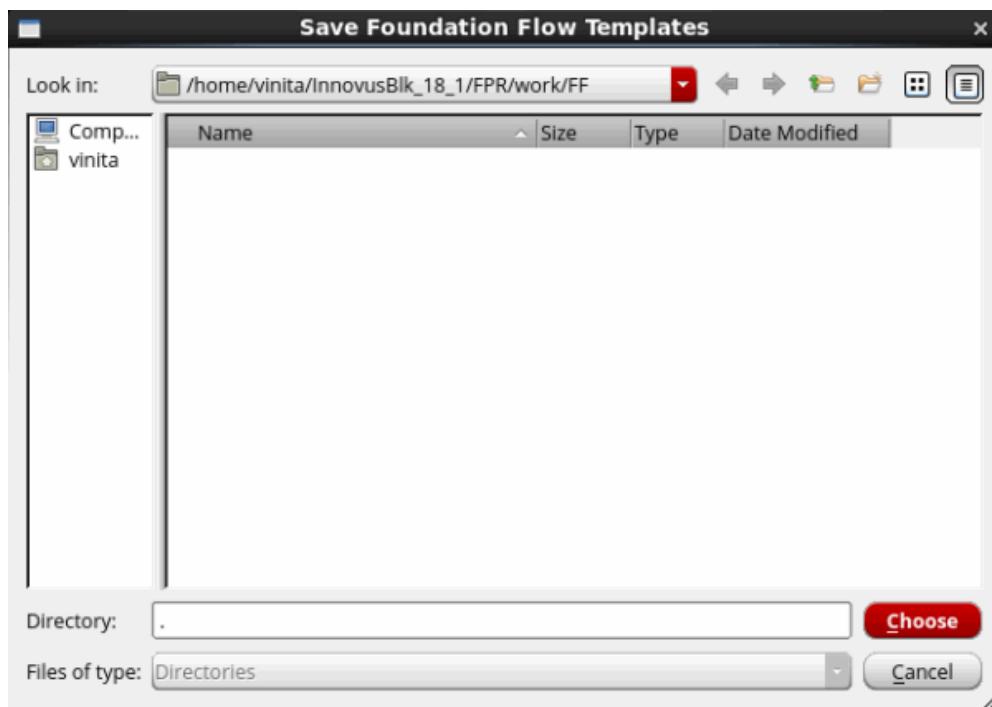
35. To display the Create Analysis Views form, click **Continue**.

36. Review your setup.

37. Click **Continue**.
38. In the interest of time, to accept the defaults in the Setup Your Power form, click **Continue**.
39. To display the Set Up Tool Specific Options form, click **Continue** again.
40. Click **Continue** repeatedly until you see the final screen that completes your foundation flow setup.
41. Click **Done**.
42. To save all your files, click **OK** in the **Save Scripts** form.
43. To save the scripts that are needed to run the next step, in the Innovus window, choose **Flows – Create Foundation Flow Template – Save**.
44. Make sure that the directory that is set is the following:

FPR/work/FF

45. Enter a period (.) in the directory field.



46. Click **Choose**.

47. Exit the Innovus platform.

Generating Foundation Flow Scripts and Adding a Plugin

Now you use the generated *setup.tcl* to generate Foundation Flow scripts.

1. In a separate *csh* window, run the following commands to replace the generated *SCRIPTS* directory with the corrected *SCRIPTS* directory, making sure that you are in the FF directory:

```
mv SCRIPTS SCRIPTS.old  
mv SCRIPTS.save SCRIPTS
```

Because of an error in some versions of the Innovus software, the generated scripts in the *SCRIPTS* directory will not run as expected. Therefore, a corrected *SCRIPTS.save* directory has been created and saved in the FF directory.

2. Run the following command:

```
tclsh SCRIPTS/gen_flow.tcl -d . all
```

This command uses the Foundation flow code generator to generate the scripts required for implementation, as well as the makefile.

3. In a separate *csh* window, change to the plugin directory by entering:

```
cd PLUG/INNOVUS
```

4. Edit the *pre_place.tcl* file to add a command to read in a scan DEF before placement.

```
defIn ../scan_input.def
```

```
File Edit View Search Terminal Help  
#####  
# PRE-PLACE PLUG-IN  
#  
# This plug-in script is called before placeDesign from the run_place.tcl flow  
# script.  
#  
# Example tasks include:  
#     - Power planning related tasks which includes  
#         - Power planning for power domains (ring/strap creations)  
#         - Power Shut-off cell power hookup  
#####  
defIn ../scan_input.def
```

5. Save the file.

6. In the *work/FF* directory, copy the following file:

```
cp inn_config.tcl innovus_config.tcl
```

7. Edit the *innovus_config.tcl* to **uncomment** the *pre_place_tcl* variable and to point to the plugin file that you modified.

```
set vars(pre_place_tcl)
"PLUG/INNOVUS/pre_place.tcl"

#####
# Define user plug-ins scripts ...
#-----
#set vars(always_source_tcl)      ""
#set vars(pre_init_tcl)          ""
#set vars(post_init_tcl)         ""
set vars(pre_place_tcl)          "PLUG/INNOVUS/pre_place.tcl"
#set vars(place_tcl)             ""
#set vars(post_place_tcl)        ""
#set vars(pre_prects_tcl)        ""
#set vars(post_prects_tcl)       ""
```

8. View the makefile called *Makefile*. Notice that there are steps that correspond to the major flow steps in implementation.

9. To run Innovus placement, use the following command:

```
make place
```

10. Verify that the plugin that you created is being picked up by the scripts. The log message should look something like the following:

```
-----
<FF> CODE GENERATION COMPLETE
<FF> ... VERSION -> 18.1
<FF> ... RUN DIRECTORY -> /FPR/work/FF
<FF> ... SCRIPTS -> .
<FF> ... PLUGINS -> 1 defined, 1 found
<FF> ... REPORT -> ./check.rpt
```

What is the WNS and TNS after placement?

Answer: _____

What are the other implementation steps that you can run through the makefile?

Answer: _____

11. If time permits, run additional make commands and record the slack.

Summary

In this lab, you

- ◆ Used the Foundation Flow Wizard to create a *setup.tcl* file.
- ◆ Used the *setup.tcl* file and the Foundation Flow code generator to create scripts and run though parts of the implementation flow.

