2022 Digital IC Design

2016 IC Design Contest Preliminary : Local Binary Patterns, LBP

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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | Clock  width | 1(ns) | Gate-level simulation time | 29850 (ns) |
|  | | | | |  | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 1229/68416 | | | |
| Total memory bit | | | | | 0/1152000 | | | |
| Embedded multiplier 9-bit element | | | | | 0/300 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 把這題切成8個state，idle\_st作為一開始初始的狀態，當gray\_ready再開始進入功能操作的狀態，且將lbp\_addr設在128，接著read\_col\_st作為讀取一開始左邊和中間的直行，當讀取到第三個就進入read\_mv\_st，從左邊行換到讀中間行。當讀取完最左邊和中間的行之後，開始讀取最右邊那行的三個值，讀取最左上角的值的同時，將最左邊那行和最中間的值做比較。而因為大於中間的值要乘上一個倍率放入lbp\_data中，因此只要把大於中間的的那一格對應到lbp\_data的bit來存取1或0就好。讀取中間最右邊的值同時也做最中間那行與中間值的比較，且將原先中間的值左移到data暫存器的最左邊。讀取最右下角的值時，直接將讀取值存到data暫存器的中間最下面，因此data只要有7個暫存器儲存值。再來到輸出狀態，將lbp\_data輸出且把最右邊的上面兩個值左移到data暫存器中間。在此狀態也同時比較是否為最左右兩行，若是則lbp\_valid設為0 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (longest gate-level simulation time in ns)*