Data Sheet November 1, 2013 FN6742.2

Filterless High Efficiency 1.5W Class D Mono Amplifier

The ISL99201 is a fully integrated high efficiency class-D mono amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum requirement of external components and operates from a 2.4V to 5.5V input supply. It is capable of delivering 1.4W of continuous output power with less than 1% THD+N driving a 8Ω load from a 5V supply.

The ISL99201 features a high-efficiency, low-noise modulation scheme. It operates with 86% efficiency at 400mW into 8Ω and has a signal-to-noise ratio (SNR) that is better than 95dB. The ISL99201 has a micro-power shutdown mode with a typical shutdown current of 200nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The architecture of the devices allows it to achieve very low level of pop-and-click. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation.

The fully differential input of the ISL99201 provides excellent rejection of common mode noise on the input typically 75dB. EMI suppression is achieved by SRC (Slew Rate Control).

The ISL99201 oscillator can be synchronized to an external clock through the SYNC input, allowing the switching frequency to be externally defined. The SYNC input also allows multiple ISL99201 to be cascaded and frequency locked; minimizing interference due to clock intermodulation.

The ISL99201 also has excellent rejection of power supply noise, including noise caused by GSM transmission bursts and RF rectification. PSRR is typically 75dB at 217Hz. There will be 4 versions of the part; they will consist of three fixed gain settings (6dB, 9. 6dB, 12dB) and one user programmable gain setting (need external resistors).

The ISL99201 has built-in thermal shutdown and output short-circuit protection.

Features

- Filterless class D with efficiency > 86% at 400mW
- Click-pop suppression
- Slew rate control
- Spread spectrum switching
- Optional SYNC pin for master/slave operation without interface
- 1.4W into 8Ω with less than 1% THD+N
- 2.4V to 5.5V single supply voltage
- Built-in resistors to reduce board component count
- Only one external component required (Fixed gain mode)
- Short circuit and thermal protection
- Gain programmable 6dB, 9.6dB, 12dB and User programmable
- Pb-Free (RoHS compliant)

Applications

- Mobile phones
- MP3 players
- Portable gaming
- Portable electronics
- Educational toys

Ordering Information

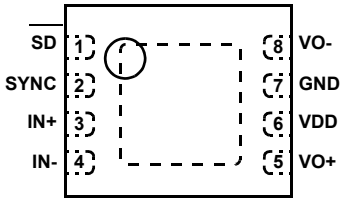
PART NUMBER	PART MARKING	GAIN SETTING (dB)	TEMP. RANGE (°C)	PACKAGE Tape and Reel (Pb-Free)	PKG. DWG. #
ISL99201IRTAZ-T (Notes 1, 2)	201A	6	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTAZ-TK (Notes 1, 2)	201A	6	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTBZ-T (Notes 1, 2)	201B	9.6	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTBZ-TK (Notes 1, 2)	201B	9.6	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTCZ-T (Notes 1, 2)	201C	12	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTCZ-TK (Notes 1, 2)	201C	12	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTDZ-T (Notes 1, 2)	201D	Prog.	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTDZ-TK (Notes 1, 2)	201D	Prog.	-40 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL99201IRTAEVZ	Evaluation Board				
ISL99201IRTBEVZ	Evaluation Board				
ISL99201IRTCEVZ	Evaluation Board				
ISL99201IRTDEVZ	Evaluation Board				

NOTES:

1. Please refer to TB347or details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-20.

Pinout

ISL99201
(8 LD TDFN)
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

Supply Voltage . . . . . -0.3V to 6V
Input Voltage . . . . . -0.3V to V_{DD}+0.3V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Operating Supply Voltage (VDD Pin) . . . . . 2.4V to 5.5V

Thermal Information

Thermal Resistance (Typical Note 3) θ_{JA} (°C/W)
TDFN Package 53
Maximum Junction Temperature (Plastic Package) -65°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation Ratings
8 Ld 3x3 TDFN
Derating Factor . . . . . 21.8mW/°C
Power Ratings
T_A = +25°C. 2.7W
T_A = +70°C 1.7W
T_A = +85°C. 1.4W
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379

Electrical Specifications Typical Values Are Tested at V_{DD} = 5V and the Ambient Temperature at +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
Output Power	P_o	R_L = 8Ω, THD = 10%, f = 1kHz, 20kHz BW, V_{DD} = 5.0V		1.4		W
		R_L = 8Ω, THD = 10%, f = 1kHz, 20kHz BW, V_{DD} = 3.6V		0.75		W
		R_L = 8Ω, THD = 10%, f = 1kHz, 20kHz BW, V_{DD} = 2.5V		0.4		W
		R_L = 8Ω, THD = 1%, f = 1kHz, 20kHz BW, V_{DD} = 5.0V		1.15		W
Efficiency	η	P_{OUT} = 1.4W, 8Ω + 33µH, V_{DD} = 5.0V		90		%
Total Harmonic Distortion + Ratio	THD+N	P_O = 1W into 8Ω each channel, f = 1kHz, V_{DD} = 5.0V		0.05		%
		P_O = 0.5W into 8Ω each channel, f = 1kHz, V_{DD} = 3.6V		0.05		%
		P_O = 0.2W into 8Ω each channel, f = 1kHz, V_{DD} = 3.6V		0.09		%
Common-Mode Rejection Ratio	CMRR	V_{IC} = 0.5V to (V_{DD} - 0.8V); R_L= 8Ω, V_{DD} = 2.5V to 5.5V		-60		dB
	$CMRR_{GSM}$	V_{CM} = 2.5V ± $1V_{P-P}$ at 217Hz, R_L= 8Ω		-60		dB
Average Switching Frequency	f_{sw}	V_{DD} = 5V	300	375	450	kHz
Differential Output Offset Voltage	V_{OOS}	G = 6dB; 9.6dB; 12dB; 28dB.		0.2	5.0	mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}		2.4		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.0V		-65		dB
	$PSRR_{GSM}$	V_{RIPPLT} = $100mV_{RMS}$ at 217Hz (Input AC-Coupled with 2µF capacitor)		-65		dB
Supply Current	I_{IN}	V_{IN} = 0V, No load, V_{DD} = 5V		3.9		mA
		V_{IN} = 0V, No load, V_{DD} = 3.6V		3.2	3.75	mA
		V_{IN} = 0V, 8Ω + 33µH, V_{DD} = 5V		3.9		mA
		V_{IN} = 0V, 8Ω + 33µH, V_{DD} = 3.6V		3.8		mA
	$I_{\overline{SD}}$ (Note 4)	$\overline{SD}$ = GND		0.2	0.4	µA

Electrical Specifications Typical Values Are Tested at V_{DD} = 5V and the Ambient Temperature at +25°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
GAIN CONTROL						
Closed-Loop Gain		D version user program (Max Gain, Ri = 0Ω)	27.5	28.5	29.5	dB
		A version	5.7	6	6.3	dB
		B version	9.2	9.6	10	dB
		C version	11.5	12	12.5	dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = V_{DD}, A version		70		kΩ
		$\overline{SD}$ = V_{DD}, B version		46.25		kΩ
		$\overline{SD}$ = V_{DD}, C version		35		kΩ
		$\overline{SD}$ = V_{DD}, D version, Ri = 2.5kΩ		7.5		kΩ
		$\overline{SD}$ = GND		100		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}			1.2		V
Input Voltage Low	V_{IL}			0.5		V
Turn-on Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		3.5		ms
Turn-off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	E_n	V_{DD} = 3.6V, f = 20Hz to 20kHz, inputs are AC grounded, A_V = 6dB, A-weighting		27		µV
		V_{DD} = 3.6V, f = 20Hz to 20kHz, inputs are AC grounded, $A_{V\,0}$ = 6dB, no weighting		35		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 1W, R_L = 8Ω		102		dB

NOTES:

4. Limits established by Characterization and are not production tested
5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Pin Descriptions

SD

Shutdown Active Low. This signal is used to shut down and activate the part. It is 1.8V to 5V compatible. During shutdown, the part draws less than 100nA input current. Coming out of shutdown takes 3.5ms and going into shutdown is instantaneous.

SYNC

External clock input. This pin allows the chip to be synchronized to a system clock. This helps in folding the spectral components and the switching harmonic out of band of interest. The range of SYNC frequency is from 250kHz to 800kHz.

IN+

Positive Differential Input.

IN-

Negative Differential Input.

V_O+

Positive BTL output.

GND

Ground.

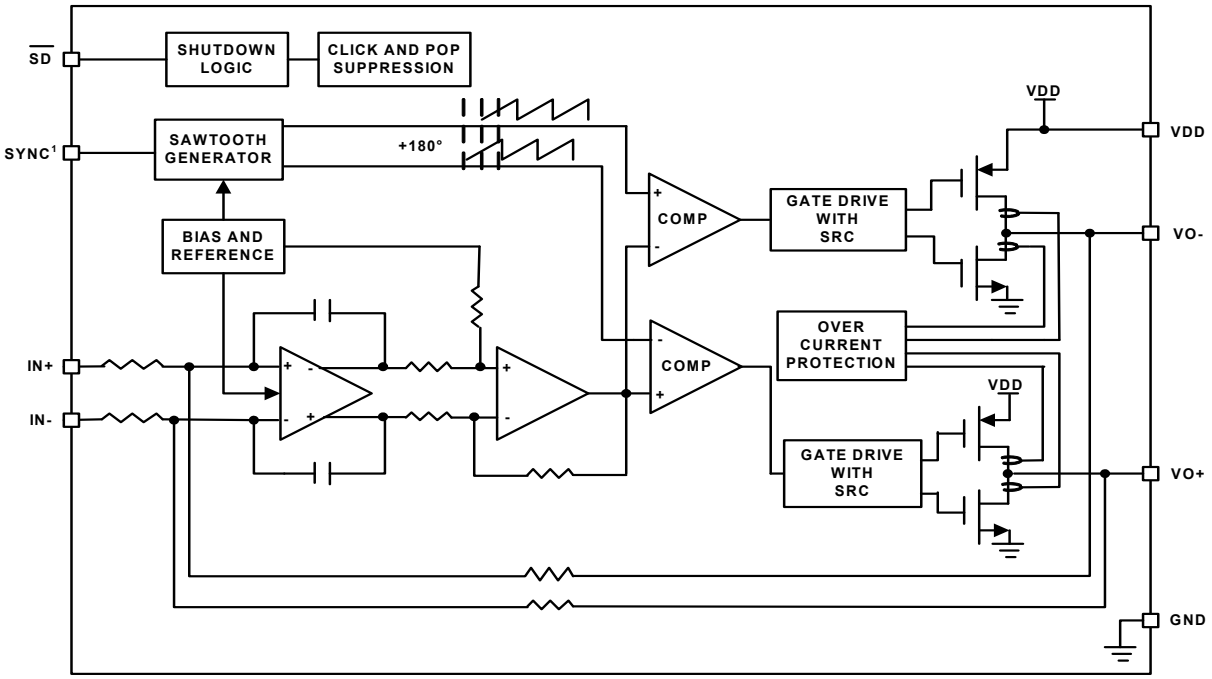
V_{DD}

Power Supply.

V_O-

Negative BTL output.

Block Diagram *(Notes)*



Notes:
Gain = 6dB, 9.6dB, 12dB (gain setting)

Gain = $\frac{140k\Omega}{(Ri + 5k\Omega)}$; with external resistor

Typical Performance Characteristics

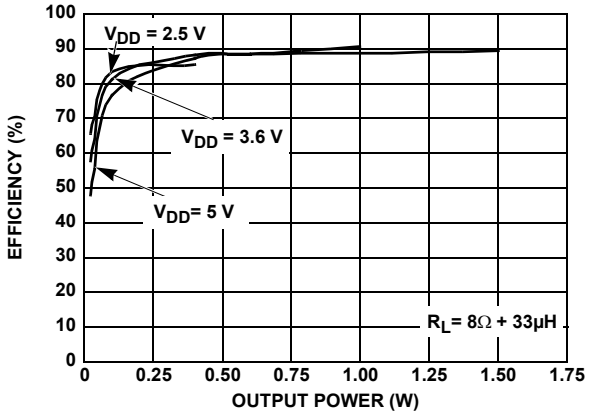


FIGURE 1. EFFICIENCY vs OUTPUT POWER

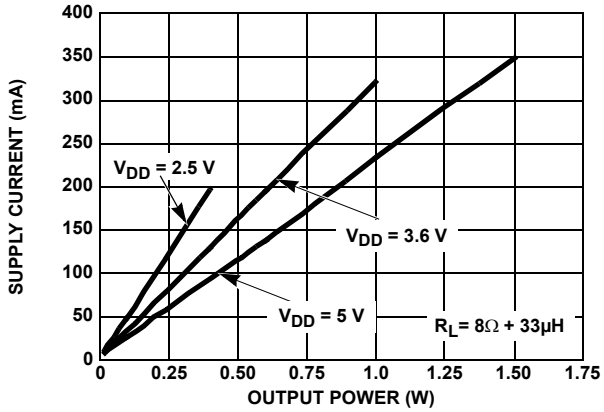


FIGURE 2. SUPPLY CURRENT vs OUTPUT POWER

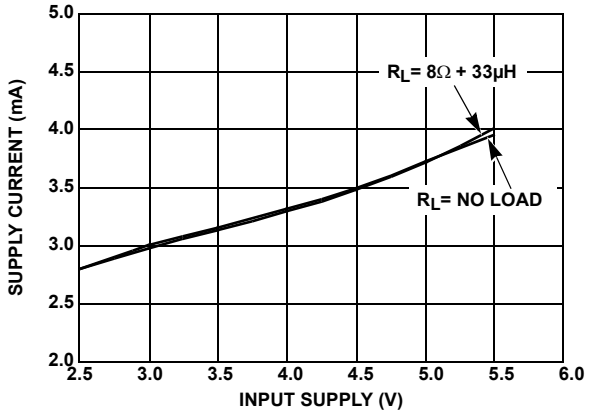


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

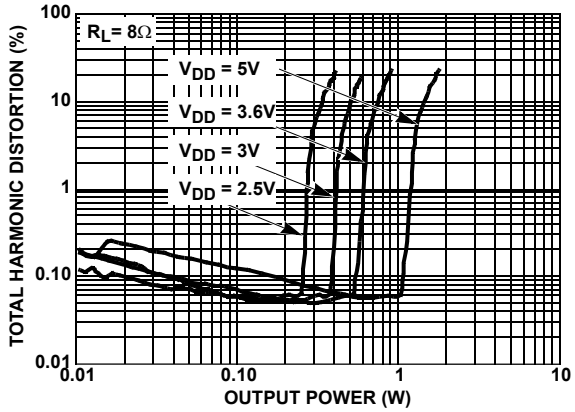


FIGURE 4. TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

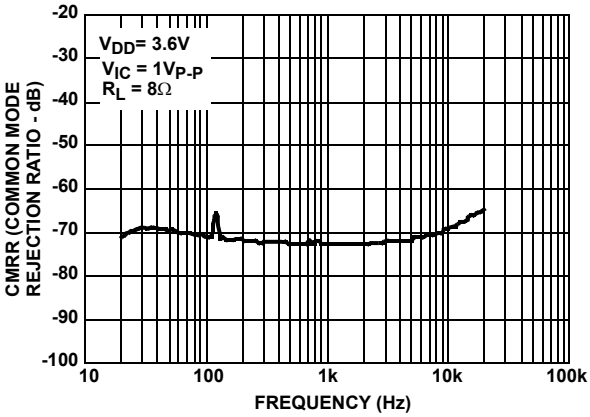


FIGURE 5. COMMON MODE REJECTION MODE vs FREQUENCY

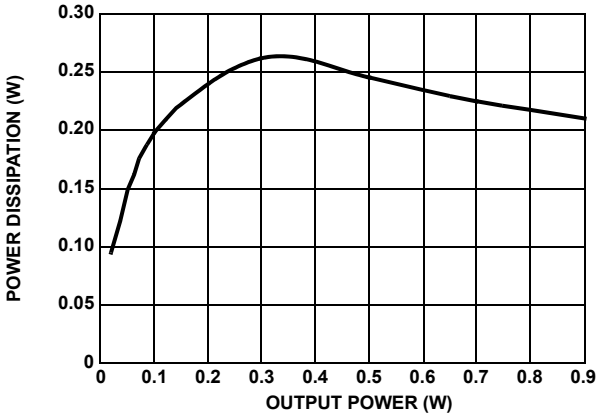


FIGURE 6. POWER DISSIPATION vs OUTPUT POWER

Typical Performance Characteristics (Continued)

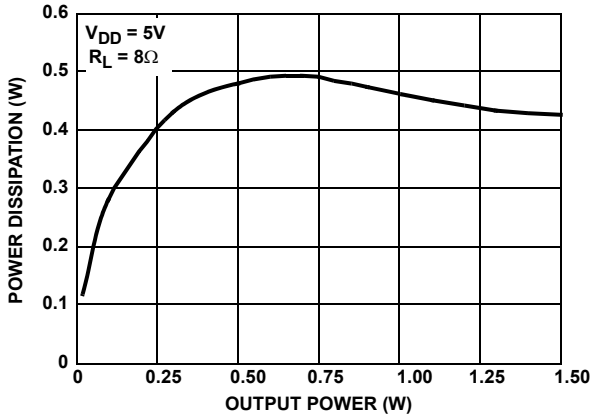


FIGURE 7. POWER DISSIPATION vs OUTPUT POWER

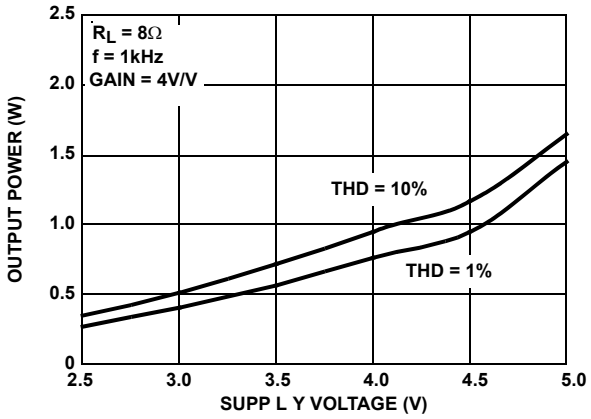


FIGURE 8. OUTPUT POWER vs SUPPLY VOLTAGE

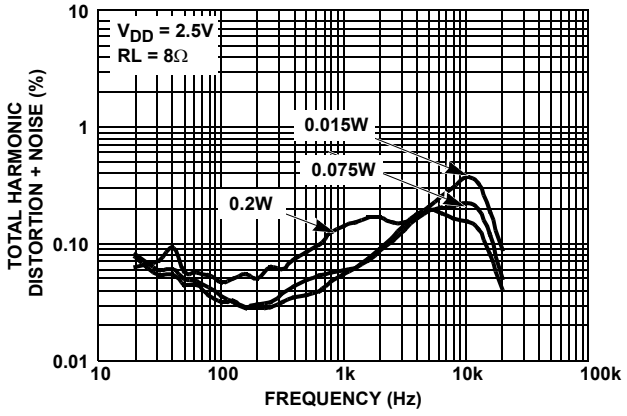


FIGURE 9. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

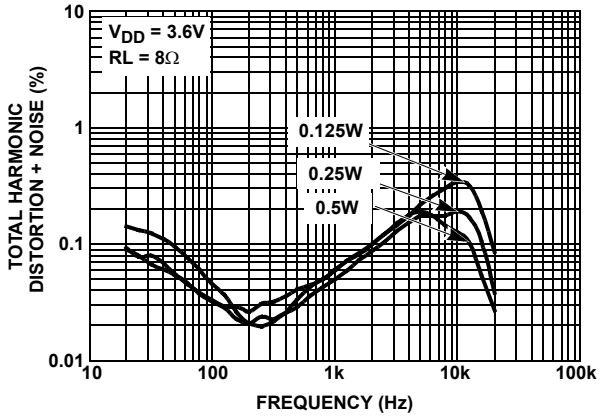


FIGURE 10. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

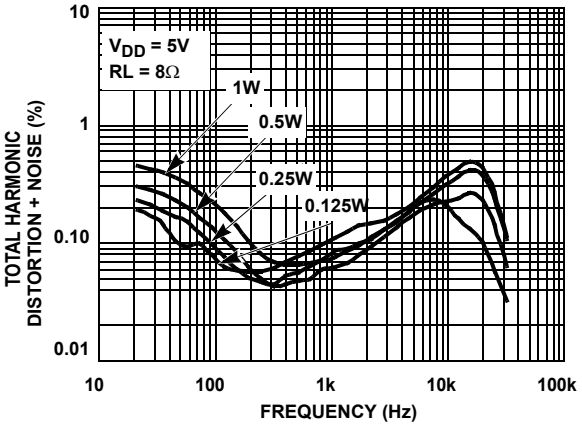


FIGURE 11. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

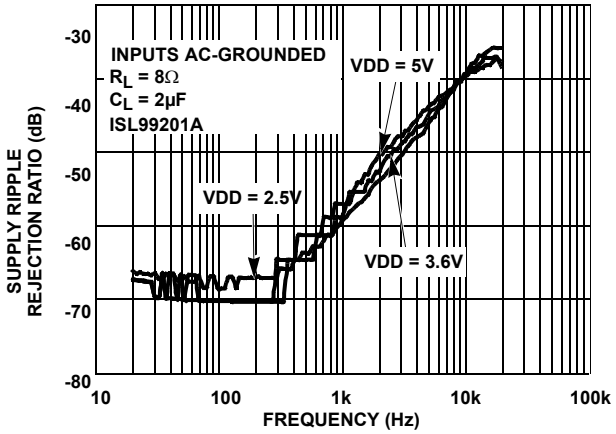


FIGURE 12. SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - ISL99201A

Typical Performance Characteristics (Continued)

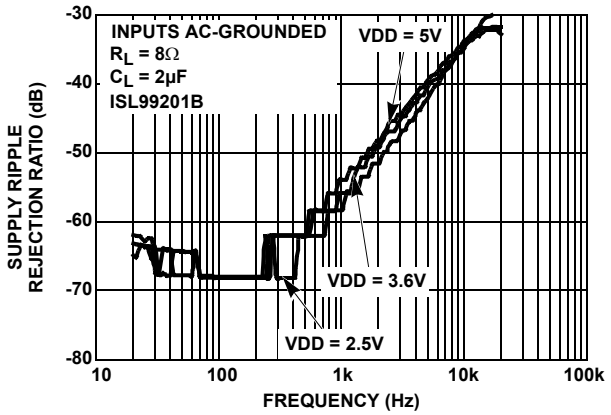


FIGURE 13. SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - ISL99201B

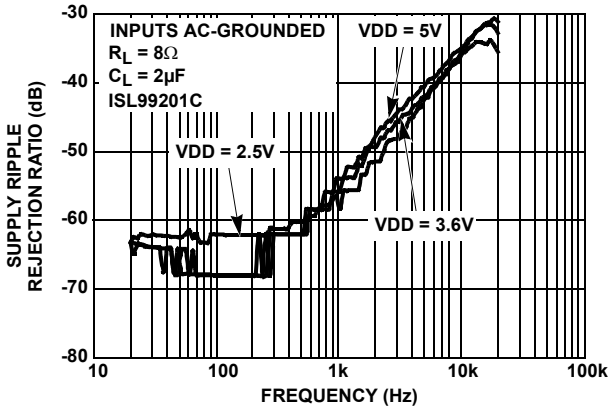


FIGURE 14. SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - ISL99201C

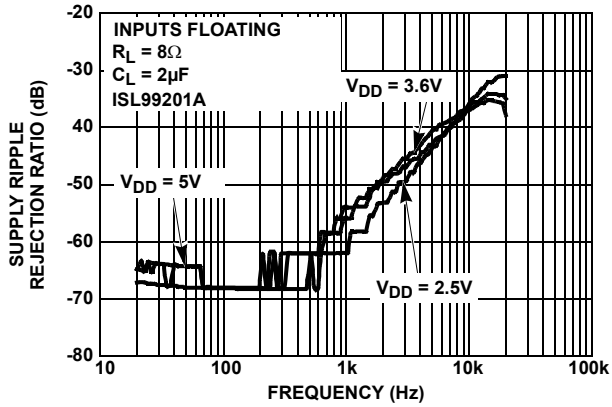


FIGURE 15. SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - ISL99201A

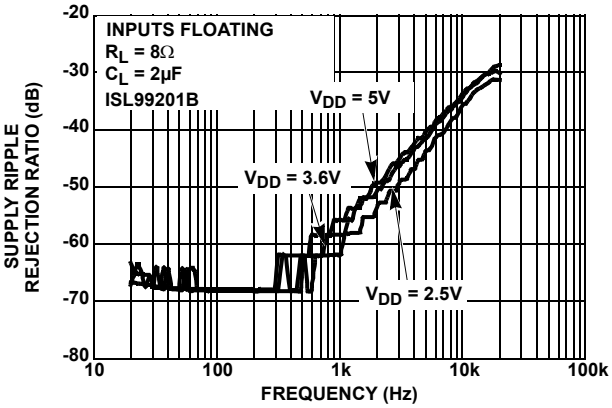


FIGURE 16. SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - ISL99201B

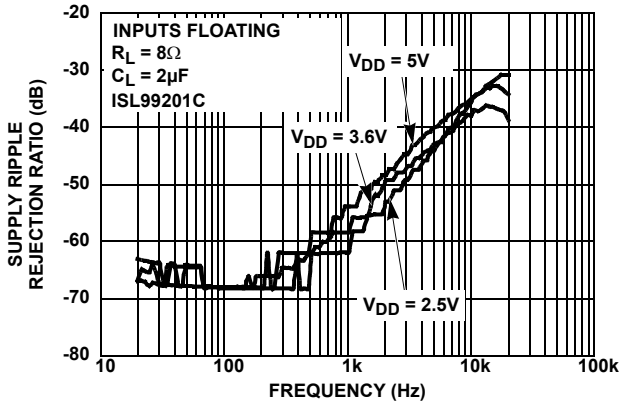


FIGURE 17. SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - ISL99201C

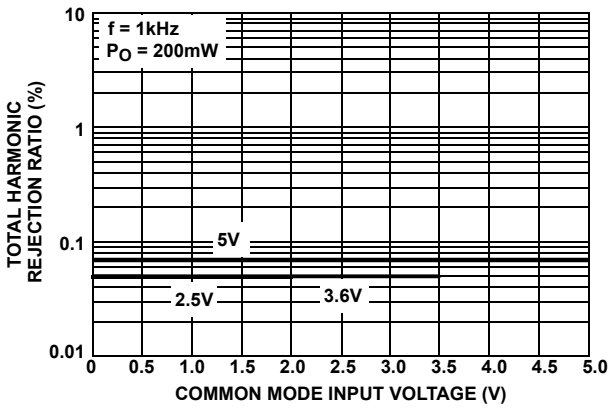


FIGURE 18. TOTAL HARMONIC DISTORTION + NOISE vs COMMON MODE INPUT VOLTAGE

Typical Performance Characteristics (Continued)

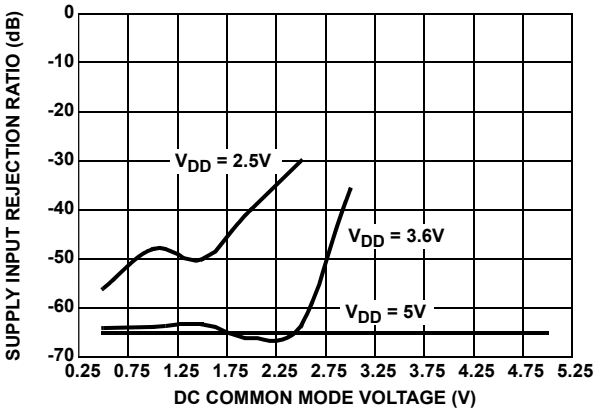


FIGURE 19. SUPPLY RIPPLE REJECTION RATIO vs DC COMMON MODE VOLTAGE

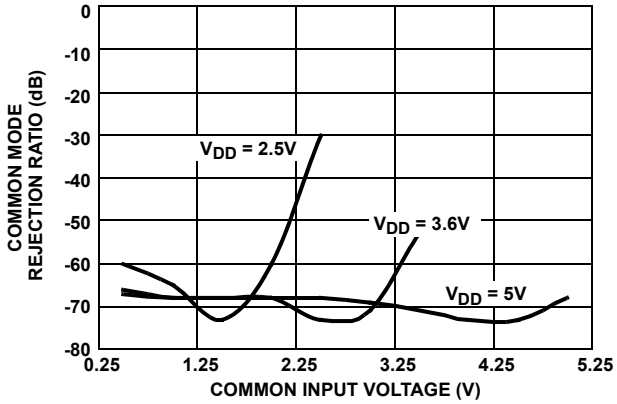


FIGURE 20. COMMON MODE REJECTION RATIO vs COMMON MODE INPUT VOLTAGE

Typical Applications

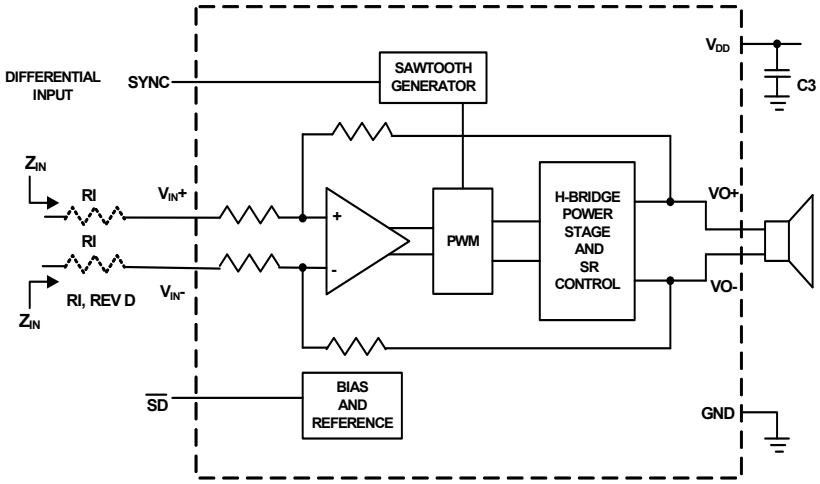


FIGURE 21. TYPICAL CIRCUIT WITH DIFFERENTIAL INPUT

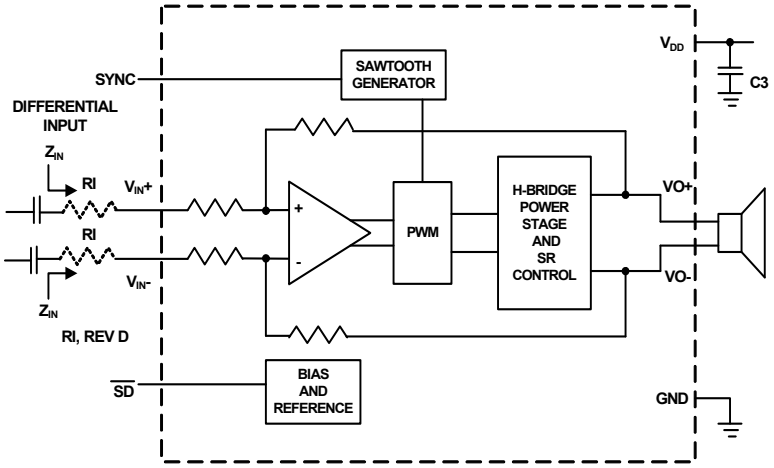


FIGURE 22. TYPICAL CIRCUIT WITH DIFFERENTIAL INPUT AND INPUT CAPACITORS

Typical Applications (Continued)

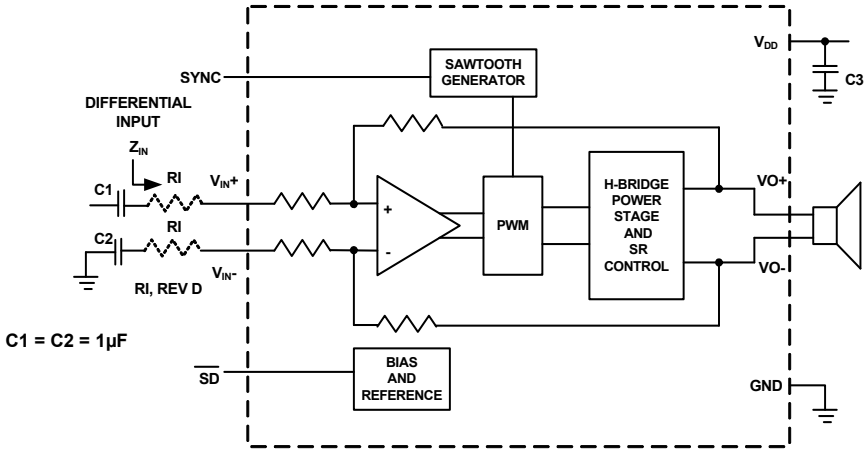
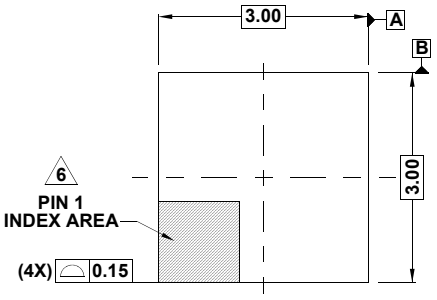


FIGURE 23. TYPICAL CIRCUIT WITH SINGLE-ENDED INPUT

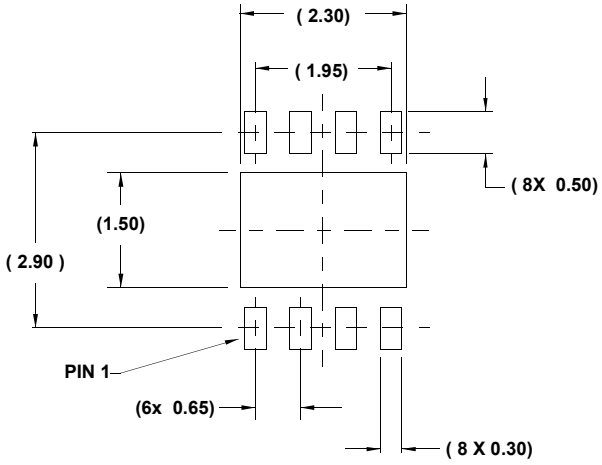
Package Outline Drawing

L8.3x3A

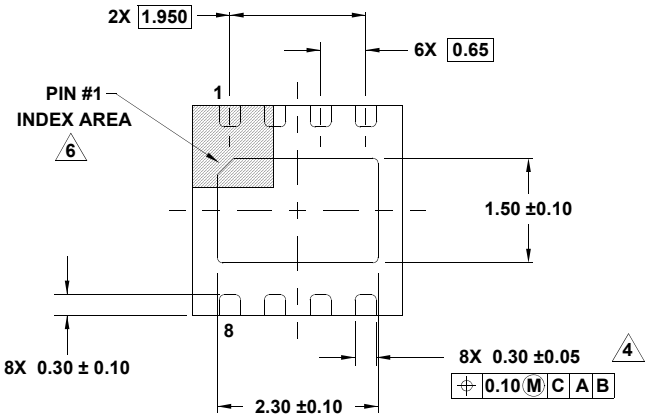
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



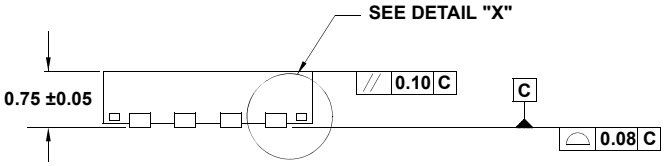
TOP VIEW



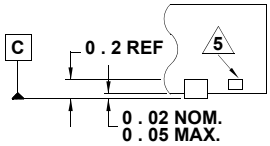
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.