CmpEzyto Sept.7

Example: Registerfile Note: 1º LACITED from 2022S Special Purpose Registers General Purpose Register Semester, Waiting List. CANVAS. SCOH. GPX CON Zº LPC1768 Pin-to-pin 9 Root Conpatable (Mbed) Prefix 3 Letters a. Stepl. MCW/spresso IDE for Port "x", X=0,1,2,3 1768 Binary Lode. Step Z. "Firmware" Upload the binary bile to the its address is 32 Bits, it maps to the memory Flash. Need a prob Step3. Internative Debugging. 3° LPCIICZY Pigi-Keyin Stock. LPC1114 Size GPP/SPI, FLASH (ON-Chip) 1/8 of the size Comparing to LEC17689 Honework (OPT) Nate: The Task of Init & Config 1. Form A Team By Wednesday
4-Pevson Can be realized by using HLL (Highlevel Language), C/C++, 2. Select/Finalize your target

to deposit A Binary Pattern to that

Memory Location (Addr. is a Pointer)

Platform. By the end of the week.

	(mpE240
	Sept.7
	For Example for Sansing ARM-11.
	GPAGNULISJ GPACON [7:4]
	m
	GPX CON it = address is 32 Bits, it maps to the memory  Map.
	it maps to the memory
	Map.
	Design Regnirements (Spec.)
_	1. 2nd Bit AS An Dutent
	1. 2nd Bit AS An Dutent 2. 3rd Bit AS An Imput
	To perform Init & Config.
*	GPAGN []:4] = 000) = 0x1
	7,18.1
	GPACON [11:8] = 0000 = 0 XO
Ħ	3rdBit
1	GPXDAT Input
	Y'X'

GPACON[3|:4] = 0×10