CMPE240
Spring2023

1/

Jan25,23.

Today's Topics:

1° Syllabus, "Greensheet" of the Class.

San José State University
College of Engineering/Computer Engineering Department
CMPE240 Advanced Microcomputer Design

S2023

Professor Hua Harry Li
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Email hua.li@sjsu.edu
Class Time: Mondays and Wednesdays 1:30-2:45 PM
Office Hours: Mondays and Wednesdays 4:30 – 5:30 PM Zoom
Zoom link: Join Zoom Meeting https://us04web.zoom.us/j/9841607683?pwd=UlA3aEk1TnV4bjNLQk5CQkw0dDk4UT09 Meeting ID: 984 160 7683 Passcode: 121092
Lecture Room: Engineering Building Room 303
Lab facility: Engineering Building Room 268
Prerequisites

Note: 1° Attendance; 2° Bring your Laptop Computer; 3° Prototype Board in Class Use/Inspection.

Prototype System { Board A: CPU Module. Board B: For Graphics Display

4° Board A: CPU NXP LPC11C24 to Replace LPC1769 (Near the End of its Life, By 2024)

5° Good Throughout the entire School Session. But it will expire By the Last Day of the Class. (May 15th).

6° Lab Access Code/Policy for the Lab Usage.

Prerequisites

CmpE 180D for non CMPE or non EE undergraduate major. Students who do not provide documentation of satisfied the class prerequisite requirements by the second class meeting will be dropped from the class.

Faculty Web Page and MYSJSU Messaging (Optional)

Copies of the course materials such as the syllabus, major assignment handouts, etc. can be found from github https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F and on SJSU CANVAS.

Note: Homeworks/Projects Announcement will be Posted on CANVAS. Submission on CANVAS only.

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Course Description

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures, SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitte timers, display adapter, and other system peripherals and bus interfaces.

Required Texts/Readings

Note: Find the Datasheet on the Class github. CMPE244

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;
- Reference: ARM11 data sheets and on-line web materials on line https://github.com/hualili/ , or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Other Readings

- The reference material for ARM CPU hardware features, application notes, class handouts and lab assignments and reports, please see Professor Li's lecture notes, PPT, sample C code etc on line https://github.com/hualili/CMPE240-Adv-Microprocessors ;
- Professor Li's book materials, ARM Microprocessor Systems (in preparation for publication) https://github.com/hualili/CMPE240-Adv-Microprocessors

Other equipment / material requirements

32Bit RISC Prototype/Development Board.

Ref:

1° CPU Datasheets

2021F-107-lpc-cpu-UM... Add files vi

2° "SCH" Design.

2021F-107b-sch-#LPC... Add file

3° Lecture Notes

2022F-101-notes-cmpe240-2022-11-30.pdf

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deadlines and penalties for adding and dropping classes

Homework/Projects

Assignments and Grading Policy

Laboratory	30%
Midterm Examination	30%
Final	40%

0 to 59 F
60 to 69 D
70 to 79 C
80 to 89 B
90 to 100 A

Option 1. Target CPU Module Board
NXP LPC 11C24 ARM CPU Module (recommended a
this course), NXP LPC1769 ARM CPU Mc

Jan29 (Monday).

1. Check the CANVAS for Homework. Honesty Pledge

2. Target platform.

Background: x86. MIPS. ARM.
CISC RISC
RISC-V

NXP LPC Family.

LPC1769 — End of Life By 2024.

LPC1768 — mbed

LPC11C24

Option1: Jetson NANO 2gb.

Option2: RISC-V FPGA Board

BoM (Bill on Material) on github.

Anchor Elektronics.

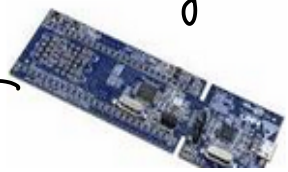
2021F-107-lpc-cpu-UM...

2021F-107b-sch-#LPC...

Example: SCH for LPC1768

Note1. CPU module, see Fig.1, its Two Connectors match the Pins in the Sch. Here

Fig.1



Note2: To make sure match the pins in the Sch to its physical Connector

Note3: Naming Convention — Enumeration Starts with Index 1 for the first pin.

J2 or J6

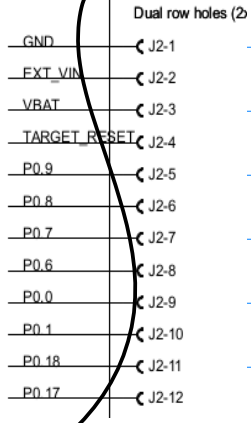
Note4: Pin Connectivity Information should be tied to its physical Device. Fig.1 And to its CPU Datasheet. ----→

→ Eventually to Software IDE.

Note5: J2-1, J2-2, ... ; And Chip pin Name & Number Such as P0.9, P0.8, ...

For LPC1768 is No Need

mbed	LPCXpresso
GND	GND
VIN (4.5-14V)	VIN (4.5-5.5V)
VB (battery supply)	VB (battery supply)
nR (reset)	RESET_N
SPI1-MOSI	P0.9 MOSI1
SPI1-MISO	P0.8 MISO1
SPI1-SCK	P0.7 SCK1
GPIO	P0.6 SSEL1
UART1-TX / I2C1-SDA	P0.0 TXD3/SDA1
UART1-RX / I2C1-SCL	P0.1 RXD3/SCL1
SPI2-MOSI	P0.18 MOSI0
SPI2-MISO	P0.17 MISO0



Functional Description of Each Pin, such as MOSI ... etc.

(Master Out Slave Input)

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Homework: Due A week from today.

1. Download NXP MCU Xpresso,
2. Install MCU Xpresso;
3. Start MCU Xpresso, then Screen Capture of your MCU Xpresso Start Page, make sure it has your Personal identifier on it.

Feb 1st (Wed)

Note: 1° Attendance Sheet

2° Ref. from the Class github.

2023S-102-MCUXpresso_IDE_Installation_...

3° LPC module to be finalized today by the Class. Purchasing CPU module by the end of the day today.

LPC11C24 / LPC1769

CPU module Board B — for Graphics Engine Design Emulation. pre-fab.

LPC1769 End of Life

Option1 Purchase Out-of-Stock. ~16 weeks.

Option2 Removal of All parts. Except the CPU module.

Example: Continuation of the SCH.

1. Pg. 9 → "P" Port, General Purpose port → ARM multiplexing. Each pin can have more than one functions. → Init & Config. → more than one port.

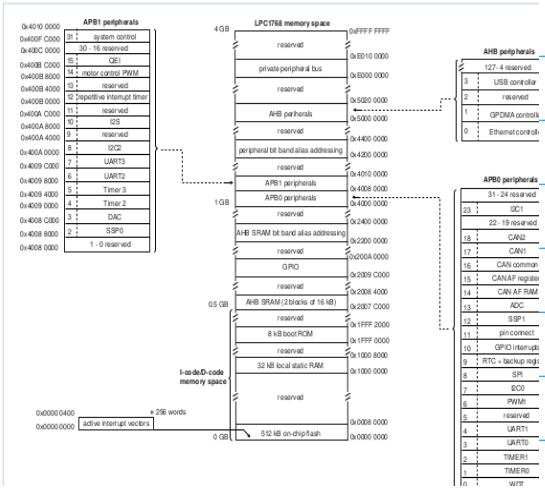
2. Connection to CPU Datasheet.

UM10360

LPC176x/5x User manual

Rev. 3.1 — 2 April 2014 User manual

PP.14 Memory map.



P12.

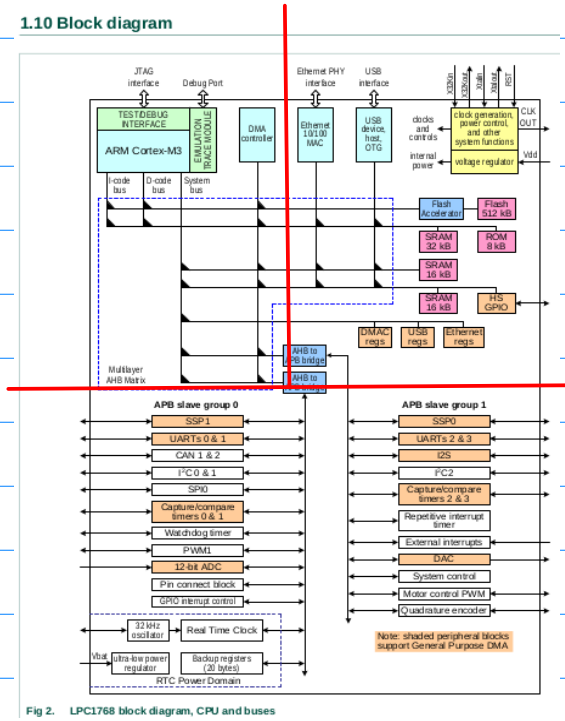
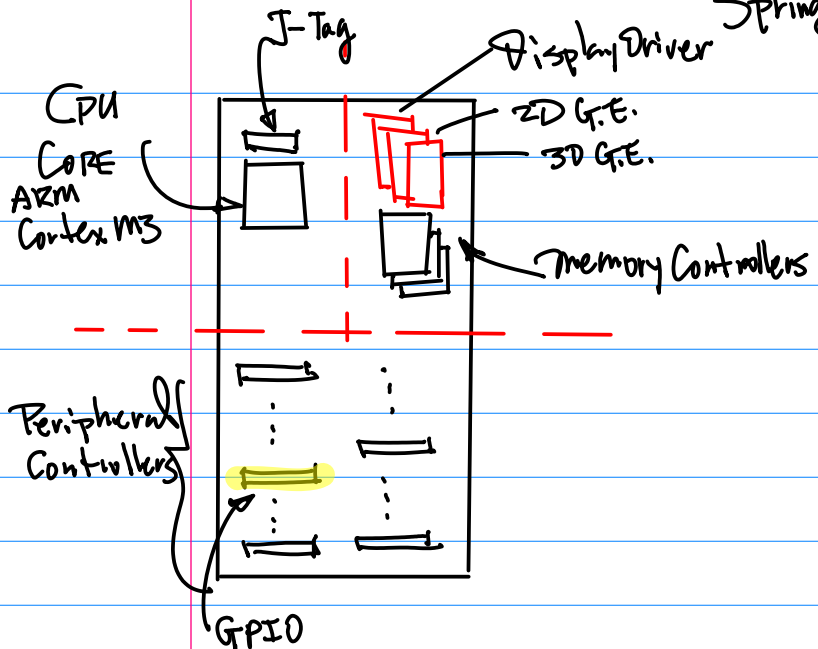


Fig 2. LPC1768 block diagram, CPU and buses



Now, find the pin(s) of the Port in the SCH.

Feb 6 (Monday).

Note: 1° CANVAS Submission of the prerequisite proof By Wednesday.

2°. Screen Capture of MCU Xpresso Installation. (Be Sure to have your Personal Identifier on the Screen).

3° Bring Your LPC CPU module to the class.

Example: Continuation of CPU Architecture

Ref. CPU Datasheet pp.13, pp.12.

Discussion On the CPU Block Diagram.

1° Display Driver.

2° 2D Graphics Processing Engine

3° 3D Graphics Processing Engine. J.T.U.

4° Video Codec. { Encoder MPEG4/H.264 265 26X
Decoder

Pixel Graphics.

Vector Graphics. (Display Drive, 2D G.E, 3D G.E.)

5° General Discussion of the CPU Architecture

(1) 32Bit RISC Architecture.

ALU. Bit width. 32bit

Register File { Special Purpose Registers. 32bits
General Purpose Registers.

Any meaningful A/L Ops.

Init & Config.

32bit

Bus Systems { Addr ~ 32bit/Uni-Directional
Data ~ 32bit/Bi-directional.
~~Control Bus~~

(2) memory map. $2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2}$

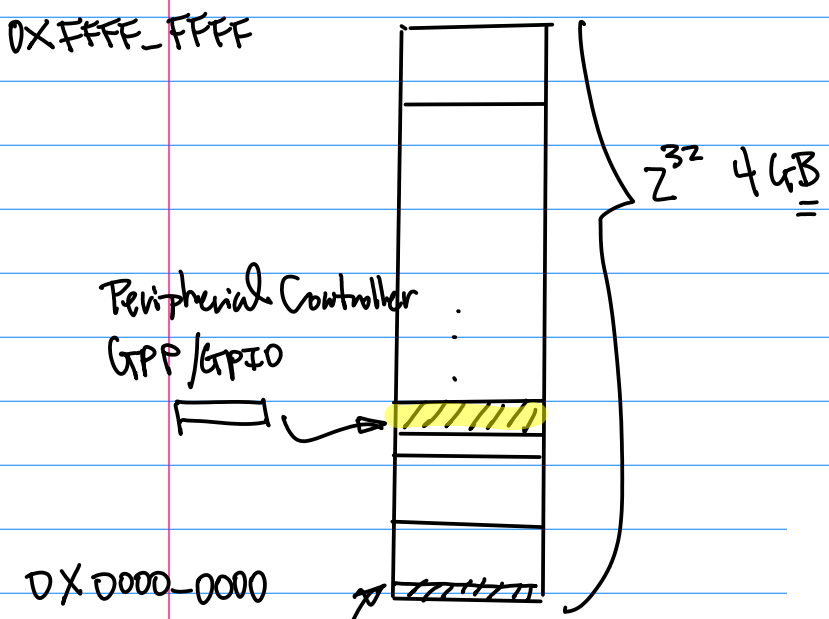
1K

1 Meg

1 Gig

4 G.B. Byte

Byte Addressable machine. ~ minimum mem. Cell with An unique addr. is a Single Byte.



a. Power-up Address: ~ when the CPU is powered up, it will go to this memory location to fetch the 1st Executable instruction

b. 8 memory Banks. Equal size of memory Blocks.

$$2^{32}/8 = 2^{32}/2^3 = 2^{29} = 2^9 \cdot 2^{20}$$

512 | Meg.

1st BANK is enumerated as BANK0, ..., the Last BANK is Bank7.

c. We use 3 Bits from the Address Bus to define the starting Addr. of Each Bank. " Little Endian "

$a_{31} a_{30} \cdots a_1 a_0$

$a_{31} a_{30} a_{29} : a_{28} \cdots a_1 a_0$

$a_{31} a_{30} a_{29} : a_{28} \cdots$

0 0 0 : 0 BANK0 0X0...
0 0 1 : 0 BANK1 0X2000_0000
0 1 0 : 0 BANK2 0X4000_0000
1 1 1 : 0

d.

UM10360
Chapter 2: LPC176x/5x Memory map
Rev. 3.1 — 2 April 2014 User manu

2.1 Memory map and peripheral addressing

The ARM Cortex-M3 processor has a single 4 GB address space. The following table shows how this space is used on the LPC176x/5x.

Table 3. LPC176x/5x memory usage and details

Address range	General Use	Address range details and description
0x0000 0000 to	On-chip non-volatile	0x0000 0000 - 0x0007 FFFF For devices with 512 kB of flash memory

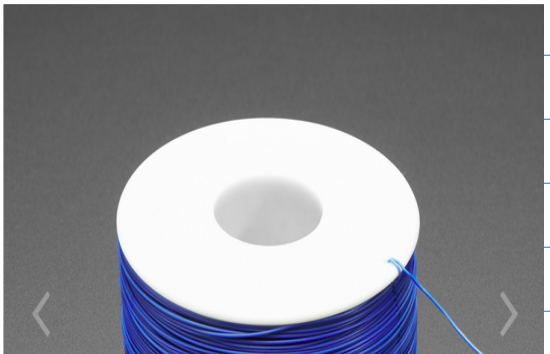
Address for GPIO Controller. 0X2...
0X4...

Feb 8. (Wed).

Note: Inspection of CPU module.
1° LPC1769 or LPC11C24;
2° Layout Design. CPU module Location Standoffs. Wire#

Prototyping wire
30AWG Blue 28~32 AWG

Product ID: 1446 $7.50



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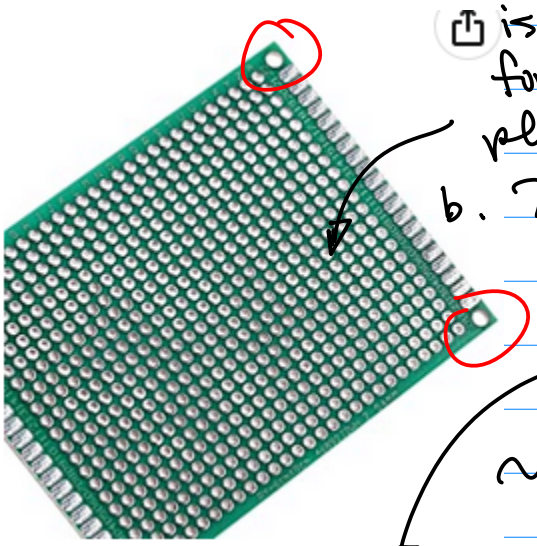
Prototype Board, Note: a. Through-Hole is uniformly formed. with plate coating



b. Mounting holes at corners.

c. Standoffs.

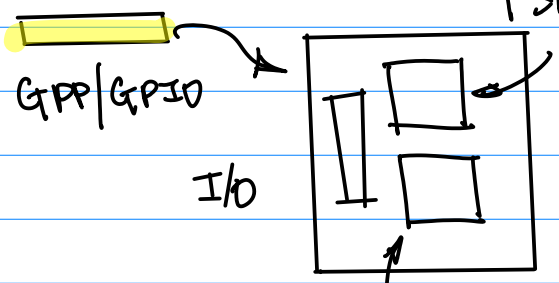
~ $5 - $15

Note: Please Bring 1° Your LPC CPU Module; 2° USB Cable; 3° Laptop with MCU Expresso for Inspection.

Example: Continuation of CPU Architecture Discussion

Note! 1° A GPP/GPIO Controller is mapped to the memory map. Read CPU Datasheet to find its Location;

2° Special Purpose Registers.



Special Purpose Registers.

Task1: Init & Config.

Naming Convention: RISC (uniformity, Regularity, Orthogonality)

Root (3 Letters)

CON

Prefix 3 Letters + Root 3 Letters

GPI

GPP

GPØ, GP1, GPx

GPPCON

Software to Drive the Peripheral Controller

Compiler, gcc. Open Source → Porting Target CPU

CmpE240

Spring2023

2nd Special Purpose Register

GPx + DAT

Root.

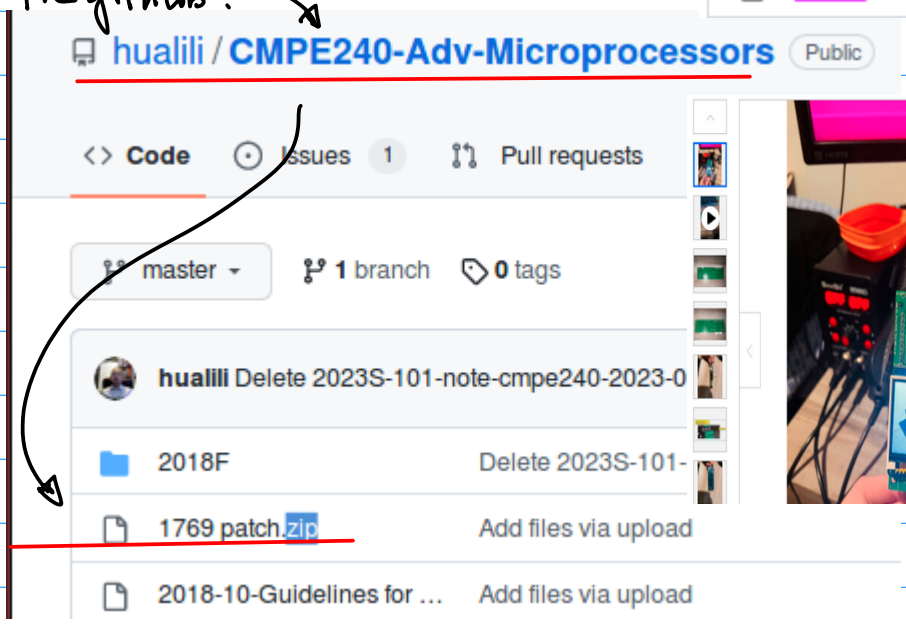
GPIODAT.

Feb13 (Monday).

Example: Start-up MCU Xpresso.

1. Install MCU Xpresso. Start the MCU. → Project Browser (Top Left Panel) → A pannel Beneath it, "Import Project", Double Click / Select to open it, then follow the steps to import 1769 patch.

2. the LPC1769 patch is posted on the github.



3. Connect your LPC GPU module (LPC1769) Browse the imported 1769 projects.

a/

find a project with a key word "Blinky" Then, use "Debug" option to Build it, And to observe the LED on the GPU module flashing.

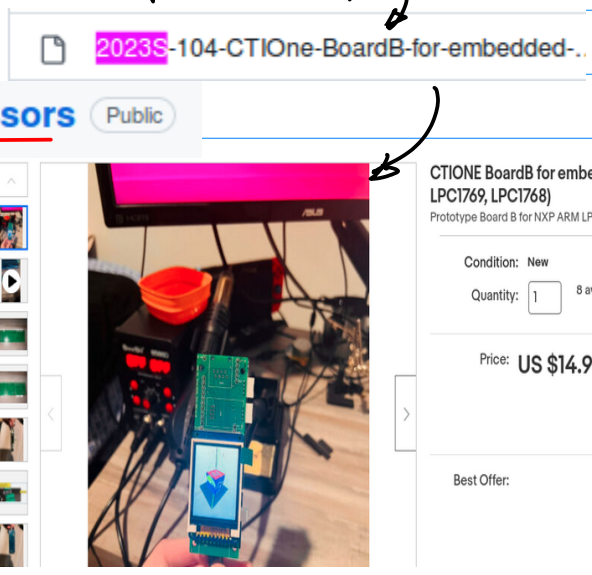
4. Then Browse the LPC1769 Patch, Locate 17xx.h which realizes the task of Porting the target platform (1769) to the IDE Software.

Resources: The posted zip files. (projects).

LPC1769 patch → gpio.zip (IIC24) → drawline.zip (IIC24)

2D Graphics → 2D+3D projects for IIC24.

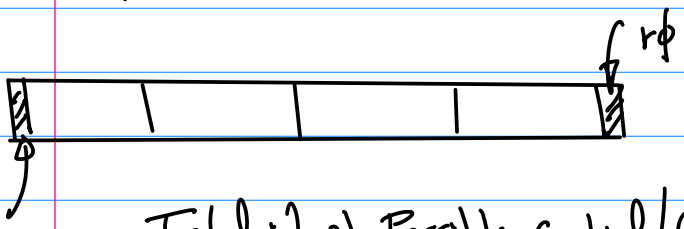
Note: for IIC24 Board)



https://www.digikey.com/en/products/detail/adafruit-industries-llc/358/5801368

Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

Example: GPxCON 32 bit.



Total No. of Possible Control/Config

$OPS = 2^{32}$

From CPU Datasheets, Inspection:

from github ~ Cmpe244

Notation: Vector Notation

GPACON[3:0]

2021F-105-#0-cpu-arm...

GPACONSLP	0x7F00800C	R/W	Port A Sleep mode Co
GPAPUDSLP	0x7F008010	R/W	Port A Sleep mode Pu

GPACON	Bit	Description	
GPA0	[3:0]	0000 = Input 0010 = UART RXD[0] 0100 = Reserved 0110 = Reserved	0001 = Outpu 0011 = Reser 0101 = Reser 0111 = Exter
GPA1	[7:4]	0000 = Input 0010 = UART TXD[0] 0100 = Reserved	0001 = Outpu 0011 = Reser 0101 = Reser

The 1st Pin of the GPIO port.

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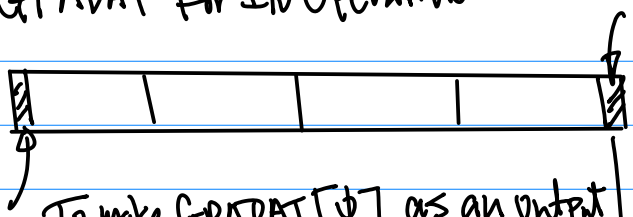
GPADAT For I/O operation



To make GPADAT[0] as an output pin 0 we will have to make GPACON[3:0] = 0x1

GPACON	Bit	Description	Initial State
GPA0	[3:0]	0000 = Input 0001 = Output 0010 = UART RXD[0] 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = External Interrupt Group 1 [0]	0000
GPA1	[7:4]	0000 = Input 0001 = Output	0000

From the SCH, we can find the physical pin to realize output function.

Source: 17xx.h

The mapping from CPU Architecture to the C-Code is defined by 17xx.h file with statements like:

LPC_GPIO0->FIODIR 0x.....

Memory Addr.

CPU Datasheet

from *.h file

Feb 15 (Wed)

Ref: 1° GPIO Code for LPC11C24

2022F-103i-lpc11c24-gpio-archive-2022-9-20.zip

2022F-103j-lecGPIO-v4-2017-2-22.pdf

For LPC1769, the Code/Project

GPIO 2015-1-30.zip

2° GPIO I/O Design.

Special purpose Register

3°. Mapping/Porting Architecture to C-code.

```
LPC_GPIO0->FIOSET

LPC_GPIO0->FIOCLR
```

```
#include "../../../tool
#ifdef __USE_CMSIS
 /* CMSIS: the Cortex M
                    */
#include "LPC17xx.h"
```

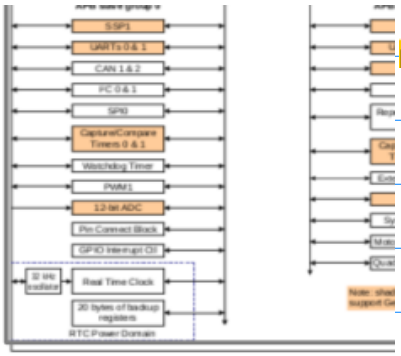
like the following
#define SPR 0x2000_0000
map the CPU architecture to the arm gcc compiler

Note: 1° FIODIR, CPU Datasheet.

```
LPC_GPIO0->FIODIR

LPC_GPIO0->FIOSET

LPC_GPIO0->FIOCLR
```



CPU

Background:

Exercise: Must Do

① Locate LPC17xx.h

② Find GPIO0 part of the Code.

③ Locate LPC_GPIO0->FIODIR

Find its Address.

2° Naming Convention.

Product family → Peripheral controller → Special Purpose Register

(4) Use CPU Datasheet to
Verify its Address in LPC17xx.h.

Continuation:
CPU Datasheet Table 102.
Discussion on Bit Settings.

Bit	Symbol	Value	Description
31:0	FIO0DIR FIO1DIR FIO2DIR FIO3DIR FIO4DIR		Fast GPIO Direction PORTx control bits. Bit 0 in FIOxDIR controls pin Px.0, bit 31 in FIOxDIR controls pin Px.31.
		0	Controlled pin is input.
		1	Controlled pin is output.

a.

Bit 3 for pin 3 Bit 2 for pin 2

b.


```
LPC_GPIO0->FIODIR = 0x4;
```

c.

Ref: LCD Display for LPC11C24

2022F-103f-LCD-connectivity-LPC11C24-hl-bj-2022-9-30.pdf

LPC11C24 Connectivity Table to

HL (2022-9-30) corrected this typo by replacing LPC 1769 to LPC11C24

Table 5. Connectivity Table of LPC11C24 and LCD

LPC11C24	Description	LCD
1. J6-28	3VOUT	VCC
2. J6-1	GND	GND
3. J6-8	SSEL0	TFT_CS
4. J6-14	RST	RESET
5. J6-13	D/C	A0
6. J6-5	MOSI0	SDA
7. J6-7	SCK0	SCK
8. J6-28	3VOUT	LED

Brand Walfront

TFT LCD Display:
Screen:https://www.amazon.com/gp/product/B07BFV69DZ/ref=ppx_yo_dt_b_search_asin_title?ie=UTF8&psc=1

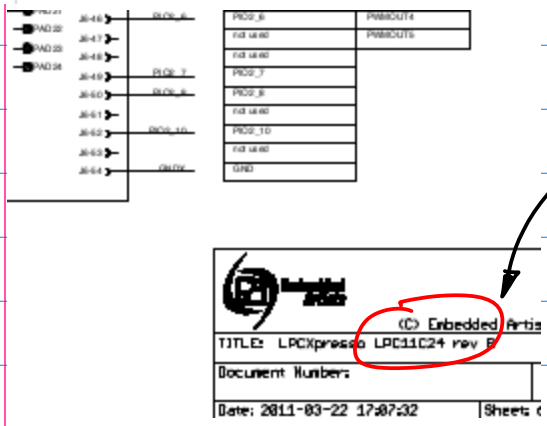
1.8 inch SPI TFT LCD Display Module for ST7735 128x160 51/AVR/STM32/ARM 8/16 bit

Visit the Walfront Store
20 ratings
Amazon's Choice in LCD Graphic Displays by Walfront

-10% $15.55
Price: $17.66
prime One-Day
& FREE Returns
Includes $1.71 Prime savings

Ref: CPU Datasheet for LLC24

1. 2022F-103g-lpc11c24-cpu-datasheet-UM10398.pdf Add files via upload
2. 2022F-103h-SCH-LPCXpressoLPC11C24revB.pdf Add files via upload
3. 2022F-103i-lpc11c24-gpio-archive-2022-9-20.zip Add files via upload



Feb 20 (Monday).

Note: 1° Homework Coming on CANVAS;

Today's Topics:
1° Summary on GPIO
2° Hardware for Graphics 2D Engine

Example: Ref CPU Datasheet Table 102. for FIODIR S.F.R.

Note: 1° Addr. for the S.F.R. Need to Be Cross-refer'd in MCUXpresso Code.

2° FIODIR Multiple. Registers

access to a group of bits in a single GPIO port independently from other bits in the same port.

Table 102. GPIO register map (local bus accessible registers - enhanced GPIO features)

Generic Name	Description	Access	Reset value[1]	PORTn Register Name & Address
FIODIR	Fast GPIO Port Direction control register. This register individually controls the direction of each port pin.	R/W	0	FIO0DIR - 0x2009 C000 FIO1DIR - 0x2009 C020 FIO2DIR - 0x2009 C040 FIO3DIR - 0x2009 C060 FIO4DIR - 0x2009 C080
FIOMASK	Fast Mask register for port. Writes, sets, clears, and reads to port (done via writes to FIOPIN, FIOSET, and FIOCLR, and reads of FIOPIN) alter or return only the bits enabled by zeros in this register.	R/W	0	FIO0MASK - 0x2009 C010 FIO1MASK - 0x2009 C030 FIO2MASK - 0x2009 C050 FIO3MASK - 0x2009 C070 FIO4MASK - 0x2009 C090

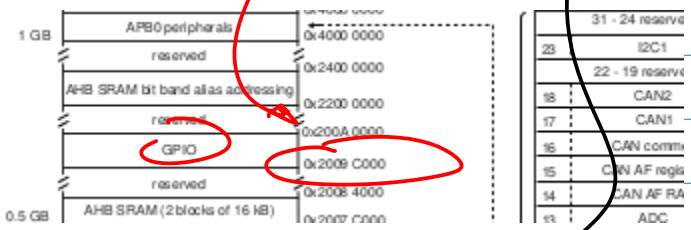
Connection To Coding: C/C++

FIO0DIR → LPC_GPIO0 → FIO0DIR

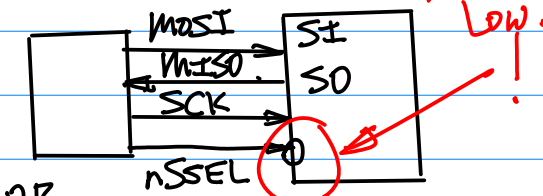
0X2009_C003 — r0

0X2009_C000 : — r3 | 0X2009_C000

Connection To Mem map



LPC1102/4 — LCD Active Low.



OR 1769

Fig.1.

30. Addr. for Byte Addressable Machine, 4 Addresses.

FIO0DIR[rx':rx], for Example

FIO0DIR[4:3]

40 Bit (Binary) Pattern for the SFR.

Table 105. Fast GPIO port Direction control byte and half-word accessible register description

Generic Register name	Description	Register length (bits) & access	Reset value	PORTn Register Address & Name
FIOxDIR0	Fast GPIO Port x Direction control register 0. Bit 0 in FIOxDIR0 register corresponds to pin Px.0 ... bit 7 to pin Px.7.	8 (byte) R/W	0x00	FIO0DIR0 - 0x2009 C000 FIO1DIR0 - 0x2009 C020 FIO2DIR0 - 0x2009 C040 FIO3DIR0 - 0x2009 C060 FIO4DIR0 - 0x2009 C080
FIOxDIR1	Fast GPIO Port x Direction	8 (byte)	0x00	FIO0DIR1 - 0x2009 C001

Responsible for P0.0 ~ P0.7 (8 pins).

"1" for Output, "0" for the input.

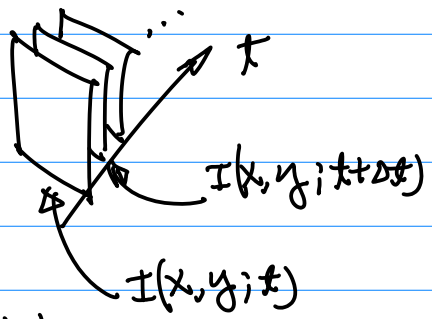
* Consider Hardware Design for LCD Display.

Background: SPI. Enable LCD Display Device.

Serial Peripheral Interface.

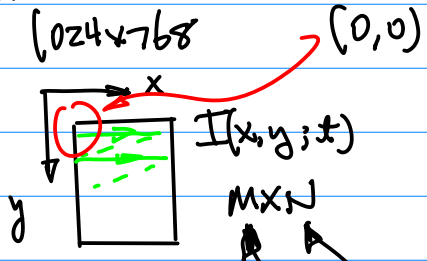
Bit Rate ~ 100Mbps.

Note: Bit Rate Discussion.



Graphics Display Resolution:

1024x768



Scans:

Top Left Corner (0,0),

From Left to Right

Top to Bottom.

No. of pixels/Row

No. of Rows Per frame.

30 Frames Per Second (FPS)

24 Bits of color. (Color Depth)

$1024 \times 768 \times 30 \times 24$ bit/sec.

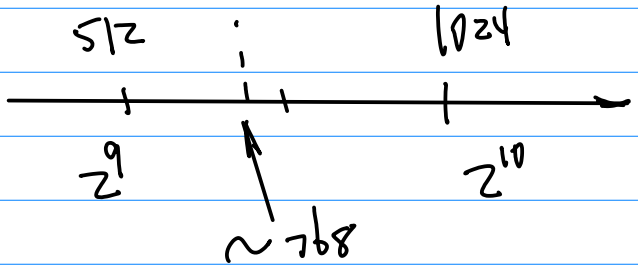
$2^{10} \quad 2^{9} \quad 2^{5} \quad 2^{5} = 1K \cdot 1K \cdot 2^{9}$

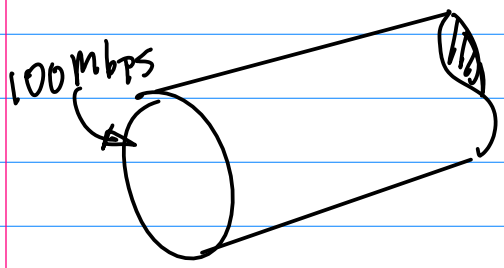
$1 \quad 2^{10} = 1\,Meg \times 512$

$1K \quad 1K = 512\,Mbps$ //

Now, Let's go to Sck of the Target GH.

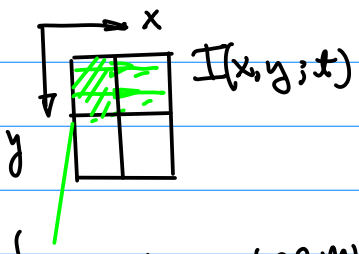
2022F-103h-SCH-LPCXpressoLPC11C24revB.pdf





LPCXpresso			
	GND	GNDX	J6-1
	VIN (4.5-5.5V)	EXT_POWX	J6-2
	not used		J6-3
	PIO0_0 RESET	PIO0_0	J6-4
	PIO0_9 MOSI0/SWO	PIO0_9	J6-5
	PIO0_8 MISO0	PIO0_8	J6-6
	PIO2_11 SCK0	PIO2_11	J6-7
	PIO0_2 SSEL0	PIO0_2	J6-8
A	PIO1_7 TXD	PIO1_7	J6-9
L	PIO1_6 RXD	PIO1_6	J6-10
	PIO0_7	PIO0_7	J6-11
	PIO2_0	PIO2_0	J6-12
X	PIO2_1	PIO2_1	J6-13
	PIO2_2	PIO2_2	J6-14
	PIO0_11 AD0	PIO0_11	

Dual row holes (2x27), 100 mil spaci



Build Connectivity Table

CPU pin PinNo./Name	Connector Info	Note
PIO0_9/MOSI0	J6-5/MOSI0	

$1/4 \times 512 > 100\,Mbps$

1/4 of the Resolution $1024 \rightarrow 1024/2 = 512$

SPI I/F: "3+1" $768 \rightarrow 512/2 = 256$

- MISO Mast Input / Slave Output
- MOSI Master Out / Slave Input
- SCK (Clock Output)

} 3

- SSEL (nEN: Active Low, Output from the master)