San José State University
College of Engineering/Computer Engineering Department
CMPE240 Advanced Microcomputer Design

S2023

Professor Hua Harry Li
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Class Time: Mondays and Wednesdays 1:30-2:45 PM
Office Hours: Mondays and Wednesdays 4:30 – 5:30 PM Zoom
Zoom link: Join Zoom Meeting https://us04web.zoom.us/j/9841607683?pwd=UlA3aEk1TnV4bjNLQk5CQkw0dDk4UT09 Meeting ID: 984 160 7683 Passcode: 121092
Lecture Room: Engineering Building Room 303
Lab facility: Engineering Building Room 268

Prerequisites

CmpE 180D for non CMPE or non EE undergraduate major. Students who do not provide documentation of satisfied the class prerequisite requirements by the second class meeting will be dropped from the class.

Faculty Web Page and MYSJSU Messaging (Optional)

Copies of the course materials such as the syllabus, major assignment handouts, etc. can be found from github https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F and on SJSU CANVAS.

Course Description

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures, SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter r timers, display adapter, and other system peripherals and bus interfaces.

Program Outcomes

1. Being able to demonstrate an understanding of advanced knowledge of the practice of computer engineering, from vision to analysis, design, validation and deployment.
2. Being able to tackle complex engineering problems and tasks, using contemporary engineering methodologies and tools.

Course Goals and Student Learning Objectives

Course goals

CMPE 240 is an advanced logic design and architecture course that teaches various system buses, organization of different system memories and peripherals, and most importantly, their interface design with system bus using timing diagrams. Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of forty-five hours over the length of the course (normally 3 hours per unit per week with 1 of the hours used for lecture) for instruction or preparation/studying or course related activities including but not limited to internships, labs. Other course structures will have equivalent workload expectations as described in the syllabus.

Students Learning Objectives

1. Being able design a system bus.
2. Being able to understand memory sub-systems and design their interface with a system bus.
3. Being able to design system peripherals and interface them to the system bus.
4. Being able to understand the overall system functionality .

Required Texts/Readings

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;
- Reference: ARM11 data sheets and on-line web materials on line https://github.com/hualili/ , or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Other Readings

- The reference material for ARM CPU hardware features, application notes, class handouts and lab assignments and reports, please see Professor Li's lecture notes, PPT, sample C code etc on line https://github.com/hualili/CMPE240-Adv-Microprocessors ;
- Professor Li's book materials, ARM Microprocessor Systems (in preparation for publication) https://github.com/hualili/CMPE240-Adv-Microprocessors

Other equipment / material requirements

32Bit RISC Prototype/Development Board.

Library Liaison (Optional)

N/A

Classroom Protocol

Participation and attendance are required, no late arrival times please. No cell phone use in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/ **.** Students should be aware of the current deadlines and penalties for adding and dropping classes.

Assignments and Grading Policy

Laboratory	30%
Midterm Examination	30%
Final	40%

0 to 59 F
60 to 69 D
70 to 79 C
80 to 89 B
90 to 100 A

Option 1. Target CPU Module Board

NXP LPC 11C24 ARM CPU Module (recommended as the replacement for LPC1769 for this course), NXP LPC1769 ARM CPU Module (towards the end of life by and around 2024).

Option 2. Other CPU Module Boards

Nvidia Jetson NANO board as a target platform in addition to NXP LPC platform.
https://www.google.com/search?channel=fs&client=ubuntu&q=nvidia+jetson+nano+2gb+developer+kit

Open source architecture RISC-V FPGA board with Verilog Implementation of IP core and RTOS software tools, in additional to NXP LPC platform.
https://riscv.org/wp-content/uploads/2017/02/riscv_fosdem17.pdf

Prototype Board

Using wire wrapping board is required. Note, using prebuild PCB board as a LCD display board to couple with the target CPU module board is permitted.

Policies on exams and late assignments
Quizzes, midterm and final are not postponed or retaken under any circumstances. The only exception is medical emergencies accompanied with doctor's report. The lab reports can be delayed under special circumstances. If you know you will delay a report for some unavoidable reason please see me as soon as possible. Extra credit may be available for optional project(s) upon discussion with the course instructor. 10% penalty is given for late project submission. B is the passing grade for the course. Final exam date is published by university schedule. No grade on participation. Attendance is not used as a criterion for grading according to Academic Policy F-69-24.
Note: 1. No late projects/homework submission is accepted. For unexpected situations late penalty of marks reduction will apply. 2. All exams are in class, in person. The electronic submission of the answer papers are only accepted through the university CANVAS system.

University Policies

Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Department Policies

All non-proctored report (or similar sized) assignments in courses where some of the final grade depends on prose writing will be submitted to turnitin.com.

Student Technology Resources (Optional)

Computer labs for student use are available in the Academic Success Center located on the 1st floor of Clark Hall and on the 2nd floor of the Student Union. Additional computer labs

may be available in your department/college. Computers are also available in the Martin Luther King Library. A wide variety of audio-visual equipment is available for student checkout from Media Services located in IRC 112. These items include digital and VHS camcorders, VHS and Beta video players, 16 mm, slide, overhead, DVD, CD, and audiotape players, sound systems, wireless microphones, projection screens and monitors.

Learning Assistance Resource Center (Optional)

The Learning Assistance Resource Center (LARC) is located in Room 600 in the Student Services Center. It is designed to assist students in the development of their full academic potential and to motivate them to become self-directed learners. The center provides support services, such as skills assessment, individual or group tutorials, subject advising, learning assistance, summer academic preparation and basic skills development. The LARC website is located at http:/www.sjsu.edu/larc/.

SJSU Writing Center (Optional)

The SJSU Writing Center is located in Room 126 in Clark Hall. It is staffed by professional instructors and upper-division or graduate-level writing specialists from each of the seven SJSU colleges. Our writing specialists have met a rigorous GPA requirement, and they are well trained to assist all students at all levels within all disciplines to become better writers. The Writing Center website is located at http://www.sjsu.edu/writingcenter/about/staff//.

Peer Mentor Center (Optional)

The Peer Mentor Center is located on the 1st floor of Clark Hall in the Academic Success Center. The Peer Mentor Center is staffed with Peer Mentors who excel in helping students manage university life, tackling problems that range from academic challenges to interpersonal struggles. On the road to graduation, Peer Mentors are navigators, offering "roadside assistance" to peers who feel a bit lost or simply need help mapping out the locations of campus resources. Peer Mentor services are free and available on a drop –in basis, no reservation required. The Peer Mentor Center website is located at http://www.sjsu.edu/muse/peermentor/ .

CMPE 240 Adv. Microcomputer Design

The schedule is subject to change with fair notice in class.

Table 1 Course Schedule

Week	Topics, Readings, Assignments, Deadlines
1	Organizational Meeting and Introduction, Overview of a RISC Microprocessor System with CPU datasheet.
2	Review of the RISC CPU architecture: CPU core, peripheral controllers, internal buses, and memory controllers as well as graphics engine. Design a microprocessor system with CPU module and with RS232 debugging capability.
3	Continue to review RISC CPU and peripheral controllers, software development tool, NXP Xpresso (IDE: integrated development environment), I/O peripheral controllers, GPIO and SPI controller for design and building SPI interface, such as graphics display/processing unity and/or FLASH memory unity.
4	Memory Map, Power-up Address, special purpose registers and their initialization and configuration, as well as debugging. Description and design of a bidirectional system bus and I/O with case study on graphics acceleration engine design. Introduction to SPI based LCD interface and prototyping design and implementation.
5	SPI Interface and SPI graphics display unity (LCD) design. 2D vector graphics and its implementation. 2D Vector graphics processing engine
6	Advanced MCU design: GE (graphics engine) design, 2D graphics vector graphics processing for ARM Cortex Core. LCD Display adapter design. Implementation of LCD display with 2D GE vector graphics.
7	CPU Architecture, continue with GE design with interrupt techniques, system timer, interrupt vector table, interrupt service routine (ISR) techiniques.
8	Midterm
9	3D vector graphics processing for ARM Cortex Core. LCD Display adapter design. Implementation of LCD display.
10	3D vector graphics processing, world to viewer transformations, and linear decoration algorithm for ARM Cortex Core. Implementation of 3D perspective projection and linear decoration algorithm.
11	3D vector graphics processing and prototype board implementation for transformation pipeline, shadow computation.
12	GE (graphics engine) design, 3D vector graphics processing, texture mapping and animation implementation, diffuse reflection computation.
13	ExTNT technique integration with LCD display and 3D GE acceleration

Week	Topics, Readings, Assignments, Deadlines
	engine.
14	Inter-processor communications.
15	Integration of the prototype board with 2D and 3D GE for the ARM CPU.
16	Comprehensive final exam.