

# CMPE240 Spring 22

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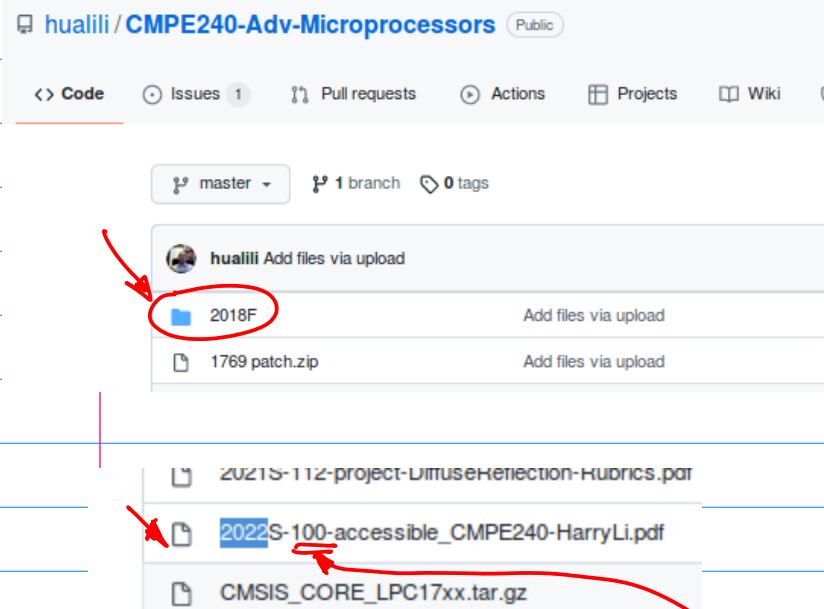
Jan 26 (Wed)

Today's Topics: Introduction  
& Organizational meeting.

HARRY LI, Ph.D.

GreenSheet: On-Line from github

<https://github.com/hualili/CMPE240-Adv-Microprocessors>



Naming Convention: Yr + Semester + ID +  
Name of the Doc.

E-mail: hua.li@sjsu.edu

Text message: (650) 400-1116

Office Hours: Mondays & Wednesdays  
4:30 - 5:30 PM.

Office hours Zoom link: Join Zoom Meeting  
[https://us04web.zoom.us/j/9841607683?](https://us04web.zoom.us/j/9841607683?pwd=UIA3aEk1TnV4bjNLQk5CQkw0dDk4UT09)  
pwd=UIA3aEk1TnV4bjNLQk5CQkw0dDk4UT09  
Meeting ID: 984 160 7683 Passcode:  
121092

TextBooks + Ref

1. No text Book, But NXP CPU Datasheet  
is utilized as a Base Line Ref

2. SCH Design of the CPU module,  
PP5 (Rev.D.)

Prototype Board: Each person will  
Build his/her Prototype System.

Team work is encouraged, form 4 people  
team for this Class. However all the  
work has to be done individually.

Grading: midterm 30%  
Format: Written Exam But

Need to have prototype ready to execute  
programs, And get photos of your  
Prototype Board.

Final Exam: 40%, Similar format as  
the midterm.

Homework, Projects counts Another 30%.

Written Announcement on White Board  
(Lecture Notes) And SJSU CANVAS.

Late Project submission will have 1 pt.

Penalty per each Lecture Day.

Introduction.

1. Bill of material for LPC1769  
Prototype Board Design.

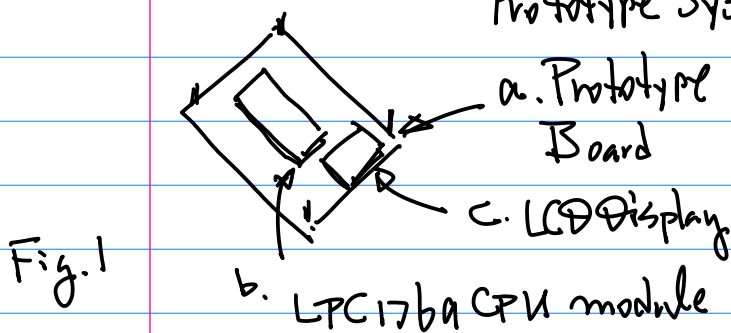
Jan 31 (Monday)

Today's Topic: Introduction.

Prototype System.

Task: 1. Form 4 Person Team  
Work Together throughout the  
entire Semester. By this Wednesday.

Prototype System.



Note: a. Adequate Size  
Not Too big, to host LPC1769  
module & LCD Display module,  
plus "Glue" Logic.

"Glue Logic" GPIO Circuit as  
a part of the "Glue"

Ethernet Connector, RJ45,  
in the future for possible  
networking Applications,  
TCP/IP, micro-Web Server.

4" x 3" Or Similar Size.  
16 cm x 11 1/2 cm.

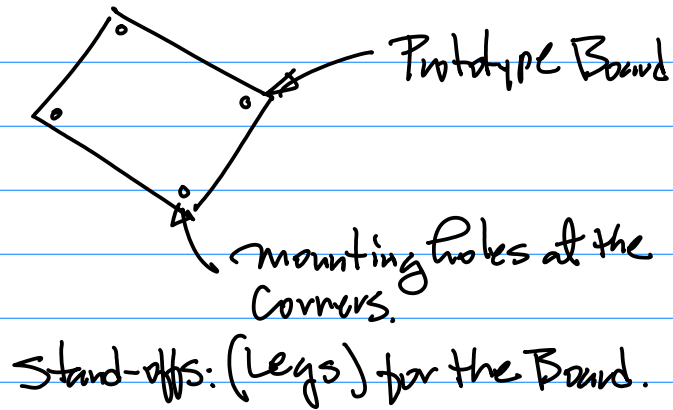


Fig. 2 CPU

Digi-Key, or Mouser Electronics

CPU: Cortex M3

c. LCD Display module

SPI (Serial Peripheral Interface)  
Software Driver function(s) are  
Provided/Accessible

- LPC 1769
- Color TFT LCD display  
Resolution : 128x160,  
Pixel Depth: 18-bit (262,144) colors  
Controller: ST7735  
Interface: SPI interface

LCD Pins

LPC1769 Pins

From the class github

## LCD module

2021F-113-LCD-TFT (ThinFilmTransistor).jpg

2021F-114-display-NEC-3P5-LCD-68775.pdf

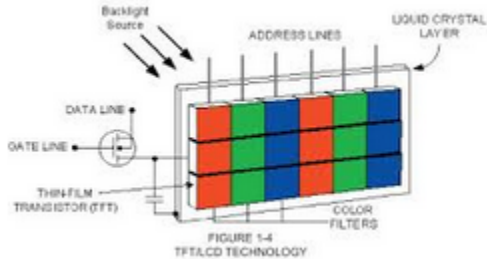


Fig.3

Components for:

Power Unit Design Need

GPIO (General Purpose I/O)

LPC1769 is powered with 2 Options.

Option 1: USB Cable Connection to provide power from the host (PC) to LPC 1769 CPU module.

for Debugging/Testing Purpose But not for Deployment

Option 2: External Power to the prototype System. To Allow you Deployment of the prototype System. → Mandatory, By

the last project, each prototype will have to deployed with External Power.

7.5V ~ 9V DC @  
1500 mA ~ 4000 mA

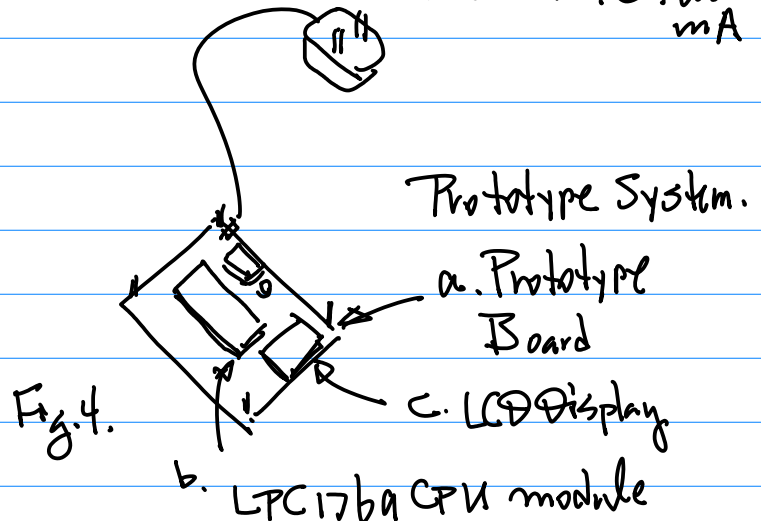


Fig.4.

Build Option 2 Power Unit Circuit is required Now, Before the first Project.

Components for the Power Unit

① Wall-mount Adapter.

Spec. 7.5 ~ 9V DC

1500 mA ~ 4000 mA.

Or Battery Pack.

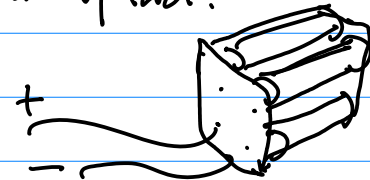


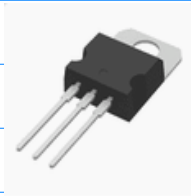
Fig.5

② Red LED indicator, to show Power is on/off.

$V_{LED} \approx 1.2 \text{ VDC}$ ; 8 ~ 10 mA

③ Power Regulator IC 7805, or 1117.

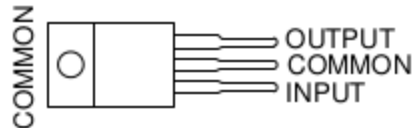
Fig.6



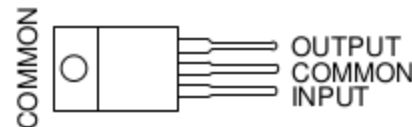
STMicroelectr  
L7805CV ...  
\$0.63  
Digi-Key

- 3-Terminal Regulators
- Output Current up to 1.5 A
- Internal Thermal-Overload Protection

KC (TO-220) PACKAGE  
(TOP VIEW)



KCS (TO-220) PACKAGE  
(TOP VIEW)



Note: 78xx family  
7812, 7805 etc.

## μA7800 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS056J - MAY 1976 - REVISED MAY 2003

(4) Right Angle (plug) connector



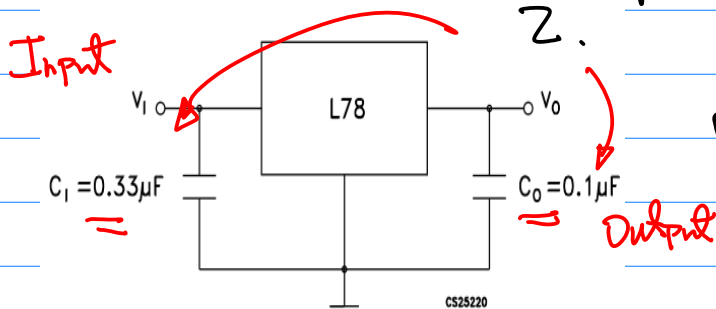
Kobiconn  
151-7620E-DC  
\$1.14  
Mouser Electronics

Fig.7

(5) Assorted Resistors (A few hundred  
ohms to a few Mega Ohms).

(6) Compensating Caps.

Figure 5. Application circuits



Comments for GPIO

Use GPI "Hello, the world"  
for Debugging Input {0's  
1's  
Output {0's  
1's

Feb 2nd (Wed)

Today's Topics:

1° Bill of Material

2° CPU Datasheet, Architecture

Options for the target platform.

(LPC1769)

a. NVDA (Nvidia) Jetson Nano  
Caution: Device Driver Programming  
in U.S. Kernel Space.

5% Bonus. Implementation at  
Registers/Hardware Level, LCD

Fig.8

LCD has to the Same SPI I/F  
for NAND & LPC1769.

GPP I/O Output Testing.

Example: GPIO I/O Testing Circuit

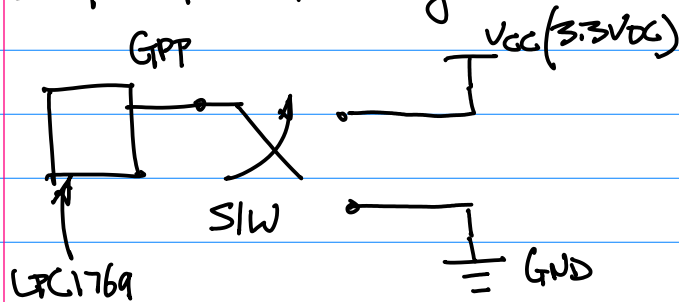


Fig. 1.

GPP: General Purpose Port,  
Same as GPIO.

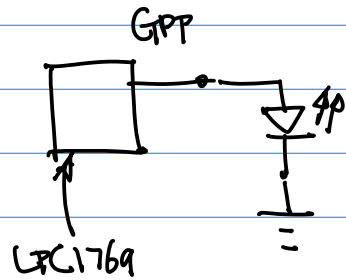
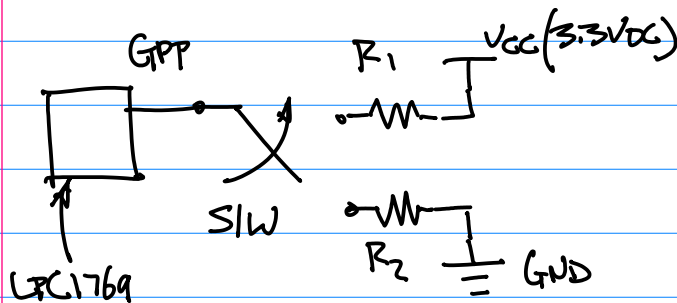
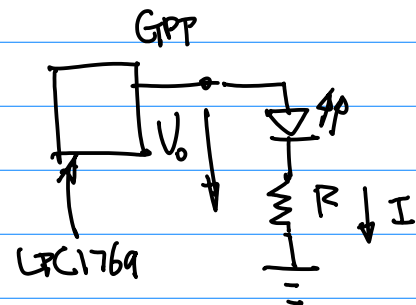


Fig. 2



Better Design.

Fig. 6.

Consider Resistor Value Calculation

$$V_{CC} = 3.3VDC, V_{out} = 3.3VDC$$

(GPP)

Select Resistor Value to Regulate  
the Amount of Current  $\sim 10mA$

$$\text{Hence, } R_{1,2} = \frac{V_{CC}}{10mA} = \frac{3.3}{10 \times 10^{-3}} \\ = 330 \Omega$$

Calculation of the Resistor

$$V_o = V_{LED} + IR \quad \dots (1)$$

$$V_{LED} \approx 1.2V, I = 10mA, V_o = 3.3V$$

(CMOS)

Substitute the  
above Conditions into Eqn(1),

$$3.3 = 1.2 + R \times 10 \times 10^{-3}$$

$$R = \frac{2.1}{10^{-2}} = 2.1 \times 10^2 = 210 \Omega$$

Note: please use right size of the  
prototype wire  
26 ~ 30 AWG.



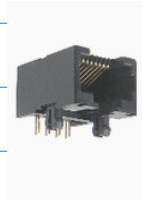
Strideday™ 26 AWG 100m  
amazon.com



200m 30AWG Blue...

Note: Optional — Right Angle

RJ-45 Connector. (8 pos)  
(Female)

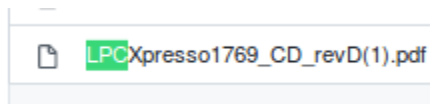


Modular Jack  
8P8C PCB ...  
\$0.69  
PEconnecto...

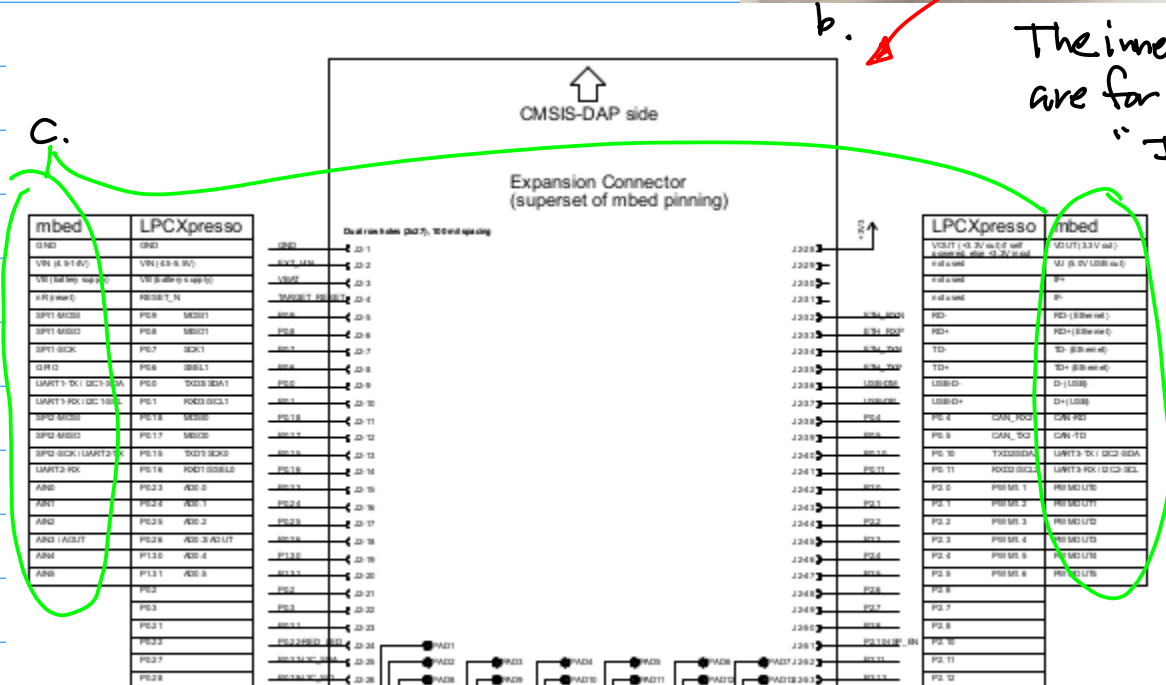
Exercise: Bring your Prototype Board together w/ LPC1769 CPU module to the next class.

2. Form 4-person Team, have a Coordinator, And report your team formation By next class.

Example: LPC1769 CPU module Schematics



a. CPU module and Schematics in b.  
c. LPC1769 mbed.





Exercise: How many GPIO pins?  
(for LPC1767 module)

Example: Build "Hello, the world" for the prototype system.

Example: Power Input to LPC1769

Step 1. CPU Architecture, pp.9 & 12

LPCXpresso		
GND		GND
VIN (4.5-5.5V)		EXT_VIN
VB (battery supply)		VBAT
RESET_N		TARGET_RESET
P0.9 MOSI1		P0.9
P0.8 MISO1		P0.8
P0.7 SCK1		P0.7

Note: Enumeration of the Connector pins → the first pin is marked as "1".

Note: Physical mapping of the pin to Actual module;

Note: Reset pin — provide Access to this pin in your Prototype design.

CPU Datasheet from github / ~ Cmpe244

2021F-107-lpc-cpu-UM10360.pdf

Feb 7 (Monday).

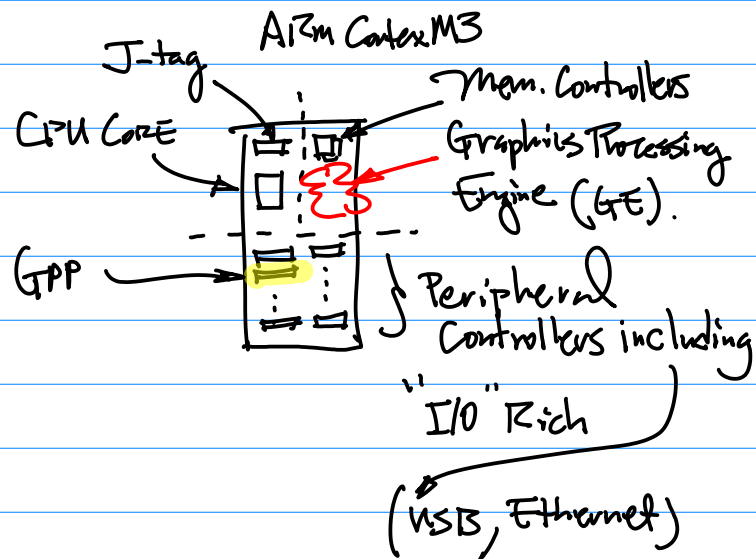
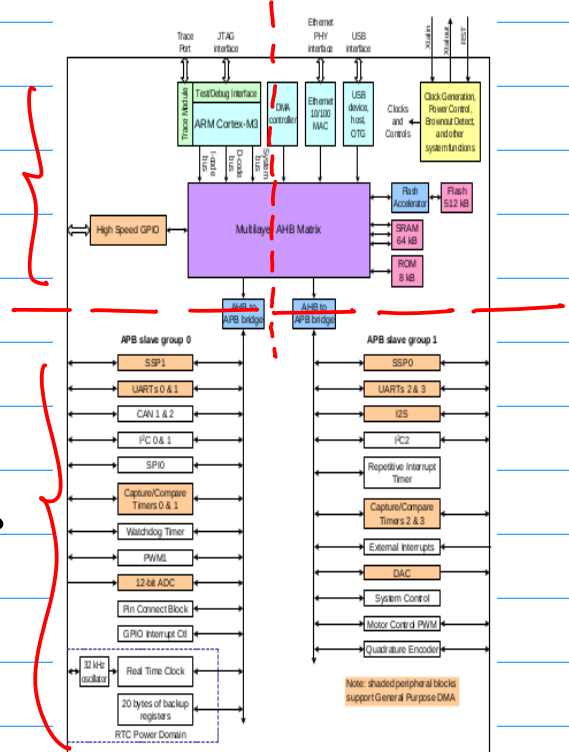
Today's Topics 1° CPU Datasheet & Schematics; 2° Hardware Design for the Prototype System.

UM10360

LPC176x/5x User manual

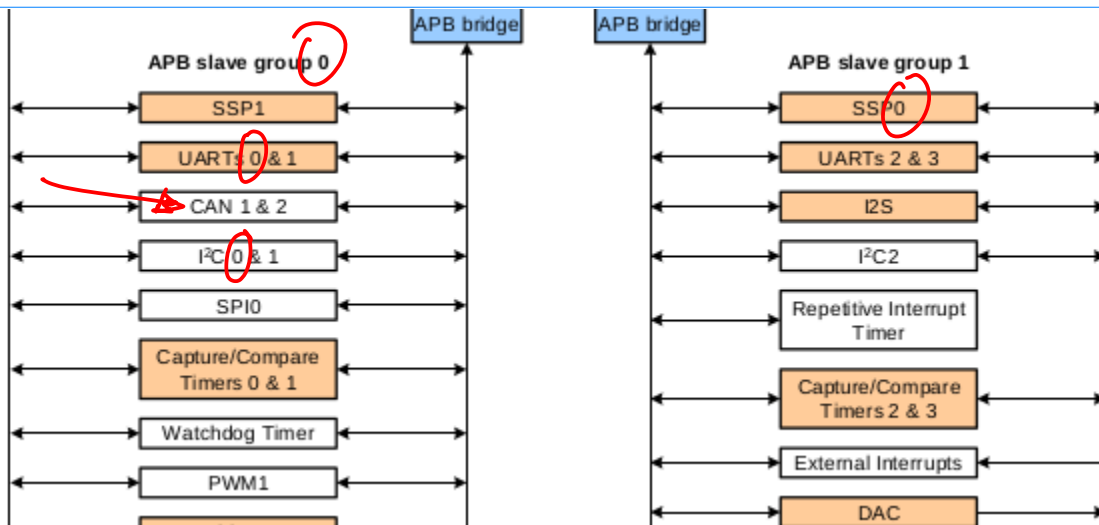
Rev. 3.1 — 2 April 2014

Peripheral Controllers



Select GPP (General Purpose Port) to Build GPIO I/O to Realize "Hello, the world" function. (with Input Testing / Output Testing Circuit.)

# Note: Peripheral Controllers



Step 2: Map the GPP to its physical Board, e.g., CPU module. Hence, we need schematics.



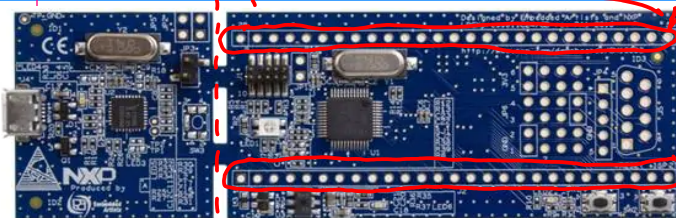
from the Class github.

a. from the schematics,

identify the first

pin, e.g., J2-1

Do the Same of your physical CPU module. J2 connector CPU module



Interfaced to the host

LPCXpresso		Dual row holes (2x27), 11
GND		GND J2-1 a.
VIN (4.5-5.5V)		EXT_VIN J2-2
VB (battery supply)		VBAT J2-3
RESET_N		TARGET_RESET J2-4
P0.9 MOSI1		P0.9 J2-5
P0.8 MISO1		P0.8 J2-6
P0.7 SCK1		P0.7 J2-7
P0.6 SSEL1		P0.6 J2-8
P0.0 TXD3/SDA1		P0.0 J2-9
P0.1 RXD3/SCL1		P0.1 J2-10
P0.18 MOSI0		P0.18 J2-11
P0.17 MISO0		P0.17 J2-12
P0.15 TXD1/SCK0		P0.15 J2-13
P0.16 RXD1/SSEL0		P0.16 J2-14
P0.23 AD0.0		P0.23 J2-15
P0.24 AD0.1		P0.24 J2-16
P0.25 AD0.2		P0.25 J2-17
P0.26 AD0.3/AOUT		P0.26 J2-18
P1.30 AD0.4		P1.30 J2-19
P1.31 AD0.5		P1.31 J2-20
P0.2		P0.2 J2-21
P0.3		P0.3 J2-22
P0.21		P0.21 J2-23
P0.22		P0.22-RED_LED J2-24
P0.27		P0.27-I2C_SDA J2-25
P0.28		P0.28-I2C_SCL J2-26
P2.13		P2.13 J2-27



## Step 3. Select 2 GPIO Pins

One for Input Testing Circuit, P0.2 Input, P0.3 Output  
The other for Output Testing Circuit.

Connectivity & Pin Assignment Table  
3 col. format

P0.26	AD0.3/AOUT	P0.26	J2-18
P1.30	AD0.4	P1.30	J2-19
P1.31	AD0.5	P1.31	J2-20
P0.2		P0.2	J2-21
P0.3		P0.3	J2-22
P0.21		P0.21	J2-23
P0.22		P0.22-RED_LED	J2-24
P0.27		P0.27-I2C_SDA	J2-25
P0.28		P0.28-I2C_SCL	J2-26
P2.13		P2.13	J2-27

Connector Pin

CPU/Connector Pin	Description	Note
P0.2/J2-21	GPIO Input	
P0.3/J2-22	GPIO Output	

GPIO Pins, CPU Naming.

CPU Datasheet for General Purpose Port 0  
P0.17

pin. For other functions, the direction is controlled automatically.

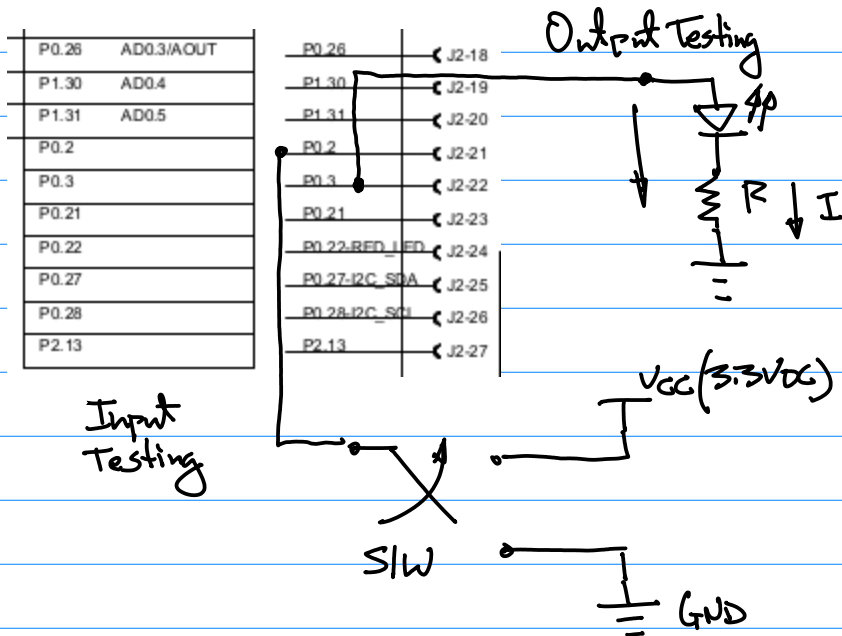
a. b. c. d. e.

**Table 80. Pin function select register 0 (PINSEL0 - address 0x4002 C000) bit description**

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.0	GPIO Port 0.0	RD1	TXD3	SDA1	00
3:2	P0.1	GPIO Port 0.1	TD1	RXD3	SCL1	00
5:4	P0.2	GPIO Port 0.2	TXD0	AD0.7	Reserved	00
7:6	P0.3	GPIO Port 0.3	RXD0	AD0.6	Reserved	00
9:8	P0.4	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00

**PINSEL0** Special Purpose Register

PINSEL0[5:4] =  $\begin{cases} 00 & \text{GPIO} \\ 01 & \text{Tx} \\ 10 & \text{ADC} \\ 11 & \text{Not used.} \end{cases}$   
2 bits @ Bit 4 & 5



pp14.

Homework: Due A week from today (Feb 14).

1° Draw Schematics Design for GPIO Testing.

2° Take a photo of your prototype Board. To capture the work-in-progress

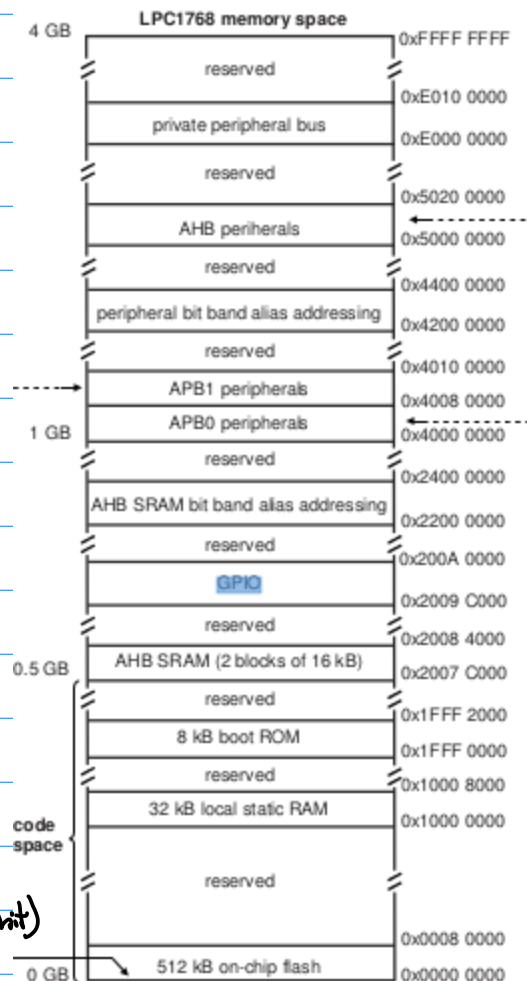
3° Combine 1° & 2° into One Pdf, then Zip it. Submit your Work online to SJSU CANVAS.

Consider CPU Architecture Discussion.

Example: CPU Block Diagram →

Memory Map.

1. 32 Bit Architecture { ALU (Arithmetic Logic Unit)  
R.F. (Register files)  
Bus System { Data ~  
Addr. ~ } Bank of Registers, 32 bit  
32 bit



# CmpE240 Spring 22

11

2. Addr. Bus 32 Bit.

Least Significant bit (Little Endian)

$a_{31} a_{30} a_{29} \dots a_2 a_1 a_0$

32 bits Address

"Little Endian" v.s. Big Endian

Most Significant Bit

Feb 9 (Wed) Today's Topics:

1° CPU Architecture;

2° MCU Xpresso, IDE, GPIO Testing Program.

Example: Compilation & Build

First Firmware Program for GPIO I/O Testing.

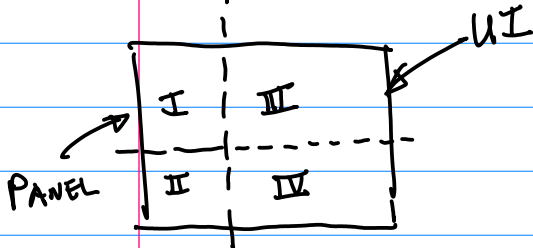
Note: Visit NXP website, Sign up to become a Developer.

Download MCU Xpresso.

Version 11.3.0

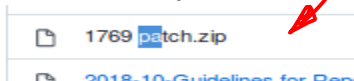
Start your IDE Xpresso.

Step 1



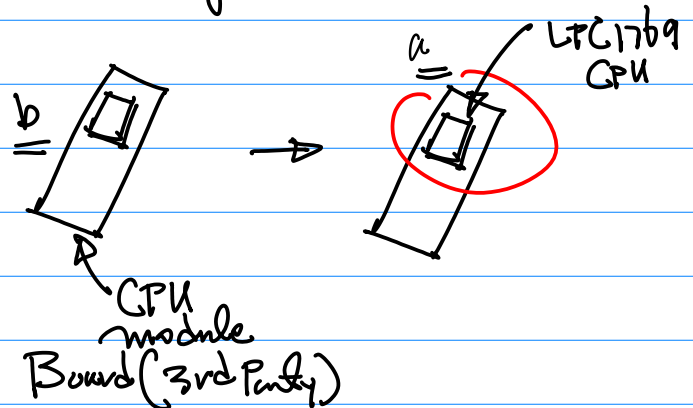
Project Panel (I):

Import LPC1769 patch from Z40 Class github.



Step 2

To set up the IDE Development Environment to match your target platform.



Go to "QuickStart" Panel to Import LPC1769 patch, And projects

Note: There are several projects, pre-tested for your references purpose including GPIO, SPI, etc.

Step 3

2018S-11-GPIO-2015-1-30.zip

Import GPIO Project (Sample code) for your Homework.

Step 4. Build & Execute GPIO Sample Project Highlight GPIO project at the project Panel → Move to

Quickstart Panel, click on "Build" to Build it.

Note: If not the first time, then Click on "Clean" to Clean it.

Step 5 Flash/Write to FLASH memory, then executing the Program Step by Step (or Execute the entire program).

Note: For Debugging, you will need to make sure the IDE setting is for "Semi-Host", e.g. your Host Laptop will be allowed communication to the Board During Debugging Process. However, when doing deployment, choose "Host" settings instead in the Board Configuration.

Homework: (Due  $1\frac{1}{2}$  weeks from Today)  
Feb 21, Monday 11:54 pm.

1. Build A Prototype System for GPIO Testing, Infrared Testing.
2. Provide Schematic Drawing. Use the tool of your preference.
3. Take a photo showing LED on! And Entire System (Prototype + Host with USB Link)
4. Provide modify C code as a Separate file.

5. Put Everything into One pdf Except C code.

6. Zip the Submission, use Naming convention

7. First Name - Last Name - SID - GPIO.zip  
Submit to CANVAS.