CMPE240
Spring2023

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Jan25,23.

Today's Topics:

1° Syllabus, "Greensheet" of the Class.

San José State University
College of Engineering/Computer Engineering Department
CMPE240 Advanced Microcomputer Design

S2023

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Class Time: Mondays and Wednesdays 1:30-2:45 PM
Office Hours: Mondays and Wednesdays 4:30 – 5:30 PM Zoom
Zoom link: Join Zoom Meeting https://us04web.zoom.us/j/9841607683?pwd=UlA3aEk1TnV4bjNLQk5CQkw0dDk4UT09 Meeting ID: 984 160 7683 Passcode: 121092
Lecture Room: Engineering Building Room 303
Lab facility: Engineering Building Room 268
Prerequisites

Note: 1° Attendance; 2° Bring your Laptop Computer; 3° Prototype Board in Class Use/Inspection.

Prototype System { Board A: CPU Module. Board B: For Graphics Display

4° Board A: CPU NXP LPC11C24 to Replace LPC1769 (Near the End of its Life, By 2024)

5° Good Throughout the entire School Session. But it will expire By the Last Day of the Class. (May 15th).

6° Lab Access Code/Policy for the Lab Usage.

Prerequisites

CmpE 180D for non CMPE or non EE undergraduate major. Students who do not provide documentation of satisfied the class prerequisite requirements by the second class meeting will be dropped from the class.

Faculty Web Page and MYSJSU Messaging (Optional)

Copies of the course materials such as the syllabus, major assignment handouts, etc. can be found from github https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F and on SJSU CANVAS.

Note: Homeworks/Projects Announcement will be Posted on CANVAS. Submission on CANVAS only.

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Course Description

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures, SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitte timers, display adapter, and other system peripherals and bus interfaces.

Required Texts/Readings

Note: Find the Datasheet on the Class github. CMPE244

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;
- Reference: ARM11 data sheets and on-line web materials on line https://github.com/hualili/ , or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Other Readings

- The reference material for ARM CPU hardware features, application notes, class handouts and lab assignments and reports, please see Professor Li's lecture notes, PPT, sample C code etc on line https://github.com/hualili/CMPE240-Adv-Microprocessors ;
- Professor Li's book materials, ARM Microprocessor Systems (in preparation for publication) https://github.com/hualili/CMPE240-Adv-Microprocessors

Other equipment / material requirements

32Bit RISC Prototype/Development Board.

Ref:

1° CPU Datasheets

2021F-107-lpc-cpu-UM... Add files vi

2° "SCH" Design.

2021F-107b-sch-#LPC... Add file

3° Lecture Notes

2022F-101-notes-cmpe240-2022-11-30.pdf

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deadlines and penalties for adding and dropping classes

Homework/Projects

Assignments and Grading Policy

Laboratory	30%
Midterm Examination	30%
Final	40%

0 to 59 F
60 to 69 D
70 to 79 C
80 to 89 B
90 to 100 A

Option 1. Target CPU Module Board
NXP LPC 11C24 ARM CPU Module (recommended a
this course), NXP LPC1769 ARM CPU Mc

Jan29 (Monday).

1. Check the CANVAS for Homework. Honesty Pledge

2. Target platform.

Background: x86. MIPS. ARM.
CISC RISC
RISC-V

NXP LPC Family.

LPC1769 — End of Life By 2024.

LPC1768 — mbed

LPC11C24

Option1: Jetson NANO 2gb.

Option2: RISC-V FPGA Board

BoM (Bill on Material) on github.

Anchor Elektronics.

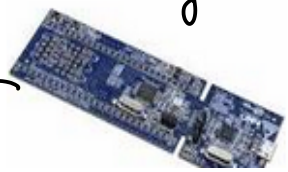
2021F-107-lpc-cpu-UM...

2021F-107b-sch-#LPC...

Example: SCH for LPC1768

Note1. CPU module, see Fig.1, its Two Connectors match the Pins in the Sch. Here

Fig.1



Note2: To make sure match the pins in the Sch to its physical Connector

Note3: Naming Convention — Enumeration Starts with Index 1 for the first pin.

J2 or J6

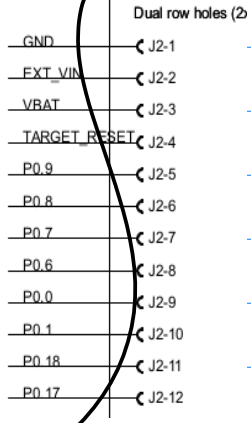
Note4: Pin Connectivity Information should be tied to its physical Device. Fig.1 And to its CPU Datasheet. ----→

→ Eventually to Software IDE.

Note5: J2-1, J2-2, ... ; And Chip pin Name & Number Such as P0.9, P0.8, ...

For LPC1768 is No Need

mbed	LPCXpresso
GND	GND
VIN (4.5-14V)	VIN (4.5-5.5V)
VB (battery supply)	VB (battery supply)
nR (reset)	RESET_N
SPI1-MOSI	P0.9 MOSI1
SPI1-MISO	P0.8 MISO1
SPI1-SCK	P0.7 SCK1
GPIO	P0.6 SSEL1
UART1-TX / I2C1-SDA	P0.0 TXD3/SDA1
UART1-RX / I2C1-SCL	P0.1 RXD3/SCL1
SPI2-MOSI	P0.18 MOSI0
SPI2-MISO	P0.17 MISO0



Functional Description of Each Pin, such as MOSI ... etc.

(Master Out Slave Input)

Homework: Due A week from today.

1. Download NXP MCU Xpresso,
2. Install MCU Xpresso;
3. Start MCU Xpresso, then Screen Capture of your MCU Xpresso Start Page, make sure it has your Personal identifier on it.