

CMPE240
Spring 2023

v/

Jan 25, 23.

Today's Topics:

1° Syllabus, "Greensheet" of the Class.

San José State University
College of Engineering/Computer Engineering
Department
CMPE240 Advanced Microcomputer Design

S2023

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Class Time: Mondays and Wednesdays 1:30-2:45 PM

Office Hours: Mondays and Wednesdays 4:30 – 5:30 PM Zoom

Zoom link: Join Zoom Meeting [https://us04web.zoom.us/j/9841607683?](https://us04web.zoom.us/j/9841607683?pwd=U1A3aEk1TnV4bjNLQk5CQkw0dDk4UT09)

pwd=U1A3aEk1TnV4bjNLQk5CQkw0dDk4UT09 Meeting ID: 984 160 7683 Passcode: 121092

Lecture Room: Engineering Building Room 303

Lab facility: Engineering Building Room 268

Prerequisites

Note: 1° Attendance; 2° Bring your Laptop Computer; 3° Prototype Board in Class Use/Inspection.

Prototype System { Board A: CPU module.

Board B:

For Graphics Display

4° Board A: CPU NXP LPC1114 to

Replace LPC1769 (Near the End of Its Life, By 2024)

6° Lab Access Code/Policy for the Lab Usage.

5° Good Throughout the entire School Session. But it will expire By the Last Day of the Class. (May 15th).

Lab facility: Engineering Building Room 268

Prerequisites

Cmpe 180D for non CMPE or non EE undergraduate major. Students who do not provide documentation of satisfied the class prerequisite requirements by the second class meeting will be dropped from the class.

Faculty Web Page and MYSJSU Messaging (Optional)

Copies of the course materials such as the syllabus, major assignment handouts, etc. can be found from github <https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F> and on SJSU CANVAS.

Note: Homeworks/Projects Announcement will be Posted on CANVAS. Submission on CANVAS only.

Course Description

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures, SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter, timers, display adapter, and other system peripherals and bus interfaces.

Required Texts/Readings

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;
- Reference: ARM11 data sheets and on-line web materials on line <https://github.com/hualili/>, or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Note: Find the Datasheet on the Class github. CMPE244

Other Readings

- The reference material for ARM CPU hardware features, application notes, class handouts and lab assignments and reports, please see Professor Li's lecture notes, PPT, sample C code etc on line <https://github.com/hualili/CMPE240-Adv-Microprocessors> ;
- Professor Li's book materials, ARM Microprocessor Systems (in preparation for publication) <https://github.com/hualili/CMPE240-Adv-Microprocessors>

Other equipment / material requirements

32Bit RISC Prototype/Development Board.

Ref:

1. CPU Datasheets

2021F-107-lpc-cpu-UM... Add files vi

2. "SCH" Design.

2021F-107b-sch-#LPC... Add file

3. Lecture Notes

2022F-101-notes-cmpe240-2022-11-30.pdf

deadlines and penalties for adding and dropping classes

Homework/Projects

Assignments and Grading Policy

Laboratory	30%
Midterm Examination	30%
Final	40%

0 to 59 F
60 to 69 D
70 to 79 C
80 to 89 B
90 to 100 A

Option 1. Target CPU Module Board

NXP LPC 11C24 ARM CPU Module (recommended as
this course). NXP LPC1769 ARM CPU Mc

Jan 29 (Monday).

1. Check the CANVAS for Homework. Honesty Pledge
2. Target platform.

Background: x86, MIPS, ARM.
CISC RISC
RISC-V

NXP LPC Family.

LPC 1769 — End of Life
By 2024.

LPC 1768 — mbed

LPC 11C24

Option 1: Jetson Nano 2gb.

Option 2: RISC-V FPGA Board

BOM (Bill of Material) on github.

Anchor Electronics.

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Example: SCH for LPC1769

Note¹: CPU module, see Fig.1, its Two Connectors match the Pins in the SCH. here

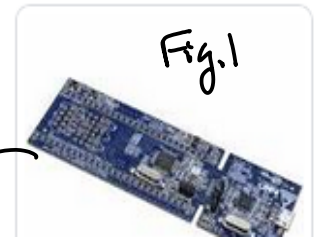
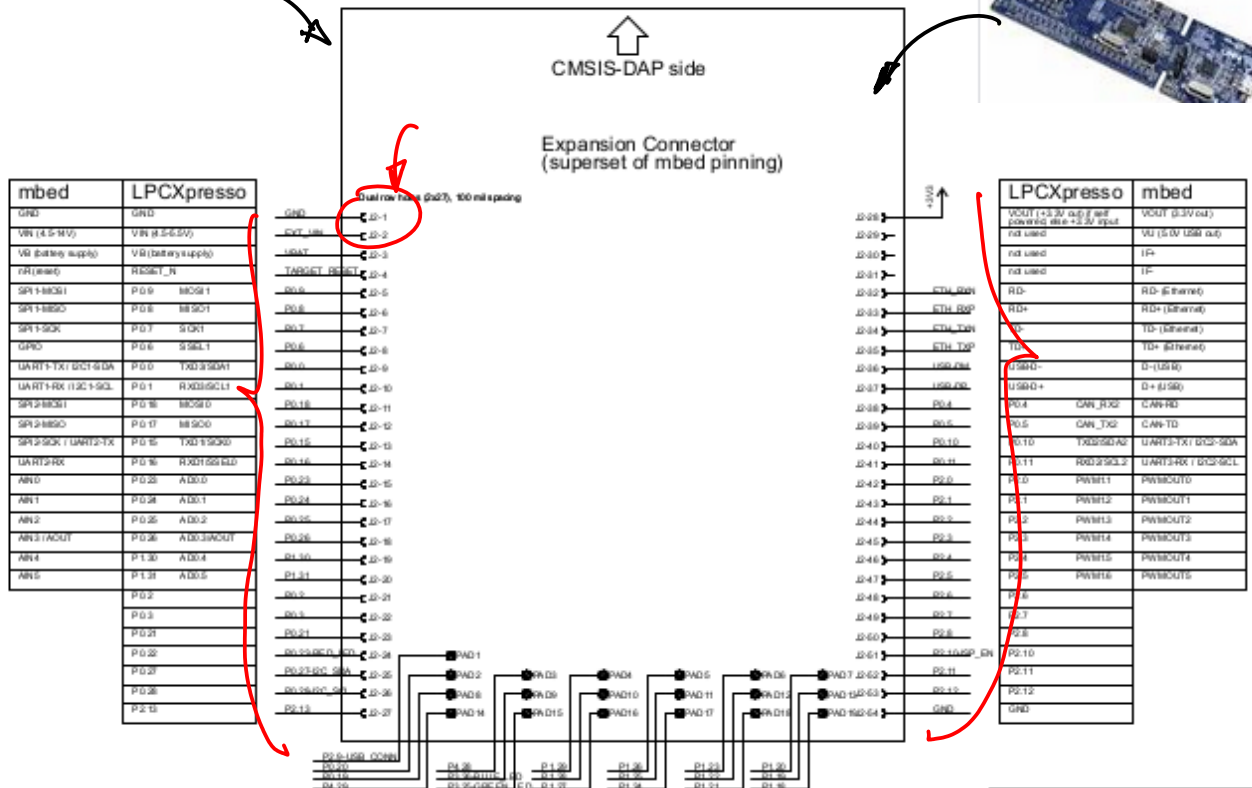


Fig.1



Note²: To make sure match the pins in the SCH to its physical Connector

Note³: Naming Convention — Enumeration Starts with Index 1 for the first pin.

J2 or J6

Note⁴: Pin Connectivity Information should be tied to its physical Device. Fig.1 And to its CPU Datasheet. --->

Eventually to Software IDE.

Note⁵: J21, J22, ... ; And Chippin Name & Number Such as p.p.9, P.p.8. ...

For LPC1768
↓ No Need

mbed	LPCXpresso
GND	GND
VIN (4.5-14V)	VIN (4.5-5.5V)
VB (battery supply)	VB (battery supply)
nR (reset)	RESET_N
SPI1-MOSI	P0.9 MOSI1
SPI1-MISO	P0.8 MISO1
SPI1-SCK	P0.7 SCK1
GPIO	P0.6 SSEL1
UART1-TX / I2C1-SDA	P0.0 TXD3/SDA1
UART1-RX / I2C1-SCL	P0.1 RXD3/SCL1
SPI2-MOSI	P0.18 MOSI0
SPI2-MISO	P0.17 MISO0

Dual row holes (2)	
GND	J2-1
EXT_VIN	J2-2
VBAT	J2-3
TARGET RESET	J2-4
P0.9	J2-5
P0.8	J2-6
P0.7	J2-7
P0.6	J2-8
P0.0	J2-9
P0.1	J2-10
P0.18	J2-11
P0.17	J2-12

Functional Description of Each Pin, such as MOSI ... etc. (Master Out Slave Input)

Homework: Due A week from today.

1. Download NXP MCU Xpresso,
2. Install MCU Xpresso;
3. Start MCU Xpresso, then Screen Capture of your MCU Xpresso Start Page, make sure it has your Personal identifier on it.

Feb 1st (Wed)

Note: 1st Attendance Sheet
2nd Ref. from the Class github.

2023 S-102-MCUXpresso_IDE_Installation_...

3rd LPC module to be finalized today by the Class. Purchasing CPU module by the end of the day today.

LPC1114
CPU module Board B
for Graphics
Engine Design
Emulation.
pre-fab.

LPC1769
End of Life
Optional Option 2
Purchase Removal of
Out-of-Stock. All parts.
~16 weeks. CPU module.

Example: Continuation of the SCH.

1. P1.9 → "P" Port, General Purpose port → AROM multiplexing
Each pin Can have more than one

functions. → Init & Config.

More than one port.

2. Connection to CPU Datasheet.

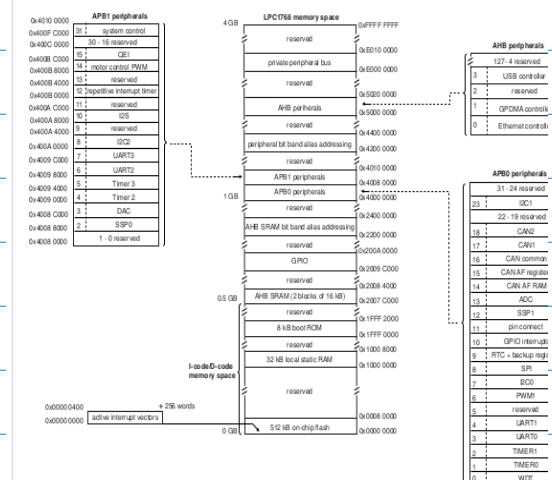


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LPC176x/5x User manual
Rev. 3.1 — 2 April 2014

User manual

PP.14 Memory map.



PI2.

1.10 Block diagram

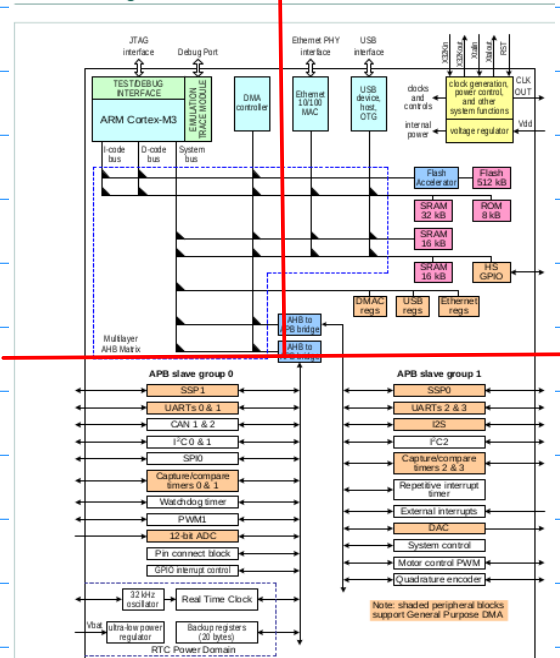
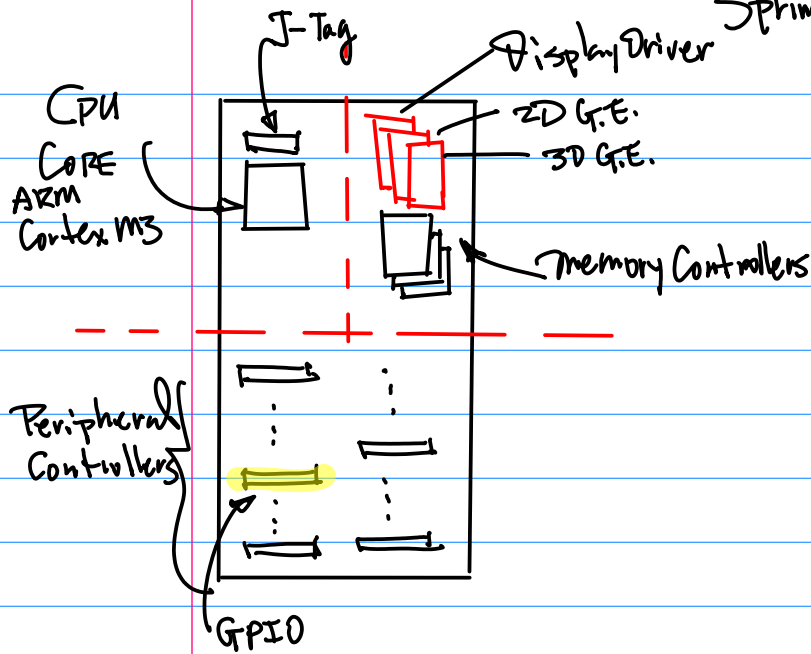


Fig 2. LPC1768 block diagram, CPU and buses



Now, find the pin(s) of the Port in the SCH.

Feb 6 (Monday).

Note: 1° CANVAS Submission of the prerequisite proof By Wednesday.

2° Screen Capture of MCU Xpresso Installation. (Be Sure to have your Personal Identifier on the Screen).

3° Bring Your LTC CPU module to the class.

Example: Continuation of CPU Architecture

Ref. GPU Datasheet pp.13, pp.12.

Discussion On the CPU Block Diagram.

1° Display Driver.

2° 2D Graphics Processing Engine

3° 3D Graphics Processing Engine. I.T.U.
4° Video Codec. } Encoder MPEG4 12bit
Decoder 265 26x
Pixel Graphics.
Vector Graphics. (Display Driver, 2D G.E., 3D G.E.)

5° General Discussion of the CPU Architecture

(1) 32 Bit RISC Architecture.

ALL. Bit width. 32bit 32bits
Register File { Special Purpose Registers.
General Purpose Registers.
Any meaningful A/L OPS.
Init & Config. 32bit

Bus Systems { Addr ~ 32bit/Uni-directional
Data ~ 32bit/Bi-directional.
~~Control Bus~~

(2) memory map. $2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2$
1K
1Meg
1Geg

4 G.!? Byte

Byte Addressable machine. ~ minimum mem. Cell with An unique addr. is a Single Byte.

0xFFFF_FFFF

Peripheral Controller
GPIO/GPIO

0x0000_0000

a. Power-up Address: ~ when the CPU is powered up, it will go to this memory location to fetch the 1st Executable instruction

b. 8 memory Banks. Equal size of memory blocks.

$$2^{32}/8 = 2^{32}/2^3 = 2^{29} = 2^9 \cdot 2^{20}$$

512 Meg.

1st BANK is enumerated as BANK 0, ..., the last BANK is BANK 7.

c. We use 3 Bits from the Address Bus to define the starting Addr. of Each Bank.

" Little Endian "

$a_{31} a_{30} \dots a_1 a_0$

$a_{31} a_{30} a_{29} \dots a_{28} \dots$

0 0 0 . 0 BANK 0 0x0...
0 0 1 . 0 BANK 1 0x2000-0000
0 1 0 . 0 BANK 2 0x4000-0000
:
1 1 1 . 0

d.

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Chapter 2: LPC176x/5x Memory map
Rev. 3.1 — 2 April 2014

User manual

2.1 Memory map and peripheral addressing

The ARM Cortex-M3 processor has a single 4 GB address space. The following table shows how this space is used on the LPC176x/5x.

Table 3. LPC176x/5x memory usage and details

Address range	General Use	Address range details and description
0x0000 0000 to 0x0000 0000	On-chip non-volatile	0x0000 0000 - 0x0007 FFFF For devices with 512 kB of flash memory

Address for GPIO Controller. 0x2...
0x4...

Feb 8. (Wed).

Note: Inspection of CPU module.

1° LPC1769 or LPC1114;

2° Layout Design. CPU module Location Standoffs. Wire#

Prototyping wire

30AWG Blue

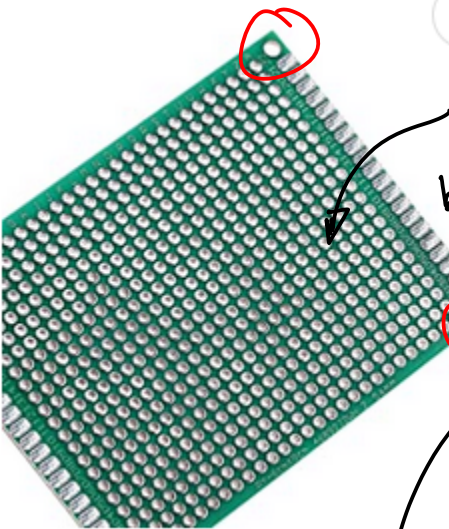
28~32 AWG

Product ID: 1446

\$7.50



Prototype Board, Note: a. Through-Hole

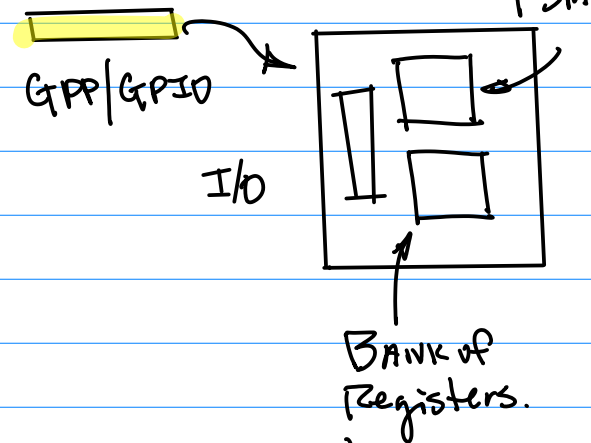


b. is uniformly formed with plate coating
c. Mounting holes at corners.

c. Standoffs.

~ \$5-\$15

2° Special Purpose Registers.



Special Purpose Registers.

Task 1: Init & Config.

Naming Convention: TISC
(Uniformity, Regularity, Orthogonality)

Root (3 Letters)

↓ CN

Prefix + Root
3 Letters 3 Letters

GPI

↓

GPP

↓

GP0, GP1, GPx

GP0CON

Software to Drive the Peripheral Controller

↓
Compiler, gcc. Open Source → Target CPU

Note: Please Bring Your 1° CPU module; 2° USB Cable; 3° Laptop with MCU Expresso for Inspection.

Example: Continuation of CPU Architecture Discussion

Note! A GPP/GPIO Controller is mapped to the memory map. Read CPU Datasheet to find its Location;

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2nd Special Purpose Register

GPx + DAT

Root.

GP0 DAT.