

Aug. 21 (Monday).

Organizational meeting.

1. github.

<https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F>

2.

Course and Contact Information

Instructor(s): Harry Li

Office Location: Engineering Building, Room 267A

Telephone: (650) 400-1116

Email: hua.li@sjsu.edu

Office Hours: M.W. 3:00-4:00 pm

→ In Person.

Class Days/Time: Mondays, Wednesdays, 1:30-2:45 pm

Classroom: Engineering Building, Room 331

Prerequisites: CmpE 180D for non CMPE or non EE undergraduate
documentation of having satisfied the class prerequisite requirement
dropped from the class.

3. Emphasis on the Advanced Nature of the
Microprocessor Systems. → Embedded
Nature, ARM CPU. → GPU: graphics Processing
Unit

Architecture of a computing system including system bus, memory subsystems and peripherals.
Uni-directional and bidirectional bus architectures. SRAM and FLASH memories and their interfaces with
the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter receiver, timers,
display adapter, and other system peripherals and bus interfaces.

→ Engine for Deep Learning, AI etc.

4. Hands-on.

Datasheets. → Spec. → Hardware
Prototype
Board
With Color
LCD
Display

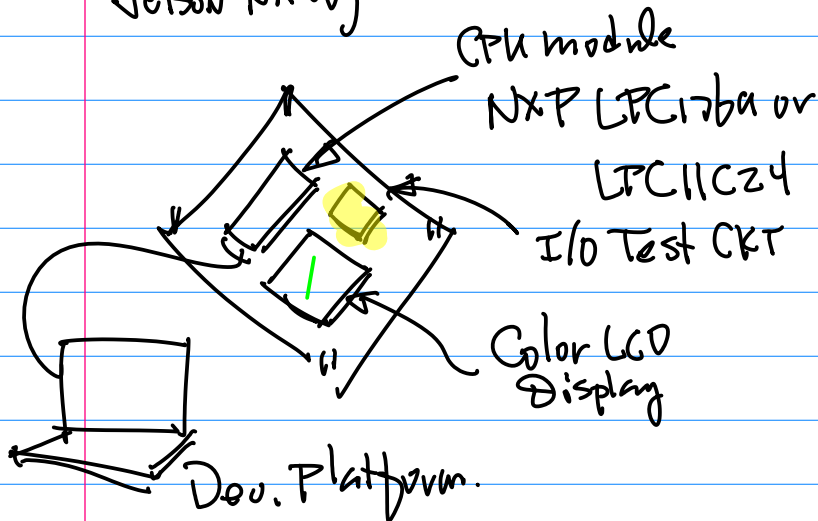
2D
Graphics
Engine

↓

3D Graphics Engine



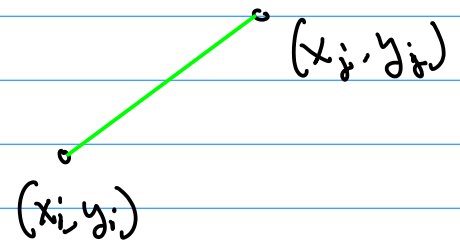
Benchmarking (with Ref. to NVDA
Jetson Nano)



Live Drawing Sample Code.

(x_i, y_i) Starting pt.

(x_j, y_j) Ending pt.



Action Item (Homework, No Submission)

About 22,800,000 results (0.59 seconds)



NXP Semiconductors

<https://www.nxp.com>

NXP Semiconductors: Automotive, IoT & Industrial Solutions

NXP is a global semiconductor company creating solutions that enable secure connections for a smarter world.

Results from nxp.com



Note: Homework/Projects are ^{to be} posted
on CANVAS, with written
Requirements. Those are the
material to be submitted.

5. PPTs, Lecture Notes (White Board Notes),
Datasheet(s), are posted on the
github.

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;

- Reference: ARM11 data sheets and on-line web materials on line <https://github.com/hualili/>, or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Note: 1° Initial Sample Projects, ~ A Dozen
Sample Projects.

2018F Add files via upload
1769 patch.zip Add files via upload

GPP (General Purpose Port)

Target CPU
NXP LPC1114
LPC1769

Next Level of the Sample Code

2018S-10-LCD-DrawLi... Add files via upload

The Code was for LPC1769,
But Newer Samples for GPP, Graphics
Display for LPC1114 were developed
and posted on the github.

The Lower After
Sample Code for
2D & 3D Engine Design.

PPT material in pdf.
will be used in the Class.

Datasheet. Note: 1° CPU Datasheet is in CMPE244 folder

2° CPU Datasheet

SCH"

Grading Information

Quiz, Homework, Projects	30%
Midterm Examination	30%
Final Examination	40%

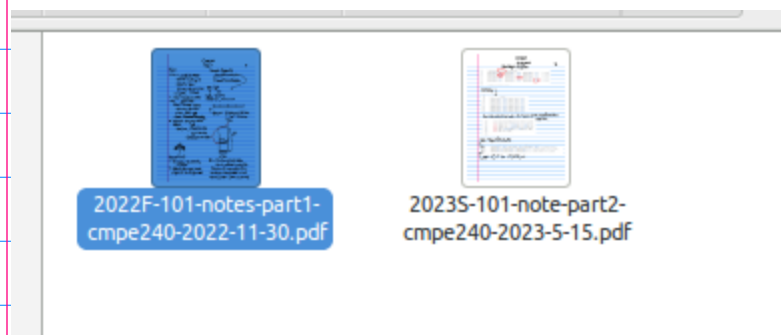
August 23rd (Wed)

Announcement :

1° Lab Space Rm 268

2° CANVAS to be up by
this week.

Introduction.



Example: Architecture of LPC1114
(LPC1114)

Can be purchased from
digi-key.com or
Mouser Electronics



NXP Semiconductors

<https://www.nxp.com/general-purpose-mcus/lpc11...>

Scalable Entry Level 32-bit Microcontroller (MCU) based ...

The LPC11Cxx MCU family is designed for 8/16-bit micro-controller operations,



CmPE 240
Fall 2023

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Restore Session

Utility/CmPE240-ADV-MicroProce... OM13093UL NXP USA INC. | DEVE...

← → ↺ 🏠

https://www.digikey.com/en/products/detail/nxp-usa-inc/O

Search

DigiKey All Products Enter keyword or part #

Product Index > Development Boards, Kits, Programmers > Evaluation Boards > Embedded MCU, DSP Evaluation Boards > NXP USA Inc. OM13093UL

OM13093UL




Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

Digi-Key Part Number	568-14402-ND
Manufacturer	NXP USA Inc.
Manufacturer Product Number	OM13093UL
Description	LPCXPRESS0 LPC11C24 EVAL BRD
Manufacturer Standard Lead Time	16 Weeks
Detailed Description	LPC11C24 LPCXpresso™ LPC11C00 ARM® Cortex®-M Evaluation Board
Customer Reference	<input type="text" value="Customer Reference"/>

Note: Please Start the
Purchasing Process.
Note: CPU Datasheet.



2011

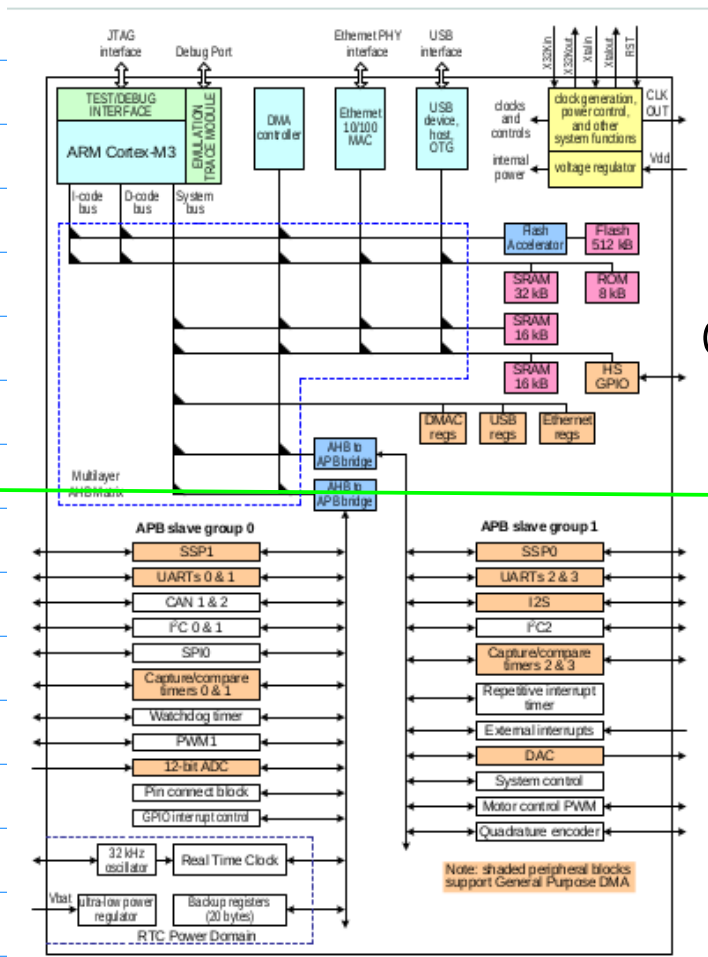
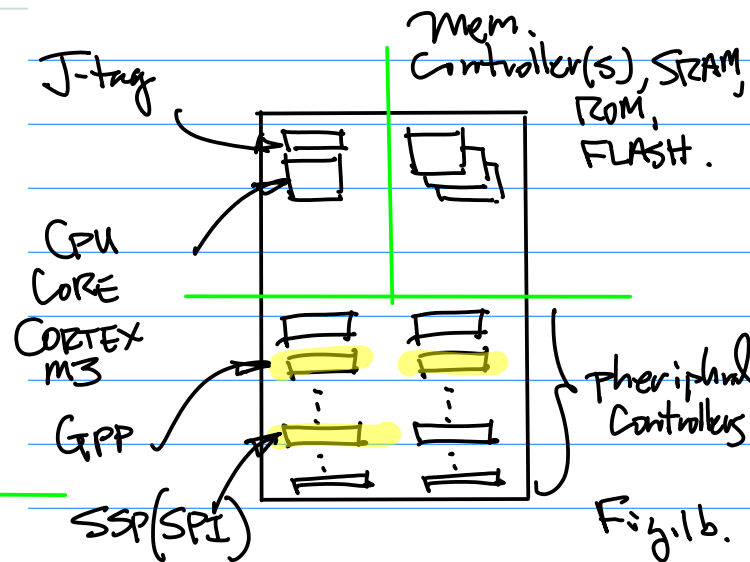
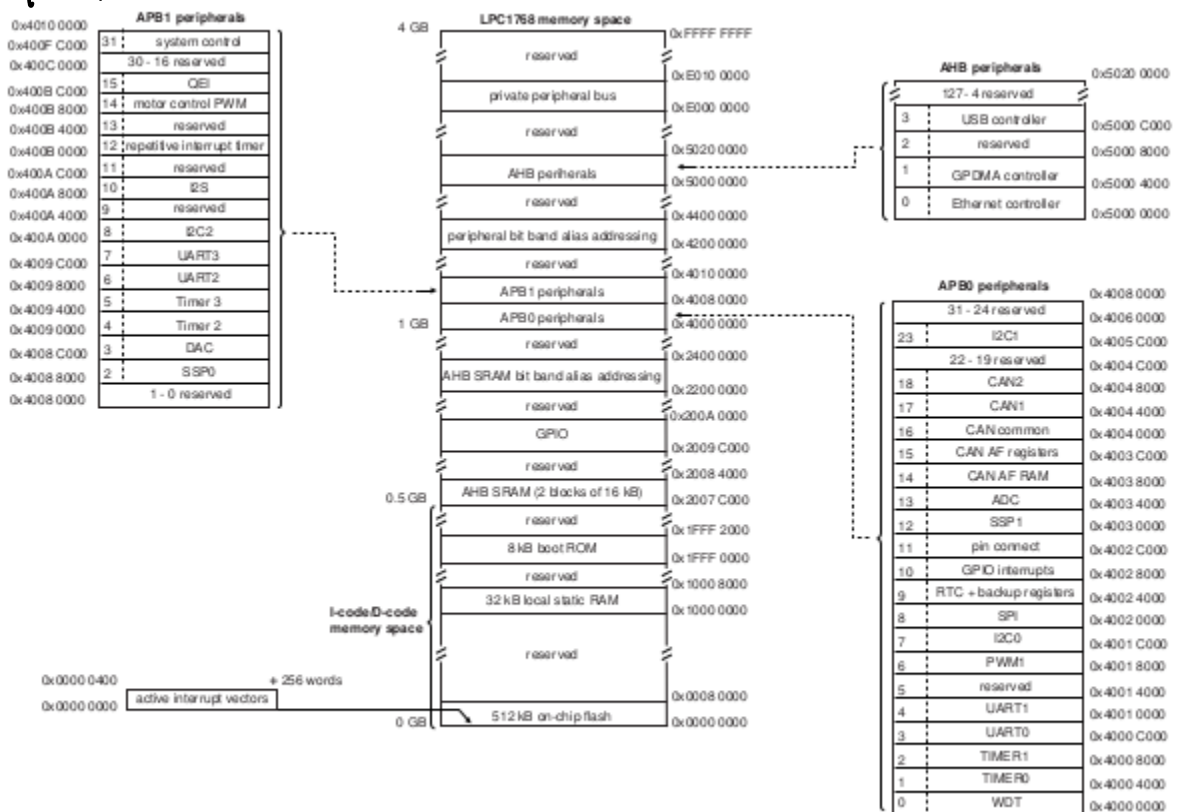


Fig 1.a



GPP/GPIO: General Purpose
or
General Purpose I/O
S.P.I. (Serial Peripheral Interface)
Note: One of the GPPs supports
Ex.Int. (External Interrupt).

Memory Map.



CmPE240

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Note: For the memory map Discussion:

1° RISC: Reduced Instruction Set Computer.

ARM.
MIPS (Golden Rules:
Uniformity,
Regularity,
Orthogonality)

3° Byte Addressable Machine.

A smallest memory cell with an Unique Address is a Single Byte.

2° 32 Bit RISC Processor → 32bit

Architecture

32bit Addr. Bus.

32bit Data Bus.

32bit R.F. (Register File)

{ GPRs (General Purpose Registers) 32bits.
SPRs (Special Purpose Registers)

3 Cats.

32bit memory map.

$$2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2$$

1K
(1024)

1M
(1K x 1K)

1G

4G? Byte!

0xFFFF_FFFF

SPI Controller

0x0000_0000 →

Power-up Addr.

August 28 (Monday).

Note: 1° CANVAS is up.

2° CPU module & LCD module

ST7725 Controller
SPI - Interface

FLASH memory
ST25B.

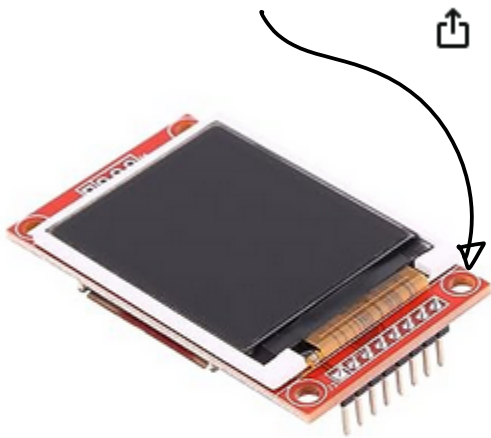
CMPE240

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cs > Computers & Accessories > Tablet Replacement Parts > LCD Displays

Note: 8-pins or 10 pins module are OK for the Implementation



1.8 inch SPI TFT LCD Display
Module for ST7735 128x160
51/AVR/STM32/ARM 8/16 bit

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4.0 ★★★★★ 42 ratings

\$10⁹⁹

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Brand Walfront

Personal All in One

computer
design type

Operating Linux

Roll over image to zoom in

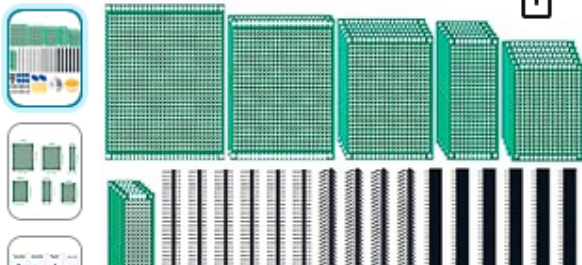
Note: ST7725 or
ST7735.

3^o Bill of Material (BOM) for
this Class:

- 1^o CPU module
- 2^o LCD module
- 3^o Wire Wrapping Board.

4" x 3" Through-Holes with
metal plating (Just
to cover the holes,
Not the Entire Board)

OR your choice



Miuzei PCB Board Prototype Kit
for Electronic Projects, Circuit
Solder Double-Side Board with 40
Pin 2.54 mm Male to Female
Headers Connector, 2P&3P Screw

Example: Memory Map.

Divide the Mem. Map into

8 Equal Banks.

		Starting Addr.	
		$a_{31} a_{30} a_{29}$	
BANK 0	First	000	0000; 0000; ...; 0000
BANK 1	2nd	001	0010; ...
BANK 2	3rd	010	0100; ..
⋮		⋮	
BANK 7	8th	111	

MSB $a_{31} a_{30} \dots a_2 a_1 a_0$ \leftarrow LSB
32 bits Addr. Bus

Note: "Little Endian" Convention

Choose $a_{31} a_{30} a_{29}$ to Identify the memory Bank.

$a_{31} a_{30} a_{29} 0; 0000; \dots; 0000$

Lowest Addr.

$a_{31} a_{30} a_{29} 1; 1111; \dots; 1111$

Highest Addr.

$$2^{32} / 2^3 = 2^{29} = 2^9 \cdot 2^{20}$$

512 / Meg.

Example: Identify One of the SPI Peripheral Controllers By mem. map.

Note: Important, to Be used in the Design Process.

Memory Bank with a Starting Addr.

$0x4000-0000 \rightarrow$

3rd BANK (BANK 0, BANK 1, BANK 2)

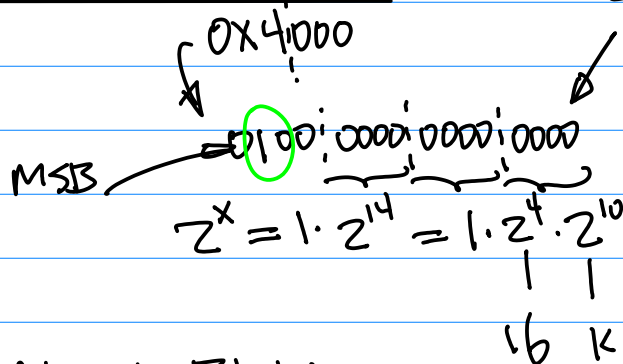
Find A SPI Block

9	RTC + backup registers	0x4002 4000
8	SPI	0x4002 0000
7	I2C0	0x4001 C000

SPI Peripheral Controller is Located at $0x4002-0000$

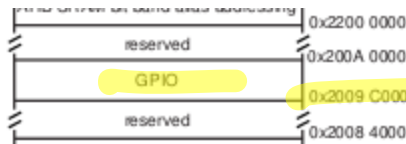
Question: How Big is the memory Block for SPI Controller?

0x4002_4000
- 0x4002_0000



Note: This Block of memory is employed for A set of SPR's (Special Purpose Registers) to perform S.P.I function.

Example: GPP (General Purpose Port)



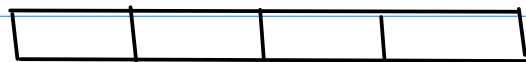
GPP (Peripheral Controller)

mem. map Location & its Block Size

SPRs (Special Purpose Registers)

Responsible for Init & Config.

Control Register.



32 bit SPR.

Naming Convention "3+3" for All if possible

Prefix 3 Letters + Root 3 Letters

August 30 (Wed)

Note: 1^o CANVAS has been updated with Homework One ON Friday, OPT. Honestly Pledge Signed Form to Be Submitted ON CANVAS.

2^o Bill of Material.

Ref: ON the github of CMPE240 2018S-2-... Bill-of-Material

3^o Homework (0 pt) Due Sept. 10 (Sun)

Installation of NXP MCU Expresso.

Submission: Screen Capture that Shows the MCU Expresso. +

Personal Identifier.

Ref: github. → PPT for MCU Expresso Configuration.

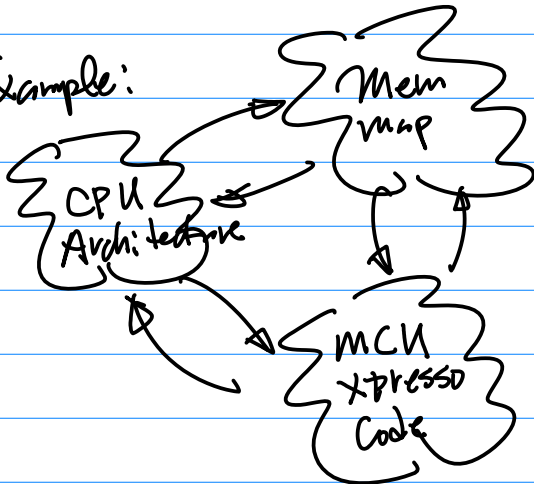
Nxp Developer Forum, pdf

Note:

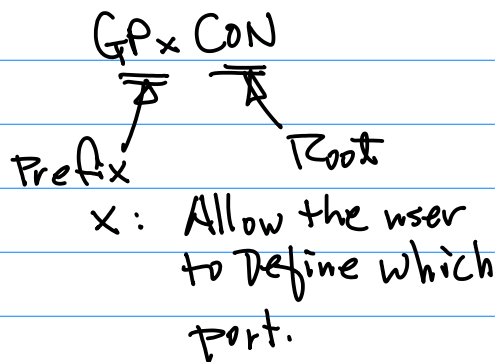
gcc/g++ → Porting to the Target → Porting to the target
Open Source CPU, NXP Board
ARM CPU Core LPC family
Cortex M3

4^o Please bring the CPU module to the class for inspection & Discussion.

Example:

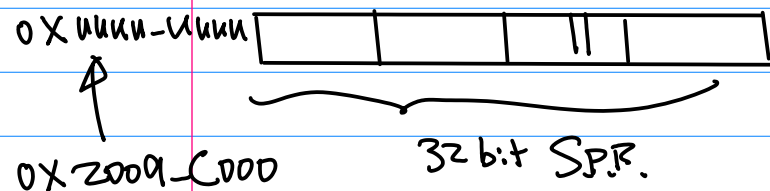


Design of GPP



Note: Multiple I/O pins possible for Each GPx

GPACON



GPA Port Pin 5 as an Output pin → Need to Identify the Bit(s) in GPACON for the selection Purpose.

Sept. 6 (Wed)

Example: Inspection of LPC1114 or LPC1769.

Purpose: Identify Pin 1 on the module. Match it up to SCh of the Board module.

Ref: On the github LPC1114 AND LPC1769.

Note: 1° Physical pin assignment, e.g. pin 1, pin 2, ..., etc.

2° Namings of the pins

- a. Connector Related
- b. CPL Datasheet Related (C/C++ IDE, Code)
- c. Functionality Related.

Use All of the above in your Connectivity Table

3° Power Pins

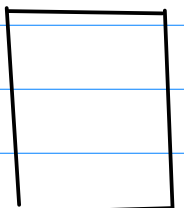
- a. V_{DD}, V_{DDT} pins
- b. GND pins

Common GND

4° SPI (Serial Peripheral Interface).



Master



"Slave"

CMPE240

F2023

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"3+1" Pins

$\left. \begin{array}{l} \text{MOSI (Master Out/Slave In)} \\ \text{MISO (.. In/.. Out)} \\ \text{SCK (Serial CLK)} \end{array} \right\} \text{"3"}$
EN/nEN Enable Active high
or Active Low.

