August 23rd (Mon).

CMPE240 Section 1.

CMPE240

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Office Hours: M.W. 3:40-4:40 pm.

Advanced Microprocessor Systems = Prototype System with A CPU module

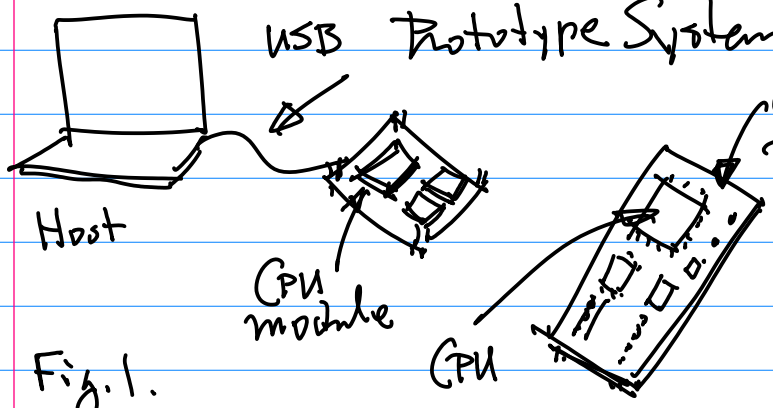


Fig. 1.

GPU (Graphics Processing Unit), Array of Processors, Machine Learning, AI. Autonomous Systems. Nvda Jetson TX2.

Textbooks, References

1° NXP LPC1769 CPU Datasheet 800+ pages Homework: Down Load pdf. Before Next Monday. Aug. 30th.

2. LPC1769 schematics of the CPU module

3. Nvda Jetson NANO Datasheet on TX2 (6 CPU + 256 GPU) 400+ pages. 5% Bonus. (optional)

4. RISC-V. Open Source Architecture, A super set of ARM. FPGA, Verilog. SoC. +RTOS. (optional) +5%

A proposal (One Paragraph) By Sept. 1st (Wed). submit to my Email;

Note: Buy LPC1769 CPU module.

digi-key.com, mouser.com, etc.

Grading Policy & Projects

2 projects (phase I & II)

2D Graphics Processing Engine → 3D Graphics Processing Engine } a le

2D Graphics Processing Engine → 3D Graphics Processing Engine { @ 3D shadow. 10% = 30pts, 30%.
& Diffuse Reflection 10%
10%

midterm: 30%, Final 40% (Comprehensive)

August 25 (Wed)
Today's Topics:
1° Bill of material
Reference: github/hwalili/Cmpe240/2018F

Option 1. (5%+) NVDA NANO
{ a. Likely Devices Drivers, O.S. C/C++, Python.
b. I/O Interface: "EdgeAI" GPIO, SPI.

Option 2. (5%+) RISC-V Target
SoC, FPGA Board,

Proposal (one paragraph), Submission By Sept 1st (Wed) via E-mail.

The B.O.M.
1. CPU module NXP LPC1769
↓
3rd Party (DigitalArt), module
To Distributors
Digikey.com, Mouser.com etc. Expecting Delays. Lead Time over 8 weeks
Alternative { Re-use the previously used module
Team (4 person)

Policy ON Project Submission.
1°. Form 3-4 person Team.
2° No Source Code/Design material Can be Copied; All Course material has to be completed individually;
3° Late Project, 10% per week;

Each person will need to have his/her Board;
Option 1: NANO. @ 400+ pages Datasheet
"firmware"
& Jetpack 4.3 or Higher
(O.S. + Libs. + Packages)

Tool for Flashing the CPU module

c. Coding in Both user & Kernel Spaces. → O.S. Distr. Toolchain, Device Driver Debugging & Development;

Option 2. RISC-V. verilog, FPGA.

2. Power Regulator IC series 7812, 7805 ... 1117

78xx

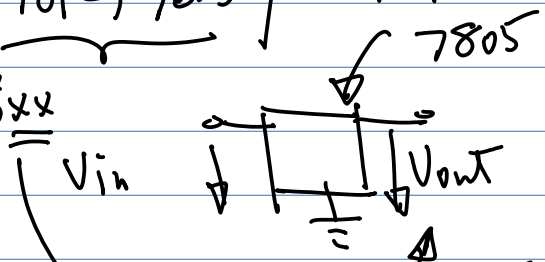


Fig.1.

"05": 5.0 VDC, "12": 12VDC

Fig.

$V_{in} \geq V_{out} + 1.5\,VDC$ ... (1)

DC Voltage Source

a. About 7805 1000 mW.

b. 7.5VDC OR 9.VDC

Wall mount Adaptor

To Vin of 7805

@ 1000mW + 500 mW = 1500mW

Current Rating.

c. Why Do we use it?

→ Deploy the System.

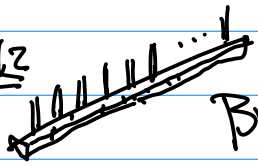
3. "Glue" Components < Resistors a. Caps 4.7 mF b.

c. LEDs. (Red, Green) for Debugging purpose, for PWR. (GPIO), I_{LED} = 4~10mA

d. Connectors.

d1 J1 for PWR Input

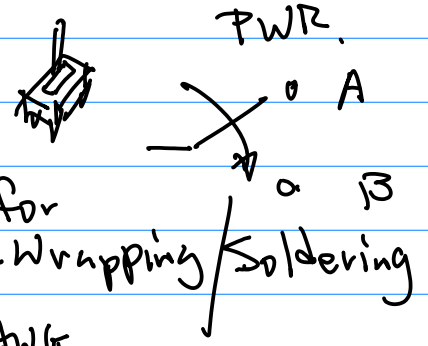
d2



to mount CPU module.

e. Switch. S/W1: to toggle PWR.

S/W2



f. Wire for Wire Wrapping / Soldering 28-30 AWG

4. Color LCD Display module

a. SPI (Serial Peripheral Interface)

b. Software Graphics (Driver) C/C++ Lib. to Activate/Initialize LCD.

MCUXpresso (I.D.E.)

S.T. Lib.

5. "Other" thing.

RJ-45 Connector Right Angle