CMPE240
Fall 2023

1/

Aug 21 (Monday).
Organizational meeting.

1. github.

https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F

2.

Course and Contact Information

Instructor(s): Harry Li
Office Location: Engineering Building, Room 267A
Telephone: (650) 400-1116
Email: hua.li@sjsu.edu
Office Hours: M.W. 3:00-4:00 pm ← In Person.
Class Days/Time: Mondays, Wednesdays, 1:30-2:45 pm
Classroom: Engineering Building, Room 331
Prerequisites: CmpE 180D for non CMPE or non EE undergradua
documentation of having satisfied the class prerequisite requireme
dropped from the class.

3. Emphasis on the Advanced Nature of the Microprocessor Systems. → Embedded Nature, ARM CPU. → GPU: graphics Processing Unit

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures. SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter receiver, timers, display adapter, and other system peripherals and bus interfaces.

→ Engine for Deeplearning, AI etc.

4. Hands-on.

Datasheets. → Spec. → Hardware Prototype Board With Color LCD Display ← 2D Graphics Engine

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CmpE240 Fall 2023

3D Graphics Engine

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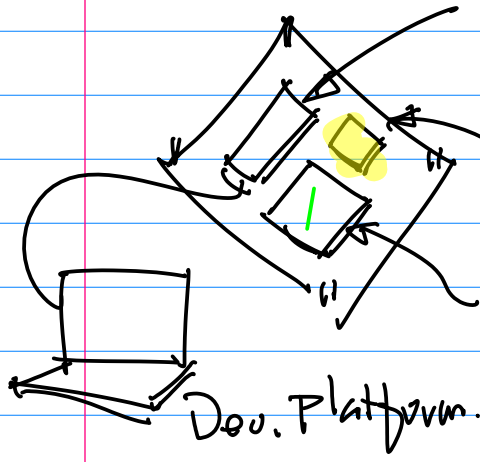
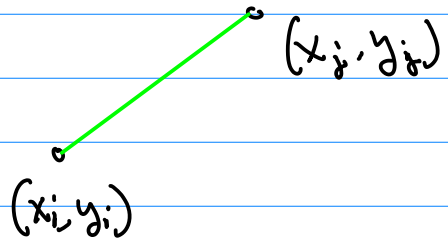
Benchmarking (with Ref. to NVDA Jetson NANO)



Live Drawing Sample Code.

(x_i, y_i) Starting pt.

(x_j, y_j) Ending pt.



Action Item (Homework, No Submission)

About 22,800,000 results (0.59 seconds)

NXP Semiconductors
https://www.nxp.com

NXP Semiconductors: Automotive, IoT & Industrial Solutions

NXP is a global semiconductor company creating solutions that enable secure connections for a smarter world.

Results from nxp.com

Note: Homework/Projects are ~~to be~~ posted on CANVAS, with Written Requirements. Those are the material to be Submitted.

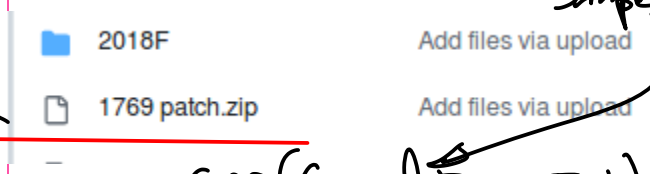
5. PPTs, Lecture Notes (White Board Notes), Datasheet(s), are posted on the github.

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;

- Reference: ARM11 data sheets and on-line web materials on line https://github.com/hualili/ , or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Note: 1° Initial Sample Projects, ~A Dozen Sample Projects.

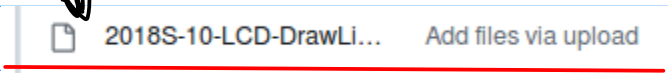


GPP (General Purpos Port)

Target CPU
NXP LPC11C24
LPC1769

The Code was for LPC17ba, But Newer Samples for GPP, Graphics Display for LPC11C24 were developed and posted on the github.

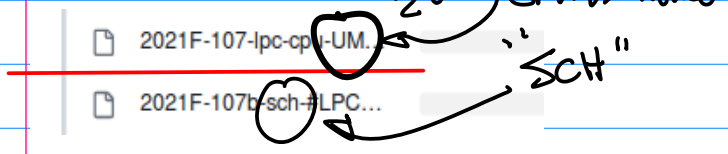
Next Level of the Sample Code



The Lower After Sample code for 2D & 3D Engine Design.

PPT Material in pdf.
will be used in the Class.

Datasheet. Note: 1° CPU Datasheet is in CMPE244 folder



Grading Information

Quiz, Homework, Projects	30%
Midterm Examination	30%
Final Examination	40%