

Aug. 21 (Monday).

Organizational meeting.

1. github.

<https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F>

2.

Course and Contact Information

Instructor(s): Harry Li

Office Location: Engineering Building, Room 267A

Telephone: (650) 400-1116

Email: hua.li@sjsu.edu

Office Hours: M.W. 3:00-4:00 pm

→ In Person.

Class Days/Time: Mondays, Wednesdays, 1:30-2:45 pm

Classroom: Engineering Building, Room 331

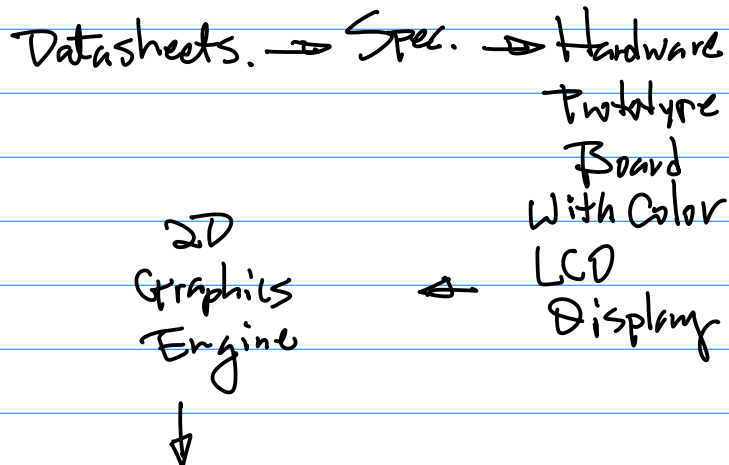
Prerequisites: CmpE 180D for non CMPE or non EE undergraduate
documentation of having satisfied the class prerequisite requirement
dropped from the class.

3. Emphasis on the Advanced Nature of the
Microprocessor Systems. → Embedded
Nature, ARM CPU. → GPU: graphics Processing
Unit

Architecture of a computing system including system bus, memory subsystems and peripherals.
Uni-directional and bidirectional bus architectures. SRAM and FLASH memories and their interfaces with
the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter receiver, timers,
display adapter, and other system peripherals and bus interfaces.

→ Engine for Deep Learning, AI etc.

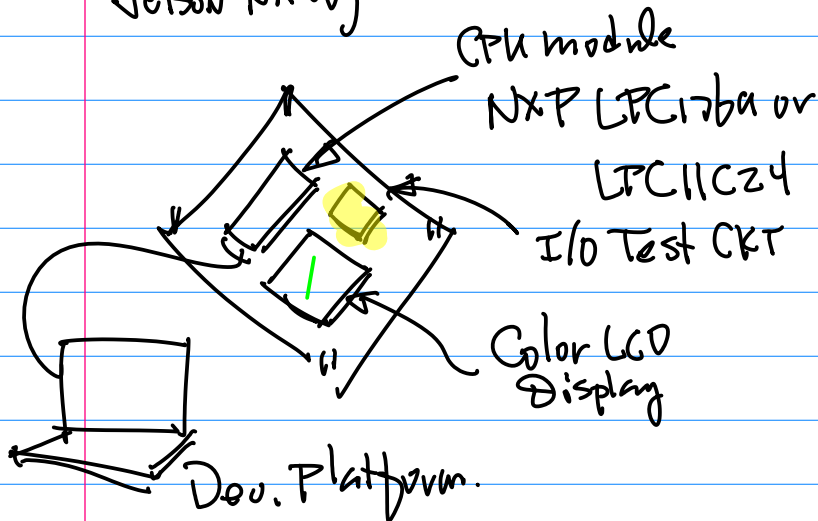
4. Hands-on.



3D Graphics Engine



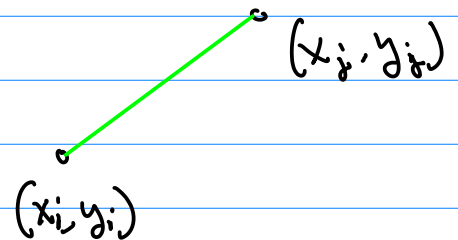
Benchmarking (with Ref. to NVDA
Jetson Nano)



Live Drawing Sample Code.

(x_i, y_i) Starting pt.

(x_j, y_j) Ending pt.



Action Item (Homework, No Submission)

About 22,800,000 results (0.59 seconds)



NXP Semiconductors

<https://www.nxp.com>

NXP Semiconductors: Automotive, IoT & Industrial Solutions

NXP is a global semiconductor company creating solutions that enable secure connections for a smarter world.

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Note: Homework/Projects are ^{to be} posted
ON CANVAS, with written
Requirements. Those are the
material to be submitted.

5. PPTs, Lecture Notes (White Board Notes),
Datasheet(s), are posted on the
github.

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;

- Reference: ARM11 data sheets and on-line web materials on line <https://github.com/hualili/>, or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Note: 1° Initial Sample Projects, ~ A Dozen
Sample Projects.

2018F Add files via upload
1769 patch.zip Add files via upload

GPP (General Purpose Port)

Target CPU
NXP LPC1114
LPC1769

Next Level of the Sample Code

2018S-10-LCD-DrawLi... Add files via upload

The Code was for LPC1769,
But Newer Samples for GPP, Graphics
Display for LPC1114 were developed
and posted on the github.

The Lower After
Sample Code for
2D & 3D Engine Design.

PPT material in pdf.
will be used in the Class.

Datasheet. Note: 1° CPU Datasheet is in CMPE244 folder

2° CPU Datasheet

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Grading Information

Quiz, Homework, Projects	30%
Midterm Examination	30%
Final Examination	40%

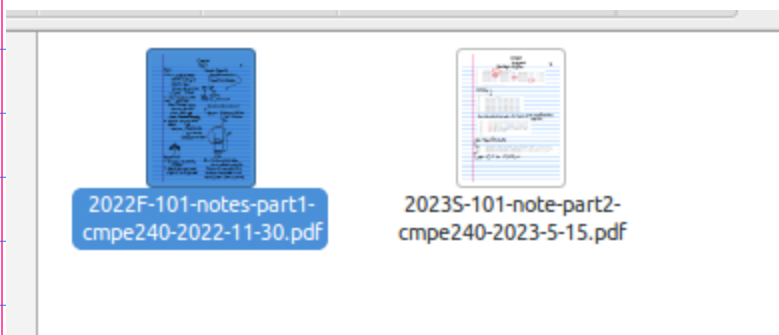
August 23rd (Wed)

Announcement :

1° Lab Space Rm 268

2° CANVAS to be up by
this week.

Introduction.



Example: Architecture of LPC1769
(LPC1114)

Can be purchased from
digi-key.com or
mouser electronics



NXP Semiconductors

<https://www.nxp.com/general-purpose-mcus/lpc11...>

Scalable Entry Level 32-bit Microcontroller (MCU) based ...

The LPC11Cxx MCU family is designed for 8/16-bit micro-controller operations,



CmPE 240
Fall 2023

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Restore Session

Utility/CmPE240-Adv-MicroProce

OM13093UL NXP USA INC. | DEVE

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https://www.digikey.com/en/products/detail/nxp-usa-inc/O

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Product Index > Development Boards, Kits, Programmers > Evaluation Boards > Embedded MCU, DSP Evaluation Boards > NXP USA Inc. OM13093UL

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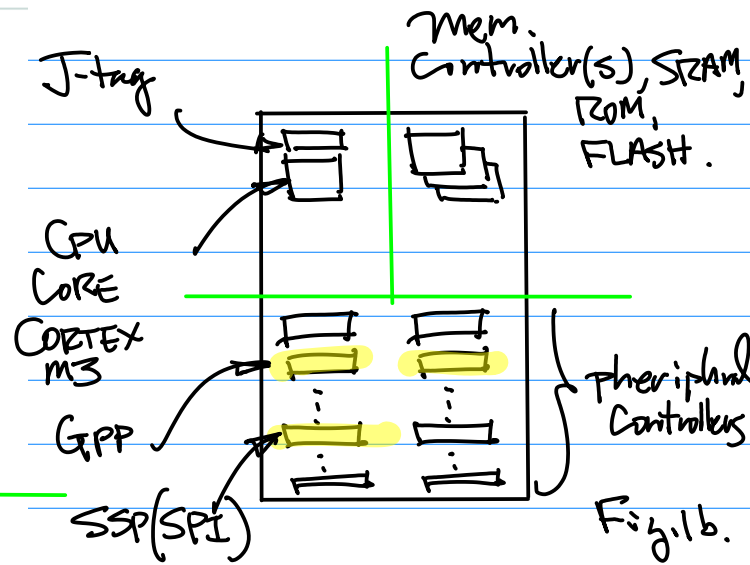
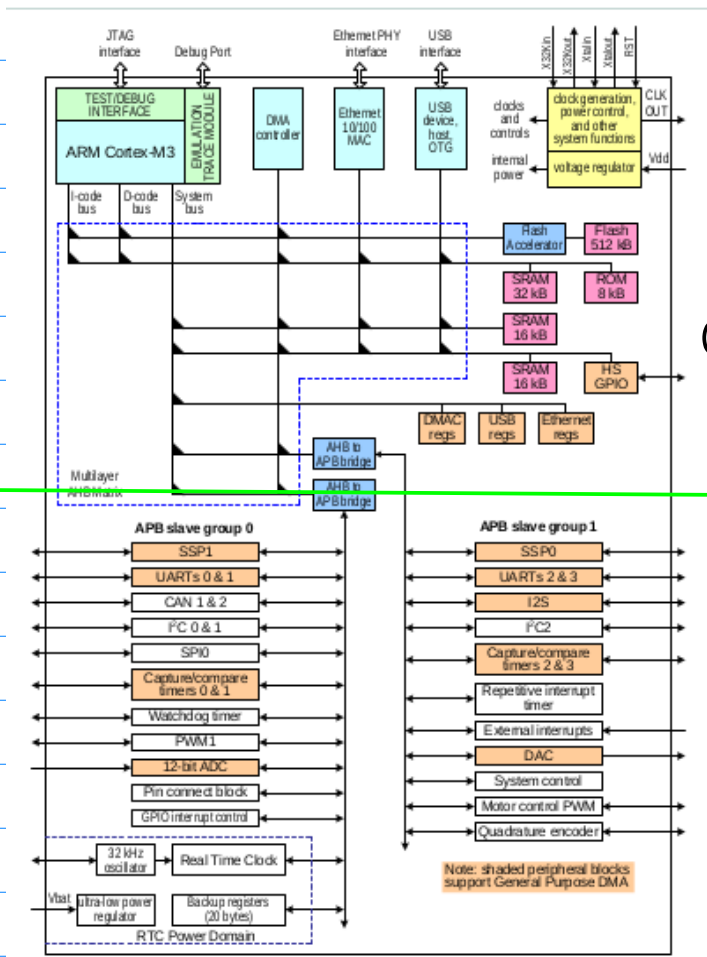
Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

Digi-Key Part Number	568-14402-ND
Manufacturer	NXP USA Inc.
Manufacturer Product Number	OM13093UL
Description	LPCXPRESS0 LPC11C24 EVAL BRD
Manufacturer Standard Lead Time	16 Weeks
Detailed Description	LPC11C24 LPCXpresso™ LPC11C00 ARM® Cortex®-M Evaluation Board
Customer Reference	<input type="text" value="Customer Reference"/>

Note: Please Start the
Purchasing Process.
Note: CPU Datasheet.

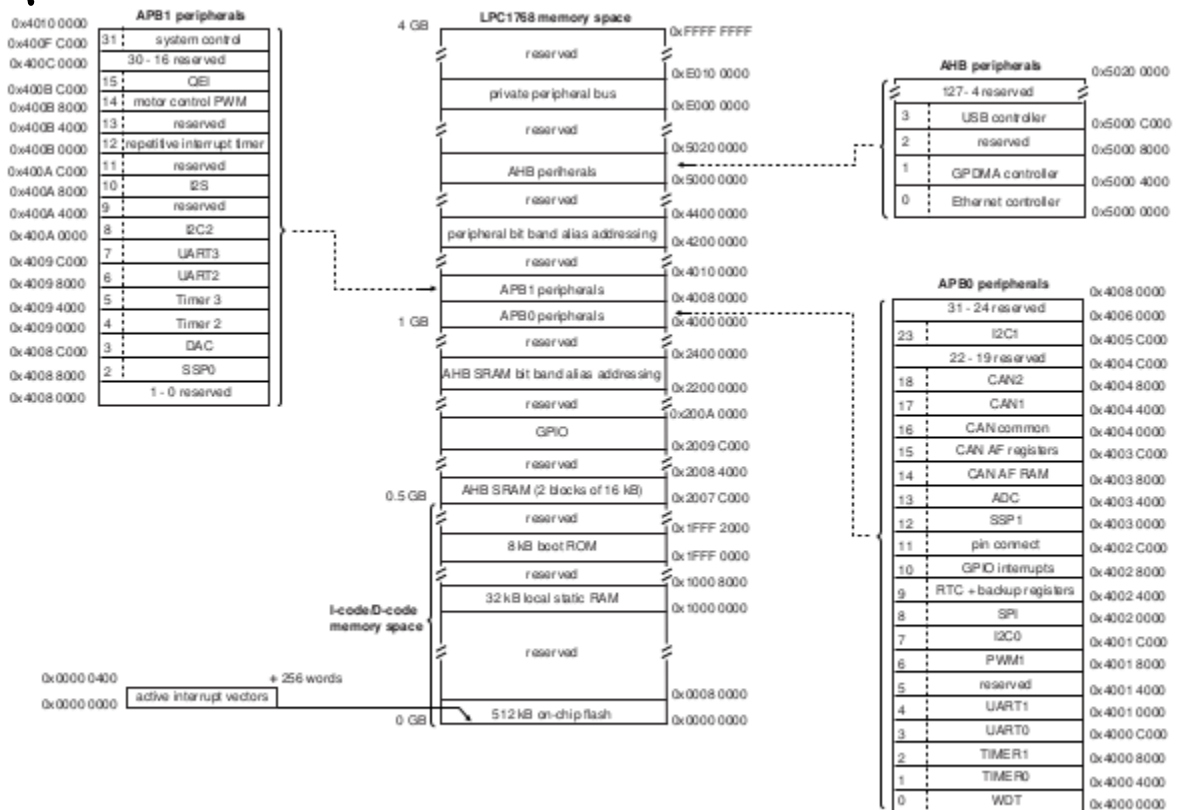


2011



GPP/GPIO: General Purpose
or
General Purpose I/O
S.P.I. (Serial Peripheral Interface)
Note: One of the GPPs supports
Ex.Int. (External Interrupt).

Memory Map.



CmPE240

F2023

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Note: For the memory map Discussion:

1° RISC: Reduced Instruction Set Computer.

ARM.
MIPS (Golden Rules:
Uniformity,
Regularity,
Orthogonality)

3° Byte Addressable Machine.

A smallest memory cell with an Unique Address is a Single Byte.

4°

2° 32bit RISC Processor → 32bit

Architecture

32bit Addr. Bus.

32bit Data Bus.

32bit R.F. (Register File)

{ GPRs (General Purpose Registers) 32bits.
SPRs (Special Purpose Registers)

3 Cats.

↓

32bit memory map.

$$2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2$$

1K
(1024)

~

1M

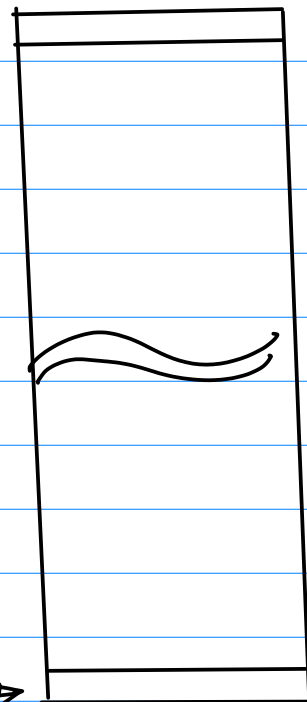
(1K x 1K)

~

1G

4G? Byte!

0xFFFF_FFFF



0x0000_0000 →

Power-up Addr.