CMPE240
Fall 2023

Aug 21 (Monday).
Organizational meeting.

1. github.

https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F

2.

Course and Contact Information

Instructor(s): Harry Li
Office Location: Engineering Building, Room 267A
Telephone: (650) 400-1116
Email: hua.li@sjsu.edu
Office Hours: M.W. 3:00-4:00 pm ← IN Person.
Class Days/Time: Mondays, Wednesdays, 1:30-2:45 pm
Classroom: Engineering Building, Room 331
Prerequisites: CmpE 180D for non CMPE or non EE undergradu
documentation of having satisfied the class prerequisite requireme
dropped from the class.

3. Emphasis on the Advanced Nature of the Microprocessor Systems. → Embedded Nature, ARM CPU. → GPU: graphics Processing Unit

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures, SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter receiver, timers, display adapter, and other system peripherals and bus interfaces.

→ Engine for Deep Learning, AI etc.

4. Hands-ON.

Datasheets. → Spec. → Hardware Prototype Board With Color LCD Display

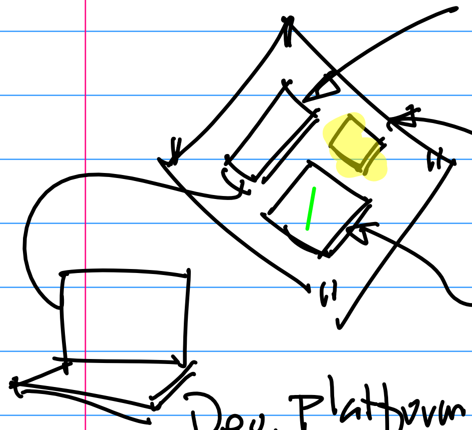
2D Graphics Engine ← Hardware Prototype Board With Color LCD Display

↓

3D Graphics Engine

↓

Benchmarking (with Ref. to NVDA Jetson NANO)



CPU module
NXP LPC1769 or
LPC11C24

I/O Test CKT

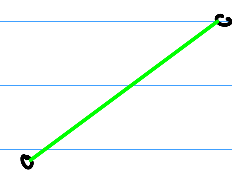
Color LCD Display

Dev. Platform.

Line Drawing Sample Code.

(x_i, y_i) Starting pt.

(x_j, y_j) Ending pt.



(x_j, y_j)

(x_i, y_i)

Action Item (Homework, No Submission)

About 22,800,000 results (0.59 seconds)

NXP Semiconductors
https://www.nxp.com

NXP Semiconductors: Automotive, IoT & Industrial Solutions

NXP is a global semiconductor company creating solutions that enable secure connections for a smarter world.

Results from nxp.com

Note: Homework/Projects are to be ~~posted~~ on CANVAS, with Written Requirements. Those are the material to be Submitted.

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5. PPTs, Lecture Notes (White Board Notes), Datasheet(s), are posted on the github.

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;

- Reference: ARM11 data sheets and on-line web materials on line https://github.com/hualili/ , or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Note: 1° Initial Sample Projects, ~A Dozen Sample Projects.

2018F	Add files via upload
1769 patch.zip	Add files via upload

GPP (General Purpos Port)

Target CPU
NXP LPC11C24
LPC1769

The Code was for LPC1769, But Newer Samples for GPP, Graphics Display for LPC11C24 were developed and posted on the github.

Next Level of the Sample Code

2018S-10-LCD-DrawLi...	Add files via upload

The Lover After Sample code for 2D & 3D Engine Design.

PPT Material in pdf.
will be used in the Class.

Datasheet. Note: 1° CPU Datasheet is in CmpE244 folder

2021F-107-lpc-cpu-UM... 2° CPU Datasheet
2021F-107b-sch-#LPC... "SCH"

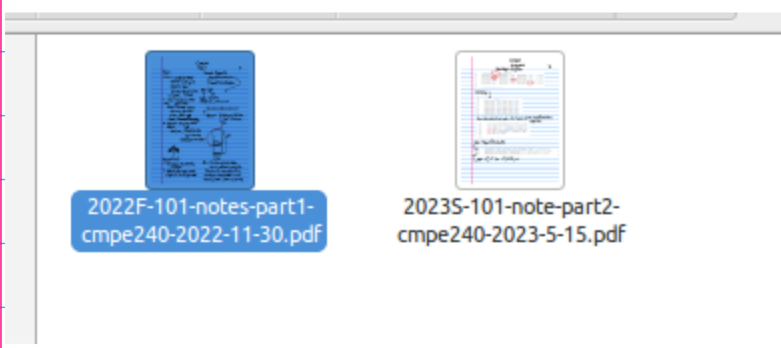
Grading Information

Quiz, Homework, Projects	30%
Midterm Examination	30%
Final Examination	40%

August 23rd (Wed)

Announcement:
1° Lab Space Rm 268
2° CANVAS to Be Up By this week.

Introduction.



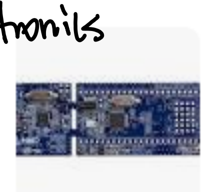
Example: Architecture of LPC1769 (LPC11C24)

Can be purchased from digi-key.com or Mouser electronics

NXP Semiconductors
https://www.nxp.com › general-purpose-mcus › lpc11...

Scalable Entry Level 32-bit Microcontroller (MCU) based ...

The LPC11Cxx MCU family is designed for 8/16-bit micro-controller operations,



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Restore Session | hualili/CMPE240-Adv-Microproce | OM13093UL NXP USA Inc. | Deve

https://www.digikey.com/en/products/detail/nxp-usa-inc/O

DigiKey | All Products | Enter keyword or part #

Product Index > Development Boards, Kits, Programmers > Evaluation Boards > Embedded MCU, DSP Evaluation Boards > NXP USA Inc. OM13093UL

Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

OM13093UL

Digi-Key Part Number	568-14402-ND
Manufacturer	**NXP USA Inc.**
Manufacturer Product Number	OM13093UL
Description	LPCXPRESSO LPC11C24 EVAL BRD
Manufacturer Standard Lead Time	16 Weeks
Detailed Description	LPC11C24 LPCXpresso™ LPC11C00 ARM® Cortex®-M Evaluation Board
Customer Reference	Customer Reference

Note: Please Start the Purchasing Process.
Note: CPU Datasheet.

2018S-3-UM10360 user manu.pdf

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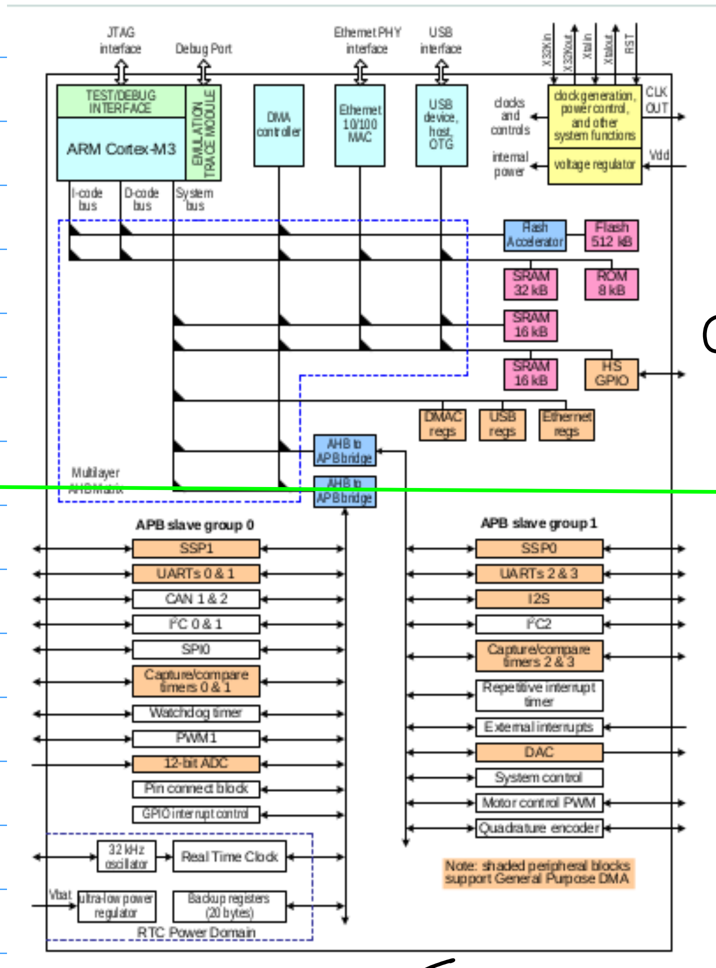


Fig 1.a

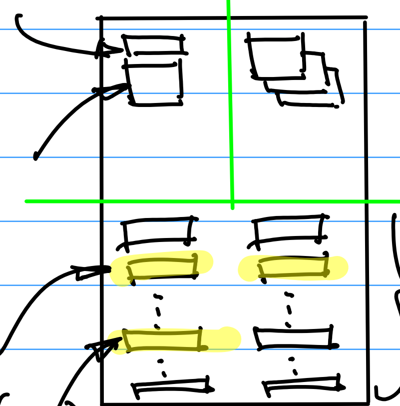
J-tag

Mem. Controller(s), SRAM, ROM, FLASH.

CPU CORE CORTEX M3

GPP

SSP(SPI)



Pheripheral Controllers

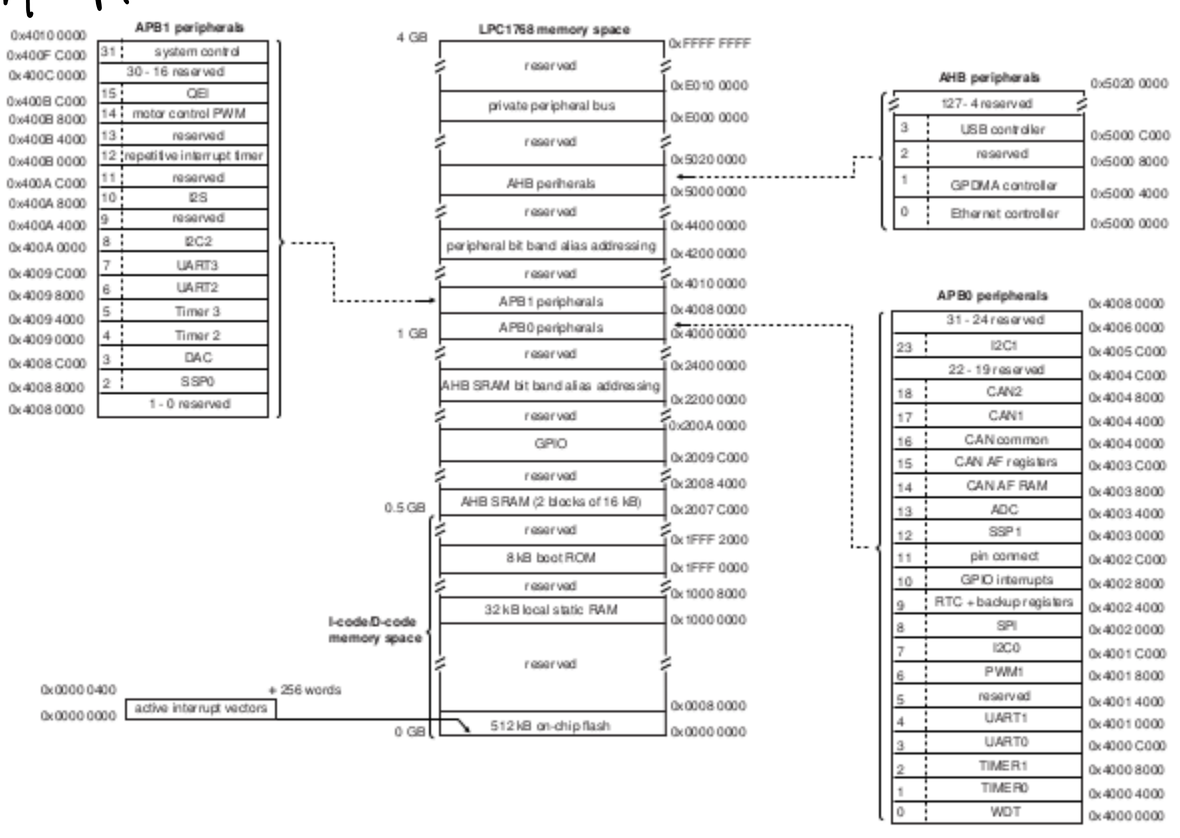
Fig. 1.b.

GPP/GPIO: General Purpose Port
or General Purpose I/O

SPI (Serial Peripheral Interface)

Note: One of the GPPs supports ExINT. (External Interrupt).

Memory Map.



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Note: For the memory map Discussion:

1° RISC: Reduced Instruction Set Computer.

ARM. MIPS (Golden Rules: Uniformity, Regularity, Orthogonality)

2° 32Bit RISC Processor → 32bit Architecture

32bit Addr. Bus.

32bit Data Bus.

32bit R.F. (Register File)

- GPRs (General Purpose Registers) 32bits.
- SPRs (Special Purpose Registers) → 3 Cats.

↓

32bit memory map.

$2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2}$

1K (1024)

1M (1K×1K)

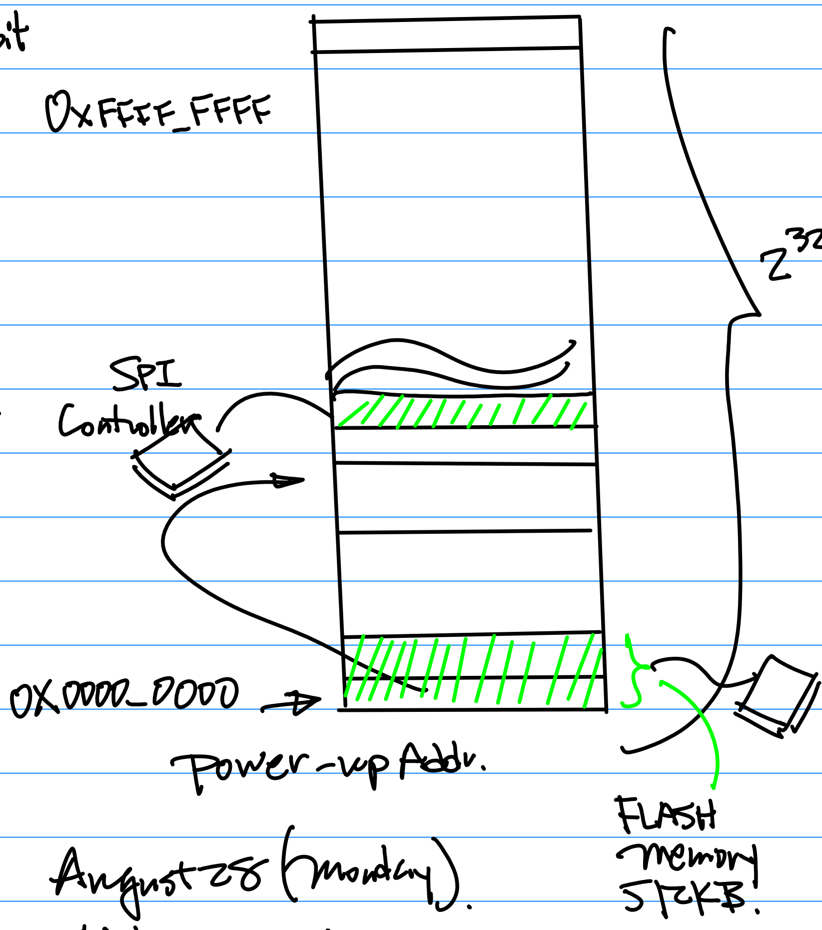
1G

4G? Byte!

3° Byte Addressable Machine.

A smallest memory cell with An Unique Address is a Single Byte.

4°



August 28 (monday).

Note: 1° CANVAS is up.

2° CPU module & LCD module

↑

ST7725 Controller

SPI - Interface

https://www.amazon.com/Display-Module-ST7735-128x160-STM32/dp/B07BFV69DZ

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Note: 8-pins OR 10 pins module are OK for the Implementation

1.8 inch SPI TFT LCD Display Module for ST7735 128x160 51/AVR/STM32/ARM 8/16 bit

Note: ST7725 OR ST7735.

Visit the Walfront Store

4.0 ★★★★☆ 42 ratings

$10.99

With **Amazon Business**, you would have **saved $85.08** in the last year. Create a free account and **save up to 5%** today.

Roll over image to zoom in

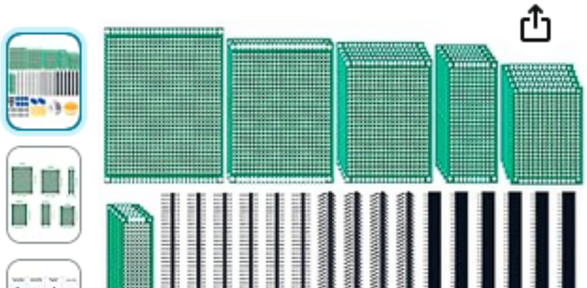
Brand	Walfront
Personal computer design type	All in One
Operating System	Linux

3° Bill of Material (BoM) for this Class:

1°. CPU module
2°. LCD Module
3°. Wire Wrapping Board.

4" x 3" Through-Holes with metal plating (Just to cover the holes, Not the Entire Board)

OR your Choice



Miuzei PCB Board Prototype Kit for Electronic Projects, Circuit Solder Double-Side Board with 40 Pin 2.54 mm Male to Female Headers Connector, 2P&3P Screw

Example: Memory Map.

Divid the mem. map into 8 Equal Banks.

		$a_{31}a_{30}a_{29}$ Starting Addr.		
BANK 0	First	000	0000 : 0000 : ... : 0000	→ 0x0
BANK 1	2nd	001	0010 : ...	→ 0x2000_0000
BANK 2	3rd	010	0100 : ..	→ 0x4000_0000
⋮		⋮		
BANK 7	8th	111		

Note: Important, to Be used in the Design Process.

MSB $\underbrace{a_{31}a_{30}\cdots\quad a_2 a_1 a_0}_{\text{32 bits Addr. Bus}}$ LSB

Note: "Little Endian" Convention

Choose $a_{31}a_{30}a_{29}$ to Identify the memory Bank.

$a_{31}a_{30}a_{29}0 : 0000 : \cdots : 0000$ Lowest Addr.

$a_{31}a_{30}a_{29}1 : 1111 : \cdots : 1111$ Highest Addr.

$$2^{32}/2^3 = 2^{29} = \underset{512}{2^9}\cdot\underset{1\,\text{Meg.}}{2^{20}}$$

Example: Identify One of the SPI Peripheral Controllers By mem. map.

Memory Bank with a Starting Addr.

0x4000_0000 → 3rd Bank (Bank 0, Bank 1, Bank 2)

Find A SPI Block

9	RTC + backup registers	0x4002 4000
8	SPI	0x4002 0000
7	I2C0	0x4001 C000

SPI Peripheral Controller is Located at 0x4002_0000

Question: How Big is the memory Block for SPI Controller?

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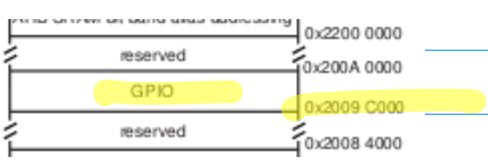
0x4002_4000
− 0x4002_0000
0x4000

MSB 0100 0000 0000 0000 LSB

$2^x = 1 \cdot 2^{14} = 1 \cdot 2^4 \cdot 2^{10}$
16 . K

Note: This Block of memory is employed for A set of SPR's (Special Purpose Registers) to perform SPI function.

Example: GPP (General Purpose Port)



GPP (Peripheral Controller)

↓

mem. map Location & its Block Size

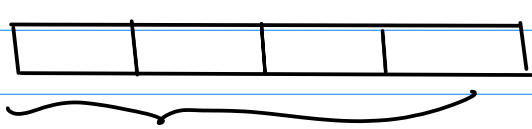
↓

SPRs (Special Purpose Registers)

Responsible for Init & Config.

↓

Control Register.



32 bit SPR.

Naming Convention "3+3" for All if Possible

Prefix 3 Letters + Root 3 Letters

August 30 (Wed)

Note: 1° CANVAS has been updated with Homework One ON Friday, Opt. Honesty Pledge Signed Form to Be Submitted ON CANVAS.

2° Bill of Material.

Ref: ON the github of CMPE240 2018S-2- ... Bill_of_Material

3° Homework (0 pt) Due Sept. 10 (Sun) Installation of NXP MCU Expresso.

Submission: Screen Capture that Shows the MCU Expresso + Personal Identifier.

Ref: github → PPT for MCUXpresso Configuration.
NXP Developer Forum, pdf

Note:

gcc/g++ Compiler Open Source → Porting to the Target CPU, NXP → Porting to the target Board

ARM CPU Core LPC family Cortex M3

4° Please bring the CPU module to the class for inspection & Discussion.

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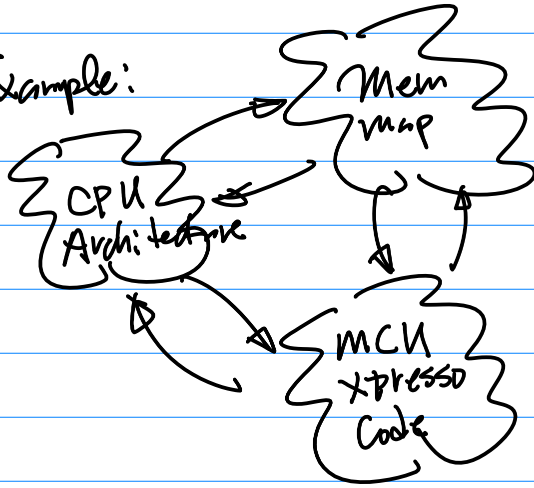
Example:



Design of GPP

GPx CON

Prefix   Root

x: Allow the user to Define which port.

Note: Multiple I/O pins possible for Each GPx

GPACON

0x uuuu-uuuu

0x2009_C000

32 bit S.P.R.

GPA Port Pin 5 as an Output pin → Need to Identify the Bit(s) in GPACON for the selection Purpose.

Sept. 6 (Wed)

Example: Inspection of LPC11C24 OR LPC1769.

Purpose: Identify Pin 1 ON the module. Match it up to SCH of the Board module.

Ref: On the github LPC11C24 AND LPC1769.

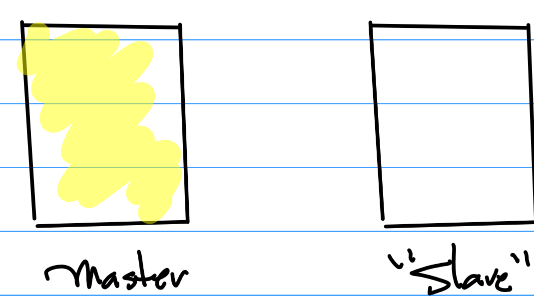
Note: 1° Physical pin assignment, e.g. pin 1, pin 2, ..., etc.

2° Namings of the pins
- a. Connector Related
- b. CPU Datasheet Related (C/C++ IDE, Code)
- c. Functionality Related.

→ Use All of the above in your Connectivity Table

3° Power Pins
- a. VIN, Vout pins
- b. GND pins → Common GND

4° SPI (Serial Peripheral Interface).



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"3+1" Pins
- MOSI (Master Out/Slave In)
- MISO (" In/ " Out)
- SCK (Serial CLK)

} "3"

- EN/nEN Enable Active high or Active Low.

J6 or J2, 40 pins Connector.

Header Connector → male

Connector Header Through Hole 16 position 0.100" (2.54mm)

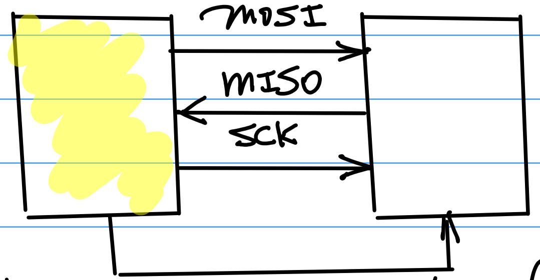


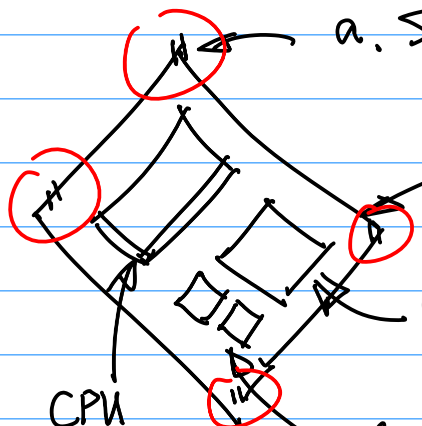
Fig.1.

Soldering the top Left Corner pins (2~3 pins) And the Bottom pin(s) (1~2 pins).

~~c. Soldering the LCD module.~~

Sept. 11 (Monday).

Note: 1° Bring your Prototype Board with the CPU Mounted On the Board.



b. "Mount" → Solder the CPU pins

Example: SPR for SSP0.

Ref: github/hualili/Cmpe244 ~ 2021F-107 or

PP431. a. 32bit SPR.
b. Name: SSP0CR0

for the peripheral controller 0. (multiple controllers)

Prefix + Root

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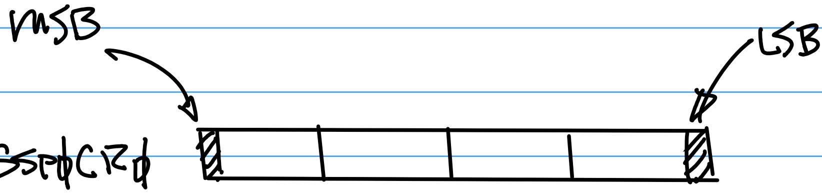
SSP0CR0

0x4008_8000



DSS

SSP0CR0[3:0] = 0111 for 8 bits Transfe

SSP0CR0[5:4] = 00 for S.P.I.

SSP0CR0[6] = 0, SSP0CR0[7] = 0 By default

SSP0CR0[15:8], SCR. Serial clock Rate

CR0 ← 8 bit → 2^8 = 256 → [0, 255]

SysCLK (System Clock) CPU Clock. ← Range to work with to define Serial clock. SCK.

↓

PCLK (peripheral clock)

1/2, 1/4, 1/8, ...

↓

SCR Controls S.P.I. Clock.

$$f_{SPI} = \frac{PCLK}{CPSDVSR * (SCR+1)} \quad \cdots (1)$$

CPSDVSR: from a SPR [2, 255] ? 254

(SCR+1): [0, 255]

Sept. 13 (Wed)

Note 1, Inspection of the prototype Board (Work-In-Progress)

Homework, Due 1 week from Today, Sept. 20 (11:59 PM)

a) ~~Build~~ / mount CPU module and SPI LCD Display module ON the prototype Board, Solder them on the Board.

b) Take a photo of your Prototype System, and Submit the photo with Caption on it, with your SID, Name. Submission on CANVAS.

Bring your Prototype Board to the class.

Example: Suppose we define

① PCLK = 20 MHz;

② f_{SPI} = 5 KHz (e.g. → 5 Kbps)

③ Design By Assigning SCR to Realize the Bit Rate Requirement.

Sol: From Eqn (1), pp 431.

$$f_{SPI} = \frac{PCLK}{CPSDVSR * (SCR+1)} \quad \ldots(1)$$

from the given Condition, we have

$$5\times10^{3} = \frac{20\times10^{6}}{CPSDVSR * (SCR+1)}$$

Design By Iteration.

First, Let CPSDVSR = 4
solve for SCR

$$CPSDVSR * (SCR+1)\Big|_{CPSDVSR=4} = \frac{\cancel{20}^{4}\times\cancel{10^6}^{10^3}}{\cancel{5}\times\cancel{10^3}}$$

$$SCR+1 = 4\times10^3/4$$

$$SCR = 1\times10^3 - 1 = 999 > 255$$

So, the Next Iteration of the Design

Let CPSDVSR = 32
from Eqn (1), we have

$$CPSDVSR * (SCR+1)\Big|_{CPSDVSR=32} = 4\times10^3$$

$$SCR+1 = 4\times10^3/32, \quad SCR = \frac{4\times10^3}{32} - 1 = 124 < 255$$

Hence, Our Design provides the following Value for the Required f_{SPI}.

CPSDVSR = 32 and
SCR = 124

↓

124 in Binary format.

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C-Code / MCU Xpresso.

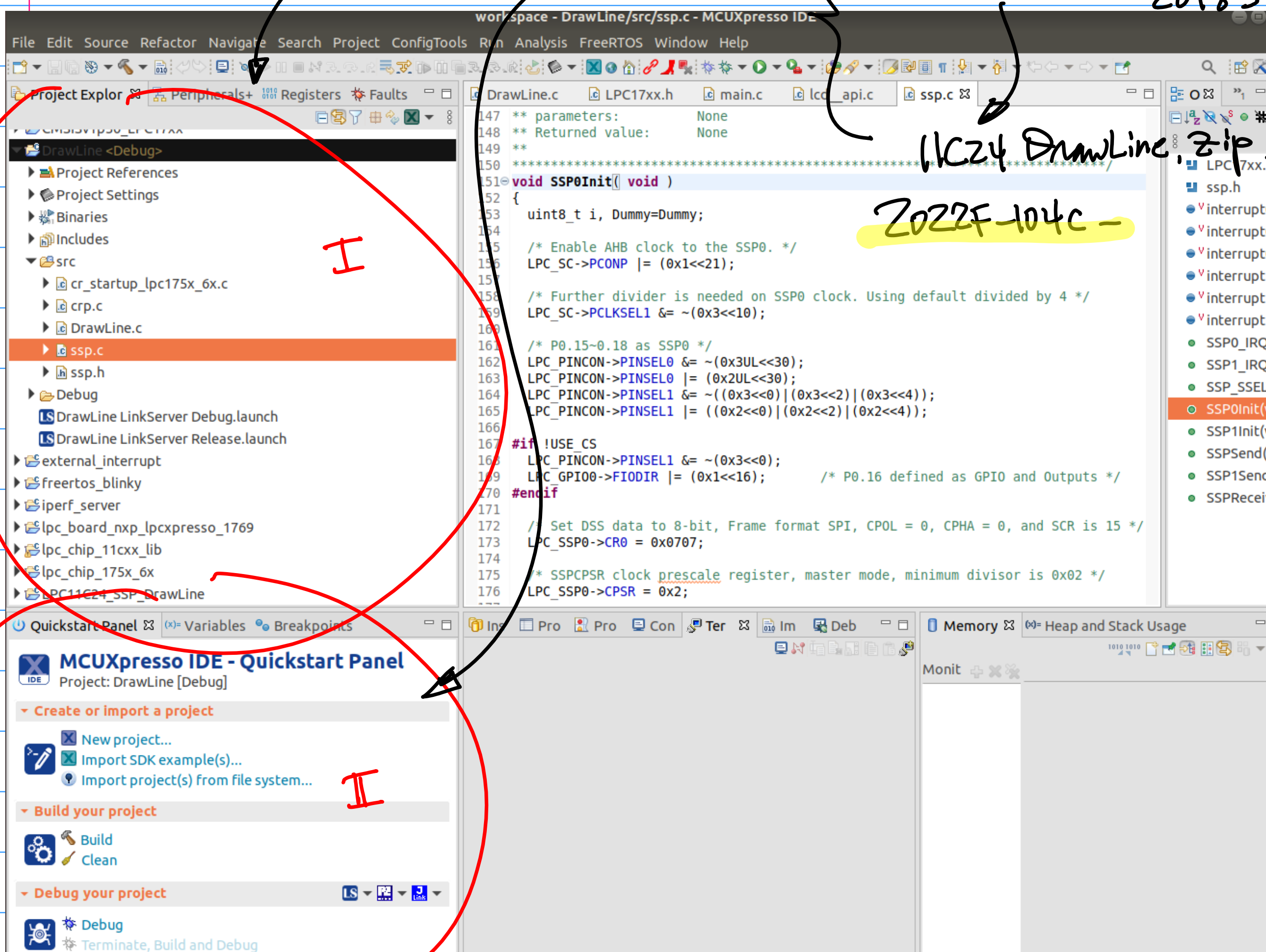
Note 1. Projects Imported into the MCUXpresso. (see I)

Note 2: Import 1769.zip (from the Class git) By using II. (GPIO project as Ref.)

Note 3: DrawLine.zip. 2018S-10-…

11C24 DrawLine.zip.

2022F-104c-



Step 1. Config the MCU Xpresso.

CPU
Board

Ref: Class PPT OR NXP

→ Step 2 Import LPC1769. patch. "zip".

→ Step 3. Import DrawLine Project (1769)

→ Step 4 Import DrawLine Project (11C24)

(x_{i+1}, y_{i+1})

(x_i, y_i)

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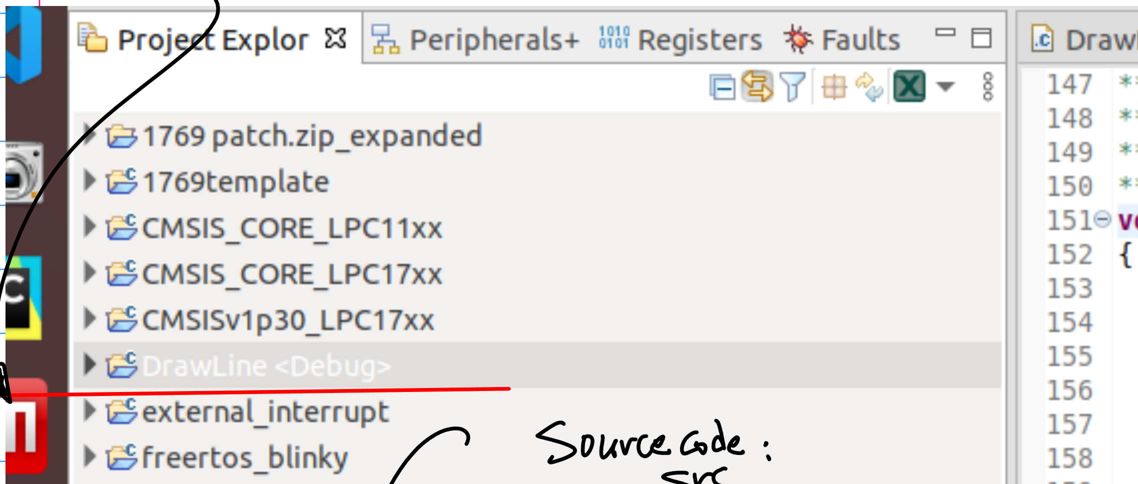
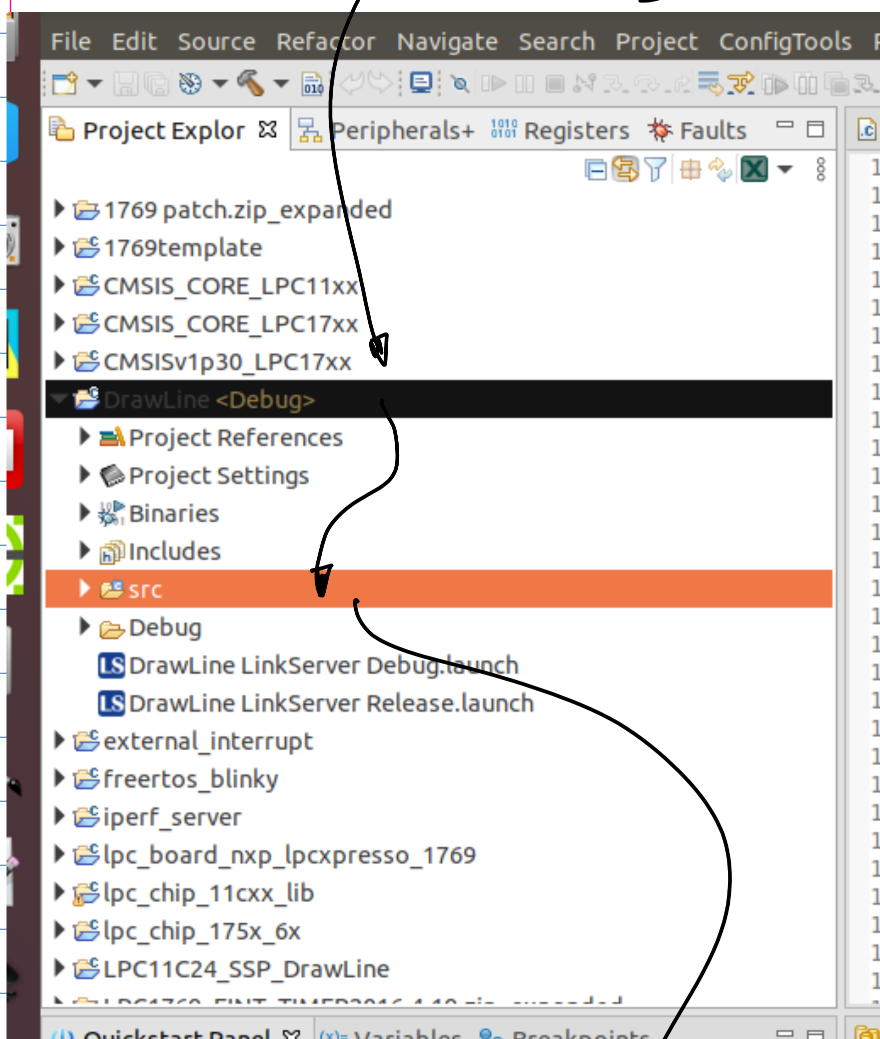
Note4. Sample Project for 1769. A Starting Point.



Source Code: src



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This is from SSP.C

Note: please Read this code!

```
** Returned value:      None
**
*****************************************************************************/
void SSP0Init( void )
{
  uint8_t i, Dummy=Dummy;

  /* Enable AHB clock to the SSP0. */
  LPC_SC->PCONP |= (0x1<<21);

  /* Further divider is needed on SSP0 clock. Using default divided by 4 */
  LPC_SC->PCLKSEL1 &= ~(0x3<<10);

  /* P0.15~0.18 as SSP0 */
  LPC_PINCON->PINSEL0 &= ~(0x3UL<<30);
  LPC_PINCON->PINSEL0 |= (0x2UL<<30);
  LPC_PINCON->PINSEL1 &= ~((0x3<<0)|(0x3<<2)|(0x3<<4));
  LPC_PINCON->PINSEL1 |= ((0x2<<0)|(0x2<<2)|(0x2<<4));

#if !USE_CS
  LPC_PINCON->PINSEL1 &= ~(0x3<<0);
  LPC_GPIO0->FIODIR |= (0x1<<16);     /* P0.16 defined as GPIO and Outputs */
#endif

  /* Set DSS data to 8-bit, Frame format SPI, CPOL = 0, CPHA = 0, and SCR is 15 */
  LPC_SSP0->CR0 = 0x0707;

  /* SSPCPSR clock prescale register, master mode, minimum divisor is 0x02 */
  LPC_SSP0->CPSR = 0x2;
```

SPI. Init & Config

Note: Naming: (Product Family) + (Peripheral Controller) + (SPR)

Note: Code ⇄ Tech. Spec.

0x0707

0000 0111 0000 0111 → Datasheet.

Sept. 18 (Monday).

Please Check CANVAS for the Homework (Prototype Board).

Example: LCD Display Pin Connectivity.

Ref: github/hualili/Cmpe240/2022f-103f_~

Fig. 1

LPC11C24 Connectivity Table t

HL (2022-9-30) corrected this typo by replacing LPC 1769 to LPC11C24

Table 5. Connectivity Table of LPC11C24 and LCD

LPC11C24	Description	LCD
1. J6-28	3VOUT	VCC
2. J6-1	GND	GND
3. J6-8	SSEL0	TFT_CS
4. J6-14	RST	RESET
5. J6-13	D/C	A0
6. J6-5	MOSI0	SDA
7. J6-7	SCK0	SCK
8. J6-28	3VOUT	LED

Brand

Personal computer design type — All in One

Operating System — Linux

a) 8 bit mode

b) SPI Interface

c) Clock Setting is default.

d) SCR (Eqn.-1)

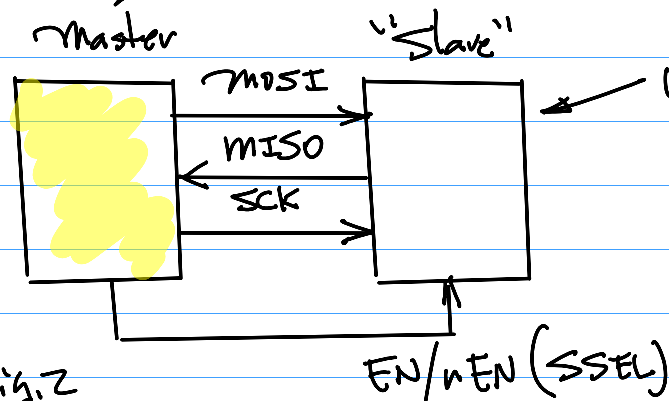
$$f_{SPI} = \frac{PCLK}{DVSR(SCR+1)}$$

SCR=7.

find f_{SPI}, Hz

Note: Toggle Between the Commands and Data

LPC11C24 OR LPC1769 (Different Connection!)



LCD Display module.

Fig.2

Note: One Clock Corresponds to ONE Bit.

Example: BitRate Calculation.

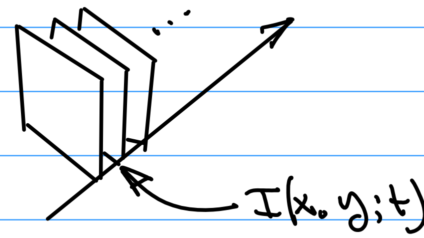


Fig.4

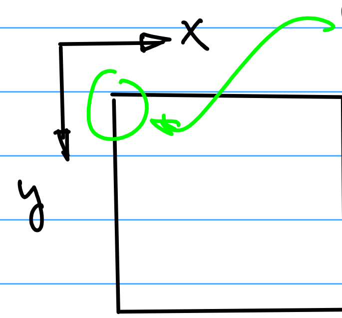
From pp.12

Note: use this table as a reference Build a Complete Connectivity table.

a) CPU pins; b) Connector pins; c) Function Name (MOSI, etc).

Given Graphics Display Resolution M×N.

physical coordinate (0,0)



Example: Continuation ON ssp0init( ) (line151).

Note: SPI Data Communication. Waveform Captured By Logic Analyer. from MOSI pin.

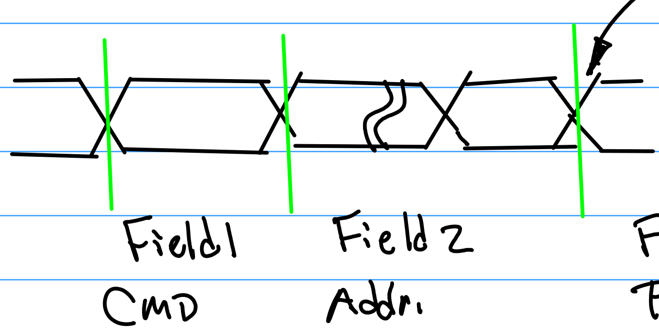
M×N

Col. Row

No. of Pixels Per Row. No. of Rows.

Fig.3

Timing Info.



Assuming the Resolution of the LCD is M×N (160×120)

Frame Rate (FPS) 30

Find the Bit Rate for SPI Interface.

$$\underbrace{160 \times 120}_{\text{Total No. of the pixels per frame}} \times \underbrace{24}_{\text{Bit/pixel}} \times \underbrace{30}_{\text{FPS}} = \begin{pmatrix} \text{1 Second} \\ \text{Total Bits} \end{pmatrix}$$

pixel Depth.

$$2^x$$

$$160 \times 120 \times 24 \times 30$$

$$2^7 \quad 2^7 \quad 2^5 \quad 2^5 = 2^{14} \cdot 2^{10} = \underbrace{2^4}_{16} \cdot \underbrace{2^{10} \cdot 2^{10}}_{1\text{K}\ \cdot\ 1\text{K} \ =\ 1\text{ Meg}} =$$

160

$2^7 = 128$ $\qquad$ $2^8 = 256$

∴ 16Mbps

Therefore, the S.P.I. Bit Rate is adequate.