CMPE240 Spring 22

1/

Left Column
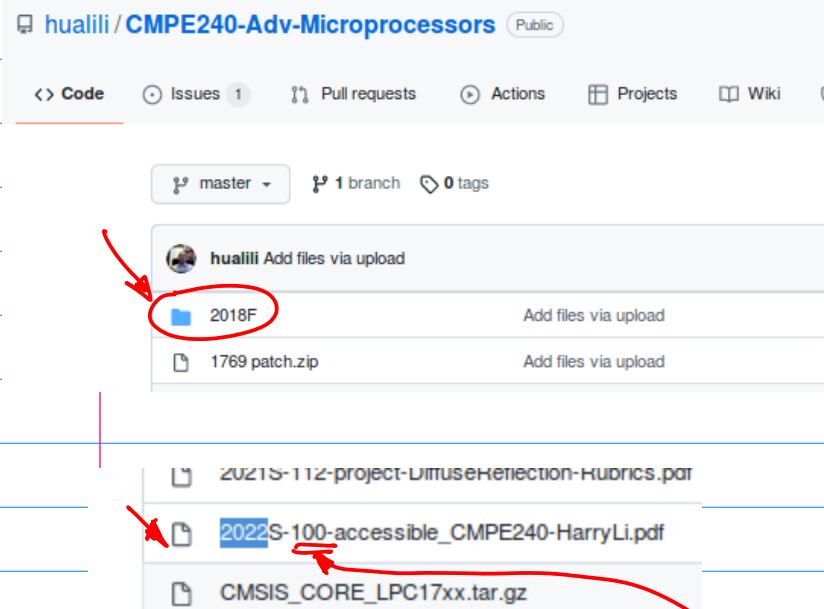
Jan 26 (Wed)

Today's Topics: Introduction & Organizational meeting.

Harry Li, Ph.D.

Green Sheet : On-Line from github

https://github.com/hualili/CMPE240-Adv-Microprocessors

Naming Convention : Yr + Semester + ID + Name of the Doc.

E-mail : hua.li@sjsu.edu

Text message : (650) 400-1116

Office Hours : Mondays & Wednesdays 4:30 - 5:30 PM.

Office hours Zoom link: Join Zoom Meeting
https://us04web.zoom.us/j/9841607683?
pwd=UlA3aEk1TnV4bjNLQk5CQkw0dDk4UT09
Meeting ID: 984 160 7683 Passcode:
121092

Right Column

TextBooks + Ref

1. No text Book, But NXP CPU Datasheet is utilized as a Base Line Ref

2. SCH Design of the CPU module. PP5 (Rev.D.)

Prototype Board : Each Person will Build his/her Prototype System.

Team work is encouraged, form 4 people team for this Class. However all the work has to be done individually.

Grading : midterm 30%
Format : Written Exam But Need to have prototype ready to Execute Programs, And get photos of your Prototype Board.

Final Exam : 40%, Similar format as the midterm.

Homework, Projects Counts Another 30%.

Written Announcement on White Board (Lecture Notes) And SJSU CANVAS.

Late Project submission will have 1 pt. Penalty Per each Lecture Day.

Introduction.

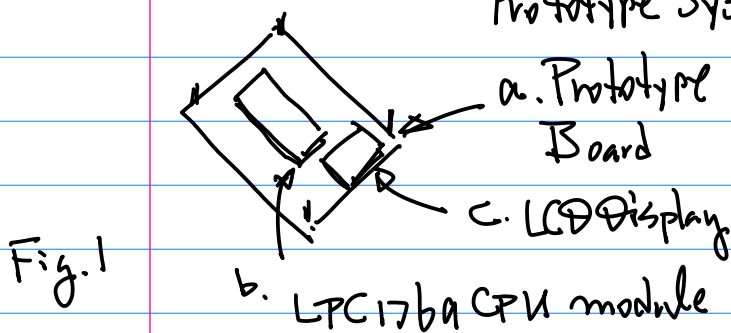1. Bill of material for LPC17b9 Prototype Board Design.

Jan 31 (Monday)

Today's Topic: Introduction.

Prototype System.

Task: 1. Form 4 Person Team

Work Together throughout the

entire Semester. By this Wednesday.

Prototype System.

a. Prototype Board

c. LCD Display

b. LPC1769 CPU module

Fig. 1

Prototype Board

mounting holes at the Corners.

Stand-offs: (Legs) for the Board.

Fig. 2 CPU

Digi-Key, or Mouser Electronics

CPU: Cortex M3

Note: a. Adequate Size

Not Too big, to host LPC1769

module & LCD Display module,

Plus "Glue" Logic.

"Glue Logic" GPIO Circuit as

a Part of the "Glue"

Ethernet Connector, RJ45,

in the future for Possible

networking Applications,

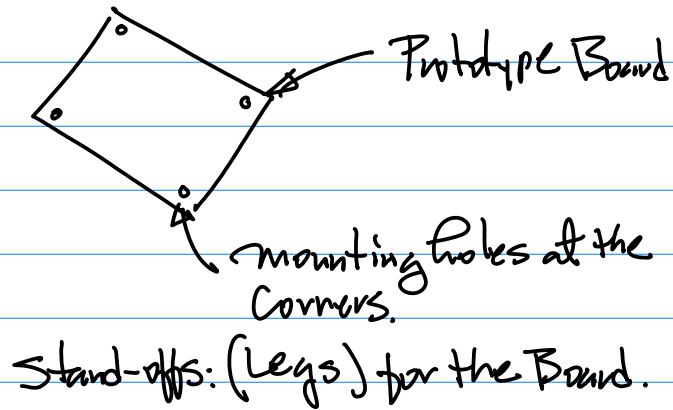TCP/IP, Micro-Web Sewer.

4" x 3" Or Similar Size.

16 cm x 11½ cm.

c. LCD Display module

SPI (Serial Peripheral Interface)

Software Driven function(s) are

Provided / Accessible

- LPC 1769
- Color TFT LCD display
  Resolution : 128x160,
  Pixel Depth: 18-bit (262,144) colors
  Controller: ST7735
  Interface: SPI interface

LCD Pins	LPC1769 Pins

From the class github

LCD module

2021F-113-LCD-TFT (ThinFilmTransistor).jpg

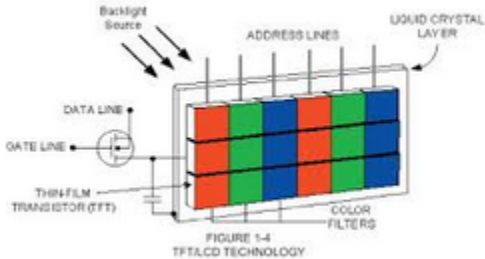2021F-114-display-NEC-3P5-LCD-68775.pdf

Fig3

FIGURE 1-4
TFT/LCD TECHNOLOGY

Components for:
Power Unit Design Need
GPIO (General Purpose I/o)

LPC1769 is powered with 2
options.

Option 1: USB Cable Connection
to Provide Power from
the host (PC) to LPC
1769 CPU module.

for Debugging/Testing Purpose
But not for Deployment

Option 2: External Power to
the prototype System. To Allow
you Deployment of the Prototype
System. → Mandatory, By

the Last project, each prototype
will have to deployed with External
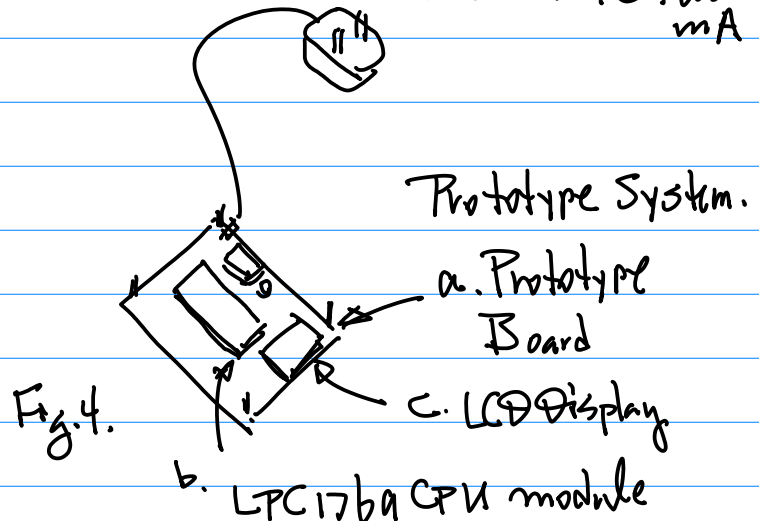Power.

7.5V ~ 9V DC @
1500 mA ~ 4000
mA

Prototype System.
a. Prototype
Board
c. LCD Display
b. LPC1769 CPU module

Fig.4.

Build Option 2 Power Unit Circuit
is required Now, Before the first
Project.

Components for the Power Unit

① Wall-mount Adaptor.
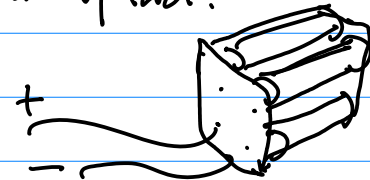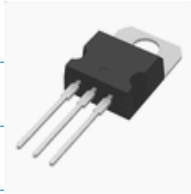Spec. 7.5 ~ 9V DC
1500 mA ~ 4000 mA.

Or Battery Pack.

+

—

Fig.5

② Red LED indicator. to Show Power
is on/off.
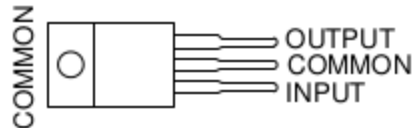$V_{LED} \approx 1.2$ VDC ; 8 ~ 10 mA

③ Power Regulator IC 7805, or
1117.

Fig 6

- 3-Terminal Regulators
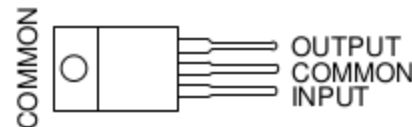- Output Current up to 1.5 A
- Internal Thermal-Overload Protection

KC (TO-220) PACKAGE
(TOP VIEW)

COMMON — OUTPUT COMMON INPUT

KCS (TO-220) PACKAGE
(TOP VIEW)

COMMON — OUTPUT COMMON INPUT

STMicroelectr
L7805CV ...
$0.63
Digi-Key

Fig. 9.

Lecture Notes is 2022S-101
in the class github.

📄 2022S-100-accessible_CMPE240-HarryLi.pdf

📄 2022S-101-Notes-2022-01-26.pdf

Note: 78xx family
7812, 7805 etc.

µA7800 SERIES
POSITIVE-VOLTAGE REGULATORS

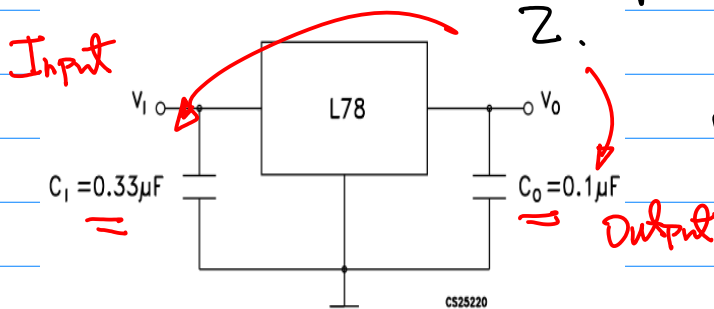SLVS056J – MAY 1976 – REVISED MAY 2003

④ Right Angle (plug) connector

Kobiconn
151-7620E-E DC
$1.14
Mouser Electronics

Fig. 7

⑤ Assorted Resistors (A few hundred
ohms to a few Mega Ohms).

⑥ Compensating Caps.

Figure 5. Application circuits

Input

V_I ○ ——— L78 ——— ○ V_O

$C_I = 0.33 \mu F$ $C_O = 0.1 \mu F$

CS25220

Note for STmicro
the Caps Required are
2.

Fig. 8

Components for GPIO
Use GPI "Hello, the wor ld"
for Debugging { Input { "0"s
                              "1"s
              Output { "0"s
                       "1"s

Feb 2nd (Wed)
Today's Topics:
1° Bill of Material
2° CPU Datasheet, Architecture

Options for the target platform.
(LPC1769)

a. NVDA (Nvidia) Jetson NAND
Caution: Device Driver Programming
in O.S. Kernel Space.
5% Bonus. Implementation at
Registers/Hardware Level, LCD

LCD has to the Same SPI I/F for NAND & LPC1769.

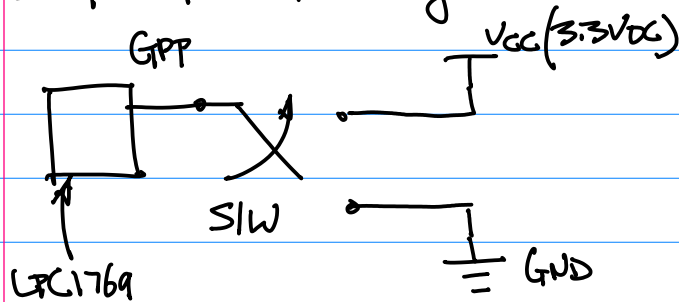GPP IIO Output Testing.

Example: GPIO I/O Testing Circuit

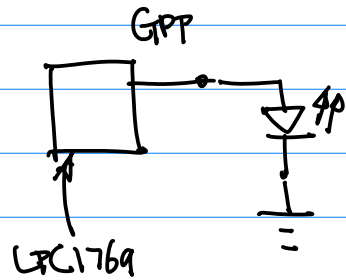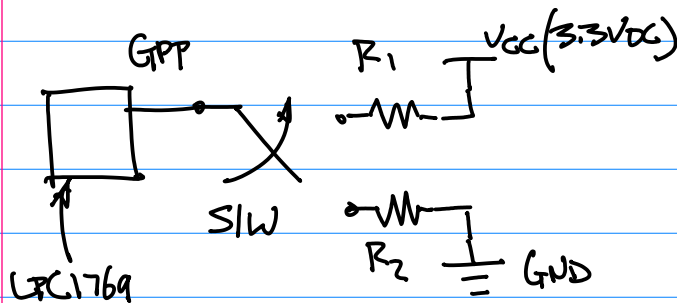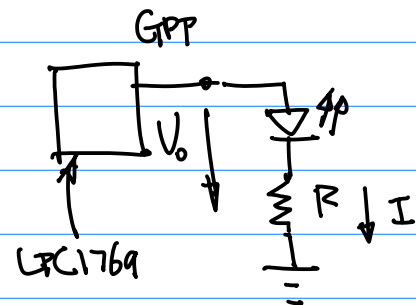Fig.1.

GPP: General Purpose Port, Same as GPIO.

Fig.2

Calculation of the Resistor

$$V_0 = V_{LED} + IR \qquad \cdots (1)$$

$V_{LED} \simeq 1.2V$, $I = 10mA$, $V_0 = 3.3V$ (CMOS)

Substitute the above conditions into Eqn(1),

$$3.3 = 1.2 + R \times 10 \times 10^{-3}$$

$$R = \frac{2.1}{10^{-2}} = 2.1 \times 10^2 = 210 \, \Omega$$

Better Design.   Fig1b.

Consider Resistor Value Calculation

$V_{cc} = 3.3VDC$, $V_{out} = 3.3VDC$ (GPP)

Select Resistor Value to Regulate the Amount of Current ~10mA

Hence, $R_{1,2} = \frac{V_{cc}}{10mA} = \frac{3.3}{10 \times 10^{-3}}$

$$= 3.3 \times 10^2 \, \Omega.$$

Note: please use right size of the protatype wire 26 ~ 30 AWG.

Note: Optional — Right Angle

RJ-45 Connector. (8 pos)
(Female)

Modular Jack
8P8C PCB ...
$0.69
PEconnecto...

1.
Exercise: Bring your Prototype Board
together w/ LPC1769 CPU
module to the next Class.
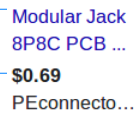
2. Form 4-Person Team, have
a Coordinator, And reprt your
team formation By next Class.

Example: LPC1769 CPU module Schematics

📄 LPCXpresso1769_CD_revD(1).pdf

a. CPU
module and
Schematics
in b.
C. LPC1768
mbed.
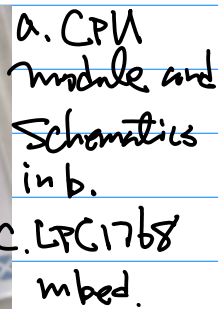
b.

The inner tables
are for 1769.
"I/o Rich"

c.

CMSIS-DAP side

Expansion Connector
(superset of mbed pinning)
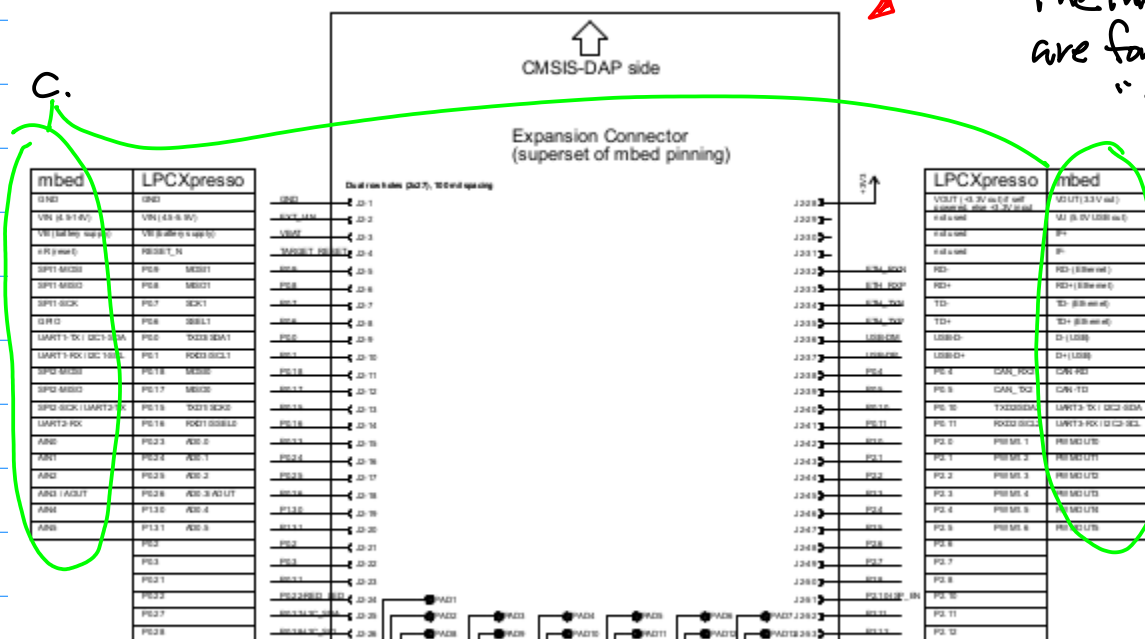
Exercise: How many GPIO pins?
(for LPC1769 module)

Example: Power Input to LPC1769

LPCXpresso	
GND	
VIN (4.5-5.5V)	
VB (battery supply)	
RESET_N	
P0.9	MOSI1
P0.8	MISO1
P0.7	SCK1

Dual row holes

GND	J2-1
EXT_VIN	J2-2
VBAT	J2-3
TARGET_RESET	J2-4 → Reset
P0.9	J2-5
P0.8	J2-6
P0.7	J2-7
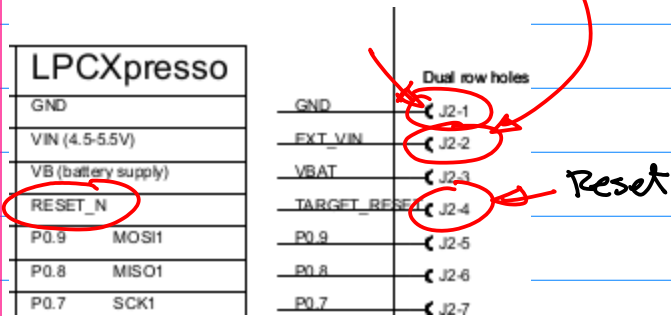
Note: Enumeration of the Connector
Pins → the first pin is
marked as "1".

Note: Physical mapping of the pin
to Actual module;

Note: Reset pin —— provide
Access to this pin in your
Prototype design.

CPU Datasheet from github/~Cmpe244

📄 2021F-107-lpc-cpu-UM10360.pdf