

CMPE240
Spring 2023

v/

Jan 25, 23.

Today's Topics:

1° Syllabus, "Greensheet" of the Class.

San José State University
College of Engineering/Computer Engineering
Department
CMPE240 Advanced Microcomputer Design

S2023

Professor Hua Harry Li
Engineering Building, Rm 267A
Phone: (650) 400-1116 for Text Message Only
Email hua.li@sjsu.edu

Class Time: Mondays and Wednesdays 1:30-2:45 PM

Office Hours: Mondays and Wednesdays 4:30 – 5:30 PM Zoom

Zoom link: Join Zoom Meeting [https://us04web.zoom.us/j/9841607683?](https://us04web.zoom.us/j/9841607683?pwd=UIA3aEkITnV4bjNLQk5CQkw0dDk4UT09)

pwd=UIA3aEkITnV4bjNLQk5CQkw0dDk4UT09 Meeting ID: 984 160 7683 Passcode: 121092

Lecture Room: Engineering Building Room 303

Lab facility: Engineering Building Room 268

Prerequisites

5° Good Throughout the entire School Session.
But it will expire by the Last Day of the
Class. (May 15th).

Note: 1° Attendance; 2° Bring your Laptop Computer; 3° Prototype Board in Class Use/Inspection.

Prototype System { Board A: CPU module.

Board B:
For Graphics Display

4° Board A: CPU NXP LPC11C24 to Replace LPC1769 (Near the End of Its Life, By 2024)

6° Lab Access Code / Policy for the Lab Usage.

Engineering Building Room 268

Prerequisites

CmpE 180D for non CMPE or non EE undergraduate major. Students who do not provide documentation of satisfied the class prerequisite requirements by the second class meeting will be dropped from the class.

Faculty Web Page and MYSJSU Messaging (Optional)

Copies of the course materials such as the syllabus, major assignment handouts, etc. can be found from github <https://github.com/hualili/CMPE240-Adv-Microprocessors/tree/master/2018F> and on SJSU CANVAS.

Note: Homeworks / Projects Announcement will be posted on CANVAS. Submission on CANVAS only.

Course Description

Architecture of a computing system including system bus, memory subsystems and peripherals. Uni-directional and bidirectional bus architectures, SRAM and FLASH memories and their interfaces with the system bus. Design of Graphics Processing Engines, interrupt controller, transmitter, timers, display adapter, and other system peripherals and bus interfaces.

Required Texts/Readings

Textbook

- NXP LPC17xx datasheets;
- LPC1768/1769 CPU Module schematics;
- Dave Jaggar, ARM Architectural Reference Manual, Prentice Hall, ISBN 0-13-736299-4;
- Reference: ARM11 data sheets and on-line web materials on line <https://github.com/hualili/>, or at the SJSU CANVAS provided copyright permitted;
- (Optional) Nvidia Jetson NANO datasheet and user menu (online from Nvidia developer website);
- (Optional) RISC-V tutorial (the link to be given in the lecture) and FPGA verilog implementation guide (the link to be given in the lecture).

Note: Find the Datasheet on the Class github. CMPE244

Other Readings

- The reference material for ARM CPU hardware features, application notes, class handouts and lab assignments and reports, please see Professor Li's lecture notes, PPT, sample C code etc on line <https://github.com/hualili/CMPE240-Adv-Microprocessors> ;
- Professor Li's book materials, ARM Microprocessor Systems (in preparation for publication) <https://github.com/hualili/CMPE240-Adv-Microprocessors>

Other equipment / material requirements

32Bit RISC Prototype/Development Board.

Ref:

1º CPU Datasheets

2021F-107-lpc-cpu-UM... Add files vi

2º "SCH" Design.

2021F-107b-sch-LPC... Add file

3º Lecture Notes

2022F-101-notes-cmpe240-2022-11-30.pdf

deadlines and penalties for adding and dropping classes

Homework/Projects

Assignments and Grading Policy

Laboratory	30%
Midterm Examination	30%
Final	40%

0 to 59 F
60 to 69 D
70 to 79 C
80 to 89 B
90 to 100 A

Option 1. Target CPU Module Board

NXP LPC 11C24 ARM CPU Module (recommended as this course), NXP LPC1769 ARM CPU Mc

Jan 29 (Monday).

1. Check the CANVAS for Homework, Honesty Pledge

2. Target platform.

Background: X86, MIPS, ARM.
CISC RISC
RISC-V

NXP LPC Family.

LPC1769 — End of Life
By 2024.

LPC1768 — mbed

LPC11C24

Option 1: Jetson NAND Zglo.

Option 2: RISC-V FPGA Board

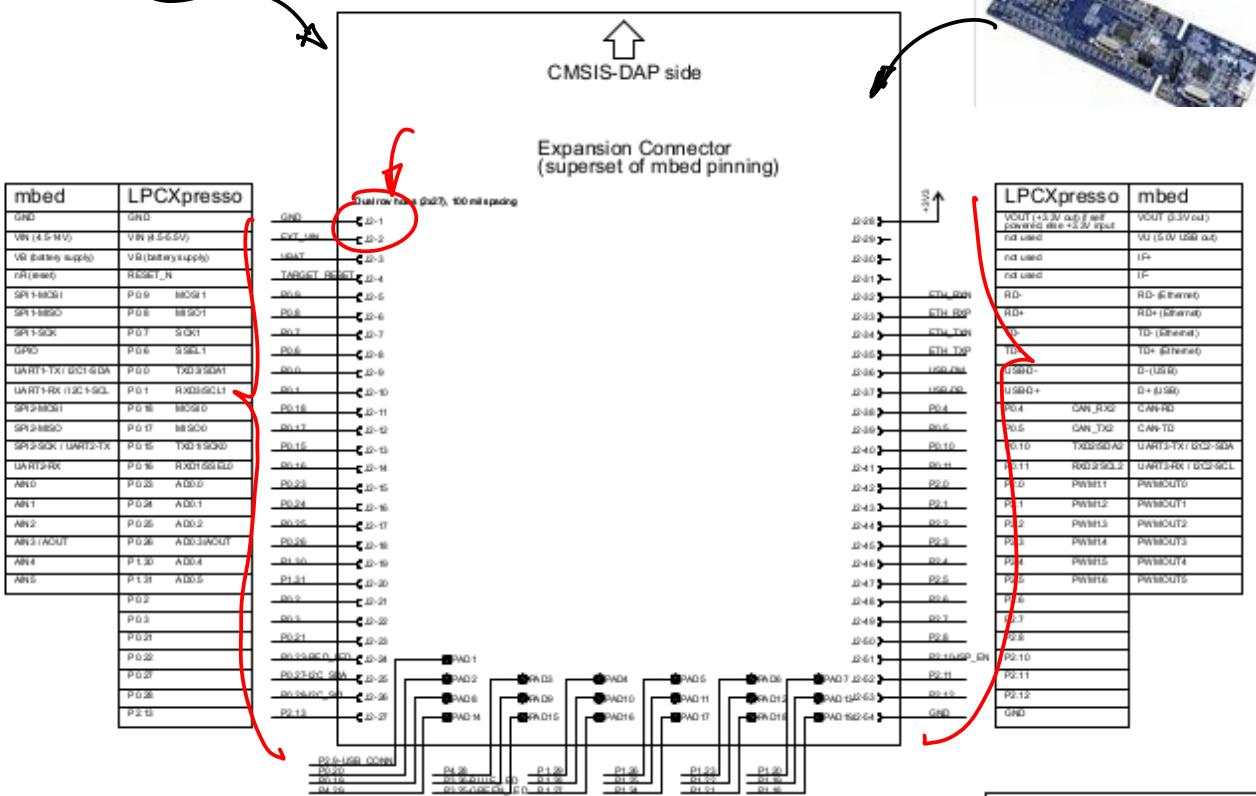
BOM (Bill of Material) on github.

Anchor Electronics.

Example: SCH for LPC1768

Note: CPU module, see Fig.1, its Two Connectors match the Pins in the Schematic

Fig.1



Homework: Due A week from today.

1. Download NXP MCUXpresso,
2. Install MCUXpresso;
3. Start MCUXpresso, then Screen Capture of your MCUXpresso Start Page, make sure it has your Personal identifier on it.

Feb 1st (Wed)

- 1^o Attendance Sheet
- 2^o Ref. from the Class github.

2023-S-102-MCUXpresso_IDE_Installation...

3^o LPC module to be finalized today by the Class. Purchasing CPL module by the end of the day today.

functions. → Init & Config.

More than one port.

2. Connection to GRU Datasheet.

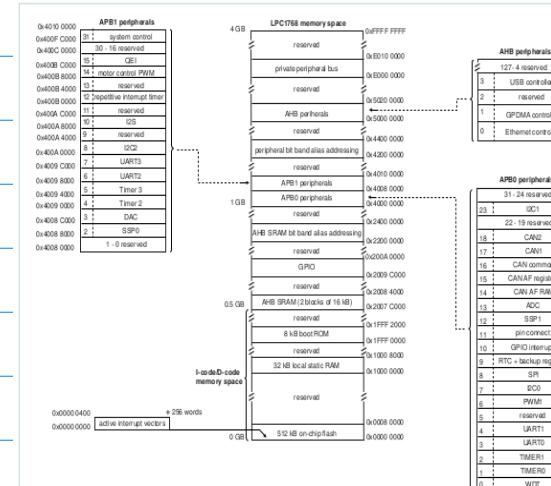


UM10360

LPC176x/5x User manual
Rev. 3.1 — 2 April 2014

User manual

PP.14 Memory map.



P12.

1.10 Block diagram

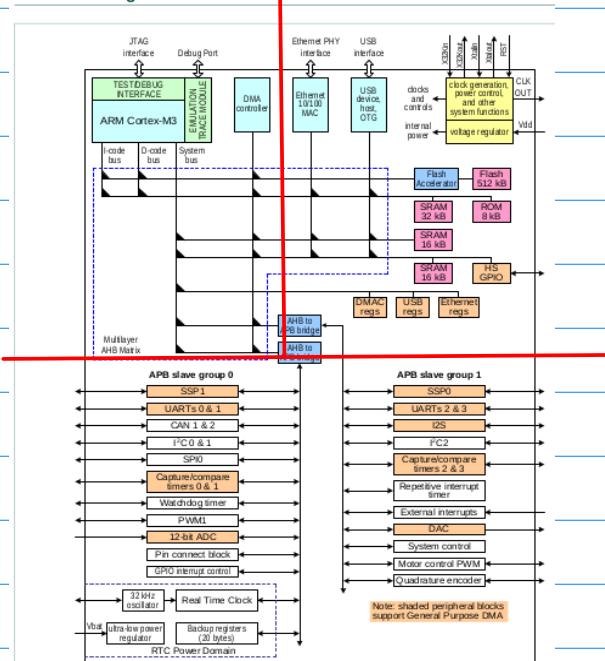


Fig 2. LPC1768 block diagram, CPU and buses

LPC11C24

LPC1769

End of Life

CPU module Board B

for Graphics
Engine Design
Emulation.
pre-fab.

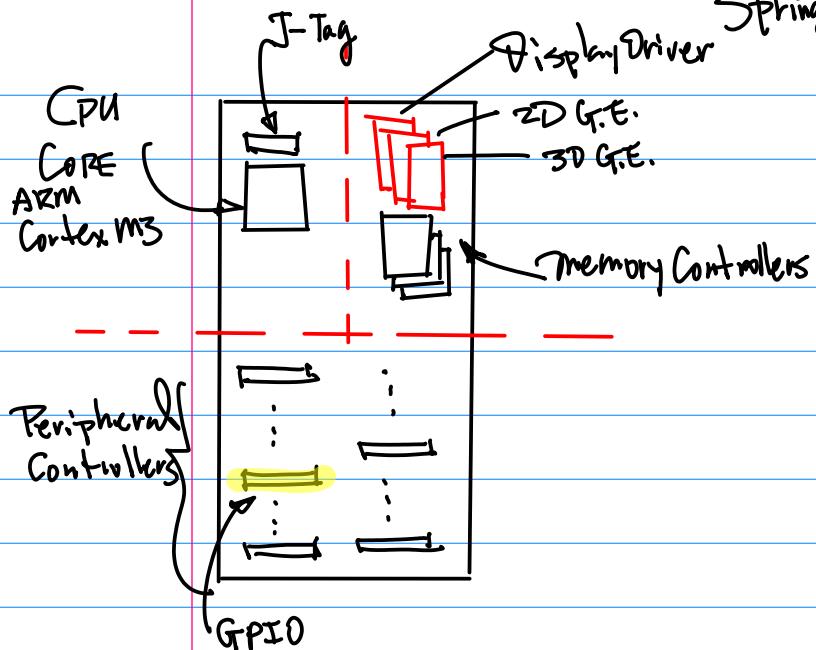
optional Option2

Purchase Removal of
Out-of- Stock. Except the
~16 weeks. CPL
module.

Example: Continuation of the SCH .

1. P_{8,9} → "P" Port, General

Purpose part → ARM multiplexing
Each pin can
have more than one



3° 3D Graphics Processing Engine. I.T.U.
 4° Video Codec. & Encoder MPEG4/H.264
 Decoder H.265
 Pixel Graphics.
 Vector Graphics. (Display Drive, 2D G.E.,
 3D G.E.)

5° General Discussion of the GPU Architecture

(i) 32 Bit RISC Architecture.

All. Bit width. 32bit 32bits
 Register File { Special Purpose Registers,
 General Purpose Registers.
 Any meaningful AL OPS. }

Init & Config. ✓
 32bit

Bus Systems { Address ~ 32bit / Uni-Directional
 Data ~ 32bit / Bi-directional.
 Control Bus

(2) memory Map. $2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^1$
 | : : :
 | K : :
 | Meg :
 | 1 Keg

4 G.? Byte

Byte Addressable machine. ~ minimum mem.
 Cell with an unique addr. is a single byte.

Discussion On the CPU Block Diagram.

1° Display Driver.

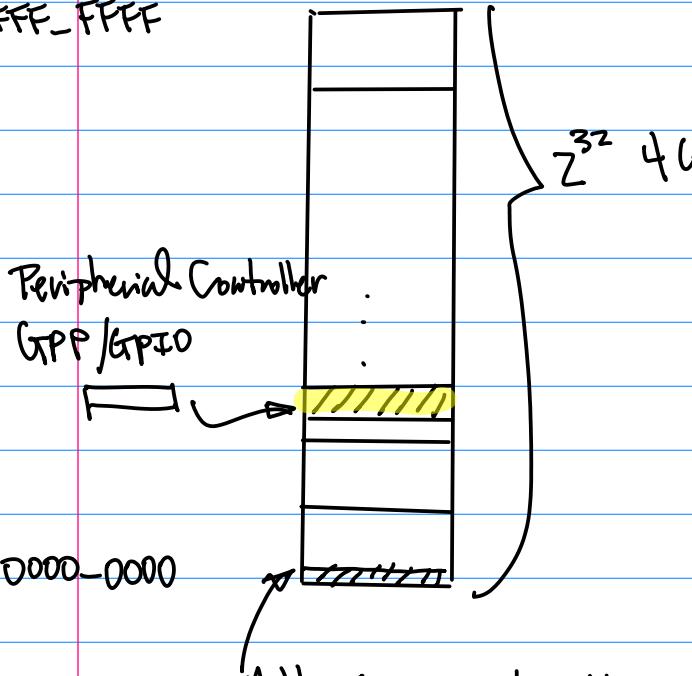
2° 2D Graphics Processing Engine

Example: Continuation of CPU
Architecture

Ref. GPU Datasheet pp.13,

pp.12.

0xFFFF_FFFF



a. Power-up Address: ~ when the CPU is powered up, it will go to this memory location to fetch the 1st Executable instruction

b. 8 Memory Banks. Equal size of memory blocks.

$$2^{32}/8 = 2^{32}/2^3 = 2^{29} = 2^9 \cdot 2^{20}$$

512 |
Meg.

1st BANK is enumerated as BANK0, ..., the last BANK is Bank7.

c. We use 3 Bits from the Address Bus to define the Starting Addr. of Each Bank.

" Little Endian "

$\alpha_3 \alpha_2 \dots \alpha_1 \alpha_0$

$\alpha_3 \alpha_2 \dots \alpha_1 \alpha_0$

$2^{32} = 4 \text{ GB}$	\dots
0 0 0 . 0	BANK0 0x0000_0000
0 0 1 . 0	BANK1 0x2000_0000
0 1 0 . 0	BANK2 0x4000_0000
\vdots	\vdots
1 1 1 . 0	\vdots

d.

UM10360

Chapter 2: LPC176x/5x Memory map
Rev. 3.1 — 2 April 2014

User manu

2.1 Memory map and peripheral addressing

The ARM Cortex-M3 processor has a single 4 GB address space. The following table shows how this space is used on the LPC176x/5x.

Table 3. LPC176x/5x memory usage and details

Address range	General Use	Address range details and description
0x0000_0000 - 0x0000_0007	On-chip non-volatile	0x0000_0000 - 0x0000_0FFF For devices with 512 kB of flash memory

Address for GPIO Controller. 0xZ---
0x4---

Feb 8. (Wed).

Note: Inspection of CPU module.

1° LPC1769 or LTC11C24;

2° Layout Design. CPU module location

Standoffs.
Wires

Prototyping wire

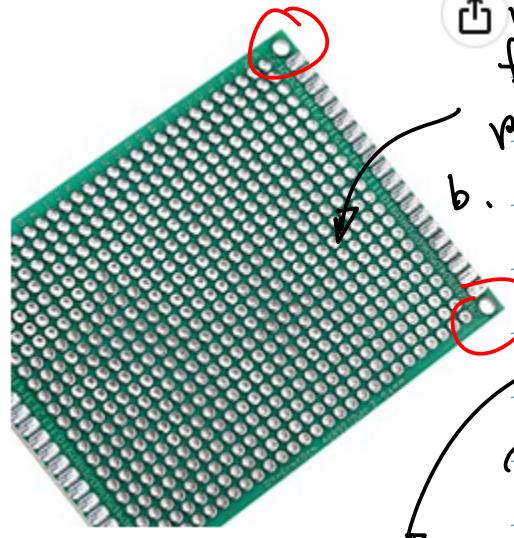
30AWG Blue

28n32 AWG

\$7.50



Prototype Board, Note:



- a. Through-Hole
is uniformly formed with plate coating
- b. Mounting holes at corners.
- c. Standoffs.

~ \$5-\$15



Exquisite Workmanship
Accurate dimensions and production methods ensure the perfect use of each component

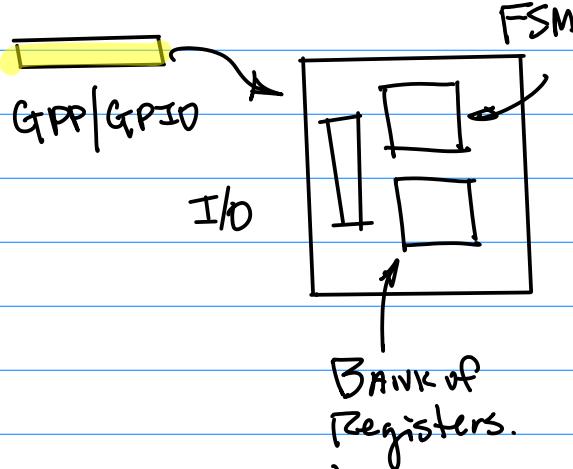
Note: Please Bring Your 1^o LTC CPU Module; 2^o USB Cable; 3^o Laptop with MCU Expresso for Inspection.

Example: Continuation of CPU Architecture

1^o Discussion

Note: A GPP/GPIO Controller is mapped to the memory map.
Read CPU Datasheet to find its Location;

2^o Special Purpose Registers.



Special Purpose Registers.

Task 1: Init & Config.

Naming Convention: URG
(Uniformity, Regularity, Orthogonality)

Root (3 letters)

↓ CON

Prefix + Root
3 letters 3 letters

GPI



GPP



GPI, GPI, GPX

GPPCON

Software to Drive the Peripheral Controller

↓
Compiler, gcc. Open Source → Target CPU

Punting

CMPE240

Spring 2023

a/

2nd Special Purpose Register

GPx + DAT

Reset.

GP&DAT.

Feb 13 (Monday).

Example: Start-up MCUXpresso.

1. Install MCUXpresso. Start the MCUX. → Project Browser (Top Left Panel) → A panel beneath it, "Import Project". Double Click / Select to open it, then follow the steps to import 17b9 patch.

2. the LPC17b9 Patch is posted on the github.



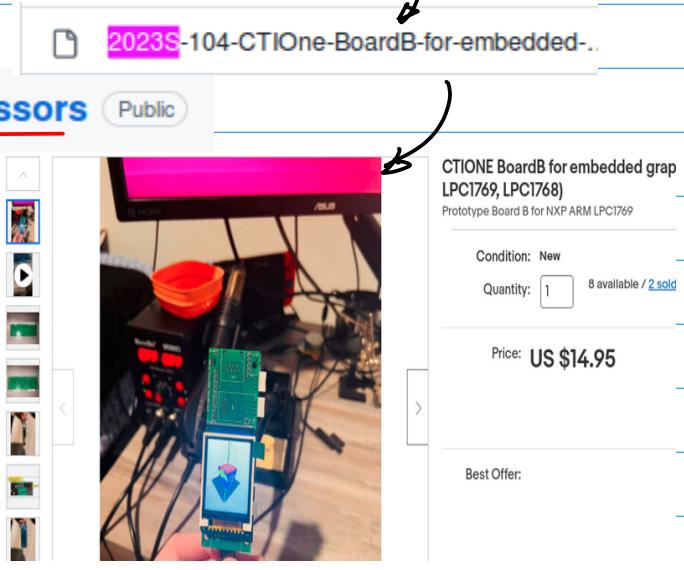
find a project with a keyword "Blanky". Then, use "Debug" option to Build it, And to observe the LED on the GPU module flashing.

4. Then Browse the LPC17b9 Patch, Locate 17xx.h which realizes the task of Porting the target platform(17b9) to the IDE Software.

Resources: The posted zip files.(projects),

LPC17b9 patch → gpio.zip → drawline (IIC24) zip
2D Graphics → 2D+3D (IIC24) projects for IIC24.

Note: for IIC24 Board)



3. Connect your LPC GPU module (LPC17b9)
Browse the imported 17b9 Projects.

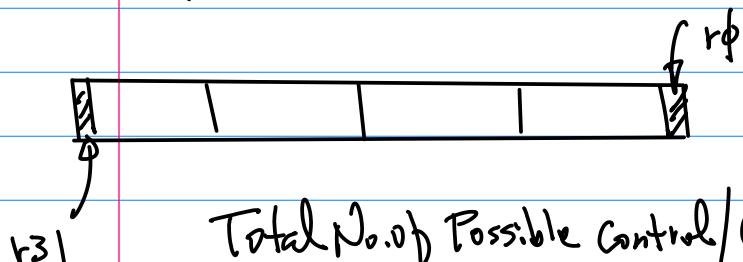


<https://www.digikey.com/en/products/detail/adafruit-industries-lc/358/5801368>



Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

Example: GPxCON 32 bit.



Total No. of Possible Control/Config
 $OPS = 2^{32}$

From CPU Datasheets, Inspection:

from github ~ Cmpe244

2021F-105-#0-cpu-arm...

Notation: Vector Notation

GPACON [3:0]

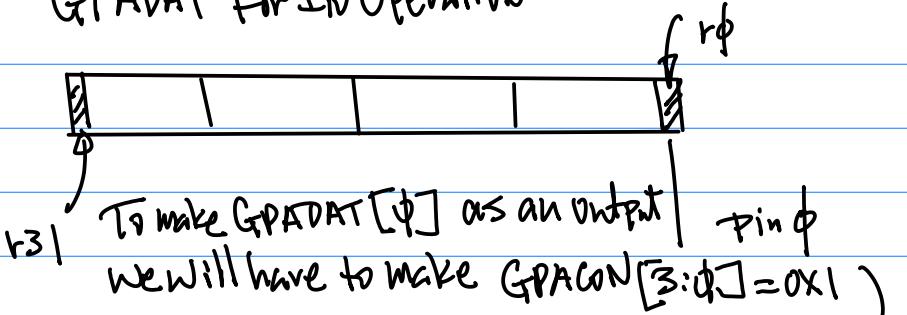
GPACONSLP	0x7F00800C	R/W	Port A Sleep mode Co
GPAPUDSLP	0x7F008010	R/W	Port A Sleep mode Pu

GPACON	Bit	Description	
GPA0	[3:0]	0000 = Input	0001 = Output
		0010 = UART RXD[0]	0011 = Reser
		0100 = Reserved	0101 = Reser
		0110 = Reserved	0111 = Extin
GPA1	[7:4]	0000 = Input	0001 = Output
		0010 = UART TXD[0]	0011 = Reser
		0100 = Reserved	0101 = Reser
		0110 = Reserved	0111 = Reser

The 1st Pin of the GPxIO Port.

CMPREGD

GPADAT For I/O operation



GPAON	Bit	Description	Initial State
GPA0	[3:0]	0000 = Input 0010 = UART RXD[0] 0100 = Reserved 0110 = Reserved	0000
GPA1	[7:4]	0000 = Input 0001 = Output	0000

From the SCD, we can find the physical pins to realize output function.

Feb 15 (wed)

Ref: 1° GPIO Code for LPC11C24

2022F-103i-lpc11c24-gpio-archive-2022-9-20.zip

2022F-103j-lec GPIO-v4-2017-2-22.pdf

For LPC1769, the Code/Project

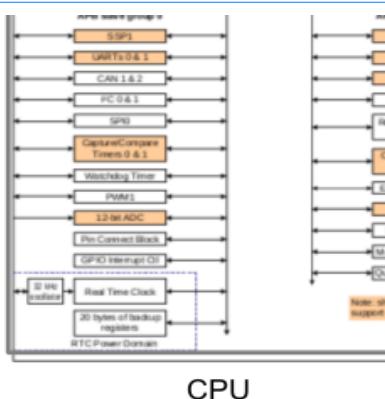
2° GPIO I/O Design.

Special purpose Register

like the following
`#define SPR 0x2000_0000`
map the CPU architecture to the arm gcc compiler

Note: 1° FIODIR, CPU Datasheet.

LPC_GPIO0->FIODIR
LPC_GPIO0->FIOSET
LPC_GPIO0->FIOCLR



2° Naming Convention.
Product Family → Peripheral Controller

Special Purpose Register

Source: 17xx.h

The mapping from CPU Architecture to the C-Code is defined by 17xx.h file with statements like:

LPC_GPIOφ → FIODIR 0x....

Memory Addr.

CPU Datasheet from .h

3° Mapping/Porting Architecture to C-code

LPC_GPIO0->FIOSET

LPC_GPIO0->FIOCLR

```
#include "../../../../tool...  
#ifdef USE_CMSIS  
/* CMSIS: the Cortex M */  
#include "LPC17xx.h"
```

Exercise: Must Do

- ① Locate LPC17xx.h
- ② Find $\text{GPIO}\phi$ part of the Code.
- ③ Locate $\text{LPC_GPIO}\phi \rightarrow \text{FIODIR}$

Find its Address.

- ④ Use CPU Datasheet to verify its Address in LTC17xx.h.

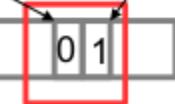
Continuation:

CPU Datasheet Table 102.

Discussion on Bit Settings.

Bit	Symbol	Value	Description
31:0	FIO0DIR		Fast GPIO Direction PORTx control bits. Bit 0 in FIOxDIR controls pin Px.0, bit 31 in FIOxDIR controls pin Px.31.
	FIO1DIR		
	FIO2DIR	0	Controlled pin is input. <i>a.</i>
	FIO3DIR	1	Controlled pin is output. <i>b.</i>
	FIO4DIR		

Bit 3 for pin 3 Bit 2 for pin 2



LPC GPIO0->FIO0DIR = 0x4; *c.*

Ref: LCD Display for LPC11C24

2022F-103f-LCD-connectivity-LPC11C24-hl-bj-2022-9-30.pdf

LPC11C24 Connectivity Table to

HL (2022-9-30) corrected this type by replacing
LPC 1769 to LPC11C24

Table 5. Connectivity Table of LPC11C24 and LCD

LPC11C24	Description	LCD
1. J6-28	3VOUT	VCC
2. J6-1	GND	GND
3. J6-8	SSEL0	TFT_CS
4. J6-14	RST	RESET
5. J6-13	D/C	A0
6. J6-5	MOSI0	SDA
7. J6-7	SCK0	SCK
8. J6-28	3VOUT	LED

Bread Wallfront

TFT LCD Display:
Screen: <https://www.amazon.com/gp/product/B07BFV69DZ/>
ref=ppx_yo_dt_b_search_asin_title?ie=UTF8&psc=1



1.8 inch SPI TFT LCD Display Module for
ST7735 128x160 51/AVR/STM32/ARM
8/16 bit

Visit the Wallfront Store

4.5 stars 20 ratings

Amazon's Choice in LCD Graphic Displays by Wallfront

-10% \$15.55

Price: \$19.99

prime One-Day

& FREE Returns

Includes \$1.71 Prime savings

Personalized All in One

Ref: CPU Datasheet for l1C24

1. [2022F-103g-lpc11c24-cpu-datasheet-UM10398.pdf](#) Add files via upload

2. [2022F-103h-SCH-LPCXpressoLPC11C24revB.pdf](#) Add files via upload

3. [2022F-103i-lpc11c24-gpio-archive-2022-9-20.zip](#) Add files via upload

Feb 20 (Monday),
Note: 1^o Homework coming on
CANVAS;

Today's Topics:

- 1^o Summary on GPIO
- 2^o Hardware for Graphics Engine ^{2D}

Example: Ref CPU Datasheet
Table 102. for
FIODIR S.P.R.

1^o
Note: Addr. for the S.P.R. Need to Be
Cross-refer'd in
MCUXpresso Code.

2^o FIODIR
multiple.
Registers

access to a group of bits in a single GPIO port independently from other bits in the same port.

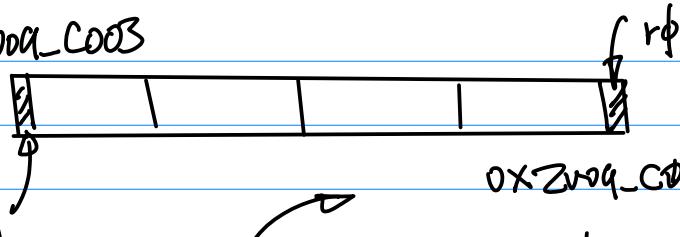
Table 102. GPIO register map (local bus accessible registers - enhanced GPIO features)

Generic Name	Description	Access	Reset value	PORTn Register Name & Address
FIODIR	Fast GPIO Port Direction control register. This register individually controls the direction of each port pin.	R/W	0	FIO0DIR - 0x2009 C000 FIO1DIR - 0x2009 C020 FIO2DIR - 0x2009 C040 FIO3DIR - 0x2009 C060 FIO4DIR - 0x2009 C080
FIOMASK	Fast Mask register for port. Writes, sets, clears, and reads to port (done via writes to FIOPIN, FIOSET, and FIOCLR, and reads of FIOPIN) alter or return only the bits enabled by zeros in this register.	R/W	0	FIO0MASK - 0x2009 C010 FIO1MASK - 0x2009 C030 FIO2MASK - 0x2009 C050 FIO3MASK - 0x2009 C070 FIO4MASK - 0x2009 C090

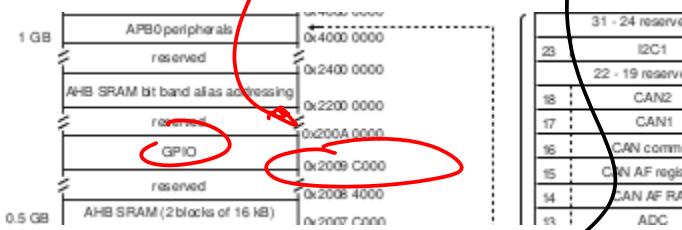
Connection To Coding: C/c++

FIO0DIR → LPC_GPIOφ → FIO0DIR

0x2009_C000 : 0x2009_C003

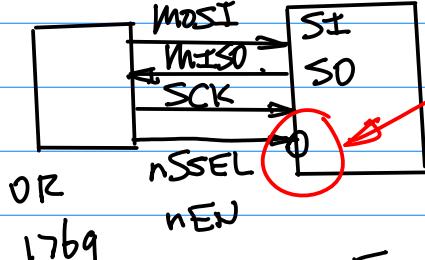


Connection To
Mem map



0x2009_C000

LPC_IIC24



LCD
Active
LOW!

Fig. 1.

30. Addr. for Byte Addressable
Machine, 4 Addresses.

Note: Bit Rate Discussion.

FIO0DIR[rx': rx], for Example

FIO0DIR[4:3]

40 Bit (Binary) Pattern for the S.P.R.

Table 105. Fast GPIO port Direction control byte and half-word accessible register description

Generic Register name	Description	Register length (bits) & access	Reset value	PORTn Register Address & Name
FIOxDIR0	Fast GPIO Port x Direction control register 0. Bit 0 in FIOxDIR0 register corresponds to pin Px.0 ... bit 7 to pin Px.7.	8 (byte) R/W	0x00	FIO0DIR0 - 0x2009_C000 FIO1DIR0 - 0x2009_C020 FIO2DIR0 - 0x2009_C040 FIO3DIR0 - 0x2009_C060 FIO4DIR0 - 0x2009_C080
FIOxDIR1	Fast GPIO Port x Direction	8 (byte)	0x00	FIO0DIR1 - 0x2009_C001

Responsible for P0.0 ~ P0.7 (8 pins).
"1" for OutInt, "0" for the input.

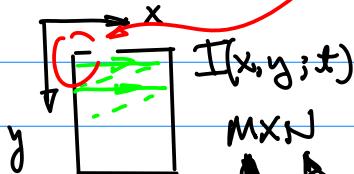
* Consider Hardware Design for
LCD Display.

Background: SPI. Enable LCD
Display Device.

Serial Peripheral Interface.
Bit Rate $\sim 100\text{Mbps}$.

Graphics
Display
Resolution:

(0,0)
 24×768



Scans:

Top Left Corner (0,0),

From left to Right

Top to Bottom.

No. of pixels/Row

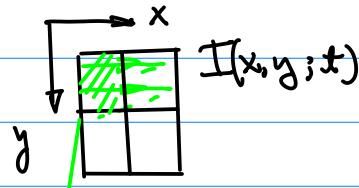
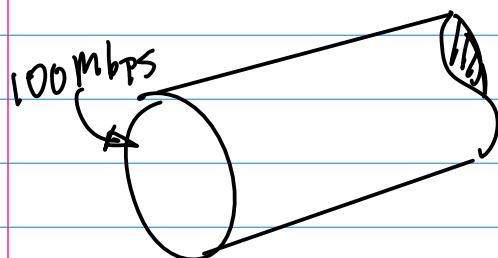
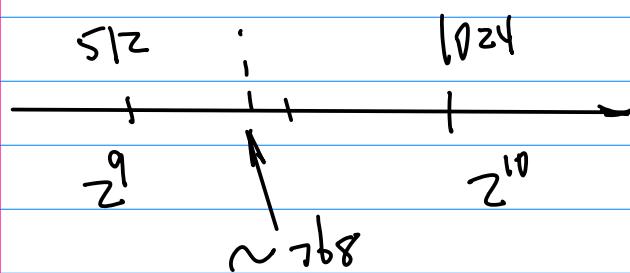
No. of Rows
Per Frame.

30 Frames Per Second (FPS)

24 Bits of color. (Color Depth)

$(0.24 \times 768 \times 30 \times 24)$ bit/sec.

$$\begin{aligned} & 2^{10} \quad 2^9 \quad 2^5 \quad 2^5 \\ & \quad \quad \quad \underbrace{\quad}_{2^{10}} = 1K \cdot 1K \cdot 2^9 \\ & 1 \quad \quad \quad \quad \quad = 1M \text{eg} \times 512 \\ & 1K \quad \quad \quad 1K \quad = 512 \text{ Mbps}, \end{aligned}$$



$$\frac{1}{4} \times 512 > 100 \text{ Mbps}$$

$\frac{1}{4}$ of the Resolution $1024 \rightarrow 1024 / 2 = 512$

SPI I/F: "3+"

$$768 \rightarrow 512 / 2 = 256$$

MISO (Master Input / Slave Output)
MOSI (Master Out / Slave Input)
SCK (Clock / Output)
SS (Slave Select / Enable): Active Low, Output from the master

Now, Let's go to Sot of the Target GRL.

2022F-103h-SCH-LPCXpressoLPC11C24revB.pdf

LPCXpresso	
GNDX	J6-1
VIN (4.5-5.5V)	
not used	J6-3
PIO0_0 RESET	J6-4
PIO0_9 MOSIO/SWO	J6-5
PIO0_8 MISO0	J6-6
PIO2_11 SCK0	J6-7
PIO0_2 SS0	J6-8
A PIO1_7 TXD	J6-9
!L PIO1_6 RXD	J6-10
PIO0_7	J6-11
PIO2_0	J6-12
X PIO2_1	J6-13
PIO2_2	J6-14
PIO0_11 AD0	J6-15

Dual row holes (2x27), 100 mil spacing

Build Connectivity Table

CPU pin	Connector	Note
pin No. / Name	Info	
PIO0_9/MOSIP	J6-5/MOSIP	

Feb 22 (Wk 6).

1° In-Class Homework 1 Pt.
Next Monday.

Homework : SPR & GPP.
In-Class.

~15 min.

Submission On-Line to CANVAS.
You will Need Laptop Computer.

Example: Continuation of Build GPIO to LCD Display Interface

CPU pin	Connector Info	Note
Pin No./Name		LCD Device
P100P-9/MOSI#	J6-5/MOSI#	SPI

Note: for LCD pin Connectivity Information
for LPC11C24

2022F-103f-LCD-connectivity-LPC11C24-hl-bj-2022-9-30.pdf

HL (2022-9-30) corrected this typo by replacing
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3. J6-8	SSEL0	TFT_CS
4. J6-14	RST	RESET
5. J6-13	D/C	AO
6. J6-5	MOSIO	SDA
7. J6-7	SCK0	SCK
8. J6-28	3VOUT	LED

3° Control Signal from the Master, CPU,
D : Data ; C : Command
Binary Value ; 4° SDA is S.I.
Serial Inpt ; 5° for Backlight

Note: 8 pin v.s. 10 pins. if for Wirewrapping

Build, then you can use any one of the
two. Check the Latest pin Layouts
for IIC24 Prefab Board.

Software Design: Theoretical Background
CPU Architecture Coding.

Coding: MCUXpresso Installation.

SDK for the target CPU
Configuration

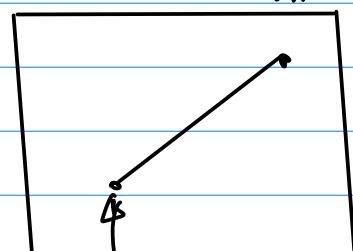
Import the existing code
LPC1769 patch.

LPC11C24 gpi0.zip

Test Drive, "Dry Run"

Ready for "DrawLine"
project (Code for
LPC1769, and code for
LPC11C24.)

$\vec{P}_{i+1}(x_{i+1}, y_{i+1})$



$P_i(x_i, y_i)$

CPU Datasheet, pp. 43)

Note: 1^o Control Register, SSP0CR0

Table 371: SSPn Control Register 0 (SSP0CR0 - address 0x4008 8000, SS 0x4003 0000) bit description

Bit	Symbol	Value	Description
3:0	DSS	0011	Data Size Select. This field controls the number of bits transferred in each frame. Values 0000-0010 are not and should not be used. A bit transfer

2^o Addr. for SSP0CR0 : 0x4008_8000.

Where is it on the Memory Map?

How is it reflected in C/C++ code,

e.g. LPC17xx.h

3^o SSP0CR0 [3:0]

Least Significant Bit
Most Significant Bit

"Little Endian"

r31

SSP0CR0 [3:0] : DataSizeSelect. (DSS).

For 8-bit Communication.

Bit	Symbol	Value	Description
3:0	DSS	0011	Data Size Select. This field controls the number of bits transferred in each frame and should not be used.
		0010	4-bit transfer
		0100	5-bit transfer
		0101	6-bit transfer
		0110	7-bit transfer
		0111	8-bit transfer
		1000	9-bit transfer
		1001	10-bit transfer
		1010	11-bit transfer
		1011	12-bit transfer
		1100	13-bit transfer

$$\text{SSP0CR0 [3:0]} = 0111 = 0 \times 7$$

Tech. Spec.
(Technical Specification)

Binary Pattern
for Init &
Config.

For SPI

$$\text{SSP0CR0 [5:4]} = 00$$

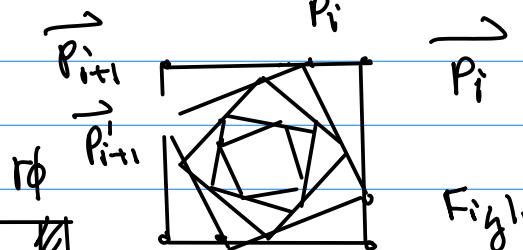
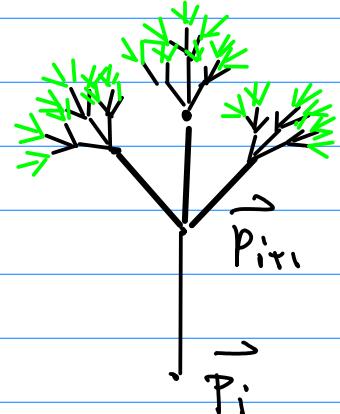
$$f_{\text{SPI}} = \frac{\text{PCLK}}{(CSDVSR * (SC2+1))}$$

$(2 \sim 255)$ ↑ ↑ ... (1)

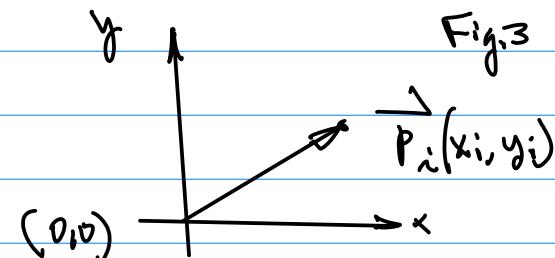
Feb 27 (Monday)

Project 1. One 2^{1/2} weeks.

Design & implement 2D Vector Graphics.

1^o Screen Saver.2^o

Background DN 2D Vector Graphics



$$\vec{P} \rightarrow \vec{P}(x, y) \rightarrow (x, y)$$

$$\vec{P}(x, y) = (x, y)$$

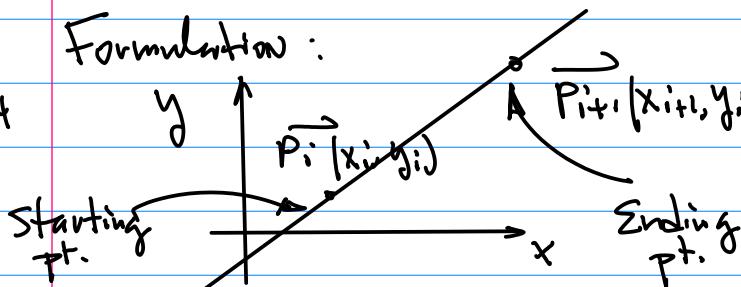
if $x < 0$, then we have all the pts defined by Eqn(z-b).

$$\vec{P}_i \rightarrow \vec{P}_i(x_i, y_i) = (x_i, y_i)$$

if $\lambda > 1$, then we have all the pts beyond the Ending Pt.

Visualize the vector $\vec{P}_i(x_i, y_i)$

Fig 4



Marchist (Wed)

Note: Project Due in 2 weeks
10 pts.

Example: Design Rotating Square

(Given $\vec{P}_i(x_i, y_i)$ and $\vec{P}_{i+1}(x_{i+1}, y_{i+1})$).

Define a directional vector.

$$\vec{d}(x, y) = \vec{P}_{i+1}(x_{i+1}, y_{i+1}) - \vec{P}_i(x_i, y_i)$$

$$= (x_{i+1} - x_i, y_{i+1} - y_i) \quad \dots (1)$$

Therefore,

$$\vec{P}(x, y) = \vec{P}_i(x_i, y_i) + \lambda \vec{d}(x, y) \quad \dots (z-a)$$

$$\vec{P}(x, y) = \vec{P}_i(x_i, y_i) + \lambda (\vec{P}_{i+1}(x_{i+1}, y_{i+1}) - \vec{P}_i(x_i, y_i)) \quad \dots (z-b)$$

where $\lambda \in (-\infty, +\infty)$

Question 1: Find the starting pt by Eqn(z-b)?

Question 2: Find the ending pt by Eqn(z-b)?

$$\lambda = 1$$

Question: Find All the pts Between \vec{P}_i and \vec{P}_{i+1} ? $0 < \lambda < 1$

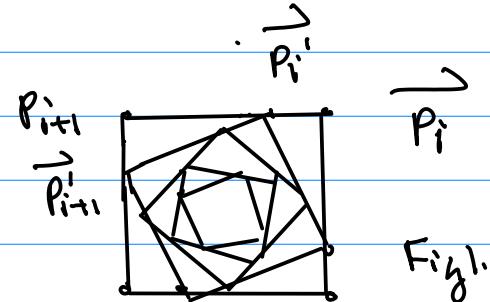


Fig.1

$$\vec{P}_{i+2}$$

Fig.1

First, To create a set of points,
 $\{\vec{P}_i(x_i, y_i) | i=0, 1, 2, 3\} \dots (1)$

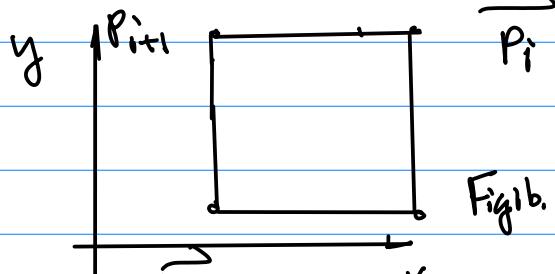


Fig.1b.

Virtual Coordinate System

Let's choose $\vec{P}_i \Big|_{i=0} = (30, 25)$

$$\vec{P}_1(10, 25), \vec{P}_2(10, 5), \vec{P}_3(30, 5)$$

Then use DrawLine Sample Code
to Draw Lines to Connect Each Pair
of points.

$$\vec{P}_0, \vec{P}_1; \vec{P}_1, \vec{P}_2; \vec{P}_2, \vec{P}_3;$$

$$\text{and } \vec{P}_3, \vec{P}_0$$

Note: in C/C++, Use mod() Function.

Then, Define the 2nd set of points.

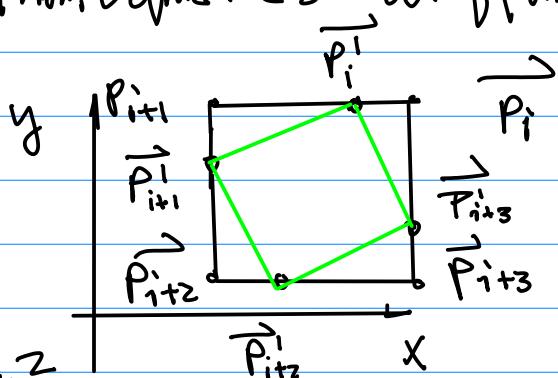


Fig. 2

Define A set of pts as

From Eqn.(2b), we have

$$\vec{P}(x, y) = \vec{P}_i(x_i, y_i) + \lambda (\vec{P}_{i+1}(x_{i+1}, y_{i+1}) - \vec{P}_i(x_i, y_i)) \dots (2)$$

$$\vec{P}_0'(x_0', y_0') = \vec{P}_0^0(x_0^0, y_0^0) + \lambda (\vec{P}_1^0(x_1^0, y_1^0) - \vec{P}_0^0(x_0^0, y_0^0)) \dots (3)$$

Coding it in C/C++

$$\vec{P}_0'(x_0', y_0') = \vec{P}_0^0(x_0^0, y_0^0) + \lambda (\vec{P}_1^0(x_1^0, y_1^0) - \vec{P}_0^0(x_0^0, y_0^0))$$

$$= (x_0^0, y_0^0) + \lambda (x_1^0 - x_0^0, y_1^0 - y_0^0)$$

Hence,

$$\left\{ \begin{array}{l} x_0' = x_0^0 + \lambda (x_1^0 - x_0^0) \\ y_0' = y_0^0 + \lambda (y_1^0 - y_0^0) \end{array} \right. \dots (4a)$$

$$\left\{ \begin{array}{l} x_0' = x_0^0 + \lambda (x_1^0 - x_0^0) \\ y_0' = y_0^0 + \lambda (y_1^0 - y_0^0) \end{array} \right. \dots (4b)$$

$$\text{lambda} = 0.2$$

$$\times [0][0] = x[0][0] + \text{lambda} * (x[1][0] - x[0][0]); \dots (5)$$

Next Step, generalize it for level $j+1$
for all the points i , ($i=0, 1, 2, 3$)

$$\vec{P}_i^{j+1} = \vec{P}_i^j + \lambda (\vec{P}_{i+1}^j - \vec{P}_i^j)$$

$$\vec{P}_i^{j+1}(x_i^{j+1}, y_i^{j+1}) = \vec{P}_i^j(x_i^j, y_i^j) + \lambda (\vec{P}_{i+1}^j(x_{i+1}^j, y_{i+1}^j) - \vec{P}_i^j(x_i^j, y_i^j)) \dots (6)$$

for the Coding :

$$\left\{ \begin{array}{l} x_i^{j+1} = x_i^j + \lambda (x_{i+1}^j - x_i^j) \\ y_i^{j+1} = y_i^j + \lambda (y_{i+1}^j - y_i^j) \end{array} \right. \dots (7a)$$

$$\left\{ \begin{array}{l} x_i^{j+1} = x_i^j + \lambda (x_{i+1}^j - x_i^j) \\ y_i^{j+1} = y_i^j + \lambda (y_{i+1}^j - y_i^j) \end{array} \right. \dots (7b)$$

Example: Design & Implement
Tree Drawing Algorithm

Next we "grow" the tree to Level 1

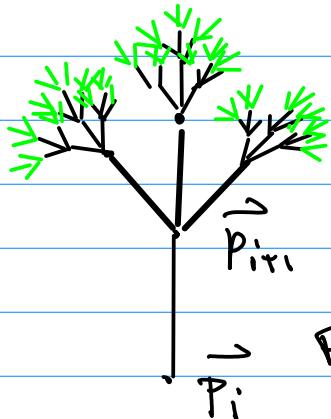


Fig.3a

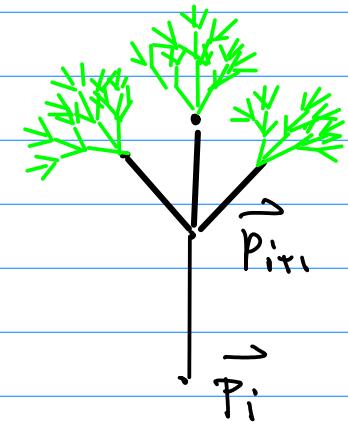
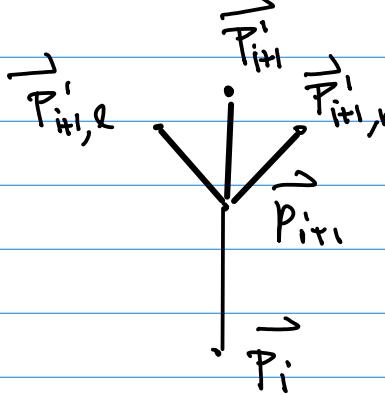


Fig.4.

where \vec{P}_{i+1} is the point

with 20% Reduction of its previous magnitude,

$$\vec{P}_{i+1}^1 = \vec{P}_i + \lambda (\vec{P}_{i+1} - \vec{P}_i) \quad | \lambda = 0.8$$

To find pts to the right & left, Let's define 2D Transforms.

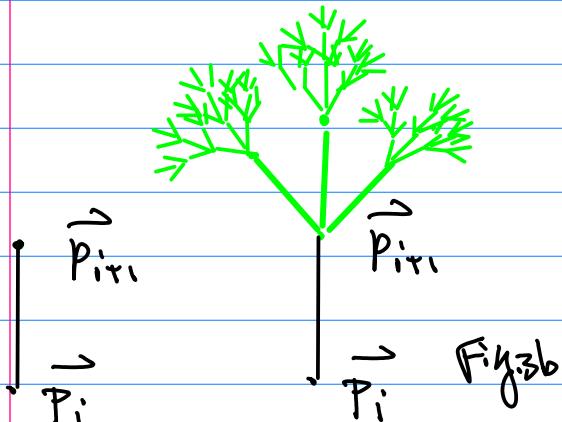


Fig.3b

Define \vec{P}_i and \vec{P}_{i+1} as points for the tree trunk.

$$\vec{P}_i(x_i, y_i) \Big|_{i=0} = \vec{P}_0(x_0, y_0) = (10, z)$$

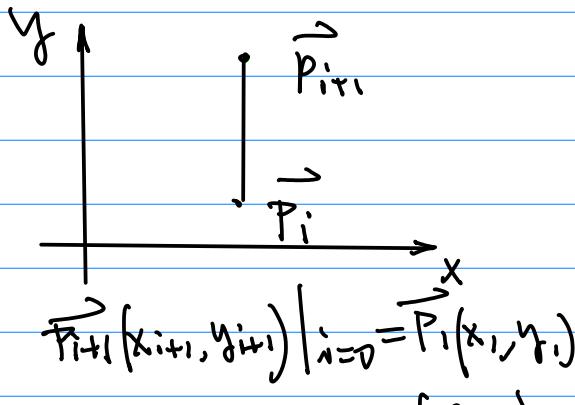


Fig.3c

$$= (10, 12)$$

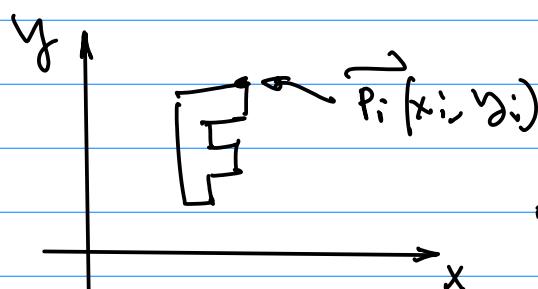


Fig.5

Define A Pattern $\{\vec{P}_i(x_i, y_i)\}_{i=0, \dots, n}\}$

1. Translation.

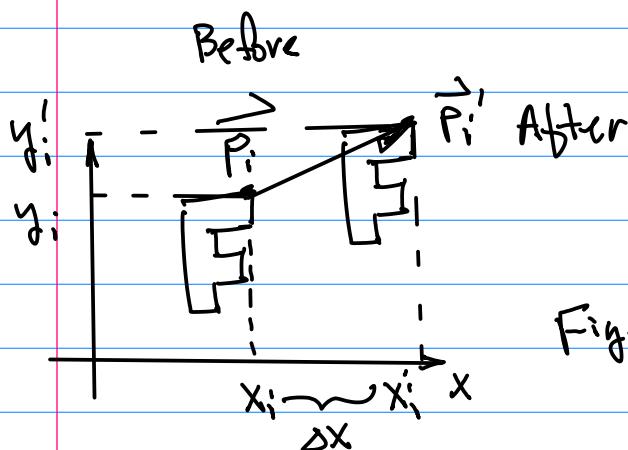


Fig.b

$$\begin{pmatrix} x'_i \\ y'_i \\ 1 \end{pmatrix} = \begin{pmatrix} 1 & 0 & \Delta x \\ 0 & 1 & \Delta y \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \\ 1 \end{pmatrix} \dots (a)$$

Rotation.

$$\{\vec{P}_i(x_i, y_i)\} \xrightarrow{\phi} \{\vec{P}'_i(x'_i, y'_i)\}$$

2. Rotation

$$\begin{pmatrix} x'_i \\ y'_i \\ 1 \end{pmatrix} = \begin{pmatrix} \cos \theta & \sin \theta & 0 \\ \sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \\ 1 \end{pmatrix} \dots (b)$$

2018F-112-lec4-2D-vectors-v3-2018-10-1.pdf

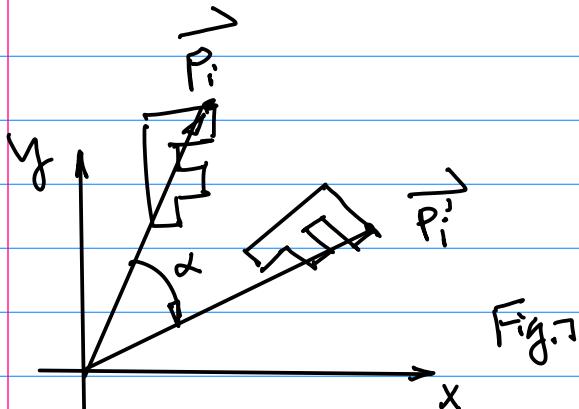


Fig.7

Clockwise Rotation $\alpha < 0$ Counter Clockwise Rotation $\alpha > 0$

Let's consider the translation.

$$(x_i, y_i) \xrightarrow{\phi=?} (x'_i, y'_i)$$

Before After

$$x'_i = ? \quad x'_i = x_i + \Delta x$$

Where $\Delta x = x'_i - x_i \dots (8a)$

Similarly

$$y'_i = y_i + \Delta y \dots (8b)$$