

Jan 27 (Wed), 2021 Harry LI

CMPE240 Welcome to 240 Section 2

Email: hua.li@sjtu.edu

Office Hours: M.W. 4:30-5:30 pm.

Zoom Based

Greensheet [github/hualili](https://github.com/hualili)

CMPE240/2018F

References:

1. Greensheet on github
(650) 400-1116 Text message
Prereq Requirements 180D

Advanced Microprocessor Systems

Smart phones \rightarrow RISC Architecture

5G, Edge AI \rightarrow IoT, AI \rightarrow GPU

Prototype System

Fully Functional Microprocessor
System

CMPE240 Feb 1 (Mon) 1/

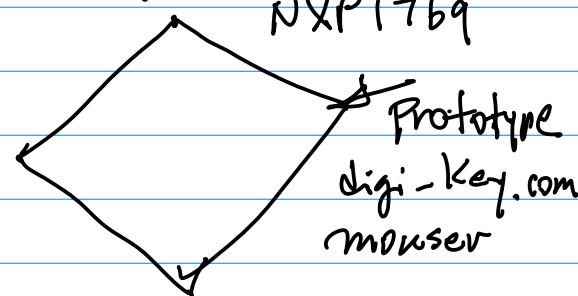
Today's Topics: 1° System Level Architecture — LPC1769

Ref: [github/hualili/cmpe240](https://github.com/hualili/cmpe240)

2018F-102 2° CPU Datasheet

Example:

1° CPU Module @ center of the System Layout Design



2° Wirewrapping Board
Dimension: 6" x 4"

with Through-Holes, Architectural and one side of Board Aspects whose through-Holes

with metal plating; ~~But~~ not the entire Board (just the through-Holes)

Action Items:

1° [github/hualili/cmpe240](https://github.com/hualili/cmpe240)

2° Prereq Requirements, 180D

3° LPC1769 CPU module

[digi-key.com](https://www.digi-key.com) OR [mouser.com](https://www.mouser.com)

3° PWR CKT: J1 Connector

Right Angle Connector;

S/W Toggle Switch; IC

Regulator 7805, 1117

Red LED 4-10mA

Resistor, Cap. (LPF)

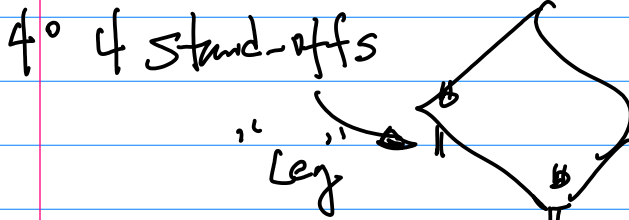
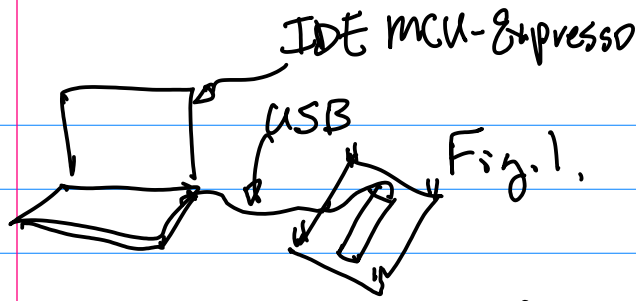
NXP.com Note: Debug/Development

No External PWR CKT

Handson: multiple projects, 3 mile Stones

4° CPU Datasheet

5° MCU expresso



Ref: CPU module Design. pdf
github, Rev. D. OR higher
From the Datasheet, Two tables
on Each Side of the CPU module
First, Left Side, the outer table
is for mbed, Not interested.

Naming Convention:

- ① CPU pin is named identical
as the name appeared in the
CPU Datasheet;
- ② The physical connector Label(s)
are given on the SCH to match
up the physical Board

Question: Find the pin for GND

From SCH,

Connectivity Table

Functional Pin	Physical Pin	Note
GND	J2-1	
VIN	J2-2	4.5~5.5VDC

Enumeration of the pin(s)
CPU pin (1st pin) starts as
"0";

CPU Datasheet 2018S-3-
UM10360
CPU Architecture, PP.9

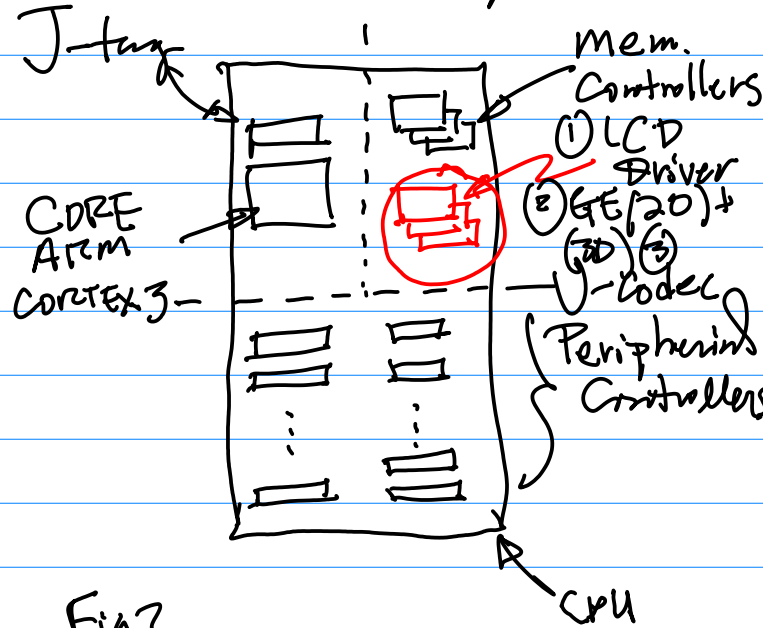


Fig 2.

Peripheral Controllers (SCH, ^{CPU} Datasheet)

Feb 3. CMPE240 HARRY LI

Note: 1° Have your Video when
Participating the Class; 2°
Honest Pledge Form/Sign
CANVAS submission By
Sat. 11:59 pm;

Today's Topics: 1° CPU
Architecture / CPU Datasheet
SCH; 2° Homework Design
of prototype Board

Peripheral Controller

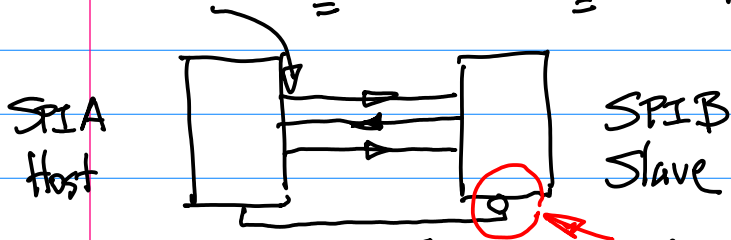
Ref: ① CPU Datasheet, pp.9.
② SCH

Example: From SCH.

1° SPI Serial Peripheral Interface

Note: RESET pin has to be Included in
Our Prototype Design

MOSI: Master Output Slave Interface



MISO: Master Input Slave Output

SCK: Serial Clock (0)

SSEL: Enable SPI Controller (on
the Slave Side, Active Low)

Note: MOSI_x, MISO_x, SCK_x,
SSEL_x, where x stands for the
xth of SPI Controller

Question: Find Number of SPI I/F
for this LPC1769 CPU?

Two SPI I/F SPI0, SPI1

2° UART (Serial I/F), Note RS232

{ TX (Transmitter)
 RX (Receiver)

3rd pin has to be a part of it: GND

Pd.0; Pd.1

Multiplexing, TX/SDA

Init & Config for Special
Purpose Registers will define
which function the pin will
I/O assume.

Action 1: Homework —
Read SCH, generate a
table for all peripheral
Controllers

Table: CPU Datasheet, pp.9

Table 2: SCH, to find subset
of the I/O Controller.

Advanced Feature:

G.E. Graphics Engine

Example: Broadcom
Pie3BT, 4 GE

NDA: GPU (Graphics
Processing Unit)

NAND 128 GPU.

TX2, 6 CPU +

256 GPU

"3+1"
pins

{ MOSI/MISO/SCK
 SSEL (Enable)

Software Implementation

for G.E (2D, 3D)

Basic Concepts.

1° RISC (Reduced Instruction
Set Computer) { ARM
 MIPS

32 Bit

4

Memory: $2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2 = 4 \text{ GB}$

1° Byte Addressable

Smallest memory with an unique address is a Single Byte

CMPE240 Feb 8 (Mon), Harry LI

1. Bill of material (git hub)

2° CPU Architecture

3. Preparation to Bring up your CPU, MCU Expresso

Two Step Process to Prepare for Prototype Board,

Step1: CPU module LPC1769

Wire wrapping (Prototype Board)
"glue" Logic Resistor, Caps,
PWR Regulator IC
(7805), Red LED, Stand-off

V_{out} 3,3VDC, 10 ~ 30mA

Estimate $3.3V / 10mA$, $3.3V / 30mA$
 3.3×10^{-2} , 1.1×10^{-2}
 Amps.

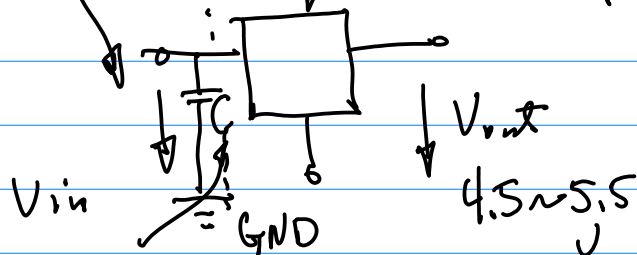
Wall mount Adaptor

110 ACV \rightarrow

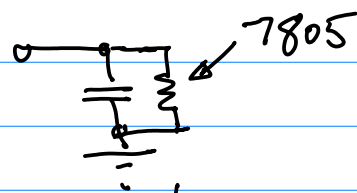
7.5VDC

1.000 ~ 1500 mA

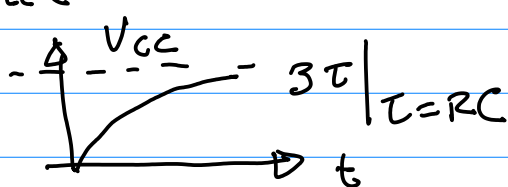
Note: PWR Regulator IC, 7805 ($\sim 2V_{DC}$)
↓ Volt drop



To Comp to Realize LPE.




$$V_c(1 - e^{-\frac{t}{RC}}) \dots (1)$$



4.7 MF

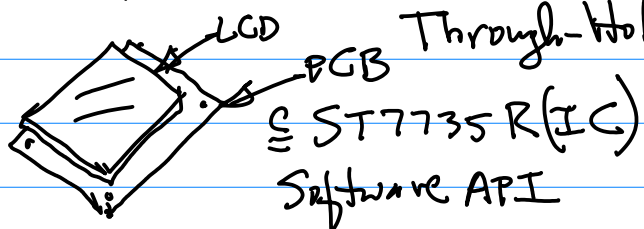
2nd part for Caps : 7805

Datasheet for 7805, Cmps are those with Polarity "  "

Bill of the Material to Build G.E.

SPI I/F Based Color LCD Device. a SPI (Not I2C)

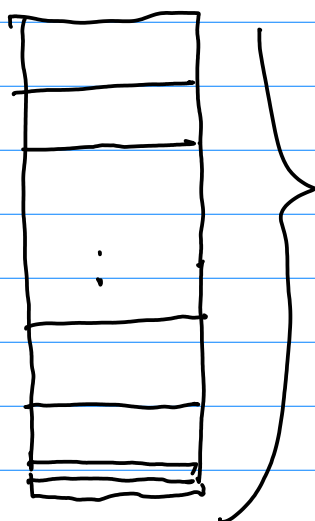
b Module - Connector



2-3 weeks

CPU Architecture Discussion

1^o memory map



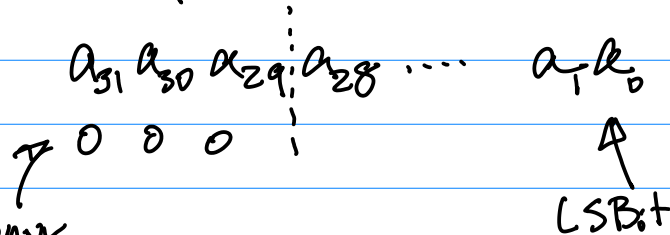
$$2^{32} = 4 \text{ GB}$$

3^o memory Bank: 8

$$4 \text{ G}/8 = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2 / 2^3$$

$$= 2^9 \cdot 2^{10} \cdot 2^{10} = 512 \text{ M}$$

Question: How many Bits from the Addr. Bus do we need to uniquely define each memory Through-Hole Bank? 3 Bits



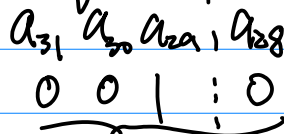
1st BANK

Starting Addr. of the 1st Bank,

Little Endian

0x0000_0000

What is the Starting Address of the 2nd Bank:



0x2000_0000 ; 2nd Bank

0x4000_0000 ; 3rd Bank

CMPE240 Feb10(Wed)

Ref: [github/hualili/CMPE240](https://github.com/hualili/CMPE240)

... 2018F-107-LEC6PP

Homework 1. Form 4-Person Team

First, Last Name, Last 4 Digits SID

E-mail Address -> Submission

2^o Byte Addressable Machine
~ whose Smallest mem. cell
with unique address is a
Single Byte

Via Email & Canvas By Thursday

11:59 Subject Title → Team Coordinator

Document Name

First-Last-CMP240

E-mail Submission.

Homework 2: (1 pt)

Requirements ① Build a prototype Board, ② Write a first program

Turn on/off LED "Hello, the world"

Note: Use Prototype Board to Build GPP I/O to Drive LED on/off

③ Build I/O Testing Circuit, the CKT input is from GPP (GPI/O)

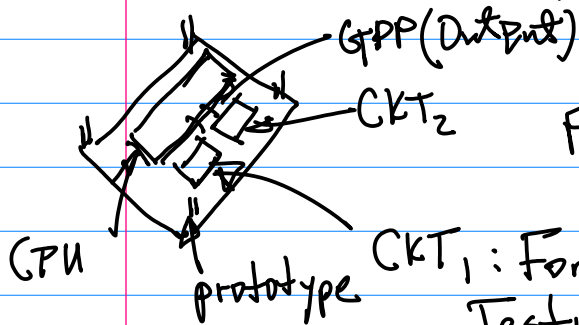


Fig. 1.

CKT₁: For Output Testing

"1" to Turn on LED

"0" to Turn off LED

CKT₂: For Input Testing

Input "1", Toggle Switch to connect GPP Input to V_{CC} (via a Resistor)

Input "0", Toggle the switch to GND (via Resistor)

④ Write one page Report (IEEE paper format) white paper Due on CANVAS

Due 2 weeks from Today, Feb 24.

Submission:

1° Project Exported

in Zip format

2° White paper, Report

3° Video Clip (up to 5 ~ 7

Seconds) Short please.

Example: From PPT on GPP I/F.

Identify CPU GPP pin

P0.3 J2-22 Input

P0.21 J2-23 Output

Consider the Output Testing CKT,

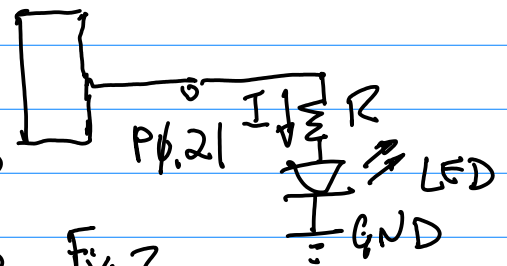


Fig. 2

$$V_{CC} = IR + V_{LED} \dots (1)$$

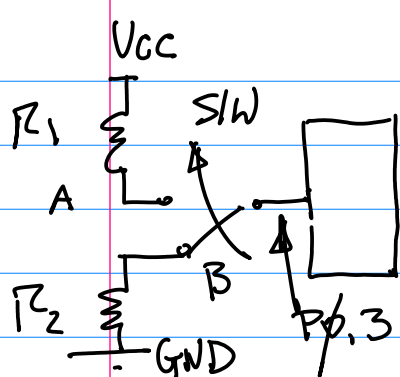
$$V_{CC} = 3.3 \text{ VDC}$$

$$I \cong 10 \text{ mA}, V_{LED} = 1.2 \text{ VDC}$$

$$3.3 = 10 \times 10^{-3} R + 1.2$$

$$R = (3.3 - 1.2) / 10^{-2} = 210 \Omega$$

Now, Let's Design CKT₂



SW:
@ A

R_2 : Output $V_{CC} = 3.3$
 $I = 4 \text{ mA}$

$$R_2 = \frac{3.3}{4 \times 10^{-3}} \approx 1 \text{ K}\Omega$$

R_1 : Output, GND

$$\frac{V_{CC}}{R_1} = 4 \text{ mA}, \quad \frac{3.3}{4 \text{ mA}} \approx 1 \text{ K}\Omega$$

System Level & Software Design

1st CPU Architecture \rightarrow mem. map
Peripheral Controllers BANK of
GPP Controller

a Power-up Address Background:
1st Address

0x0000_0000 CPU when powered up

It will fetch the 1st Executable Instruction at this Location



Fig 1

Firmware

ROM/Flash Bootloader

Branch/Jump Instruction

0x0000_0000 power up Addr.

Feb 15 Monday

Today's Topic: GPP I/O Testing

CPU Architecture & Special Purpose Registers.

Power-up Addr: Addr.
When CPU is powered, it will fetch the 1st instruction to execute at this memory location.

Firmware — A program which has been burnt into ROM/Flash

Question: How do you write C program to perform GPIO init & Config? So that I/O I/F can be established?

Hardware: Peripheral Controllers
Software

GPP General Purpose Port

(GPIO)

GPP Controller

Special Purpose Registers 32 bits:

Their function:

- a Control function: Init & Config
- b Data Exchange Function:
- c Pull up/Down

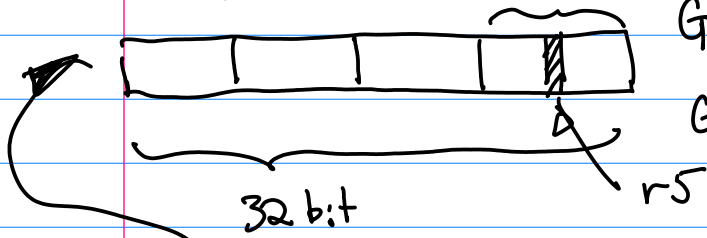
CMPE240

Naming Convention:

Prefix + Root + Postscript
 3 3 (3)
 GPx CON

General purpose GPxCON

GPP - Port | - What is the
 Size for GPxCON?



Note: 1° 0Xuuuu_uuuu
 Suppose 0X4000_0200

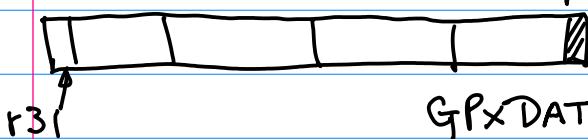


Fig 2

Question: How many Control function
 Can one Control Register define?

$$2^{32} = 4 \text{ G}$$

Now, GPxDAT, 0X4000_0204



GPxDAT[0] Fig 3.

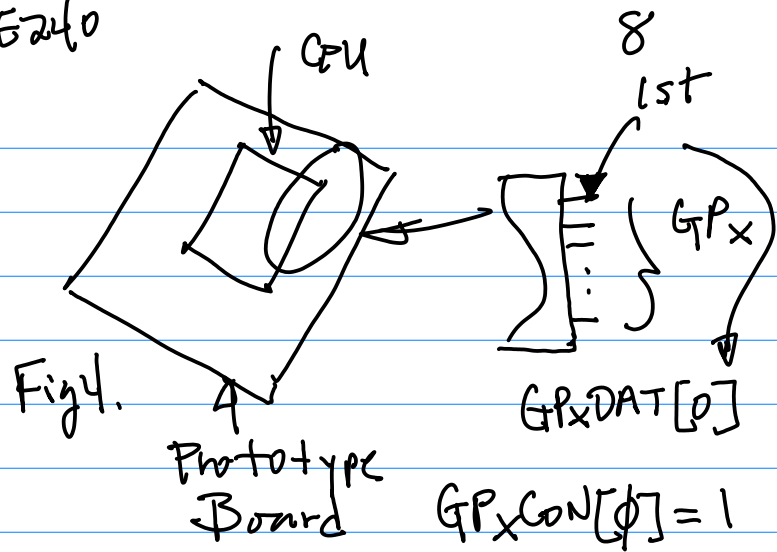


Fig 4.

Action 1: LPC1769 patch.zip

Import it as a project
 into your IDE

Test run blinky Program

To modify the GPP
 = 0 So P0.2 & P0.3

Can be employed for
 I/O Testing

Note: 1° Project Panel on the
 top left of your IDE GUI
 → Select "Blinky" By
 highlighting it.

CMPE240 Feb 17 (W)

Ref: 1° github/Runalili/
 CMPE240/2018S-11-
 GPIO2015-1-30.zip

2° ~ /cmpe240/
 Endian) 2018-10-LCD -

DrawLine.zip

3° ~ /2018F/2018F-107-~
(For GPP)

4° ~ /2018F/2018F-109
(For SPI LCD)

5° ~ /cmpe240/2018S-10-~
DrawLine.zip
(For 2D GE-Line Plot)

Topics: 1° SPRs for SPI LCD
I/F; 2° SPRs for GPP.

Init & Config of Peripheral Controller(s)

GPP
SPI (Serial Peripheral Interface)

Note: External Connector → CPU GPP.
J2-X Pp.2, etc.

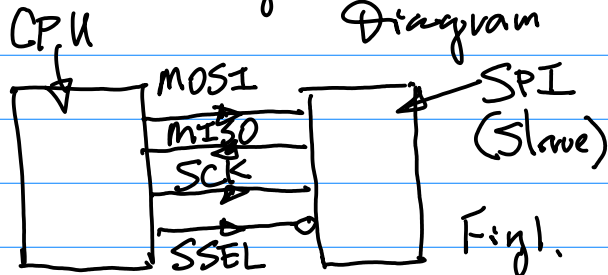
Example:

SPI Interface for Color
LCD Display.

Hardware Design
Software Design

Consider Hardware Design Block Diagram

Step 1
SPI Host



Pin Connectivity "3+1"

CPU	SPI(s)	Note
MOSI Pp.9/J2-5	SI	CPU (0)
MISO Pp.8/J2-6	SO	CPU (1)
SCK Pp.7/J2-7	CLK	CPU (0)
SSEL Pp.6/J2-8	\overline{CS} (nCS)	CPU (0) Active Low

Table 1: Connectivity Table
2018S-8-SPI (photo Board)

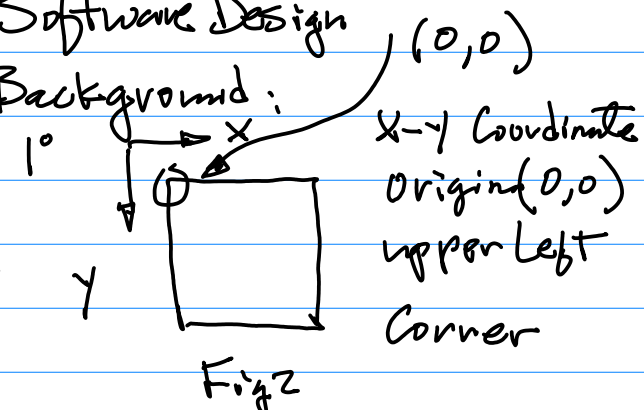
2018F-108-LCD-Connector

Note: Connectivity Table
for CPU to SPI LCD Display
Device.

Action 1: Solder up the SPI
LCD Device;

Software Design

Background:



Resolution: $M \times N$

M : No. of pixels per row

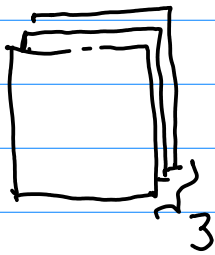
N : No. of Rows per Frame

Example: 160×120

Width
No. of Pixels/Row

Height
No. of Rows

2^o $I(x, y)$ Image plane(s)

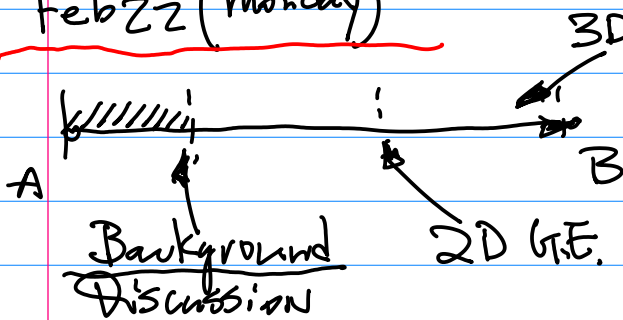


r : red;
 g : green;
 b : blue.

Fig. 1

$I(x, y) = (r(x, y), g(x, y), b(x, y))$
... (1)

Feb 22 (Monday)



GPP I/O Testing

- (1) CPU Architecture
CPU Block Diagram
- (2) SPR Init & Config.
memory map
Peripheral Controller
GPP + SPI
- (3) Implementation

Development Environment

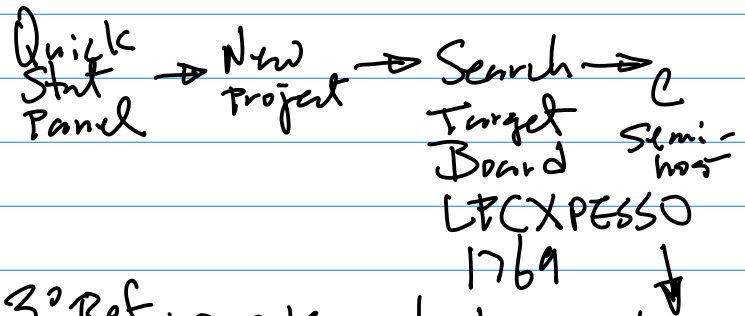
IDE \neq SDK

1^o Ref: 20215-1066-~

Note: IDE Not Backwards Compatible

Version 11.3.0 User Guide

2^o Selection of Target CPU, Target Board
LPC1769
(Picture of Board is provided)



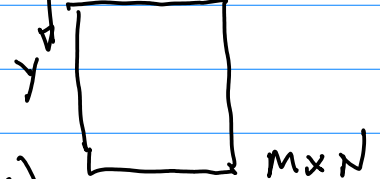
3^o Ref: 20215-106-homework

4^o Report Template
2018-10~

Discussion On Graphics

1^o Graphics
Pixel Graphics $I(x, y)$
Vertex Graphics
2D & 3D G.E.

2^o Display Device



A Scanning (Image Formation)

Start @ $(0, 0) \rightarrow$ L2R one pixel at a time, \rightarrow T2B one row at a time.

Timing Calculation

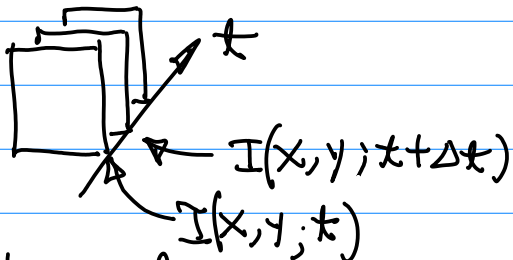
b1 Frame Rate FPS (Frame Per Second)

30 FPS

$$f_F = 30 \text{ Hz};$$

$$T_F = \frac{1}{f_F} = 33.3 \times 10^{-3} \text{ Sec.} \quad \dots (1)$$

Note: GPP PPT 2018F-107



b2 Horizontal Timing (Clock)

Given Graphics/Image with $M \times N$

$$f_H(\text{Sync}_H) = N f_F(\text{Sync}_F) \quad \dots (2)$$

b3 Pixel Timing (clock, Data Clock)

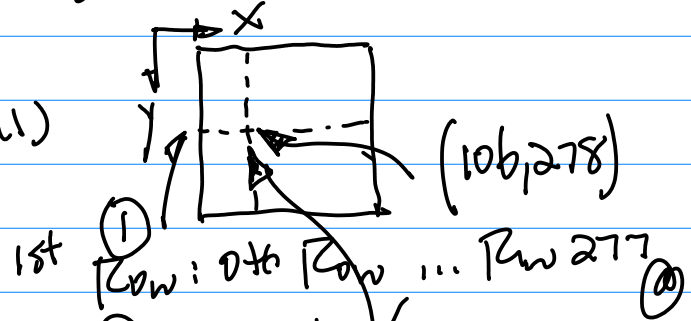
$$f_D(\text{Sync}_D) = M f_H(\text{Sync}_H) \quad \dots (3)$$

Example: Given Graphics $I(x, y)$ with 1024×768 , And find Timing for pixel $I(106, 278)$

Sol: $\text{Sync}_F = 30 \text{ Hz} (= f_F)$

$$\text{Sync}_H = N \cdot \text{Sync}_F = 768 \text{ Sync}_F$$

$$\begin{aligned} \text{Sync}_D &= M \text{ Sync}_H \\ &= 1024 \text{ Sync}_H \end{aligned}$$

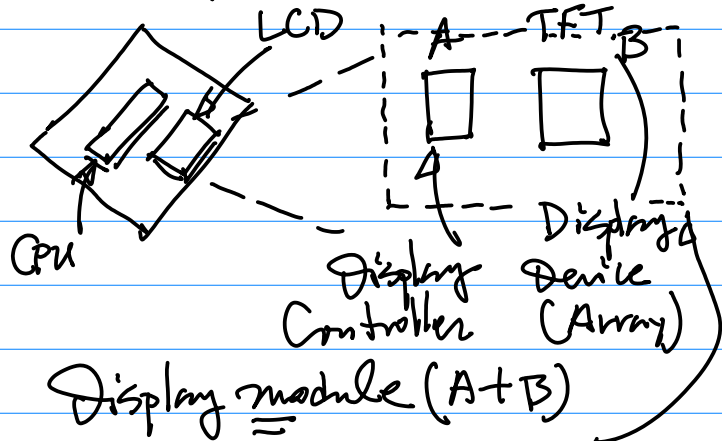


①, Beginning of Row 278
Scan 106 pixels to Reach to (106, 278), Hence $106 \frac{1}{\text{Sync}_D}$

Therefore,

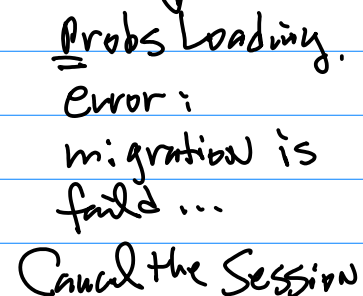
$$\begin{aligned} T &= T_{\Sigma H} + T_{\Sigma D} \\ &= 278 \frac{1}{\text{Sync}_H} + 106 \frac{1}{\text{Sync}_D} \end{aligned}$$

3rd Timing in terms of Graphics Display Controller Design.



T.F.T. Display

→ Run Debbug



SPID Controlling

March 1
Fig. 1. Sinc
Architectural Prototype
Marginalia
Chloro = vii

~~SPI~~ → ~~SPR~~ → ~~C-Code Compiler~~

C-Code Compiler → Tripartite Fig. 1.

Topics: 1^o Finish

Hardware Design (Graphics Driver)

Example: Import/Build/Debug DrawLine, Zip
Execute

Note:

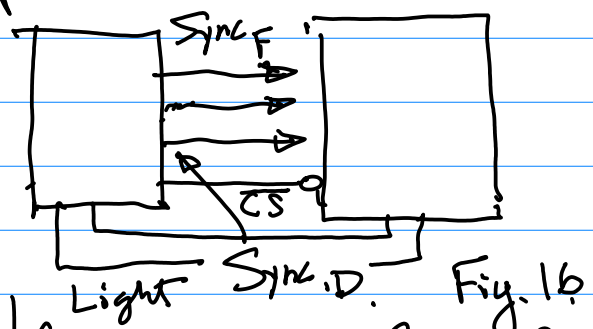
1. MCUpresso Version, 11.3.0 ✓

IDE

SDK: (LPC1769)

SDK; $\hat{=}$ No SDK for LPC1114

6 LPC1769 Pre-Built for IDE



Control Signal:
 $1^\circ nGS(\overline{CS})$

No SDK for LEC17b9

NXP
→ OpenMCU

↳ Check LPC1114
Pre-installed

Input
→ LEC17 ba
Patch.

Controller Enable

2^o Data/Command
D/ \bar{C} , or
 \bar{C}/D

Ample Build

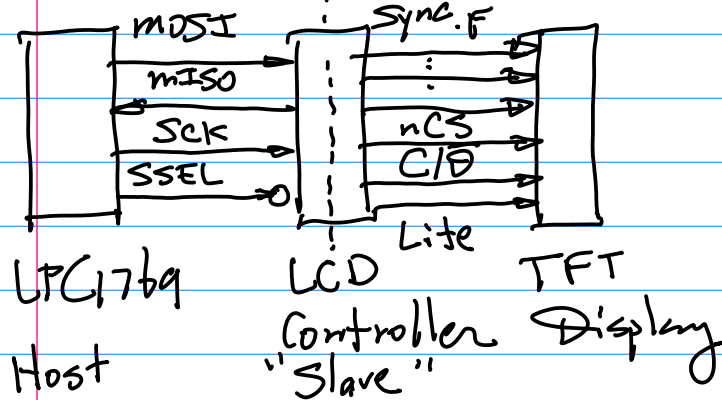
← Input DrawLine.zip

GitHub

Controller to LCD Display.

PART II:

Fig. 2



2D Graphics

Action 1. LCD Wirewrapped on the prototype Board

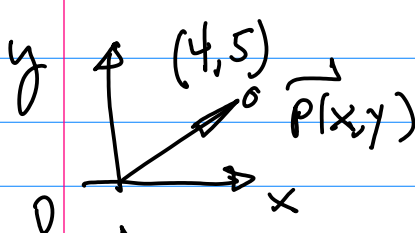
Action 2. Test DrawLine Project

Note:

1^o mathematical FormulationVectors $\vec{P}(x,y) = \vec{P} = (x,y)$

2D vector

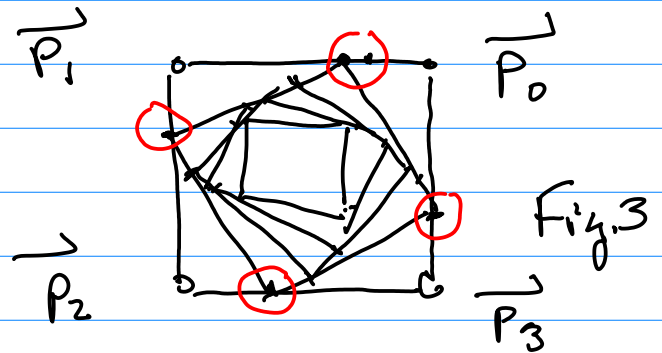
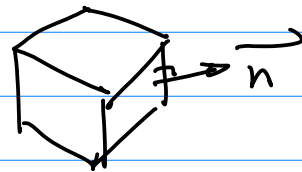
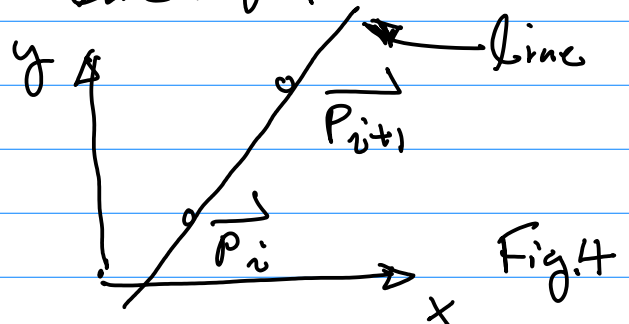
Simplified Short Hand Notation



$$\vec{P}(4,5) = (4,5)$$

2^o Generate A Screen Saver Based on G.E. (Vector Graphics)

Given a Set of vertices (Vertex)

Note: $\vec{P}_0, \vec{P}_1, \dots, \vec{P}_3$ are arranged in the Counter Clockwise Direction C.C.W.3^o Vector Representation of line a fix pt, and a direction

Define Direction Vector

$$\vec{D}(x,y) = \vec{P}_{i+1}(x_{i+1}, y_{i+1}) - \vec{P}_i(x_i, y_i) = \vec{P}_{i+1} - \vec{P}_i \dots (1)$$

Example: Given $\vec{P}_i(3,4)$, $\vec{P}_{i+1}(1.5,-1.1)$
Find Direction Vector?

Sol: $\vec{d}(x,y) \triangleq \vec{P}_{i+1}(1.5,-1.1) - \vec{P}_i(3,4)$
 $= (1.5, -1.1) - (3, 4) = (-1.5, -5.5)$

4. Define A Line Starting at \vec{P}_i
Ending (and) at \vec{P}_{i+1} ,

$$\vec{P}(x,y) = \vec{P}_i(x_i, y_i) + \lambda \vec{d}(x,y) \quad \dots (1)$$

\uparrow Arbitrary Pt. on the Line \uparrow Scaling factor \uparrow Direction Vector

$$\vec{P}(x,y) = \vec{P}_i(x_i, y_i) + \lambda (\vec{P}_{i+1}(x_{i+1}, y_{i+1}) - \vec{P}_i(x_i, y_i)) \quad \dots (1b)$$

From Eqn(1)

$$\lambda = 0, \vec{P}(x,y) = \vec{P}_i(x_i, y_i)$$

$$\lambda = 1, \vec{P}(x,y) = \vec{P}_{i+1}(x_{i+1}, y_{i+1})$$

$0 < \lambda < 1$, Pt Between \vec{P}_i and \vec{P}_{i+1}

5. See Fig. 3, P.P. 13

From Eqn(1b)

$$\vec{P}(x,y) = \vec{P}_i(x_i, y_i) + \lambda (\vec{P}_{i+1}(x_{i+1}, y_{i+1}) - \vec{P}_i(x_i, y_i)) \quad \dots (2)$$

for $i = 0, 1, 2, 3$

Introducing Super Script to Eqn (1b) for the level of iterations initially, Super Script starts at 0. One level higher.

$$\vec{P}_i^1(x, y) = \vec{P}_i^0(x_i^0, y_i^0) + \lambda (\vec{P}_{i+1}^0(x_{i+1}^0, y_{i+1}^0) - \vec{P}_i^0(x_i^0, y_i^0)) \quad (3)$$

↑ pt i @ next level, e.g. One level higher

Generalize it,

$$\vec{P}_i^{j+1} = \vec{P}_i^j + \lambda (\vec{P}_{i+1}^j - \vec{P}_i^j) \quad (4)$$

$$\vec{P}_i^{j+1}(x_i^{j+1}, y_i^{j+1}) = \vec{P}_i^j(x_i^j, y_i^j) + \lambda (\vec{P}_{i+1}^j(x_{i+1}^j, y_{i+1}^j) - \vec{P}_i^j(x_i^j, y_i^j)) \quad \dots (4-1b)$$

$$\left\{ \begin{aligned} x_i^{j+1} &= x_i^j + \lambda (x_{i+1}^j - x_i^j) \quad \dots (5a) \\ y_i^{j+1} &= y_i^j + \lambda (y_{i+1}^j - y_i^j) \quad \dots (5b) \end{aligned} \right.$$

March 3rd.

Example: Let Design A Square
By giving initial set of

Vertices (Vertices)

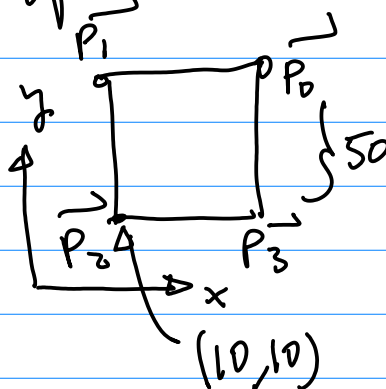
Step 1

$$\{\vec{P}_0, \vec{P}_1, \vec{P}_2, \vec{P}_3\}$$

$$\vec{P}_0(x_0, y_0) = (60, 60),$$

$$\vec{P}_1(x_1, y_1) = (10, 60),$$

$$\vec{P}_2(x_2, y_2) = (10, 10), \quad \vec{P}_3(x_3, y_3) = (60, 10)$$



Step 2. Equation(s) for all the Boundary Line

Line 1: By \vec{P}_0, \vec{P}_1

Line 2: " \vec{P}_1, \vec{P}_2

Line 3: " \vec{P}_2, \vec{P}_3

Line 4: \vec{P}_3, \vec{P}_0

$\text{mod}(3)$

Note for C/C++ Code

$$\vec{P} = \vec{P}_i + \lambda (\vec{P}_{i+1} - \vec{P}_i)$$

for line 1, 2, ..., 3. ... (1)

Note: Based Line 1, 2, ..., 3
Generate New Set of points
to form a set of Lines,

Line 1 @ one level higher

Line 2

Line 3

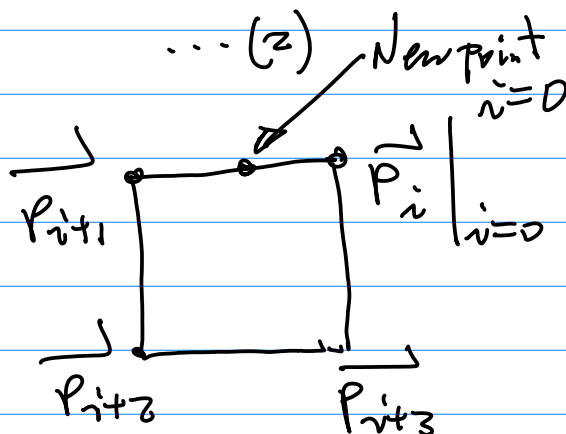
Line 4

Therefore, Eqn (1) now becomes

$$\vec{P}_{i+1}^j = \vec{P}_i^j + \lambda (\vec{P}_{i+1}^j - \vec{P}_i^j)$$

Note! for $j=0$.

for $i=0$
=



$$\vec{P}_0' = \vec{P}_0 + \lambda (\vec{P}_1 - \vec{P}_0) \quad | \quad \lambda = 0.2$$

Due to the Design
in Fig 3, PP. 13

From the given Condition

$$\vec{P}_0 = (60, 60), \vec{P}_1 = (10, 60)$$

Note $\vec{P}_0(60, 60), \vec{P}_1(10, 60)$

$$(x'_0, y'_0) = (60, 60) + 0.2((10, 60) - (60, 60))$$

$$= (60, 60) + 0.2(-50, 0)$$

From Eqn (5-b)

$$x'_0 = 60 + \lambda * (-50)$$

$$y'_0 = 60 + \lambda * 0$$

$$x'_0 = 60 + 0.2 * (-50)$$

$$y'_0 = 60 + 0.2 * 0$$