ARM11 Memory Map

Start Address	End Address	Int. ROM	Stepping Stone (NAND Ctrl.)	SROM Ctrl.	One NAND Ctrl. 0	One NAND Ctrl. 1	DRAM Ctrl 1
0x00000000	0x07FFFFFF	O[1]	-	O[1]	O[1]	-	-
0x08000000	0x0BFFFFFF	O	-	-	-	-	-
0x0C000000	0x0FFFFFFF	-	O	-	-	-	-
0x10000000	0x17FFFFFF	-	-	O	-	-	-
0x18000000	0x1FFFFFFF	-	-	O	-	-	-
0x20000000	0x27FFFFFF	-	-	O[2]	O[2]	-	-
0x28000000	0x2FFFFFFF	-	-	O[2]		O[2]	-
0x30000000	0x37FFFFFF	-	-	O	-	-	-
0x38000000	0x3FFFFFFF	-	-	O	-	-	-
0x40000000	0x47FFFFFF	-	-	-	-	-	-
0x48000000	0x4FFFFFFF	-	-	-	-	-	-
0x50000000	0x5FFFFFFF	-	-	-	-	-	O
0x60000000	0x6FFFFFFF	-	-	-	-	-	O

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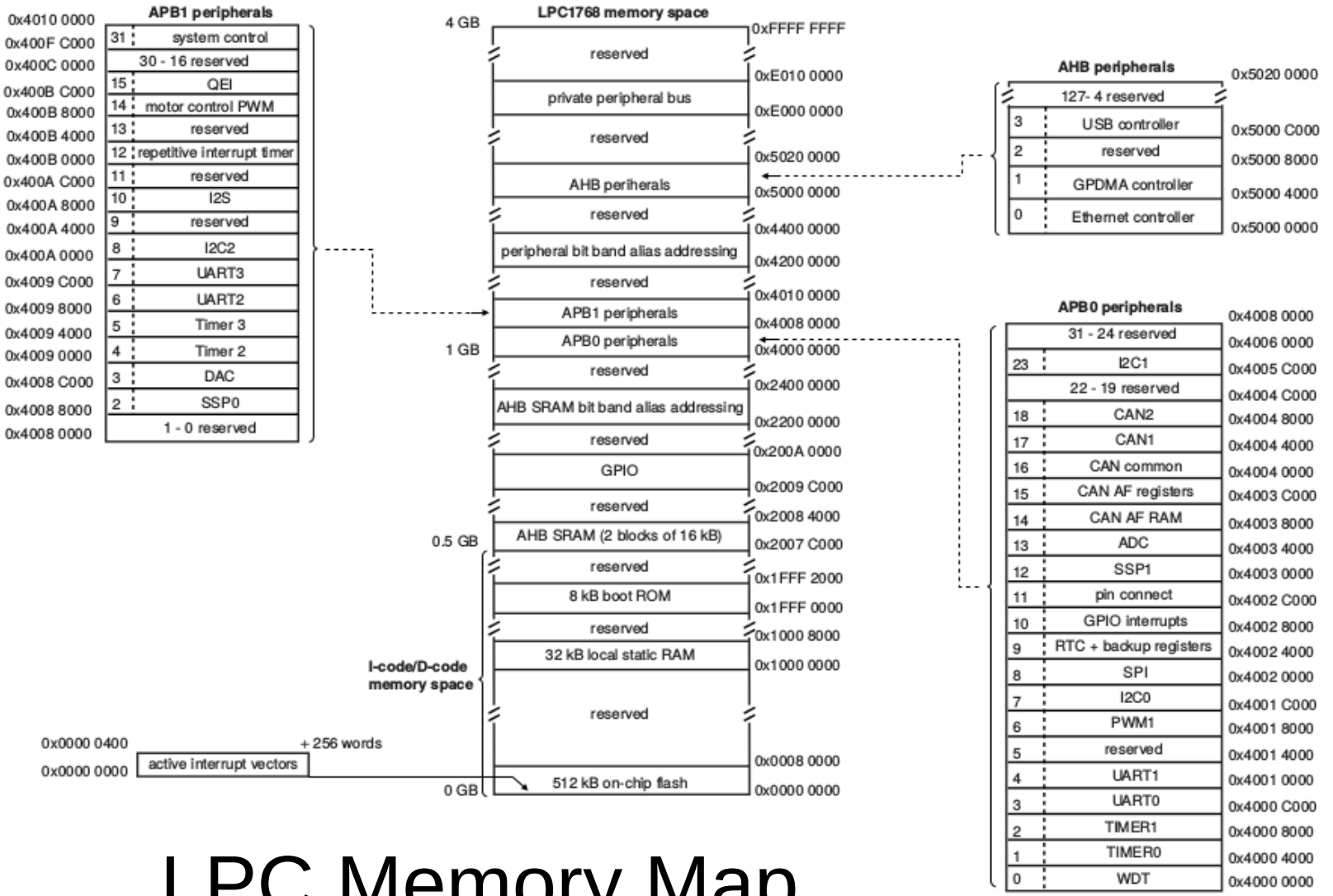

LPC Memory Map

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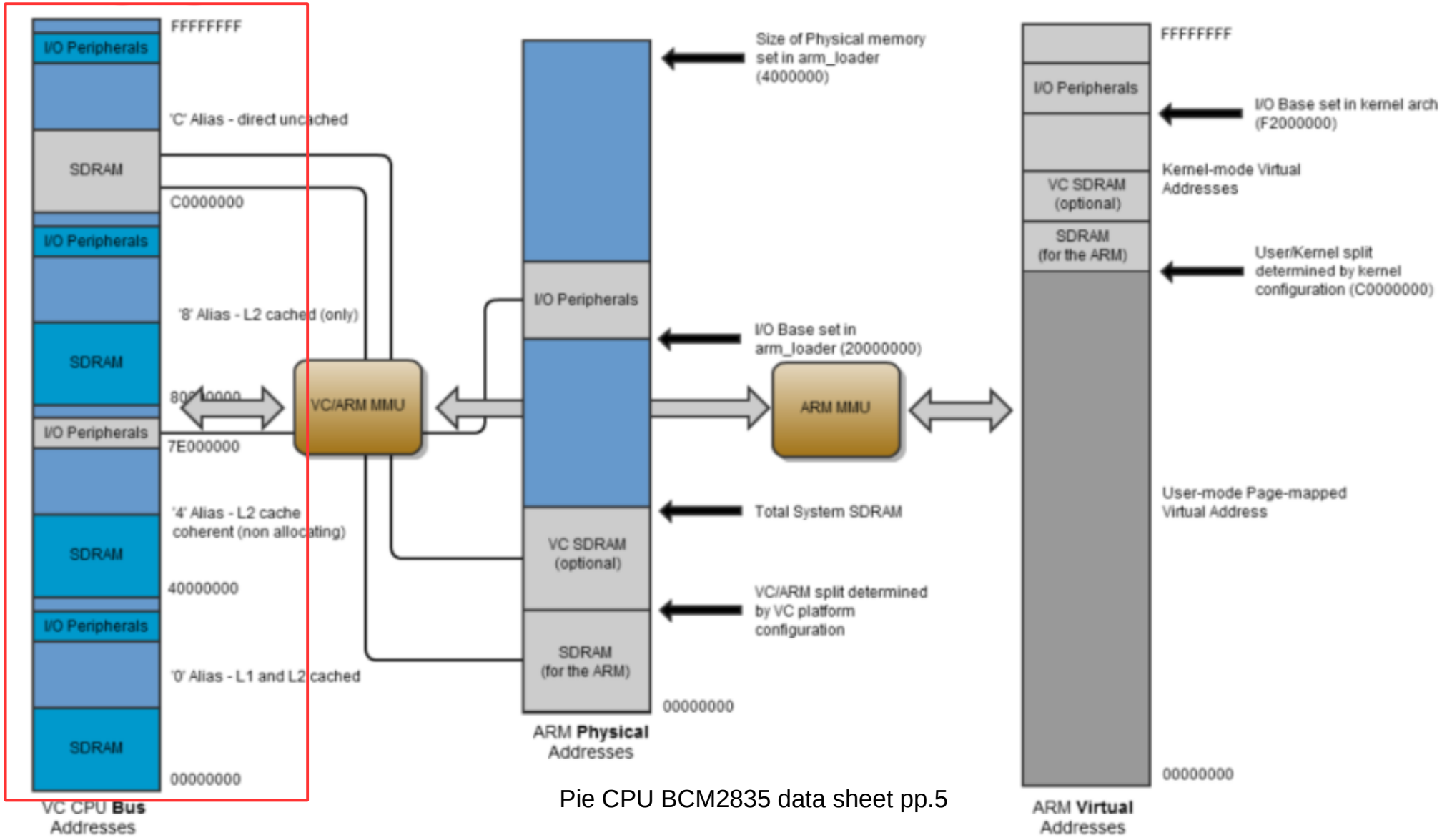

Pie CPU BCM2835 data sheet pp.5

Video Core

https://en.wikipedia.org/wiki/VideoCore

SoC	GPU		CPU				Max display	Utilizing devices
	Microarchitecture	Freq. (MHz)	Instruction set	Microarchitecture	Cores	Freq. (MHz)		
BCM2835	VideoCore 4	250	ARMv6	ARM1176	1	700	Full HD 1080p	**List** [show]

Base	Top	Attr.	Description	Notes
0x0000_0000	0x0000_00FF		Reserved	Debug Address Space
0x0000_0100	0x0000_0FFF	RWX A	Debug	
0x0000_1000	0x0000_1FFF	R X	Mode Select	On-Chip Peripherals
0x0000_2000	0x0000_FFFF		Reserved	
0x0001_0000	0x0001_7FFF	R X	Mask ROM (32 KiB)	
0x0001_8000	0x00FF_FFFF		Reserved	
0x0100_0000	0x0100_1FFF	RWX A	E51 DTIM (8 KiB)	
0x0100_2000	0x017F_FFFF		Reserved	
0x0180_0000	0x0180_1FFF	RWX A	E51 Hart 0 ITIM (8 KiB)	
0x0180_2000	0x0180_7FFF		Reserved	
0x0180_8000	0x0180_EFFF	RWX A	U54 Hart 1 ITIM (28 KiB)	
0x0180_F000	0x0180_FFFF		Reserved	
0x0181_0000	0x0181_6FFF	RWX A	U54 Hart 2 ITIM (28 KiB)	
0x0181_7000	0x0181_7FFF		Reserved	
0x0181_8000	0x0181_EFFF	RWX A	U54 Hart 3 ITIM (28 KiB)	
0x0181_F000	0x0181_FFFF		Reserved	
0x0182_0000	0x0182_6FFF	RWX A	U54 Hart 4 ITIM (28 KiB)	
0x0182_7000	0x01FF_FFFF		Reserved	
0x0200_0000	0x0200_FFFF	RW A	CLINT	
0x0201_0000	0x0201_0FFF	RW A	Cache Controller	
0x0201_1000	0x0201_FFFF		Reserved	
0x0202_0000	0x0202_0FFF	RW A	MSI	
0x0202_1000	0x02FF_FFFF		Reserved	
0x0300_0000	0x030F_FFFF	RW A	DMA Controller	
0x0310_0000	0x07FF_FFFF		Reserved	
0x0800_0000	0x09FF_FFFF	RWX A	L2 LIM (32 MiB)	
0x0A00_0000	0x0BFF_FFFF	RWXCA	L2 Zero device	
0x0C00_0000	0x0FFF_FFFF	RW A	PLIC	
0x1000_0000	0x1000_0FFF	RW A	PRCI	
0x1000_1000	0x1000_FFFF		Reserved	
0x1001_0000	0x1001_0FFF	RW A	UART 0	
0x1001_1000	0x1001_1FFF	RW A	UART 1	
0x1001_2000	0x1001_FFFF		Reserved	
0x1002_0000	0x1002_0FFF	RW A	PWM 0	
0x1002_1000	0x1002_1FFF	RW A	PWM 1	
0x1002_2000	0x1002_FFFF		Reserved	RISC-V pp. 30
0x1003_0000	0x1003_0FFF	RW A	I2C	
0x1003_1000	0x1003_FFFF		Reserved	
0x1004_0000	0x1004_0FFF	RW A	QSPI 0	
0x1004_1000	0x1004_1FFF	RW A	QSPI 1	
0x1004_2000	0x1004_FFFF		Reserved	
0x1005_0000	0x1005_0FFF	RW A	QSPI 2	
0x1005_1000	0x1005_FFFF		Reserved	
0x1006_0000	0x1006_0FFF	RW A	GPIO	
0x1006_1000	0x1006_FFFF		Reserved	
0x1007_0000	0x1007_0FFF	RW A	OTP	
0x1007_1000	0x1007_FFFF		Reserved	
0x1008_0000	0x1008_0FFF	RW A	Pin Control	
0x1008_1000	0x1008_FFFF		Reserved	
0x1009_0000	0x1009_1FFF	RW A	Ethernet MAC	
0x1009_2000	0x1009_FFFF		Reserved	
0x100A_0000	0x100A_0FFF	RW A	Ethernet Management	
0x100A_1000	0x100A_FFFF		Reserved	
0x100B_0000	0x100B_3FFF	RW A	DDR Control	
0x100B_4000	0x100B_FFFF		Reserved	
0x100C_0000	0x100C_3FFF	RW A	DDR Management	
0x100C_4000	0x17FF_FFFF		Reserved	
0x1800_0000	0x1FFF_FFFF	RW CA	Error Device	
0x2000_0000	0x2FFF_FFFF	R X A	QSPI 0 Flash (256 MiB)	Off-Chip Non-Volatile Memory
0x3000_0000	0x3FFF_FFFF	R X A	QSPI 1 Flash (256 MiB)	
0x4000_0000	0x5FFF_FFFF	RWX A	ChipLink (512 MiB)	ChipLink
0x6000_0000	0x7FFF_FFFF	RWXCA	ChipLink (512 MiB)	
0x8000_0000	0x1F_FFFF_FFFF	RWX A	DDR Memory (126 GiB)	Off-Chip Volatile Memory
0x20_0000_0000	0x2F_FFFF_FFFF	RWX A	ChipLink (64 GiB)	ChipLink
0x30_0000_0000	0x3F_FFFF_FFFF	RWXCA	ChipLink (64 GiB)	

Table 6: FU540-C000 Memory Map. Memory Attributes: **R** - Read, **W** - Write, **X** - Execute, **C** - Cacheable, **A** - Atomics

Boot Sequence RISC-V

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