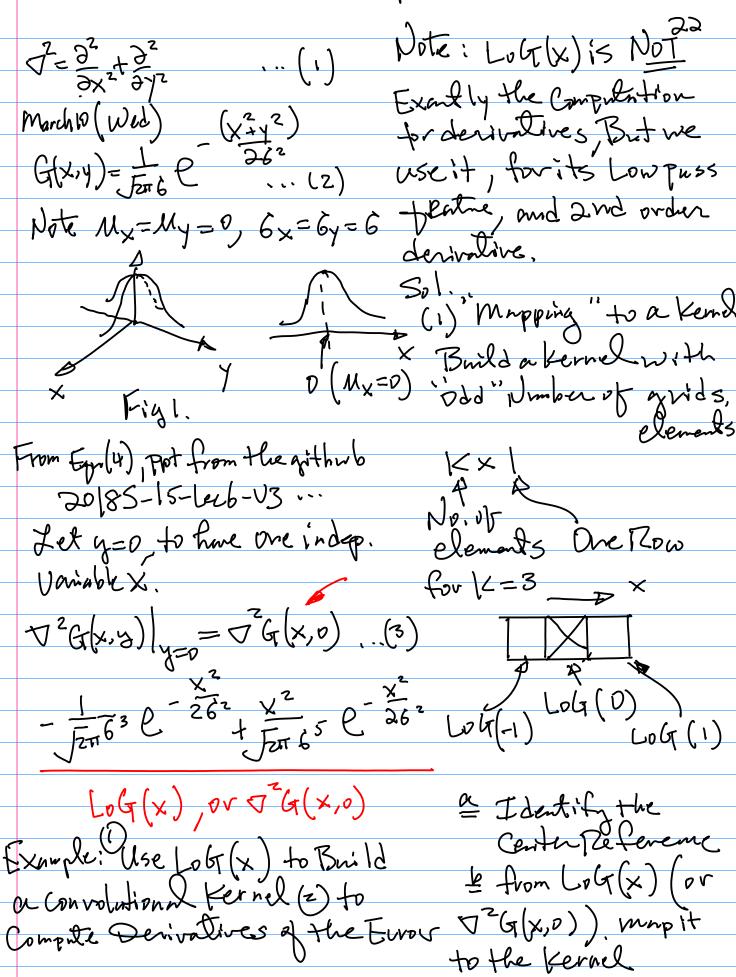
CMPEZYZ



Note CFG/CON are responsible Solve fory for Setting Rescalar Divider Driven Implementation. $f_{TWM} = \frac{50 \times 10^{b}}{}$ 20185-10-0~ (Prest). Div. PWM Driver Add Data Cycle Function to If we need from = 2×103 Device Oniver Find SPR, Set SPR. to Renlize Theoretical Aspect this frequency.) Implementation Code, From PUDatasheet CFGD

Sol 2x10 = 50x106 Toot Control Reg. Counter Rey. (Prest) Div · Compare Regi CFGO Timer $(p_{res+1}) \mathcal{D}_{iv} = \frac{50 \times 10^{b}}{2 \times 10^{3}}$ Two astrat Square Waveform Prest1) Div. = 25×103 T CMPB Let Div=16, Solve Por Pres. Prest1 = 25 x103 Trum= / Pwm $Pres = \frac{25 \times 10^3 - 16}{16} \approx 2$ CLYP + PWM = (Frescher+1) (divider) Iteration, PP 1118, CELL Datasheet Change PCLK to 10mHz, then, we have Mescaler: 8 bit, [0,255]

Drvider; 1,2,4,8,16

CMPE/FEDY2

Pres = 10×10 -16×7×103 if it is still Arem | Datasheet

16×2×103 tooloign | TCNTB - N Counts

therefore, then Low the CLYp TCMPB frum

try CLKp = 2×106. please veriby it | Zol85-10frechtrum= N ...(1) Note: SPR Responsible for CTWM Define one period; TONTB Timer Rost Buffer Duty Cycle - 2 1/0 - 2 Counts
Percentage of
Omp
Omp from= | x103 given. f moster Clock peripher al N Counts for OUT SPR. F= Fpwm. N. ... (4)

Briben Target Unknown to be
Calculated GPFCON [29:28] = LO -> PWM GPFGN[31:30]=10+0 pwm # define S3Cbyxx_ GPICON Note: T CMP B Tomparison Register 4.h 4= ~(0x3u << 28) for Duly Cycle 'AND" Deg" 2nd Counts Value For "Comp" Derived from Duty Cycle.

March 17 (Wed) from By Setting SPR'S "DR" "10" un Signed

Duty Cycle Value GPFCON (29: 28) = 10

29 March 2 Shd (Mon) S Imput Testing CKT Review. Owfort Testing CKT Resistance Unhae Calculation 1° 3± Queotians. a Basic Concepts, CPU Arch: Feature & Theoretial Aspects Block Dingram. Memory Map. Peripherial Controllers C1. PID Controller Design Pask Concepts

Block Diagram.

X(*) E(t) 2 P 5 Fig. 1

CZ A- 21 D Central

Kennels F.D. 2x1 D Central GPP (GPID) & SPRS DAT TCNTB TCNPB TCMPB CFGØ, I Architecture -> Mem -> SPR B.D. 2X1 (F.D+BD) Code ad

Juser Same

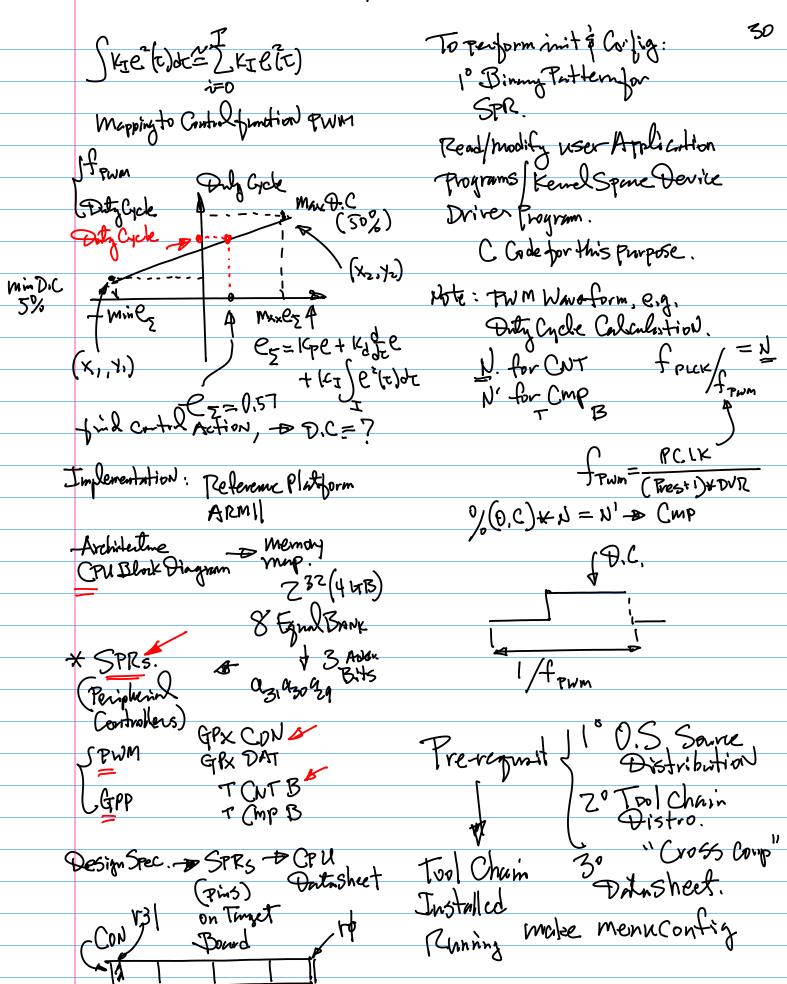
programming

Kernel Spine

Device Driver With Noise Reduction 3x1 LOW Priss Filter: G(x) Gaussian 1 2nd Order Derivation as in Computer Vision

72: Laplacian 32+22 - 22

Coff(x) Define Compilation + Build Process Programming Reginarents, No Frogram
Code
Writing
Debry Change the
existing Gode is Needed; Note: One page form la sheet is Allowed, However No Verbal & Deing Related Question (5) Description Andlor Eugles Allowed Note: Chulatro IS Allowed. SCH. Design, CKT for TWM Close Book, Close Notes Pin(5), fpm [GPID motor Drive Datasheets if needed will be Pin(s), Label(s) Stepper motor I/F provided; Convolution with Kernel(S)
Table of E(t), bind JeE(t) Convolution GPP I/O Testing (Hello, the World)



242 Continued & Kconf (at drivers

to Char) Script. Add your Device Driver Duly Cycle
MAN D.C

R (80%) make menu combig involk your Change, Campile & Brite (Module Duly for (, K, , X) Simplicity Purpose) Object "Ko" Cory USB" hplood insmod mytest. Ko (To make)
it as a put of Kernel Image) run your user application Frogram (By Colling the module)

ttps://github.com/hualili/qMRE3#3-Embedded-Systems-/blob/master/20189-16-AngularSensing-i2c

JWDE/FE373

April 5th (Monday 1. midterm Graded, theky was on line, github, search im 20195, " Key

ali onlin v / Jenen

Sensors for Driving Direction and **Turning Angle**

eCompass module:

3D accelerometer and 3D magnetometer



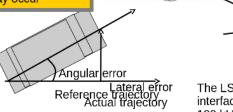
Use LSM303 or equivalent to sense the direction of the vehicle

Actual trajectory

Note: Next Project

USE 1 Sm303

Caution: Steering sensor input is not necessarily the real angle of the vehicle, "skipping" may occur



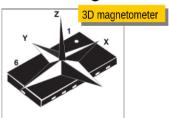
The LSM303DLHC includes an I 2 C serial bus interface that supports standard and fast mode 100 kHz and 400 kHz. The system can be configured to generate interrupt signals by inertial wake-up/free-fall events as well as by the position of the device itself.

Angular error

larry Li, Ph.D. April 2015

Reference trajectory

3D Accelerometer and 3D Magnetomete LMS303



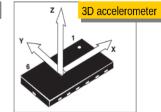


Table 9 Pin name Pin description I2C serial clock (SCL) I²C serial data (SDA)

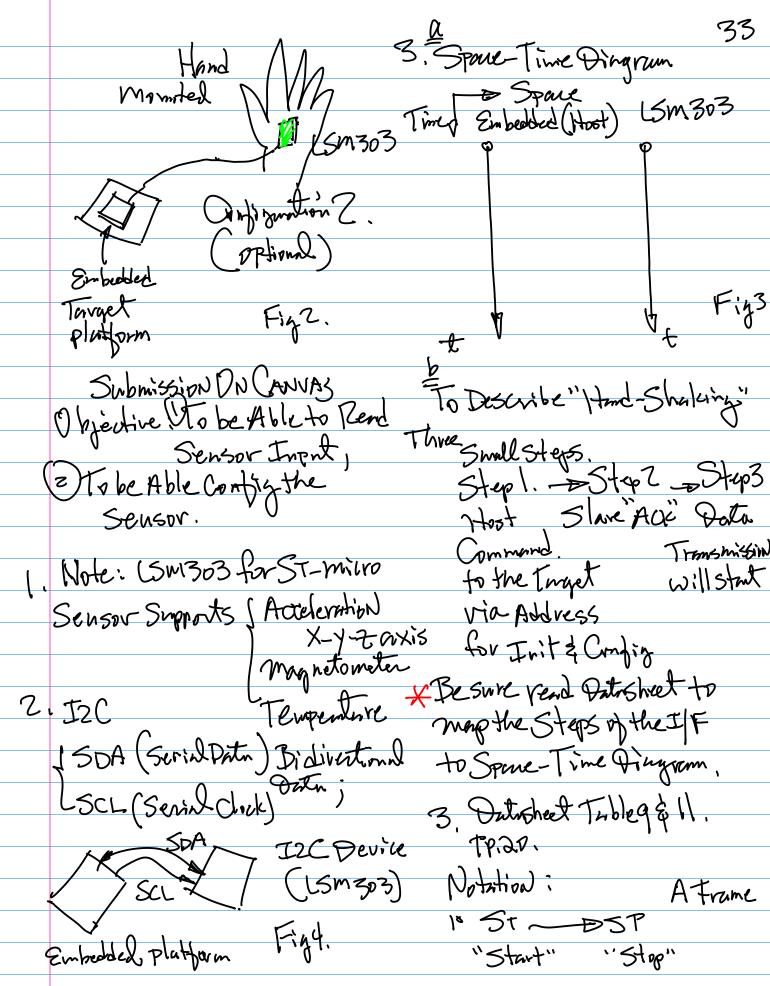
I2C Interface

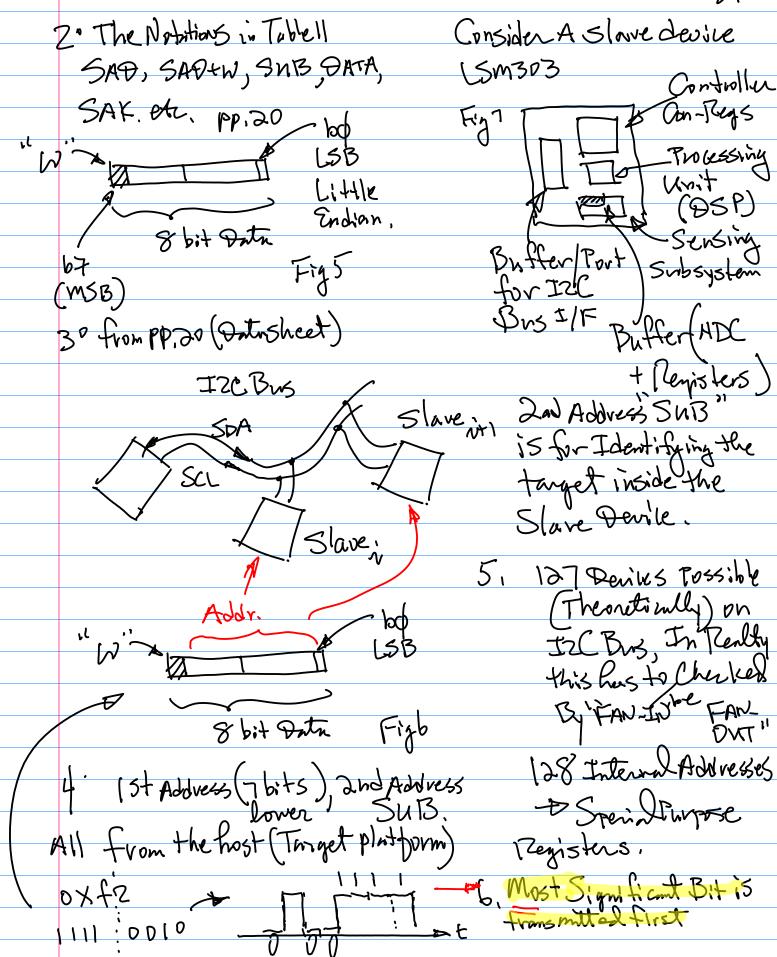
(1) The transaction started through a START (ST) signal, defined as a high-to-low on the data line while the SCL line is held high. (2) After ST, the next byte contains the slave address (the first 7 bit), bit 8 for if the master

is receiving or transmitting data.

SM 303 Sensor . Due April lb

CMFE/EEDY2





CMPE/EEDY2

Example: From Datosheet (SM303) TP.19 Table 11,12,13 Homework (IPt) Due Aweek from Today, April 14, One On CANVAS 1º Build IZC Bus Interfree with your target platform as a host, 15 m 303 slave. To be able: a kondware Implementation (e.g., mont [5m303 on the Stype motor, Or mount it to you & Trad Acceleration Onto X, Y, Z., Displayit on you terminal. & Rend magnetometer Date and display it on the terminal Note: Sample code is posted 11 as 15" basis. Repo: 20-20215-10-16m Z° Submission of Source Code, & Readnetxt

[photo(s) of your Inglementation 3xphotos, I for the entire System (with Laptop); 2 tor the Host Side, Expansion Connection is the focus ; To hat Stationary 15t Steps. SM303 motor

Option 2. \$ 5 seconds Video Clip(s) 720p or 10807 (1920×1280) Compressed, MPEGY, avi file Naming: first Name 4 Divits_ 242. Zip Note: Tablell & 12 (PP/a)

One Byte Whiting - > Miltiple Writing Tech Spec:

Host 10. 400 Hz Di

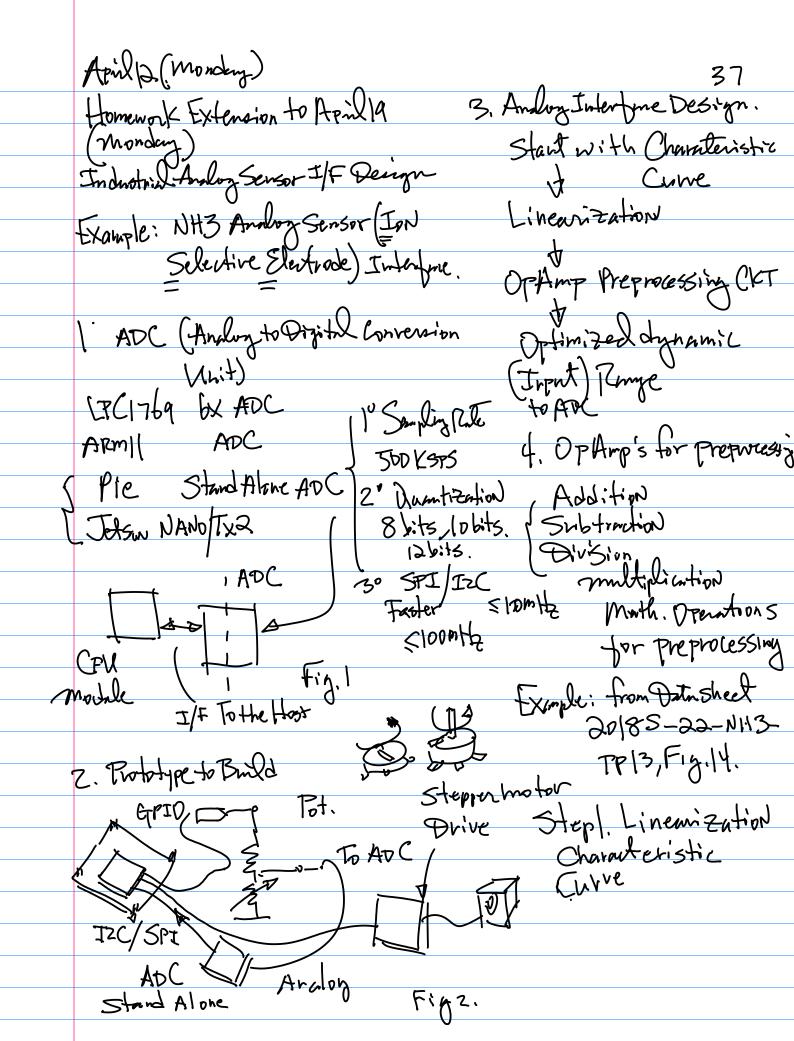
Table (Lonical Behavior) 71. X-Y Cox 10. 400 Hz Data Pate 11 X-Y DIXIS, 991. Sensor Autive (No LOW POWE) Timing (Wave from) CTRL_PEGI_A [3]=0 XIX CTRL_REGI_A [2]= 0 CTRL_PEGI_A [1]=1 CTRL_PEGI_A [D]=1 Now, the Address for the Sensor (5) and Addresses for Registers 0X3 J Control Register — Init & Confrago Heme, CTRL_PEGI_A [7:0] = SADT:] Address + SAD[] for W/R 0×13 V J=1 forw L=0 frr R Section 7.1. 8 Status Note: Use info from Tuble 14 Registers to fill in SAD+W, SAD+R Section 7.1,927,1,11 in tables 11~13, Data Registas. ZIS Complement form Note: Section 51/13 Maynetometer Table 18. Control Penjoder A

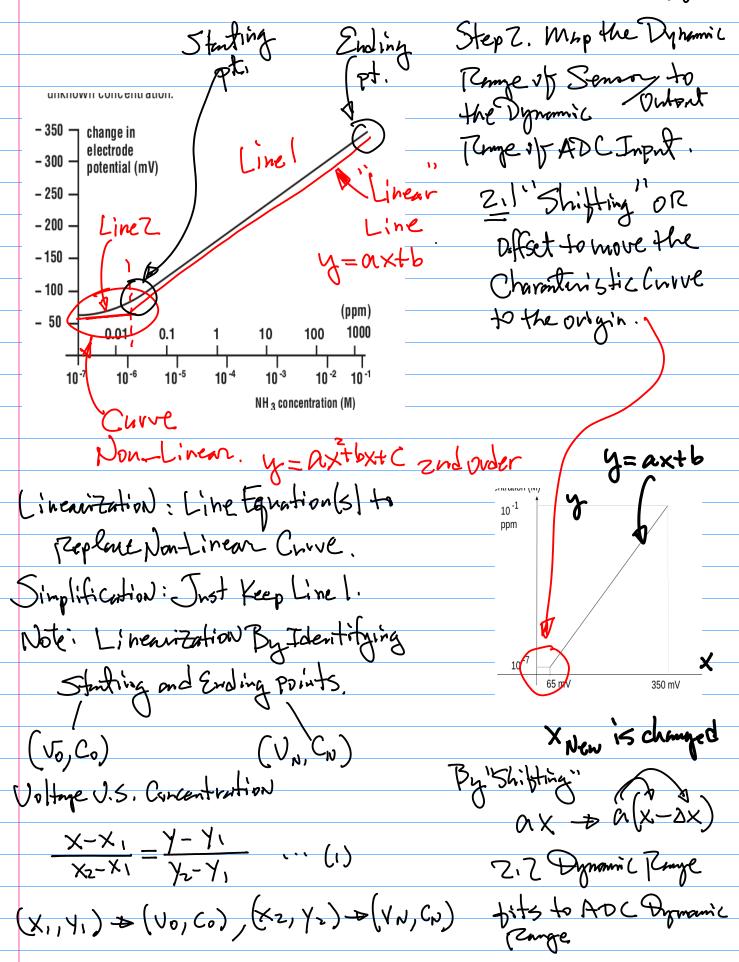
Table 18. Complement

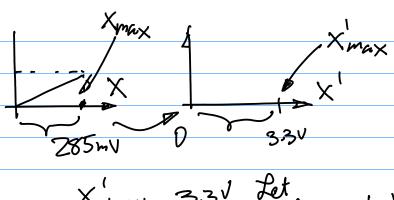
For Magnet CTRL REGI - A [7:0] 8 bits. By Negrotion

CTRL REGI - A [7:4] = 0×7

(for 11 wo Hz) + 1 Example: Table 8. Control Register A CTRLREGI_A[7:4]=0X7 Tech Spec Binny Pattern (for 4 wo Hz) + 1







× max = 3,31 fet × max 0 1285 Gain ("Scaling Fontor")

Review of Foresting Configuration optimps
OPAMP L. Non-Investing Configuration