Jan 27, 21

Welcom to

CMPE242 Harry Li

Embedded Hardware Systems

1. Green Sheet github/hwalili/cmpe242

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2. Pre-requist Requirements 180A & D

Course Description

Hands-ON.

Target Development platform

200

ARM7, 9 — Broadcom Pie3B+ Pie4 ~$60 Edge AI — High Performance platform NVDA

NXP LPC 17xx

Samsung ARM11 ~10yrs 800mHz Linux Kernel O.S. Open Source

① NANO ~$60

② TX2 ~$400 + $150 ~ $350

③ TX1 ~$399

Basic Material

Scope of the Course { Device Driver Development C/C++, Python; O.S. Kernel

Before: 3 Labs/Projects

Device Driver Sensor LSM303 → Feed Back Loop

I/F to Target Board → Human Readable file.

P.I.D Controller

Convolution

Integration (HDL)

Optional subjects

1° RISC-V Project — FPGA

Device Driver Development — O.S. Kernel Image

2° ROS (Robotics Operating System) platform Visualization Tool.

* Grading Policy

3-3-4

mid Projects ← Final

* CANVAS — EE242

① Assignments (NO)

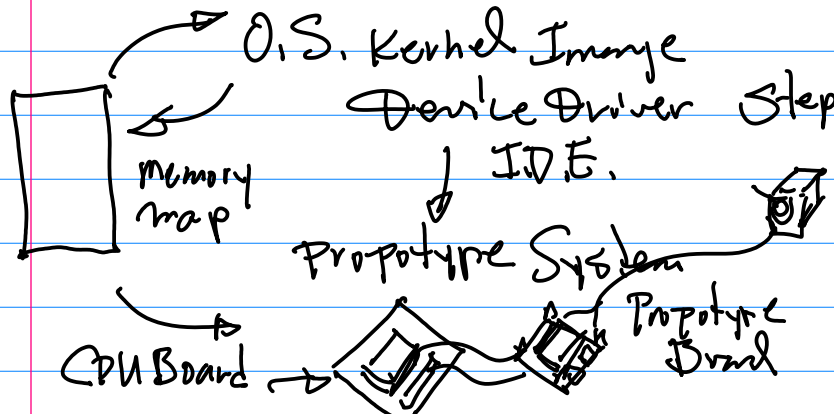
② Collection / Submission of your class work

Action 1. github/hwalili/cmpe242

2. Datasheet

{ Samsung ARM11 Datasheet
NXP LPC1769 Datasheet

Architecture NXP LPC 17xx



Action 3. Target Platform Selection of Unix-Like OS. 6) Edge AI Computing (Scalability) ⇒ GPU

Office Hours M.W. 4:30-5:30pm ON Zoom.

CMPE242 Feb1. 2021

Today's Topics: 1° System Architecture Review, CPU Datasheet; 2° Target platform

System Architecture

NVDA CPU/GPU platform. { NANO TX1, TX2 }

BroadCom, Pi 2/3/4 G.E. (Graphics Engine)

Samsung ARM 11 (9,7)

Optional Architecture RISC-V

Common Characteristics RISC

Reduced Instruction Set Computer

Optimization Not Only on the Hardware But On the Compiler Design, and System Software Design.

MIPS, ARM (Most Widely Adopted) RISC

ARM Architecture ——— Common Core

Base Line Hardware (Datasheet): ARM11

Base Line Software { O.S. (Kernel Aspects, Device Drivers.)

Linux Distribution Optimized for Embedded platform

Example: Datasheet LPC1768 ARM Cortex M3

Samsung ARM-11

NVDA ... PiEX

CPU Datasheet, LPC1769 20185-3-UM10360, PP. 9

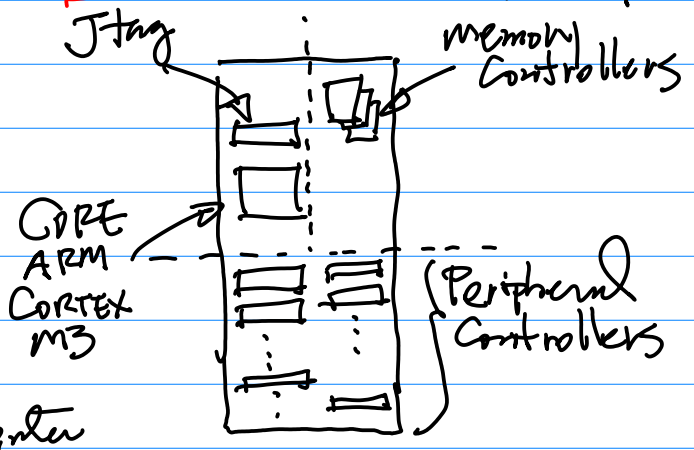


Fig1. CPU Architecture ARM Cortex M3

Note: To Be Able to Draw/Design CPU Architecture Ether this OR Your Target platform. (176a + ARM11) Base Line

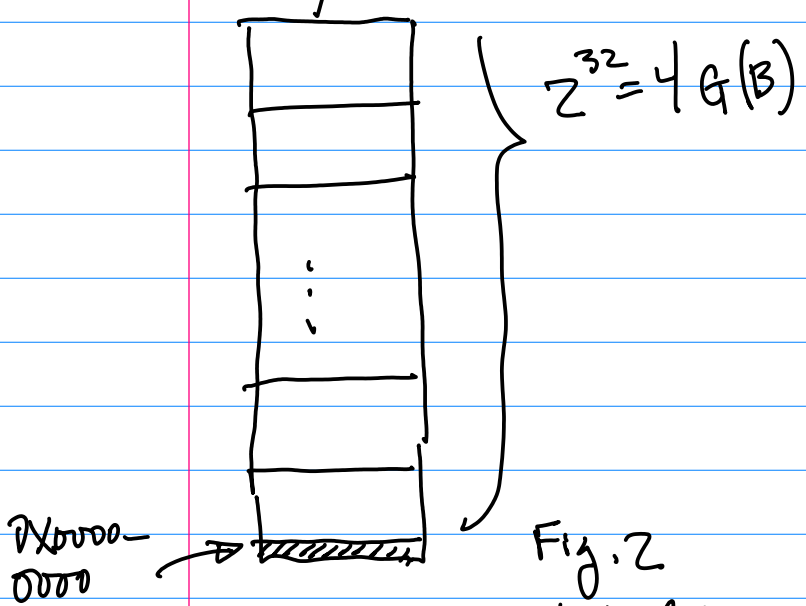


Fig. 2

① 32 Bit RISC Architecture

$2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2}$

$= \underbrace{1K \cdot 1K}_{1M} \cdot 1K \cdot 2^{2}$

$= 4\,GB \quad (1G\ Byte)$

② Byte Addressable Machine

~ whose minimum memory cell with an unique Address is a Single Byte

③ Memory Banks, 8 BANKS

Size of Each Bank: $4GB/8$

$= 2^{32}/2^{3} = 2^{32-3} = 2^{29} = 2^{9} \cdot 2^{20}$

$= 512\,MB$

Starting Address of Each Bank

Question: How many Bits needed to define the Starting Address of Each Bank? $\underline{3}$ bits, $2^3 = 8$

3 bits Needed

$a_{31}\ a_{30}\ a_{29}\ a_{28} \cdots a_1\ a_0$

Little Endian

ARM CPU can be configured at Boot Stage as either "Little Endian" or "Big Endian".

Find Starting Address for the 1st BANK:

$a_{29} = a_{30} = a_{31} = 0$

a_{28} has to be added, to form a Hex

0X0000_0000

2nd Bank's Starting Address

$a_{31}\ a_{30}\ a_{29}\ a_{28}$

0 0 1 0

0X2000_0000

3rd Banks Starting Address

$a_{31}\ a_{30}\ a_{29}\ a_{28}$

0 1 0 0

0X4000_0000

Now, Consider target Board

Conditions to qualify the selection

① ARM Based ; ② UNIX-Like O.S.

③ Establish
eco-system
Developer Base (~millions)
Linux { kernel, Image, Source Distro., Tool Chain

④ Technology Innovations / Leaders.

⑤ External Expansion Connectors