Jan 27, 21

Welcom to

CMPE242 Harry Li

Embedded Hardware Systems

1. Green Sheet github/hualili/cmpe242

E-mail: hua.li@sjsu.edu

(650) 400-1116 Text message

2. Pre-requist Requirements 180A & D

Course Description

Hands-ON.

Target Development platform

200

ARM7, 9 — NXP LPC 17xx

Samsung ARM11 ~10yrs 800mHz Linux Kernel O.S. Open Source

Broadcom Pie 3B+ Pie 4 ~$60 Edge AI

High Performance platform

NVDA

① NANO ~$60

② TX2 ~$400 + $150 ~ $350

③ TX1 ~$399

Basic Material

Scope of the Course { Device Driver Development C/C++, Python; O.S. Kernel

Before: 3 Labs/Projects

Device Driver — Sensor LSM 303 — I/F to Target Board. — Human Readable file. → Feed Back Loop P.I.D Controller Convolution

Optional subjects — Integration (HDL)

1° RISC-V Project — FPGA

Device Driver Development — O.S. Kernel Image

2° ROS (Robotics Operating System) platform Visualization Tool.

* Grading Policy

3-3-4 mid Projects ← Final

* CANVAS — EE242

① Assignments (NO)

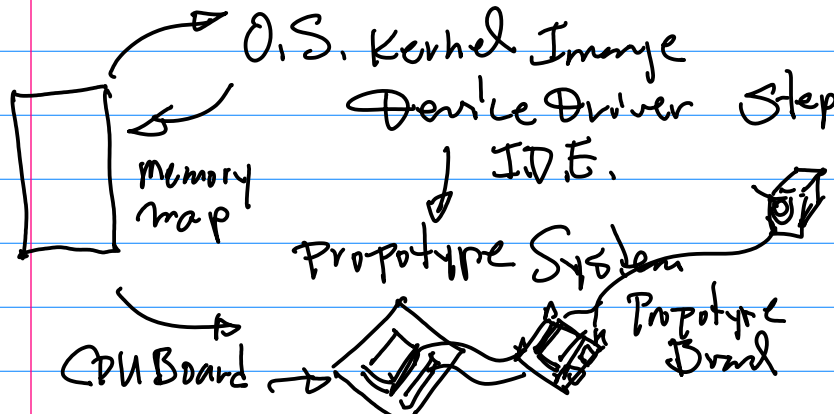
② Collection/Submission of your class work

Action 1. github/hualili/cmpe242

2. Datasheet

{ Samsung ARM11 Datasheet
NXP LPC1769 Datasheet

Architecture NXP LPC 17xx



Action 3. Target Platform Selection of Unix-Like OS. 6) Edge AI Computing (Scalability) ⇒ GPU

Office Hours M.W. 4:30-5:30pm ON Zoom.

CMPE242 Feb1. 2021

Today's Topics: 1° System Architecture Review, CPU Datasheet; 2° Target platform

System Architecture

- NVDA CPU/GPU platform. { NANO, TX1, TX2 }
- BroadCom, Pi 2/3/4 G.E. (Graphics Engine)
- Samsung ARM11 (9,7)

Optional Architecture RISC-V

Common Characteristics RISC

Reduced Instruction Set Computer

Optimization Not Only on the Hardware But On the Compiler Design, and System Software Design.

MIPS, ARM (Most Widely Adopted) RISC

ARM Architecture ——— Common Core

Base Line Hardware (Datasheet): ARM11

Base Line Software { O.S. Kernel Aspects, Device Drivers.

Linux Distribution Optimized for Embedded platform

Example: Datasheet LPC1768 ARM Cortex M3

Samsung ARM-11

NVDA ... PiEX

CPU Datasheet, LPC1769 20185-3-UM10360, PP. 9

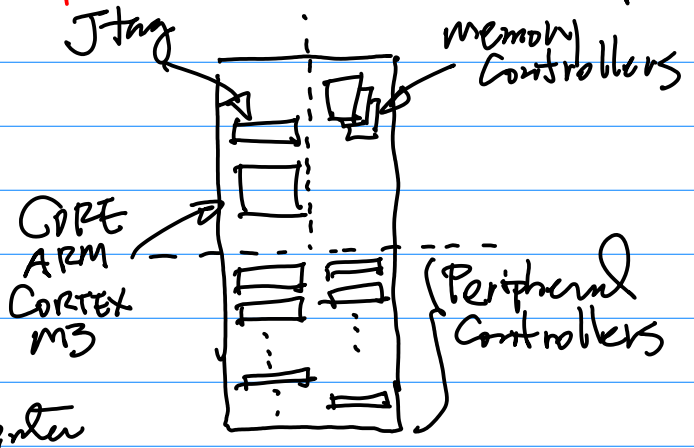


Fig1. CPU Architecture ARM Cortex M3

Note: To Be Able to Draw/Design CPU Architecture Ether this OR Your Target platform. (176a + ARM11) Base Line

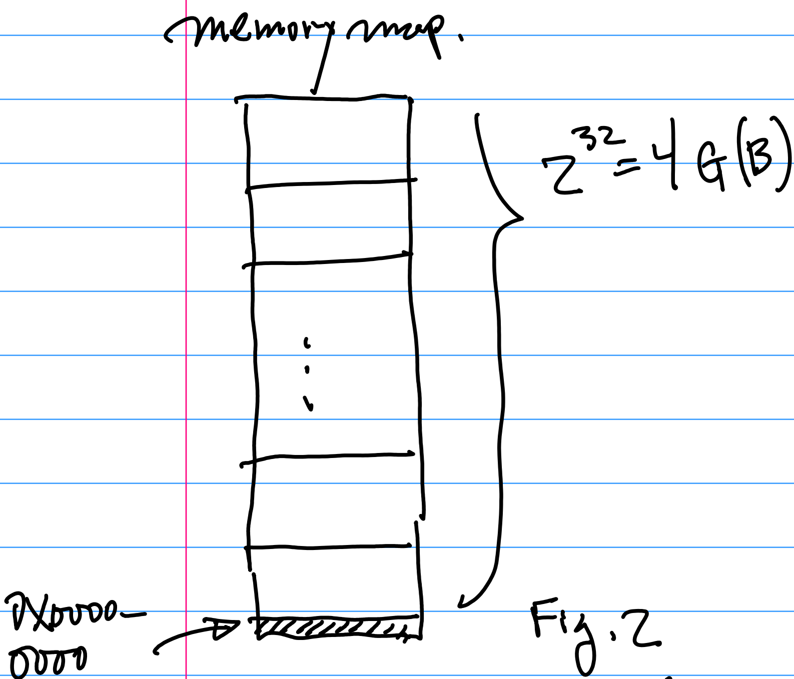


Fig. 2

① 32 Bit RISC Architecture

$2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2}$

$= 1K \cdot 1K \cdot 1K \cdot 2^{2}$ (1K · 1K = 1M, 1M · 1K = 1G)

$= 4$ GB (Byte)

② Byte Addressable Machine
~ whose mimium memory Cell with an unique Address is a Single Byte

③ memory Banks, 8 BANKS
Size of Each Bank : 4GB/8

$= 2^{32}/2^{3} = 2^{32-3} = 2^{29} = 2^{9} \cdot 2^{20}$

$= 512$ MB

Starting Address of Each Bank

Question: How many Bits needed to define the Starting Address of Each Bank? 3 bits, $2^3 = 8$

3 bits Needed

$a_{31}\, a_{30}\, a_{29} \,\vdots\, a_{28} \cdots a_1\, a_0$

(a_0 ← Little Endian)

ARM CPU Can be configured at Boot Stage as either "Little Endian" or "Big Endian".

Find Starting Address for the 1st BANK:

$a_{29} = a_{30} = a_{31} = 0$

a_{28} has to be Added, to form a Hex

0X0000_0000

2nd Bank's Starting Address

a_{31}	a_{30}	a_{29}	a_{28}
0	0	1	0

0x2000_0000

3rd Banks Starting Address

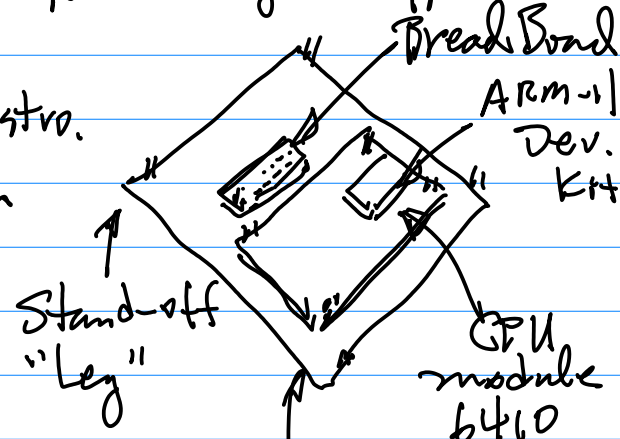
a_{31}	a_{30}	a_{29}	a_{28}
0	1	0	0

0 x 4000_0000

Now, Consider target Board
Conditions to qualify the selection

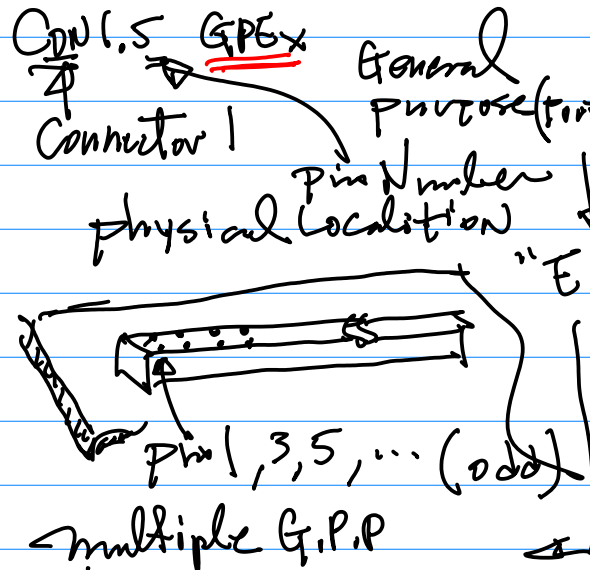
① ARM Based ; ② UNIX-Like O.S. Linux { Kernel Image, Source Distro, Tool Chain
③ Establish eco-system Developer Base (~millions)
④ Technology Innovators / Leaders.
⑤ External Expansion Connectors

Plus: many examples on Device Drivers (I2C, PWM, SPI, UART, ...)
Good learning Tool 4/5



Feb 3rd (Wed) CMPE242
Note: 1° Submission of Honest Pledge Form (Signed), CANVAS, By Sat 11:59 pm ; EE242 submission to e-mail ;
Today's Topics: 1° CPU Architecture
2° Target Board Selection — Bill of material
Ref: github
1-2020S-lect1_hardware board...
ARM-11 ① Compliant w/ Linux Open Source Distro { Kernel Sources, ARM tool chain
② Datasheet Baseline Reference Requirements, Exams
DrawBack: Lack of the Ability to handle Edge AI ; (G.E.) Tiny 6410 Kit from FriendlyARM.com, ~$90

Note: Bread Limitation — Raw High Speed ~20 MHz Cannot



Option (Pie Board 3B+, 4) $75 Pie-4, 8GB mem.

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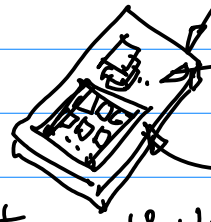
NUDA (Nvidia) ↓ NANO — 128 GPU

↓ TX2 System on module



6 GPU ARM A57?

256 GPU

Note: 1° NANO Expansion Connector, Yes (Limited I/O Function) Compare to ARM11 — SPI ✓, I2C ?, PWM

2° Kernel Source Distribution, Yes

To Become a developer, to Sign up ~$59

Option (NUDA TX2 System on module)

1° Expensive! $299 + Carrier Board $150 – Bust

Edge on AI

If this is seleted, then { 2~4 person to Share the Cost

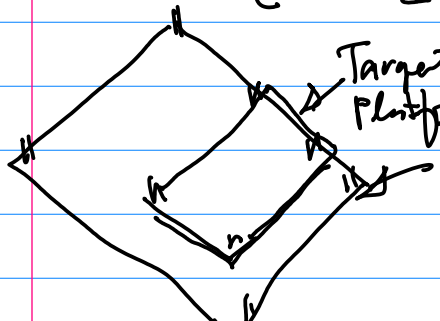
Note: 1° 4-Person Team By Next Week;

{ or Homework/Project has to Individual, Each person has your own Board;

Bill of materials:

Phase I & II { Phase I — HW1 – "Hello,..."

" II Sensors/Stepper motor Drive



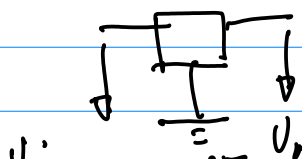
Target platform

1° Wirewrapping Board

Through-Holes w/metal plating (Not the entire side)

2° 4 Stand-offs ("Legs")

3° Components to Build PWR CKT & CKT for I/O Testing ("Hello, the world").



(To Target Board, and CKTs)

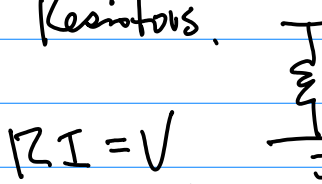
Vin — PWR Regulator IC — Vout

78xx 7805 7812

5VDC 12VDC

Red LED, 4~10mA

Resistors.



Vcc = 5.0

I = 4~10mA

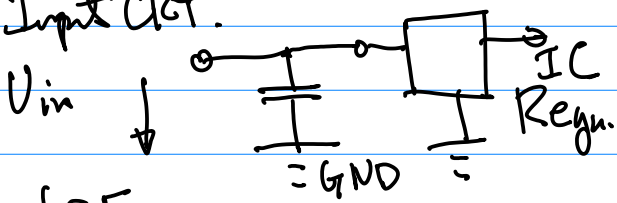
GND

$RI = V$

$R = V/I = 5/4\times10^{-3}$

$= 1.25\ K\Omega$

Cap for your External Power Input Clkt.



Vin

IC Regu.

GND

LPF (Low Pass Filter)

$C = 4.7\ \mu F$

$T = RC \rightarrow$ 3dB

4° Toggle s/w

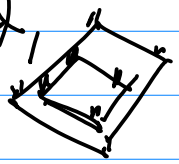
Feb 8, (Monday) CmpE242
Harry Li

Today's Topics: 1° Bill of material
2° Prepare for the 1st Assignment
"Hello, the world". 3° CPU Architecture

Bill of Material { Phase I: Target platform "Hello, the world"
Phase II: Sensors / Drive / Stepper motor / OpAmps

1. Target: ① Pic3Bt, Pic4
② NANO, TX2 (Edge AI)
③ ARM11 — Base Line Reference platform

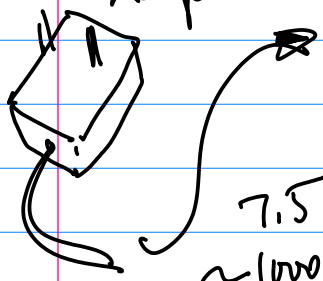
2. Prototype Board, 6" x 4"



I/O CKT
Sensors { Analog / Digital
Drive

POWER CKT: PWR Regulator IC
LM7805 20VDC drop off

3. Wall mount Adapter



7.5 VDC ~1000-1500 mA.

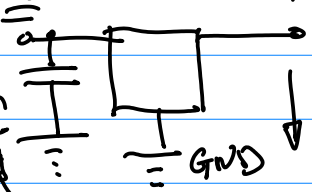
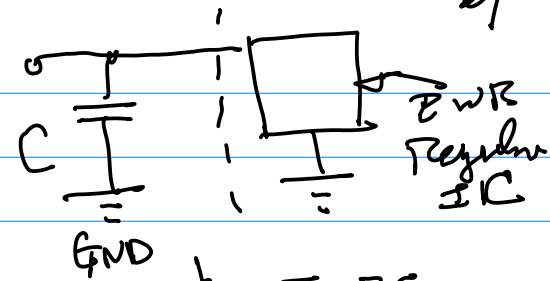


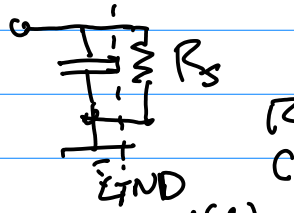
Fig1. 5 VDC

4. "Glue" Logic { Assorted Resistors 200 ~ 5 KΩ 10 KΩ
Caps { 7805
PWR Input Node
LPF (Low Pass Filter)

⑤ PWR Distribution Node

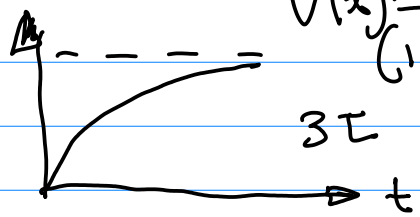


$\tau = RC$



R = 1KΩ
C = 4.7uF

$V(t) = V_{DC}(1 - e^{-\frac{t}{\tau}})$



Caps for 7805 → Datasheet
Polarity "⊥"

74xx NAND, NOR,
LED, Red, yellow, green
4~10mA

Note: you may need higher voltage source to Stepper motor Drive.
LM7812?

Connectors { External PWR
Switch (Toggle Switch)

To control PWR Source;
To Build I/O Testing

Phase II (Bill of material):

Ref: github:

1. LSM303 (I2C) → Autonomous Robot

2. optical encoder (optional) = LSM303

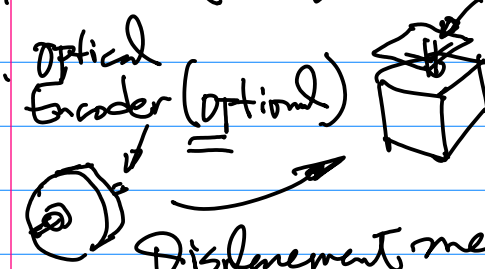
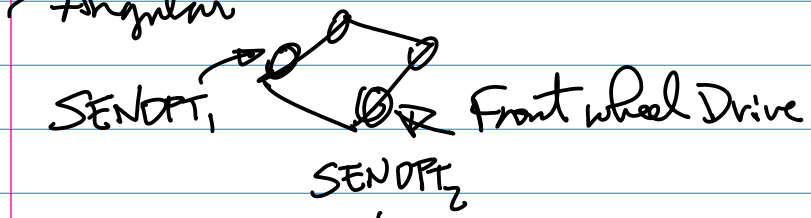
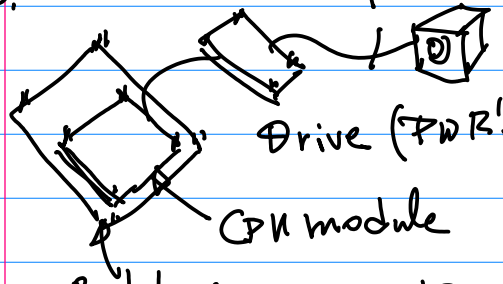


Fig2

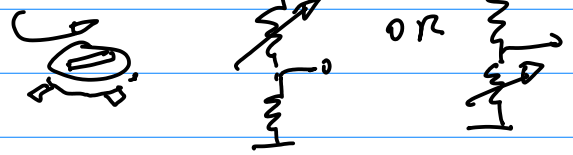


3. 4 NEMA14, 17



a. 12VDC Commonly used Source, Check Current Need!

b. Buck Converter = is good;



Consider Building "Hello, the world" Test CKT

Objectives 1. Bring up the target Board and print "your Name, Last 4 Digits Student ID"

2. Test GPIO Interface

2.1 Send Logic "1" to Turn ON On-Board LED, then flash @ 1 Hz Frequency

2.2 Send Logic "0" via gpio port to turn off on-Board LED;

2.3 Read input via GPIO port, if the input is "1", then send command to Turn ON On-Board LED

2.4. Read Inputs via GPIO Port, if the input is "0" then, Send command to Turn off the on-Board LED.

Discussion on CPU Architecture then on this Assignment.

Action 1: Form 4 person Team, Send me email First, Last Name, SID

Feb10.

Homework 1 Due Feb24 (W) 11:59pm.

CmpE/EE242 Canvas

EE242 Submission to E-mail:

Target platforms: ARM11[a] Architecture[b] O.S.[c] Driver

Base Line
- Pic ✓ (Not mine) — Kernel ✓ NM — ✓ NM
- NVDA ✓ — ✓ — ✓
  - NANO, TX2

1° Target platform Built on Prototype Board

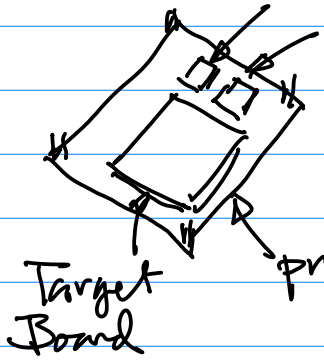


Fig.1

Ref: 1-lec1-Hardware Board-

print "Hello, the world", Drive LED ON/OFF

C/C++ or Python — Has to be the LED ON your prototype

2° GPIO Testing
- GPP Output CKT1
  - "1" Turn on LED
  - "0" Turn off LED

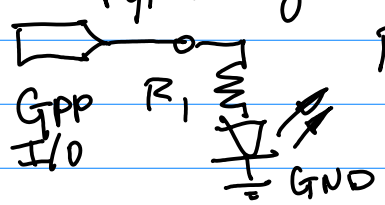
Design:

Identify the GPIO pins for Input and Output Testing CKT.

NXP LTC 1769

Pg.3 GPP Input pin

Pg.21 GPP Output Pin



$V_{GPP} = IR + V_{LED}$ ... (1)

CMOS $V_{GPP} = 3.3$ VDC

$I \simeq 10$ mA

$V_{LED} \simeq 1.2$ VDC

$3.3 = 10\times10^{-3} R + 1.2$

$R = (3.3 - 1.2) / 10^{-2}$

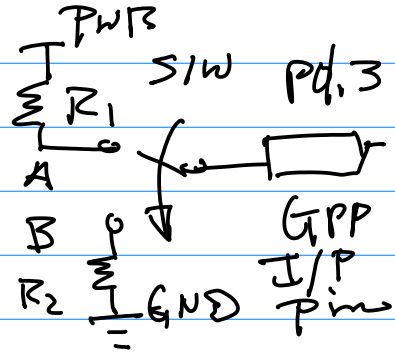
$= 210\ \Omega$

Note: Find the pin(s) from Target platform.

Pie3 GPIO14 — Pin 8

Consider Input Testing CKT

Input pin GPP { Read "1", PWR; Read "0", GND } with toggle switch



R1: $3.3 / 10\text{mA} = R_1$

$3.3 / 10\times10^{-3} = 330\ \Omega$

R2: $\frac{3.3\ (\text{from GPP})}{10\times10^{-3}} = 330\ \Omega$

CmpE242

9/

System (Architecture) & Software Design. Boot Loader { 0.5. I/O Function

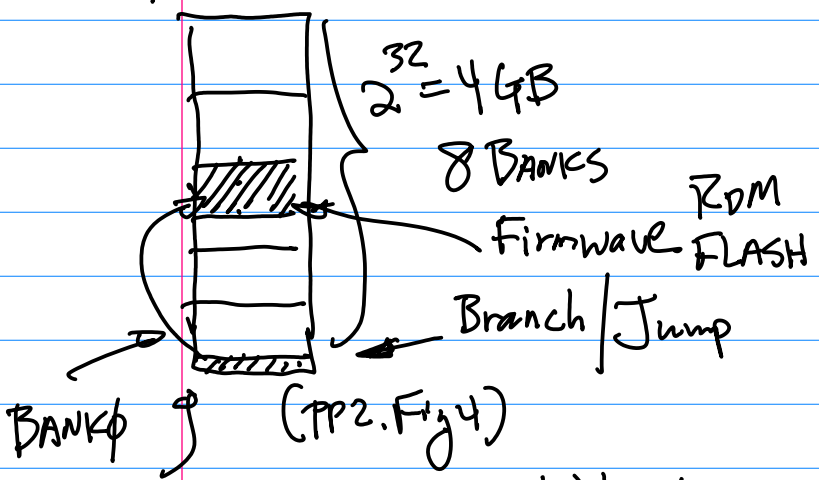
3° Source code, Binary → Zip.

4° One page Report IEEE paper format (Template is given on-Line) github

5° Form 4-person Team. Submit
First, Last Name, 4 Digits SID
E-mail Contact Information
Indicate Coordinator of the Group
By Thursday.
Note: All work has to be individual

6° Short video Clip (5–10 seconds)
Shows the Prototype Board and
Screen Capture.

Architecture



0x0000_0000 PWR-up Address
Addr. when CPU is powered up, it will fetch the 1st Instruction from this addr.