

# Option 4 RISC-V Target Development Platform



# RISC-V SiFive Team

<https://www.crowdsupply.com/sifive/hifive-unleashed/updates>



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**Jack Kang**



**Naveed Sherwani**



**Sunil Shenoy**



**The Rest of the  
SiFive Team!**

# Maix Development Kit For AI

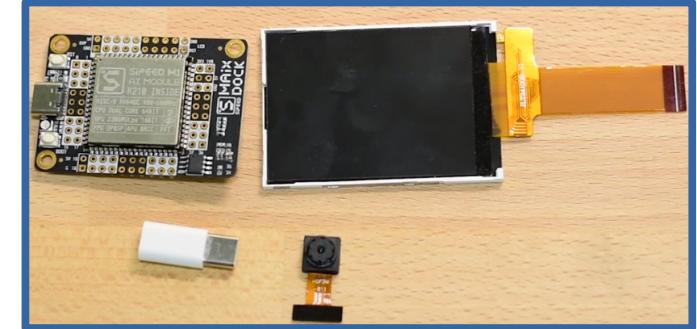
Get the one with  
WIFI support

MAIX's Deep  
learning

<https://www.seeedstudio.com/Sipeed-M1-dock-suit-M1-dock-2-4-inch-LCD-OV2640-K210-Dev-Board-1st-RV64-AI-board-for-Edge-Computing.html>

1. MAIX support fixed-point model that the mainstream training framework trains, according to specific restriction rules, and have model compiler to compile models to its own model format.

2. It support  
(2.1) tiny-yolo,  
(2.2) mobilenet-v1, and,  
(2.3) TensorFlow Lite! Many TensorFlow Lite model can be compiled and run on MAIX!

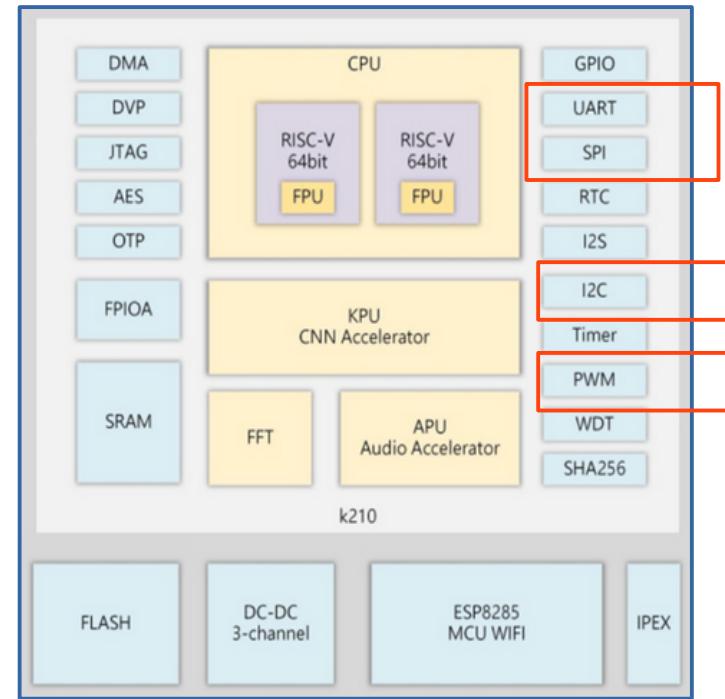
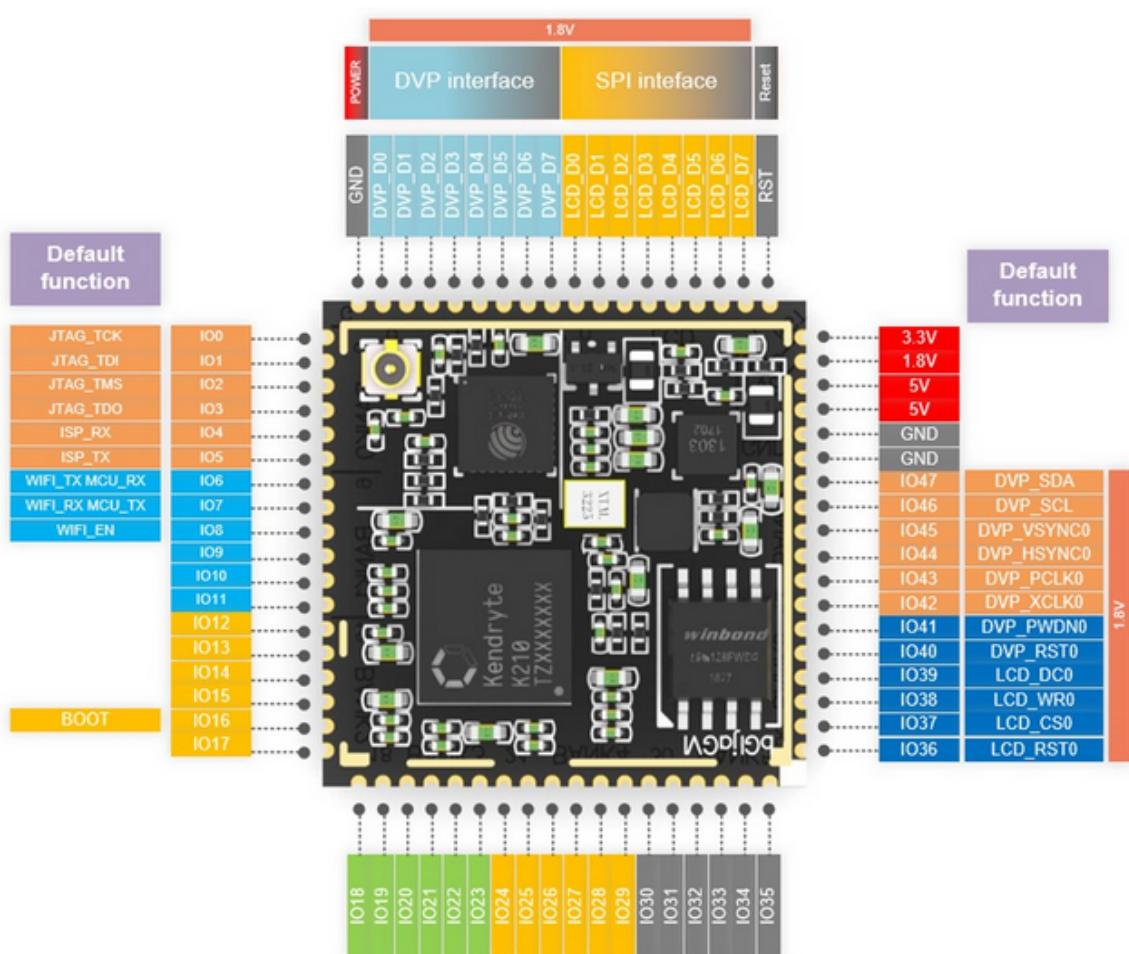


SPECS/BOARD	K210
Number of Cores	2
Architecture	64 Bit
CPU Frequency	400 MHz
Neural Network Hardware	YES
WiFi	NO
BLUETOOTH	NO
RAM	8 MB
FLASH	16 MB
GPIO PINS	48
Busses	I2C, SPI,I2S



# Maix Development Kit

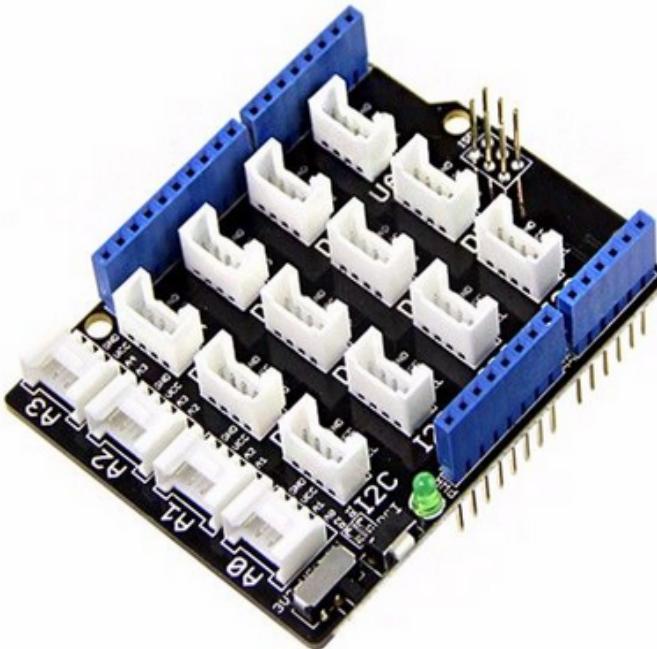
<https://www.seeedstudio.com/Sipeed-M1-dock-suit-M1-dock-2-4-inch-LCD-OV2640-K210-Dev-Board-1st-RV64-AI-board-for-Edge-Computing.html>



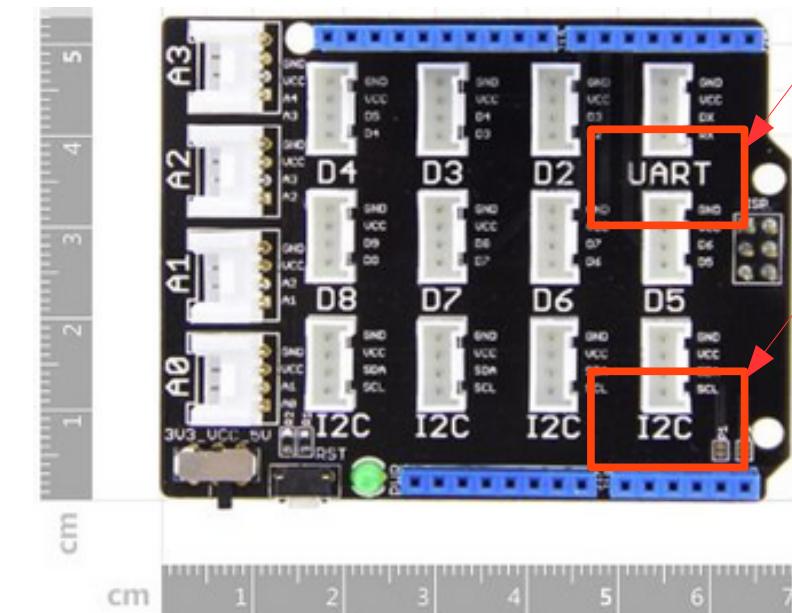
All usable IO breaks out as 1.27mm(50mil) pins, and pin's voltage is selectable from 3.3V and 1.8V.

# Maix Shield Board

Compatible with lots of Arduino board [Rich grove](#)  
connectors Same pinout as Arduino Uno R3  
Selectable voltage

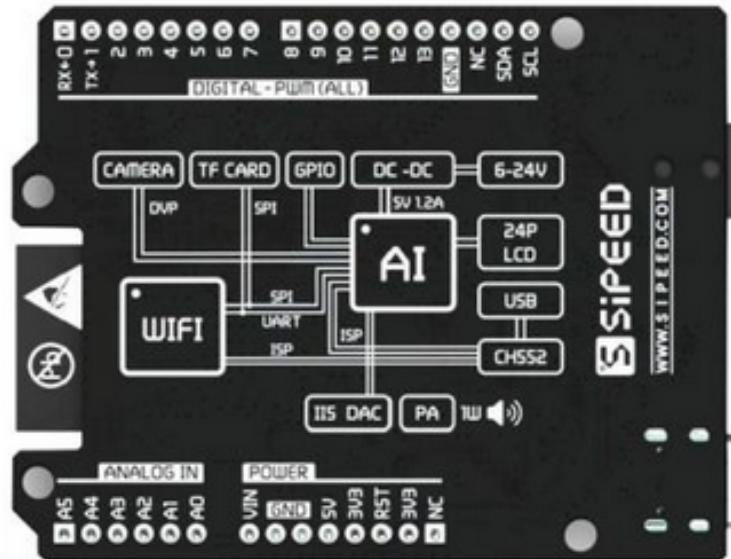
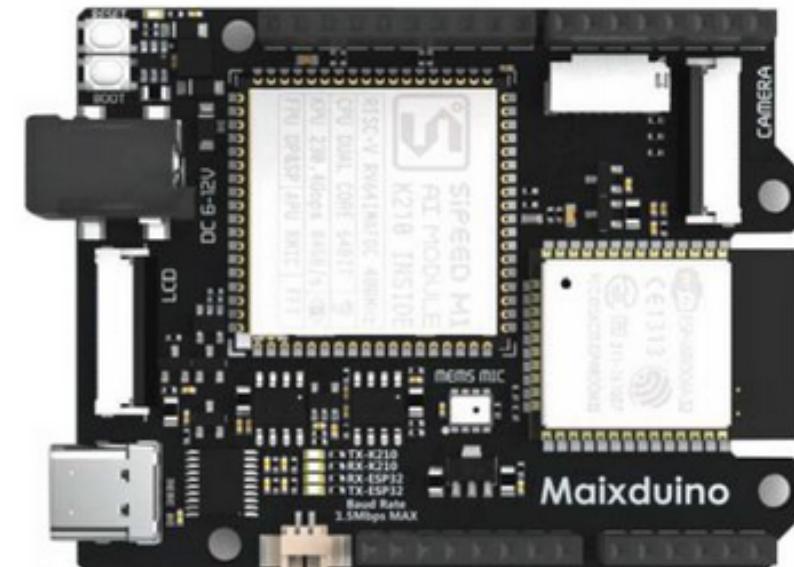
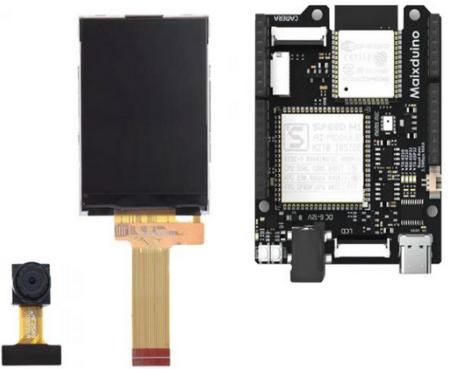


Specification	Name	Qty
Analog	A0/A1/A2/A3	4
Digital	D2/D3/D4/D5/D6/D7/D8	7
UART	UART	1
I2C	I2C	4



# Kit For AI + IoT

<https://www.seeedstudio.com/Sipeed-Maixduino-Kit-for-RISC-V-AI-IoT-p-4047.html>



# Option 6 RISC-V Target Development Platform



# RISC-V FPGA SoC

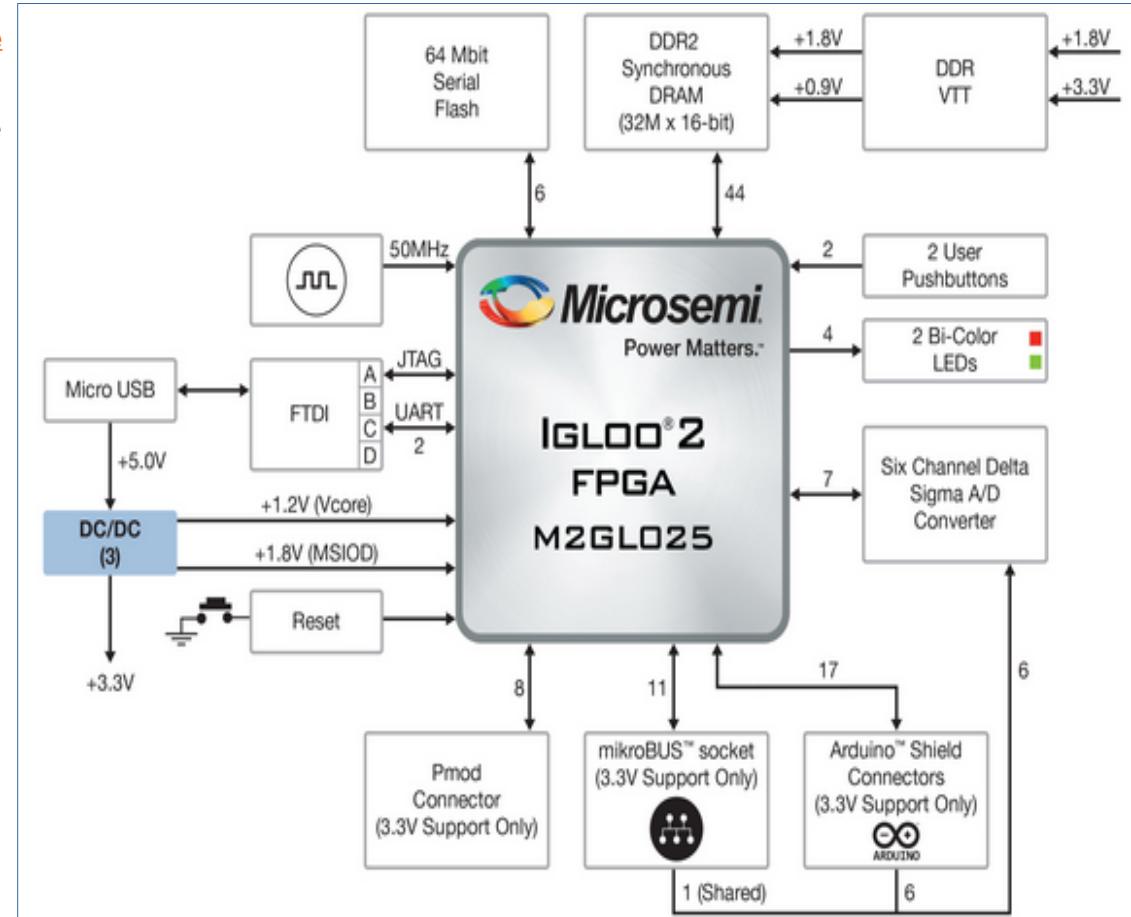
<https://www.microsemi.com/existing-parts/part/143948>

## IGLOO2 RISC-V Creative Development Board

Microsemi's IGLOO2 FPGA is **pre-programmed with a RISC-V core** and peripherals. The IGLOO2 RISC-V Creative Development Board boasts a 25K logic element (LE) FPGA, offering the lowest cost of entry for both software and hardware engineers who want to evaluate and implement their own unique designs. The out of the box demo is the RISC-V core running a hello world demo.



To order  
<https://www.futureelectronics.com/resources/videos/future-electronics-microsemi-creative-development-board>





# IGLOO2 FPGA Creative Development Board

<https://www.microsemi.com/existing-parts/part/143948>

Demos	Description
Mi-VTic Tac Toe	Based on a Mi-V softcore processor design, play the classic Tic-Tac-Toe game by yourself or with a friend. This demo supports two touchscreen TFT from Adafruit (P1651 and P1947), and includes both a backlite control and a screensaver feature.
FreeRTOS	Based on a Mi-V softcore processor design, this demo features a simple three task LED blinking program running in a FreeRTOS v8.2.3 environment. This design integrates a Terminal UART, LEDs, pushbuttons, a timer and a DDR2 controller to help you experience FreeRTOS in a FPGA setup.
ADC Read - Terminal (uses RISC-V)	Based on a Mi-V softcore processor design, a reading from the ADC channel 0 or channel 2 will be echoed on a Terminal window on a host PC using the Avalanche's user pushbuttons.
Out of the box - Risk-V Blinky (Hello World!)	Out of the box demo. "Hello World!" text is sent through a Terminal connection at power-up or board reset. Terminal text is echoed afterward and board LEDs start blinking in a defined pattern. It provides a starting point to develop bare metal RISC-V applications.

Price: \$149

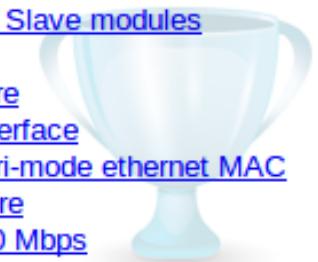
# Open Core Ethernet Controller

<https://opencores.org/>

The IP core has been chosen by [Flextronics Semiconductor](#), proven in FPGA technology and integrated into a Flextronics' design. Flextronics can offer commercial design services to companies that want to use this IP in their products - for more information fill out this [questionnaire](#).

## Most popular projects

- [I2C controller core](#)
- [SPI Verilog Master & Slave modules](#)
- [I2C Slave](#)
- [I2C master/slave Core](#)
- [SPI Master/Slave Interface](#)
- [10\\_100\\_1000 Mbps tri-mode ethernet MAC](#)
- [I2C Master Slave Core](#)
- [Ethernet MAC 10/100 Mbps](#)



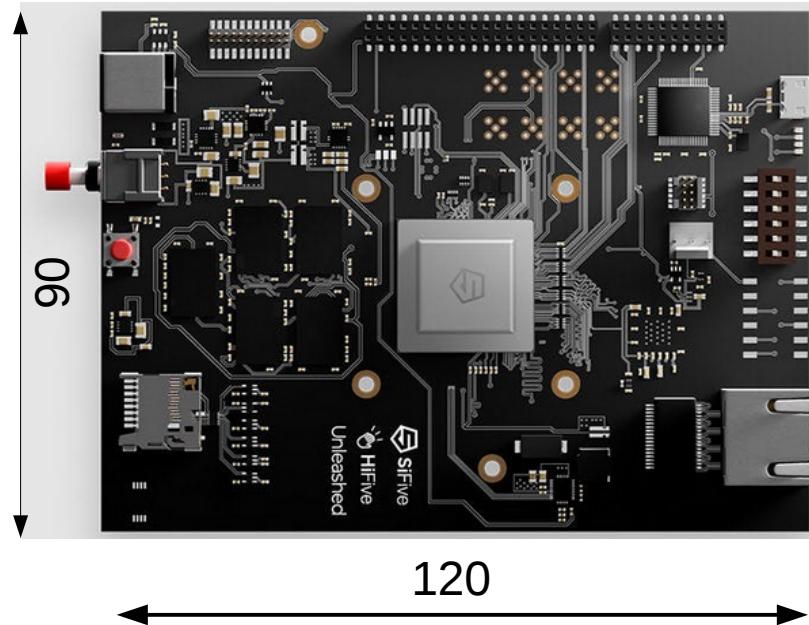
# • Freedom U540 RISC-V With Linux

<https://www.sifive.com/boards/hifive-unleashed>

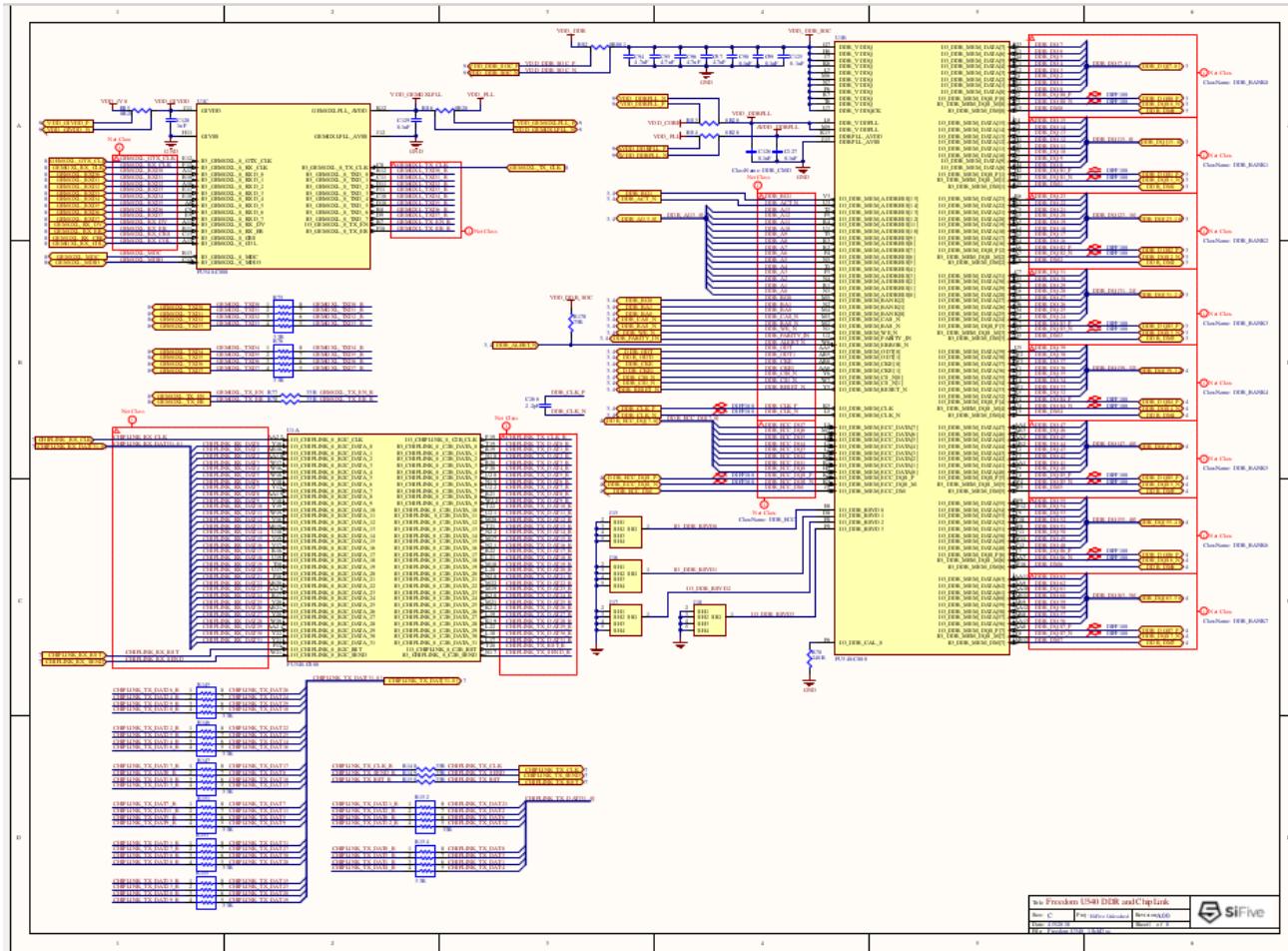
Freedom U540

4+1 multi-core design with clock speeds up to 1.5GHz, features a 2MB L2 cache, Gigabit Ethernet, 64-bit DDR4 with ECCm and is manufactured on a 28nm process. The HiFive Unleashed development board has 8GB of DDR4, 32MB quad SPI flash, microSD card for storage.

Royalty-free CPU architecture, the price remains lofty for hobbyists/enthusiasts at \$999 USD.



# •Freedom U540 RISC-V SCH

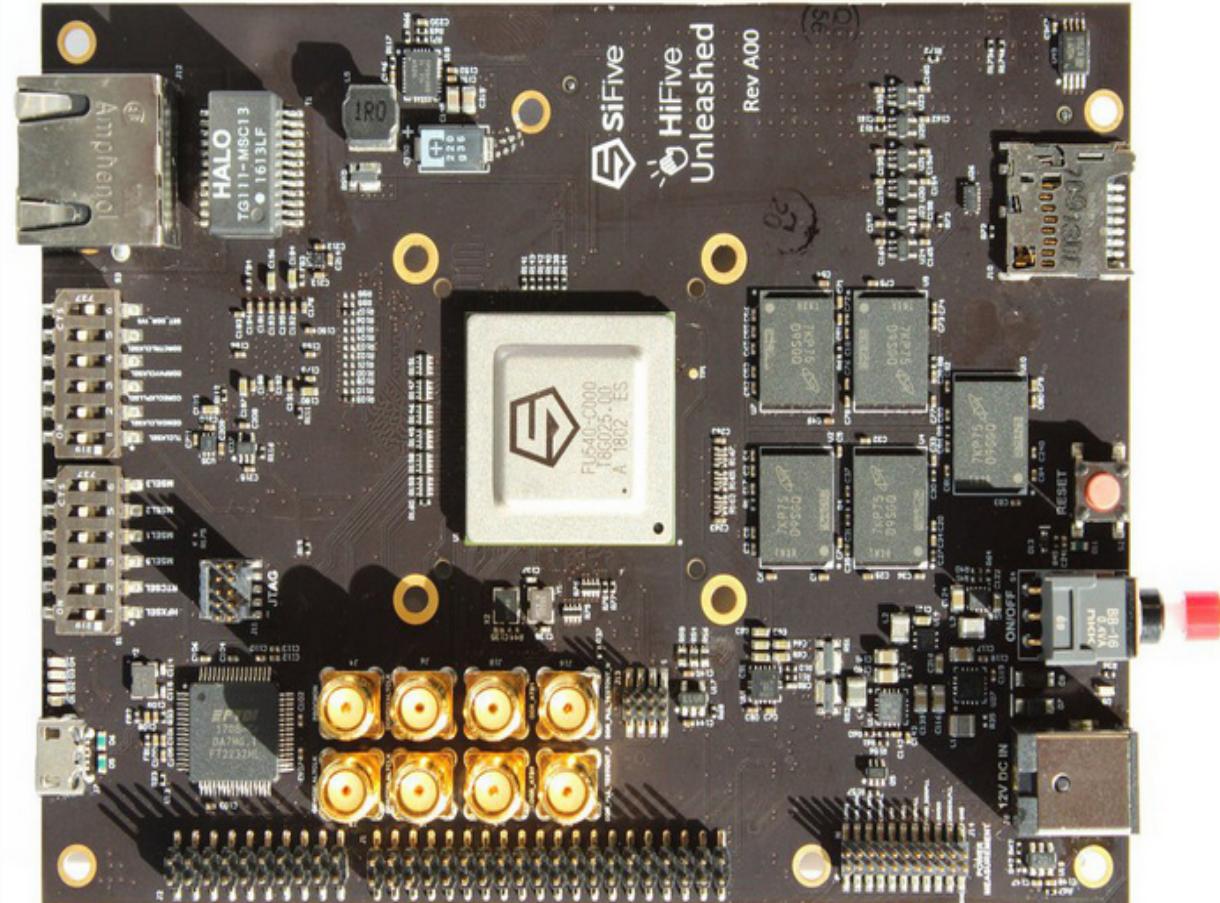


# Getting Started with Linux On HiFive

<https://risc-v-getting-started-guide.readthedocs.io/en/latest/linux-hifive-u.html>

This chapter targets Debian-based Linux flavors, and has been tested on Ubuntu 18.04.

<https://www.sifive.com/boards/hifive-unleashed>





# SiFive RISC-V Expansion Board

one year Libero GOLD License (\$995 value). Initially, the kit will include only a fixed bitstream that can enable a PCIe Root Complex.

<https://www.crowdsupply.com/microsemi/hifive-unleashed-expansion-board>

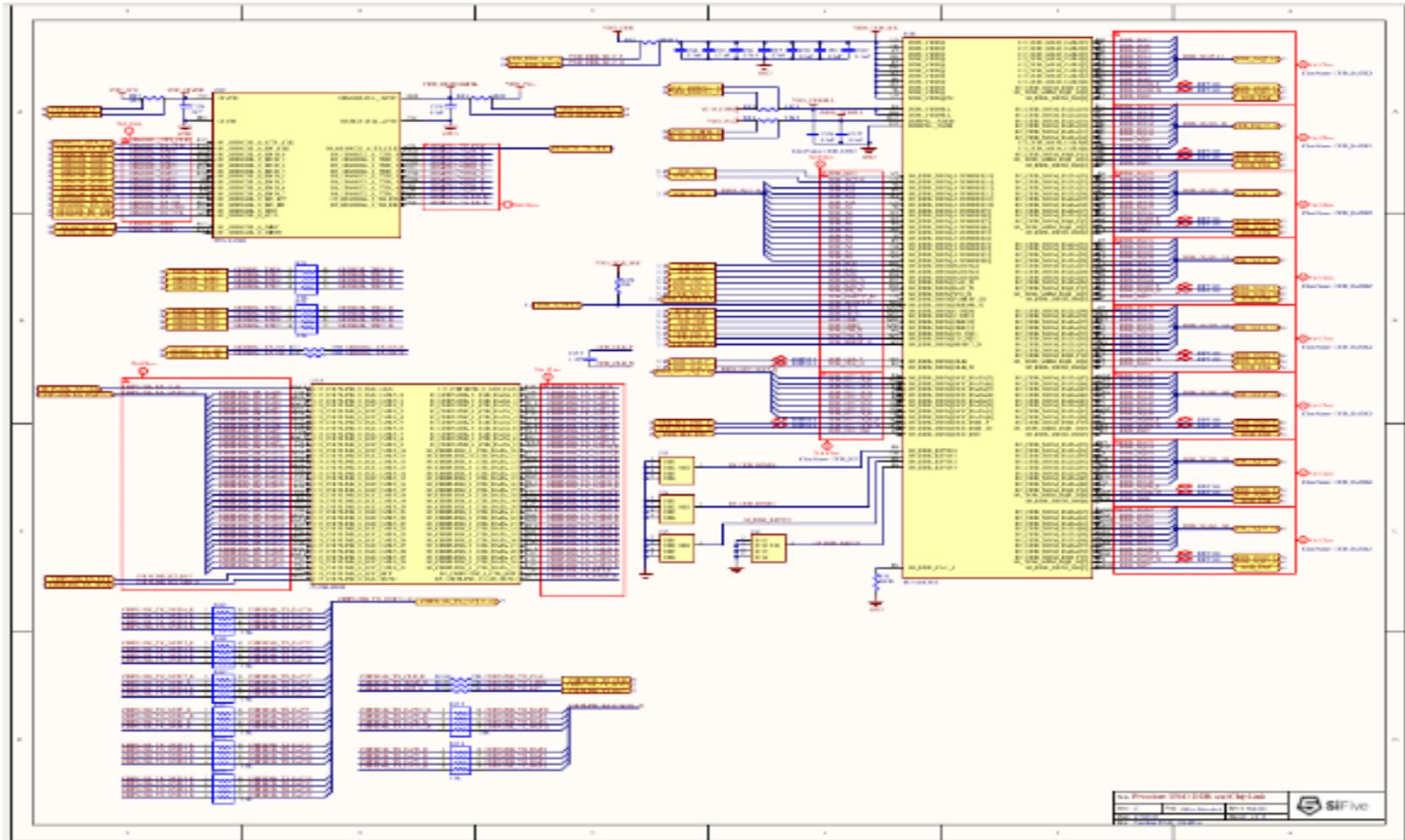
The HiFive Unleashed has a companion Expansion Board from Microsemi which features a mating connector, Polarfire FPGA and a bunch of peripheral I/O.



<https://www.crowdsupply.com/microsemi/hifive-unleashed-expansion-board>

complete Linux applications on a modern RISC-V CPU running at 1 GHz+

# Freedom U540 RISC-V SCH



# Identify CPU Pins From The Connector For SPI Interface Design

LPCXpresso			Dual row holes (2x27)
GND		GND	C J2-1
VIN (4.5-5.5V)		EXT_VIN	C J2-2
VB (battery supply)		VRAT	C J2-3
RESET_N		TARGET_RESET	C J2-4
P0.9	MOSI1	P0.9	C J2-5
P0.8	MISO1	P0.8	C J2-6
P0.7	SCK1	P0.7	C J2-7
P0.6	SSEL1	P0.6	C J2-8

