#### CMPE 242 Spring 2021 Midterm Exam Version A

First Name: Student ID:		(Total 30 points)
receive unper	All students agree, individually and collectively, the mitted aid during examinations. Engaging in such neating. By my signature, I affirm that I have adher	unpermitted actions is
Signature:	Date:	

**Please Read:** instructions for Zoon based online exam.

- 1. this is an one hour exam, starting from 3:00 and last till 4:00;
- 2. use cellphone to scan your papers, save them as pdf file, then you must convert it zip file;
- 3. Submission must be made in the zip file format on line before 4:15, late submission will make the paper disqualified; After 4:15 no submission will be accepted (based on the time stamp of the submission). Thank you and stay safe.

This Midterm Exam consists of 3 Questions, total 30 points. The Questions start next page.

**QUESTION 1 (5 points)** Using ARM-11 or your selected target platform, answer the following design questions:

1.1 (5 pts) Design input and output testing circuit by first drawing circuit schematics and then calculate resistors value to realize the above required input/output testing functions? assume LED current = 10 mA, and V led = 1.2 V.

Sol. First, Identify your Selected platfam, such as Pie, ARMII, NANO, TXZ etc. Be Sure to provide pin/Connector Specific information to Substainate your design and physical implementation.

VGPP = IR+ VLED ... (1) (mos v<sub>gpp</sub> = 3.3 UDC T~10mA VLED ~ 1,ZVXC 3,3=10×10 12+1,2 R = 3.3 - 1.2 / 2  $= 2 [0.0.2] / 10^{-2}$ 

The Dufant Testing CKT: The Juput Testing CKT

Target ARMII. (For Both I/P High & Low)

GPP RISIN PUR

JRI

GPF1 (Pin3) I GNO

The Juput Testing CKT

For Both I/P High & Low)

PMR

JRI

GPF1 (Pin3) I GNO TPWR SIW Pd.3 REGND TIPP GPFO REGND TIPP (7 in Z)

> K1: 3,3/10mA=R1 33/10×10-3=330/2 R2: 3,3 (from GPP) = 330,2 "

**QUESTION 2 (15 points)** Design a PID (proportion, integral, and derivative) controller by answering the following questions:

2.0 (1 pt) Draw a block diagram of a PID controller?

e(0)=1.3

e(t)=4.5

2.1 (2 pts) Explain the limitation of the forward difference (FD) and backward difference (BD) kernels, derive central difference (CD) kernel and explain its key feature?

2.2 (3 pts) Explain what can Laplace of Gaussian (LoG) kernel offer in terms of improving the performance of CD kernel? Find LoG(0), LoG(1) and Log(-1)? Assum sigma = 1 for simplicity (LoG(x,y) formula is given in the Appendix).

2.3 (4 pts) In a given PID controller in the Appendix, e(t) is measured and tabulated below, compute (a) the derivatives of error e(t) by convolution using the CD kernel, and the integral of error e(t) by counting the history of the error going back one time step.

2.4 (5 pts) Based on the PID Controller's e(t)\_{sigma} (Proportion, derivative, and integral error at time t), find the control action, e.g., a duty cycle (DC) of the PWM signal for time t=2. Note use the following Figure for your calculation. In this figure, the min e\_{sigma} is -500, and max e\_{sigma} is 500, the min duty cycle is 5%, the max duty

cycle is 80%			
4 0	, 1	 	 , ,

e(t)=10

Z.O PID Controller Z.I Limitation of FD: Skewed towneds X+1;

X-1;

e(t)=8

Loglo]=- I Lou(1)=0, Lobr(1)=Lobr(1)=0, see details in the Arrendix.

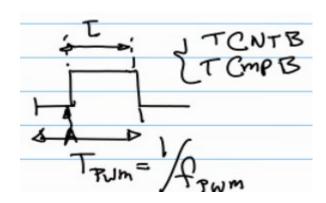
 $Z_1 + f_1 + f_2 + f_3 + f_4 + f_5 + f_6 + f_6$ 

= Kpx 10+ Kd x 1,75+ Kd x 120,25 Then, (see Appendix) = 10+1,75+120,25=132;

**QUESTION 3** (10 Points) Design PID controller for stepper motor control, by answering the following questions:

3.1 (3 pts) Design by drawing schematics for stepper motor control with your target embedded board (an external connector), a stepper motor drive board, and NEMA 14 stepper motor. Be sure to provide all the signal connections with label for each of them, and use "arrow" to indicate the signal flow direction (suppose PWM and GPP are employed in this design);

3.2 (2 pts) Suppose in you design, f  $\{pwm\} = 10KHz$ , CLK p (peripheral clock) = 25MHz, PWM duty cycle has to be set to 60% as in figure below. In ARM11, the count N for TCNTB and the count M for TCMPB special purpose registers have to calculated, find N and M?



3.3 (3 pts) Now modify the PWM driver code (see code listing in Appendix), explain in details (bitwise) what do the following 4 lines of code do?

(a) what does line 61 do? Explain in bitwise details what does line 62 do?

(b) what does line 63 do, explain bitwise details?

(c) what do line 83 and 84 do?

tmp = readl(S3C64XX GPFCON): 61

62 tmp &=  $\sim (0x3U << 28)$ ;

tmp = (0x2U << 28);63

writel(tmp, S3C64XX GRFCON);

tent = (pclk/50/16)/freq;

84 tduty = tcnt\*duty;

Compute N for SPR TCUTB;

EM for

3.4 (2 pts) Describ
a device driver for
Compiler Tool Ch 3.4 (2 pts) Describe by drawing a flow chart to describe the process of writing/modifying a device driver function? (Starting from (a) Kernel Source OS distribution, (b) Cross Compiler Tool Chain distribution, and (c) CPU datasheet, to the completion of kernel image with the device driver, be sure to include the explanation of \$make menuconfig and Kconf.

Shift Z Bits "10" 28 bits Left from Appendix Datusheet, then Butwise OR" to Set PWM.

11 read 32 bits from the GPF

Control Register

Shift ZBit"11" Z8 bits to the

left, Negate it to "op" then

Bitwise "OR", e.g., clean these Z

And  $M = 60\% N = 0.6 \times 2.5$   $= 1.5 \times 10^{3} \text{ for TCmpB,}$ Sol: 1. Design the Handware System (Finish This Design with your Tanget platform, ARMIL, Pie3B+/4, or NAND, or TXZ) Shown Belowis ARMI Based Design APM-11 CPU module Vin Stepper motor GPF DIP A+

GPF DIP A+

Step B+

Step B-GPF1: GPP Pat 7 in to Control Stepper motor Direction GPFO: PWM Dutput pm (input to the motor Drive Note: You may assume the motor drive board is configrated to 4 Step or your preferred

2. From Given Condition CLKp= 25x10 Hz, frum=10×103Hz, Hence N= CLKp/fpm = Z5x106/10x103=Z.5x10 for TOUTB

# Appendix 2 SPR for GPECON

Reference: CPU Datasheet, 10.4 REGISTER DESCRIPTION

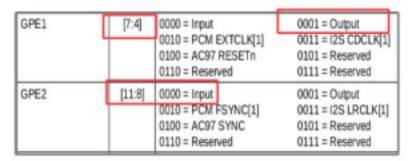
GPECON (Compiler used name: GPECON)

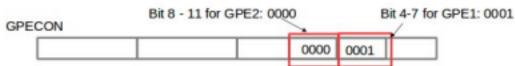
	A	
GPECON	0x7F008080	Configuration Register
GPEDAT	0x7F008084	Data Register
GPEPUD	0x7F008088	Pull up/down Register

Example: GPE Init & Config.

Set GPE1 output, "1" GPE2 input, "0"

> So the binary pattern is 0x10





There are five control registers including GPECON, GPEDAT, GPEPUD GPECONSLP and GPEPUDSLP in the Port E Control Registers.

Register	Address	R/W	Description	Reset Value
GPECON	0x7F008080	R/W	Port E Configuration Register	0x00
GPEDAT	0x7F008084	R/W	Port E Data Register	Undefined
GPEPUD	0x7F008088	R/W	Port E Pull-up/down Register	0x00000155
GPECONSLP	0x7F00808C	R/W	Port E Sleep mode Configuration Register	0x0
GPEPUDSLP	0x7F008090	R/W	Port E Sleep mode Pull-up/down Register	0x0

GPDCON	Bit	De	scription	Initial State
GPE0	[3:0]	0000 = Input 0010 = PCM SCLK[1] 0100 = AC97 BITCLK 0110 = Reserved	0001 = Output 0011 = I2S CLK[1] 0101 = Reserved 0111 = Reserved	0000
GPE1	[7:4]	0000 = Input 0010 = PCM EXTCLK[1] 0100 = AC97 RESETn 0110 = Reserved		0000
GPE2	[11:8]	0000 = Input 0010 = PCM FSYNC[1] 0100 = AC97 SYNC 0110 = Reserved		0000
GPE3	[15:12]	0000 = Input 0010 = PCM SIN[1] 0100 = AC97 SDI 0110 = Reserved	0001 = Output 0011 = I2S DI[1] 0101 = Reserved 0111 = Reserved	0000
GPE4	[19:16]	0000 = Input 0010 = PCM SOUT[1] 0100 = AC97 SDO 0110 = Reserved	0001 = Output 0011 = I2S DO(1] 0101 = Reserved 0111 = Reserved	0000

GPEDAT	Bit	Description
GPE[4:0]	[4:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPEPUD	Bit	Description
GPE[n]	[2n+1:2n] n = 0~4	00 = pull-up/down disabled 01 = pull-down enabled 10 = pull-up enabled 11 = Reserved

GPESLPCON	Bit	Description	Initial State
GPE[n]	[2n+1:2n] n = 0~4	00 = output 0 01 = output 1 10 = input 11 = Previous State	00

GPEPUDSLP	Bit	Description	
GPE[n]	[2n+1:2n] n = 0-4	00 = pull-up/down disabled 01 = pull-down enabled 10 = pull-up enabled 11 = Reserved.	

## **APPENDIX PWM Driver Function (partial list)**

```
static void PWM_Set_Freq( unsigned long freq, duty ) //Harry: add "duty"
{
    unsigned long tcon;
    unsigned long tcht;
    unsigned long tcfg1;
    unsigned long tcfg0;

    struct clk *clk_p;
    unsigned long pclk;

    unsigned tmp;

tmp = readl(S3C64XX_GPFCON);
    tmp &= ~(0x3U << 28);
    tmp |= (0x2U << 28);
    writel(tmp, S3C64XX_GPFCON);

    tcon = __raw_readl(S3C_TCON);
    tcfg1 = __raw_readl(S3C_TCFG1);</pre>
```

```
tcfg0 = __raw_readl(S3C_TCFG0);

//prescaler = 50
tcfg0 &= ~S3C_TCFG_PRESCALER0_MASK;
tcfg0 |= (50 - 1);

//mux = 1/16
tcfg1 &= ~S3C_TCFG1_MUX0_MASK;
tcfg1 |= S3C_TCFG1_MUX0_DIV16;

__raw_writel(tcfg1, S3C_TCFG1);
__raw_writel(tcfg0, S3C_TCFG0);

clk_p = clk_get(NULL, "pclk");
pclk = clk_get_rate(clk_p);
tcnt = (pclk/50/16)/freq;
tduty = tcnt*duty; //Harry: duty is x% of the period, duty cycle
```

(the above for the reference, cut from here)

#### APPENDIX GPFCON

GPFCON	Bit		Description	Initial State
GPF0	[1:0]	00 = Input 10 = CAMIF CLK	01 = Output 11 = External Interrupt Group 4[0]	00
GPF1	[3:2]	00 = Input 10 = CAMIF HREF	01 = Output 11 = External Interrupt Group 4[1]	00
GPF2	[5:4]	00 = Input 10 = CAMIF PCLK	01 = Output 11 = External Interrupt Group 4[2]	00
GPF12	[25:24]	00 = Input 10 = CAMIF YDATA[7]	01 = Output 11 = External Interrupt Group 4[12]	00
GPF13	[27:26]	00 = Input 10 = PWM ECLK		00
GPF14	[29:28]	00 = Input 10 = PWM TOUT[0]	01 = Output 11 = CLKOUT[0]	00
GPF15	[31:30]	00 = Input 10 = PWM TOUT[1]	01 = Output 11 = Reserved	00

"10" To set two

## APPENDIX LoG(x,y)

Second, Build Equation for the mapping function

$$\frac{\chi_2 - \chi_1}{\chi - \chi_1} = \frac{y_2 - y_1}{y - y_1} \dots (1)$$

Solve for y, we have

for X= ez 12)=132, y=132x7,5x104 Hence  $y = \frac{0.80 - 0.05}{500 - (-500)} \times -\frac{0.80 - 0.05}{500 - (-500)} \times (-500) + 0.05 = 0.099 + 0.425 = 0.524$ (see Fig.1.)

(X,, Y1)

$$S = \frac{0.80 - 0.05}{500 - (-500)} \times -\frac{0.80 - 0.05}{500 - (-500)} \times (-500) + 0.05$$