March 16 (Wed)

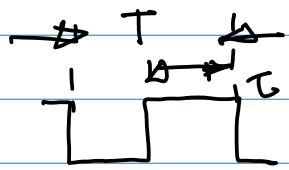
Topics: 1° PWM Architecture/Hardware Aspect — Waveforms, Timing Diagrams, SFRs

2° LSM303 Sensor I2C

Example: PWM Discussion.

f_{PWM}

Duty Cycle



Duty Cycle = t/T ... (1).

Square Wave: D.C. = 50%.

Architectural Aspects:

2021F-105-#0-cpu-arm11-2018S-29-...

6410X_UM

P1106

32 PWM TIMER

This chapter describes the functions and usage of PV

C. Prescaler for f_{PWM} Config

8 bit

P1107

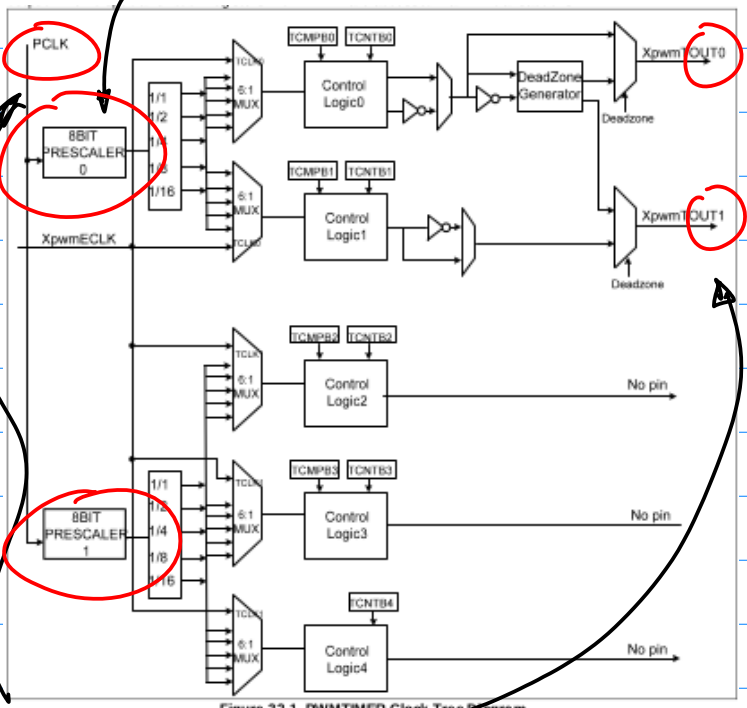


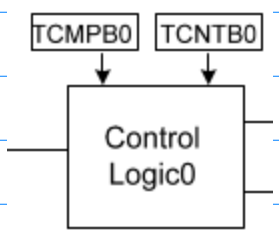
Figure 32-1. PWMTIMER Clock Tree Diagram

a. Input: PCLK peripheral clock.

1/2, 1/4, 1/8, ..., of the System Clock

b. Output (2 outputs)

d. Special Purpose Registers



CONF (Configuration Register)

CNT (Control — "Count")

CMP (Comparision)

→ define f_{pwm} & Duty Cycle.

2022S-107e-pwm-waveform-v3-2018-3-4.jpg
2022S-107f-pwm-specialPurposeRegister-v3-2018-3-4.jpg
2022S-107g-pwm-calculation-v3-2018-3-4.pdf

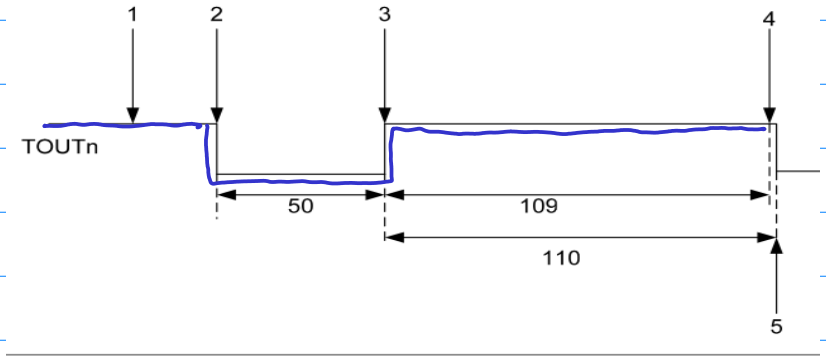
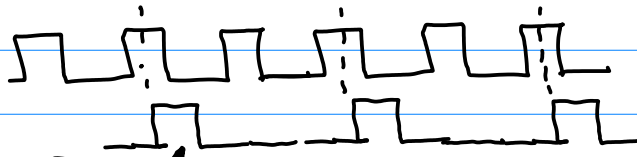


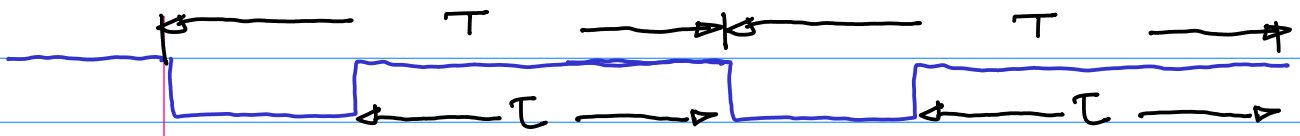
Figure 32-2. Simple Example of PWM Cycle Block Diagram

Note: Background on Counters.



Count By 2

Expand this to A counter for Both integer Number & Fractional Number (in general) ⇒ f_{PWM} (for integer Only) then, use Another Counter to get Duty Cycle.



$T = 1/f_{PWM}$ ... (2), $f_{PWM} = \frac{PCLK}{(Prescaler+1)Div}$ ... (3)

Frequency = PCLK / ({prescaler value + 1}) / {divider value}

Suppose PCLK = 1/4 (System Clock) = $\frac{1}{4}(800 \times 10^6)$

$= 200 \times 10^6$

Defined By Special Purpose Register.

Design Guidelines for PWM:

① CNT (TCNTBφ) Define f_{PWM}
Control Count / Timer / Buffer φ for PWM φ

② Cmp (TCMPBφ) Defines Duty Cycle
Comparision

③ CONF Configuration Register. Defines f_{PWM}

Example: Suppose PCLK = 500×10^6 (mHz), Suppose to Drive A Stepper Motor f_{PWM} = 2 KHz = 2×10^3

Find the Counts N for TCNTBφ

$\frac{PCLK}{N} = f_{PWM}$ ... (4)

$\frac{PCLK}{N} = f_{PWM}$, Substitute the design Requirements into it.

$\frac{50\times10^6}{N} = 2\times10^3$,

$\therefore N = \frac{50\times10^6}{2\times10^3} = 25\times10^3$

Verify if TCNTBϕ can hold up to that Number

PP1117

32.4 SPECIAL FUNCTION REGISTERS

32.4.1 REGISTER MAP

Register	Offset	R/W	Descrip
TCFG0	0x7F006000	R/W	Timer Configuration Registe two 8-bit Prescaler and Dea
TCFG1	0x7F006004	R/W	Timer Configuration Registe and DMA Mode Select Bit
TCON	0x7F006008	R/W	Timer Control Register
TCNTB0	0x7F00600C	R/W	Timer 0 Count Buffer Regis
TCMPB0	0x7F006010	R/W	Timer 0 Compare Buffer Re
TCNTO0	0x7F006014	R	Timer 0 Count Observation
TCNTB1	0x7F006018	R/W	Timer 1 Count Buffer Regis

2^{32}

32.4.1.4 TCNTB0 (Timer0 Counter Register)

Register	Offset	R/W	
TCNTB0	0x7F00600C	R/W	Timer 0 Count I

Conclusion: 5-Steps operation of PWM. Can be described as (1) Count By N with Eqn (4), PP3., And deposit N into TCNTBϕ; (2) Deposit Count M into TCMPBϕ, where $M = (D.C.) \times N$ ... (5)

(3) The Down Counting will decrement TCNTBϕ's Count by 1 at a time, And a Comparison is made to TCMPBϕ, if matched, then trigger the Output to "1", Down Counting continues till the Count in TCNTBϕ = 0 One period is reached. Then Repeat this process.

Feb. 21. 21.

Example: Suppose CLK = 50 MHz, Design Implementation Technique to produce $f_{PWM} = 1000$ Hz, to Drive Stepper Motor Controller, in addition, Duty Cycle is 30%.

Find: (1) $TCNTB_n$ = ? (2) Find TCMP

Sol First find the Counts N Based on the given condition.

$\frac{50\times10^6}{N} = f_{PWM}$, ... (1)

$N = \frac{50\times10^6}{1\times10^3} = 5\times10^4 \rightarrow$ Hex

$f_{PWM} = 1000$

TCNTn

TCMPBn

Second, Duty Cycle = 30%

$$N_{cmp} = N \times 30\% \Big|_{N=5\times10^4} = 5\times10\times.3$$

$$= 1.5\times10^4.$$

Draw the Waveform.