CmpE244
Fall 2023

1/

August 21 (Monday)

Organizational Meeting.

1. The "Greenshot" is posted on the github

Note: Bring your Laptop Computer to the Class.

https://github.com/hualili/CMPE244

Course and Contact Information

Instructor:	Harry Li, Ph.D. Professor, Computer Engineering D State University
Office Location:	Engineering Building 267A
Telephone:	(408) 924-4060 (650) 400-1116
Email:	hua.li@sjsu.edu
Class Days/Time:	Mondays and Wednesdays, 4:30 pm – 5:45 pm, Aug
Office Hours:	Mondays and Wednesdays, 3:00 pm – 4:00 pm
Classroom:	Engineering Building Room 295
Prerequisites:	CMPE 180A and CMPE 180D, classified standing, c Artificial Intelligence or Computer Engineering or S majors only.

2. Emphasis on POSIX O.S. Linux Open Source O.S. & Device Drivers Programming and Development. Scalability & Vertical Solution.

Course Description

Experiments dealing with advanced embedded software programming concepts, interfacing techniques, hardware organization, and software development using embedded systems. Individual projects.

3. Course Format: In-Person.
Hands-on Class. Prototype System

Option1. NVDA Jetson NANO. GPU (128) CPU
4 GB Version JetPack

Option2. BroadCom Pie3B+, Pie4.

option3. RISC-V FPGA Dev. Board. + FreeRTOS

Has limitted Processing Power. May Not meet the Need for Our Project

Selection Decision in 1 week

Option4. NXP LPC11C24 or LPC17xx, RTOS. NXP Dev. Forum.

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4. TextBook & References

Set I: Datasheet(s), CPU Datasheet, Developer Guide; Set II: NVDA Developer Forum. Set III: PPTs, Sample Code, Handouts in the Class github.

Course Materials

Instructor's teaching materials and online resources.
1. Professor's git: https://github.com/hualili/CMPE244
2. Jetson NANO Jetpack download https://developer.nvidia.com/embedded/downloads

Other Equipment / Material

1. Hardware Equipment: You may choose any one of the following options. For detailed selection information, I will cover it in the introduction session of the class. Option 1. Nvidia Jetson NANO Board with minimum 2 GB RAM; or Option 2. Pie 3B+, or Pie 4; Option 3: Nvidia Jetson Tx2 developer kit; or Option 4: LPC1769 CPU Module: https://www.mouser.com/NXP-Semiconductors/Embedded-Solutions/Engineering-Tools/Embedded-Processor-Development-Kits/Development-Boards-Kits-ARM/_/N-cxd2t?P=1z0jm4m&Keyword=LPC1769&FS=True&gclid=Cj0KCQjwqKuKBhCKARIsACf4XuHyN8WfqtQ24WGgtoMdKd6n-kI7c-YNz-r1hTcPt0ErdZN62jrMQmgaAtXZEALw_wcB or Option 5: Samsung ARM11 developer platform.
2. Linux Host Machine (Ubuntu 18.04) .

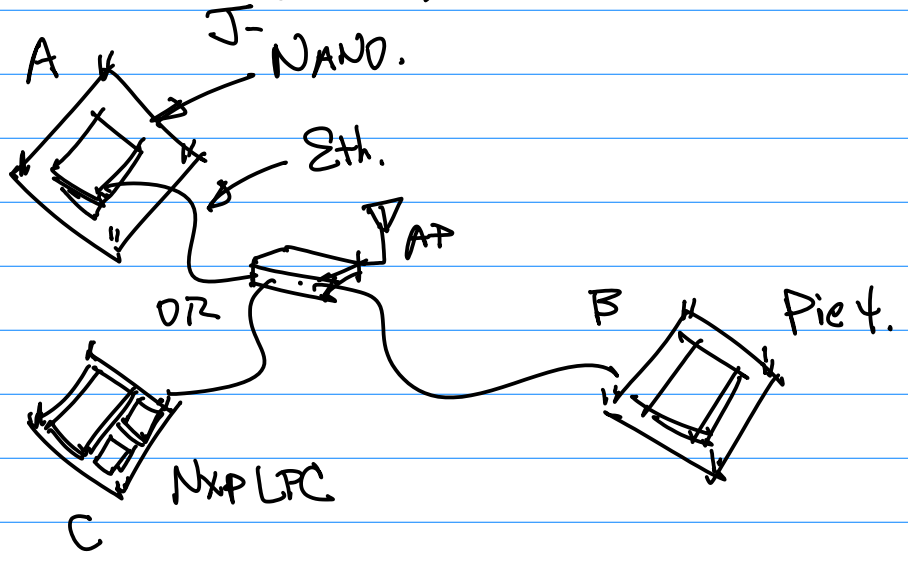
Naming Convention:

2021F-114-handout-gpi... Add files via upload
2021F-114b-pwm-nano... Add files via upload

yr. Semester ID

A & B
A & C

Note: Regarding The Selection of A Target Platform:



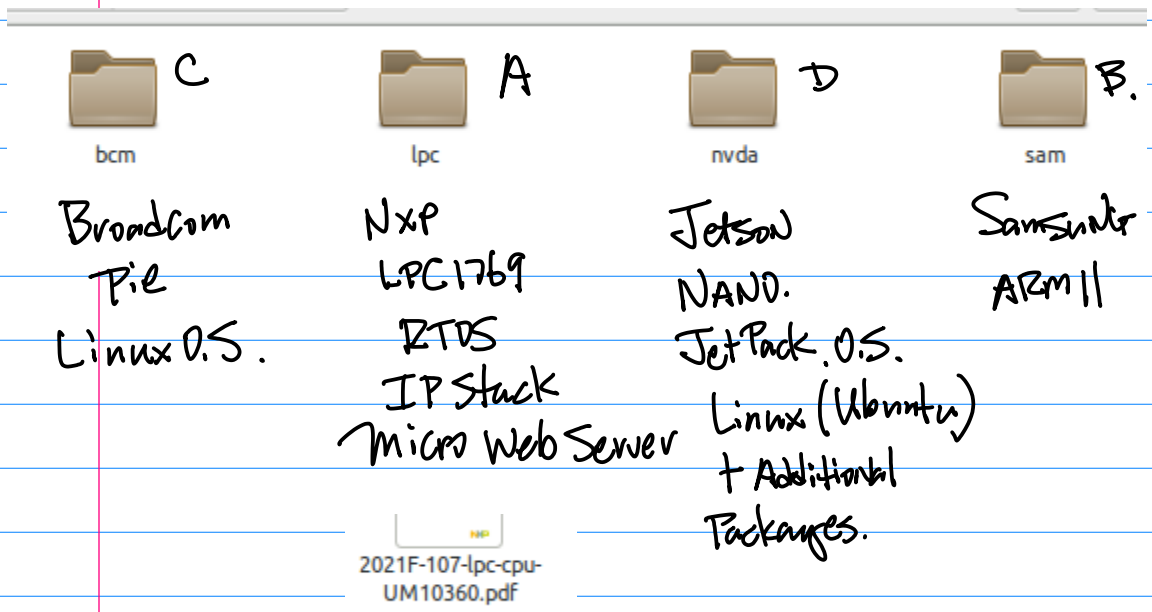
5. Grading Policy

Project Assignment: (Two Projects) Phased
15% (pts) for the assigned projects.
15% for the Semester Long Project

Assignments and projects:	30%
Midterm Exam:	30%
Final Exam:	40%
Total:	100%

August 23rd (Wed)
Introduction
Note: IZm268

Ref:
Datasheets.



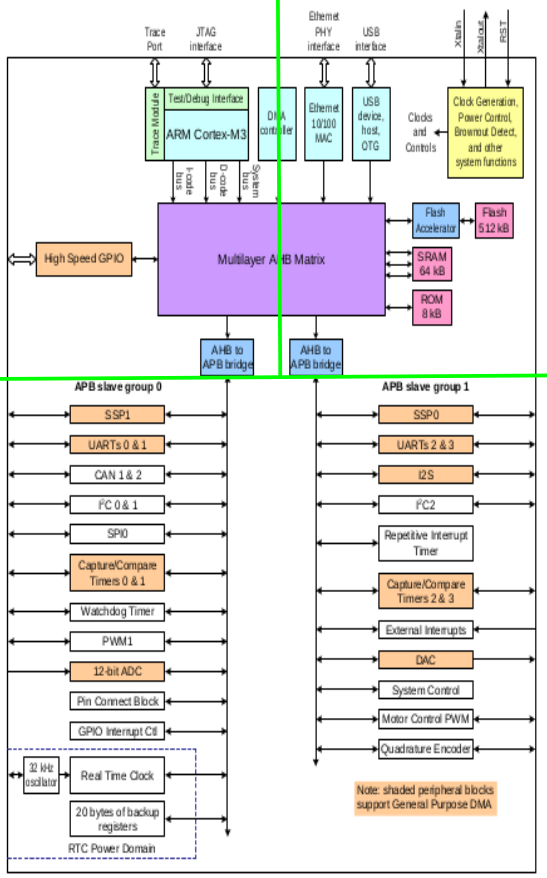


Fig 1. LPC1768 simplified block diagram

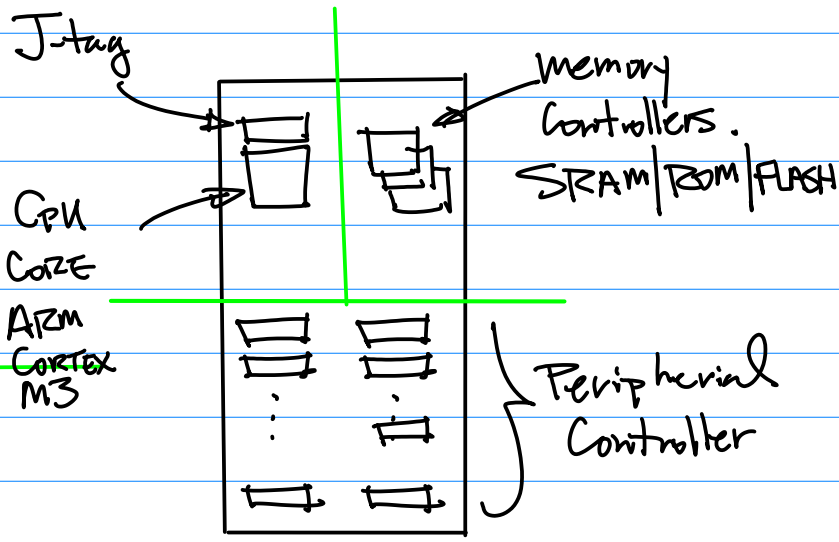


Fig. 1

Note1: The CPU Block Diagram for LPC1769 is a Sample for the Rest of the target platforms, e.g. Pre3/4; Sam's ARM 11; NVDA Jetson NANO

Note2:

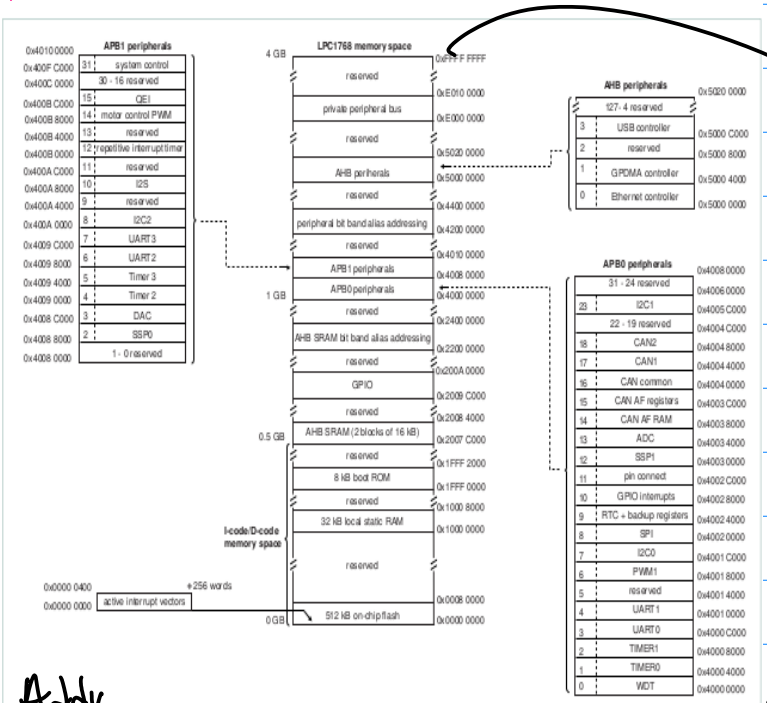
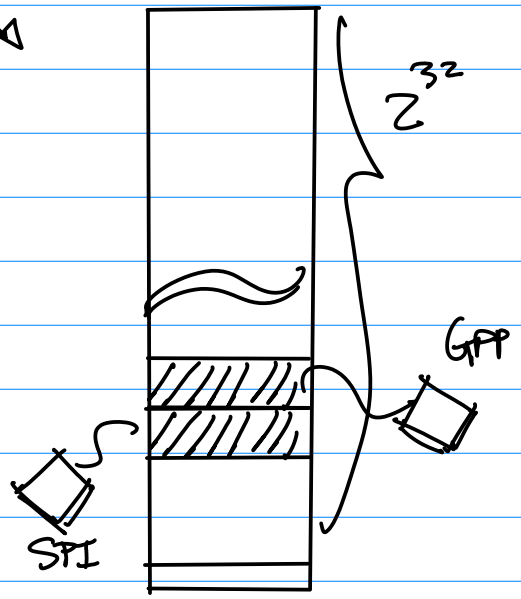


Fig.2



0x0000_0000 PWR-up Addr.

Addr.

$2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2}$

1024 : : 4

1K : :

1meg. :

1G.

4 G Addresses.

Datasheets.

2021F-105-#0-cpu-arm11-2018S-29-CPU_S3C6410X.pdf

Locate the page with the top level Description of the CPU Architecture

Example: "B", Sam's CPU ARM11

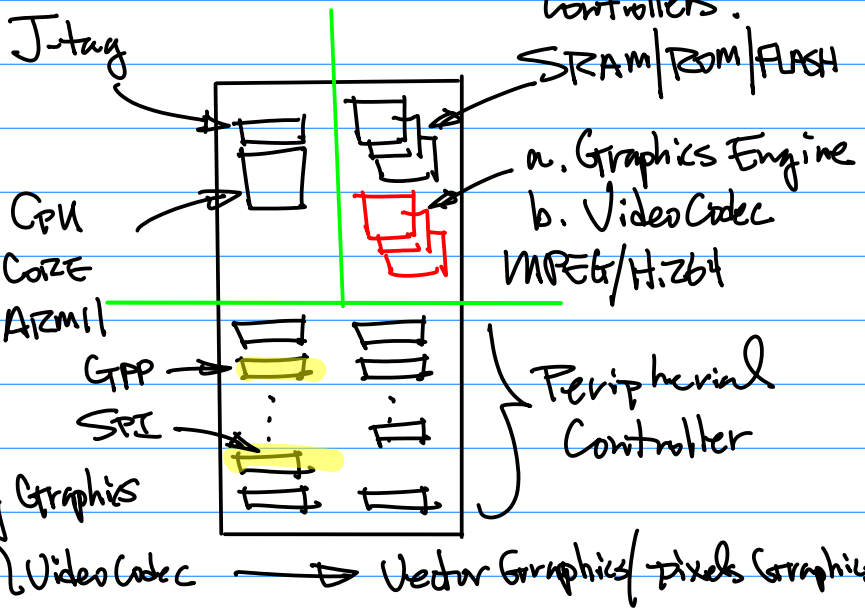


Fig.3.

Differentiation { Graphics
Video Codec → Vector Graphics / pixels Graphics

Example: Connection to (Embedded) Software Architecture

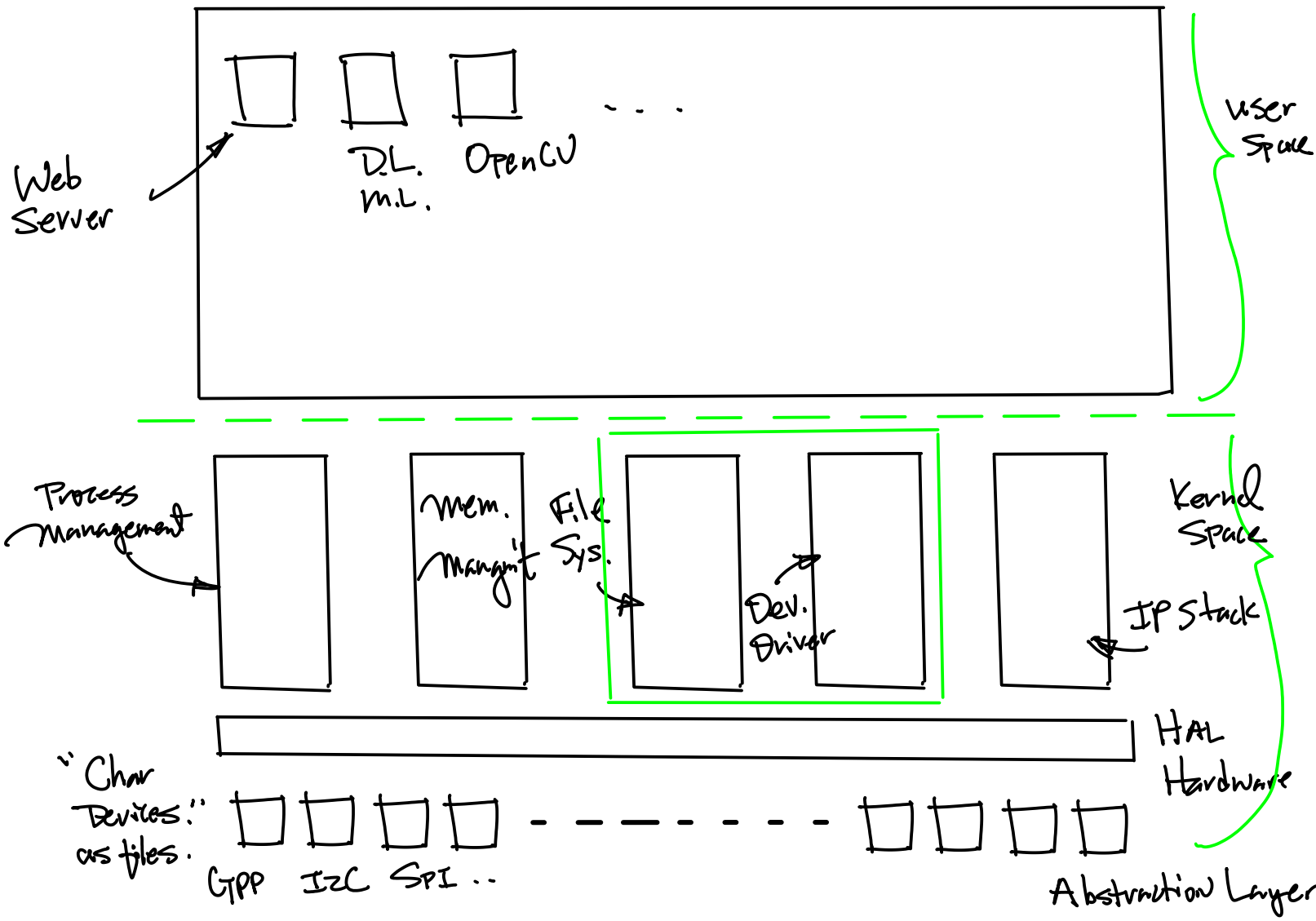


Fig. 1.

Note: Data Size for 1080P Image or 720P

August 28 (Monday)

Note: 1° Brief Description on the Scope of Semester-Long Project.

Embedded Software; Kernel O.S. Device Driver → Apps for iphone/Android phone

2° CANVAS is up. Honesty pledge

3° Target platform → Minor upgrade to Enable RTC By Adding On-Board Battery

Example: Continuation of the Introduction/Embedded Software Architecture.

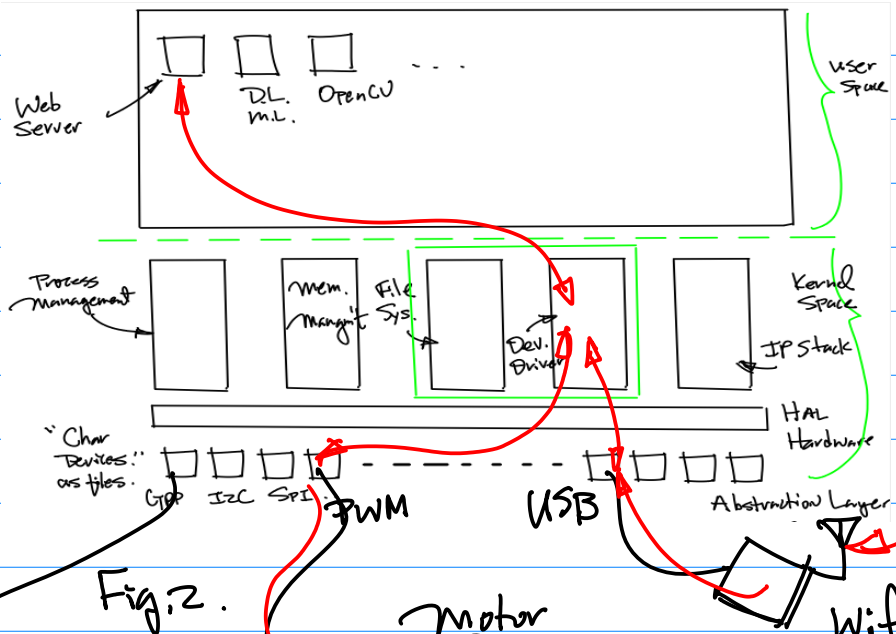
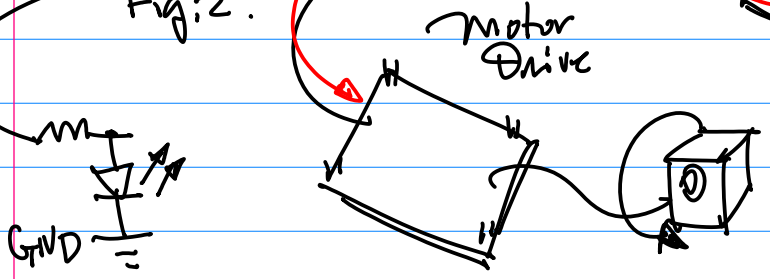


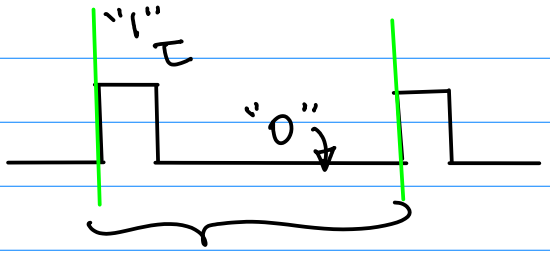
Fig.2.



Wifi/BT

Fig.2

Note: PWM — Pulse Width Modulation.



T One Period

Duty Cycle $\triangleq \tau / T$ ... (1)

f_{PWM} ... (2)

The Software Tools: One of them is open source gcc, or g++ Compiler.

C/C++ → Assembly Output

Porting.

- Match to the Core (ISA: Instruction Set Architecture)
- Device Drivers Customization.

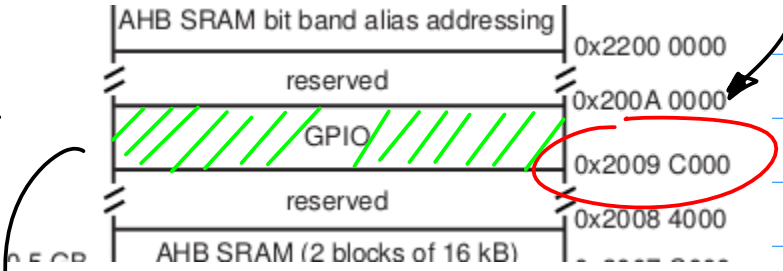
Peripheral Controller
A set of Special purpose Registers.

Identify A peripheral controller, GPP

Most Likely this SPR has the Addr in the Block.
ISA
0x2009_C000

Then, make a GPP as
(1) Output Port
(2) Turn on "LED"
(3) Turn off the "LED"
See Fig.3.

Fig.3.



Memory is designated for SPR's (Special Purpose Registers)

Go to 32Bit Control/Configuration Register. To Define Init & Config. for GPP output.

Control & Configuration Register

0xuuuu_uuuu

0x2009_C000

GPx_CON

For Selection of Port & Pin(s).

4 G Possible Configurations Theoretically
$(2^{32} = 2^2 \cdot 2^{10} \cdot 2^{10} \cdot 2^{10})$

1K 1K 1K

1M

1 G.

It has its unique Address (at the multiple of 4).

Coding (Software Aspect)
Write 32 bits unsigned Data as Init & Config pattern to select the GPP & the pin as output.

Next. Naming Convention.
Guideline:
RISC → UC Berkeley, David Patterson
Stanford, John Hennessy.

August 30 (Wed)

Note: 1° CANVAS is up.
Honesty Pledge to Be Signed
And Submit ON CANVAS
By this Friday 11:59 pm.

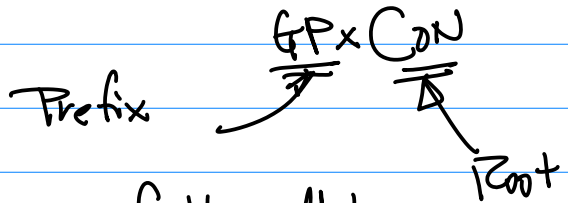
2° Please Bring the target platform to the Class. Next Wednesday.

3° (Written Requirements) in 2 Week
Bring up your target platform
By Down Loading Kernel OS.
Image to A micro-SD Card,
then boot the System.
then Screen Capture with your personal identifier, Submit it ON CANVAS.

4° Create A ChatGPT Account, Python interface to Chat GPT (3.5) API.

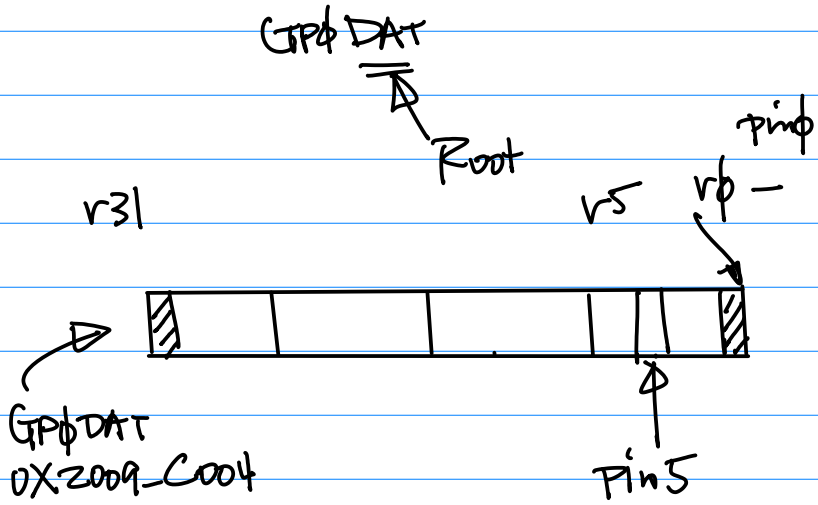
Example: Continued.
Naming Convention of the Control & Configuration Register.
By John Hennessy. Golden Rules
Uniformity,
Regularity,
Orthogonality
"3+3" Naming Convention

Prefix + Root
3 Letters 3 Letters.



for the multiple GPPs,
we have
GPBCON, GPICON, etc.
Suppose we want to use GPB pin 5 as an Output to turn ON/off LED.

Design 2nd SPR.



place "1" @ r5 to Output Logical high.
"0" .. ...
Low.

#define GPBCON
.. GPBDAT

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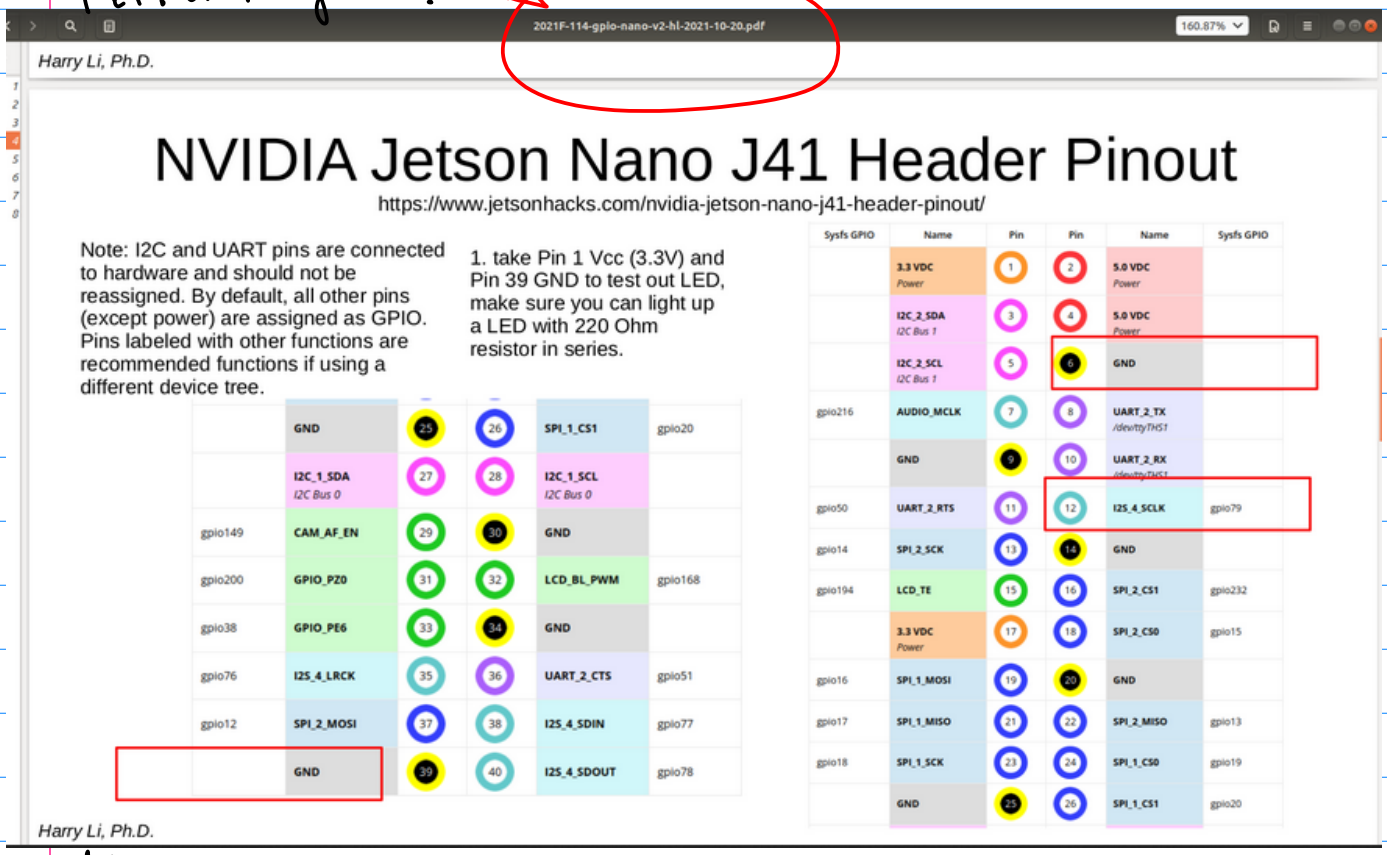
Porting Porting
gcc/g++ → ARM → CORTEX
Porting ↓
Board

Sept 6 (Wed).

Note: 1° Target Board
Inspection:

Purpose: J41 Connector
RTC Battery
Ref: ON the github. 2021F-114~



Note: 1° Power Pins
- GND: 6/9/25/39
- Vout 3P3VDC/5VDC Pin1 Pin2,4.
- Vin: J25 (5A or higher @5VDC)

Note2° GPIO

J41 Pins	CPU Functionality
J41-12	gpio79
J41-40	gpio78

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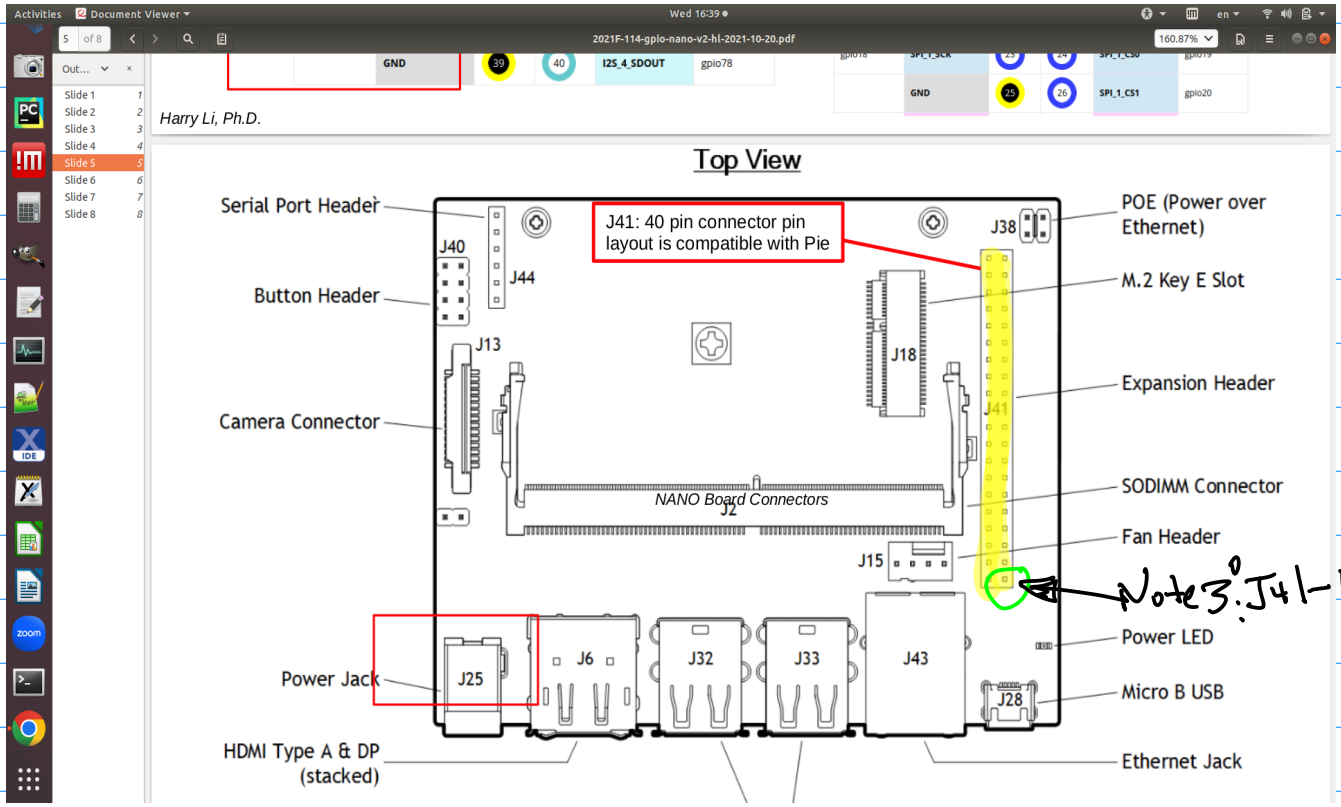
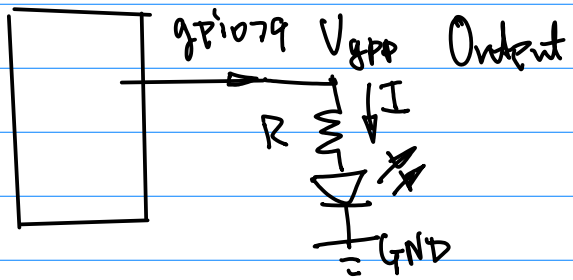
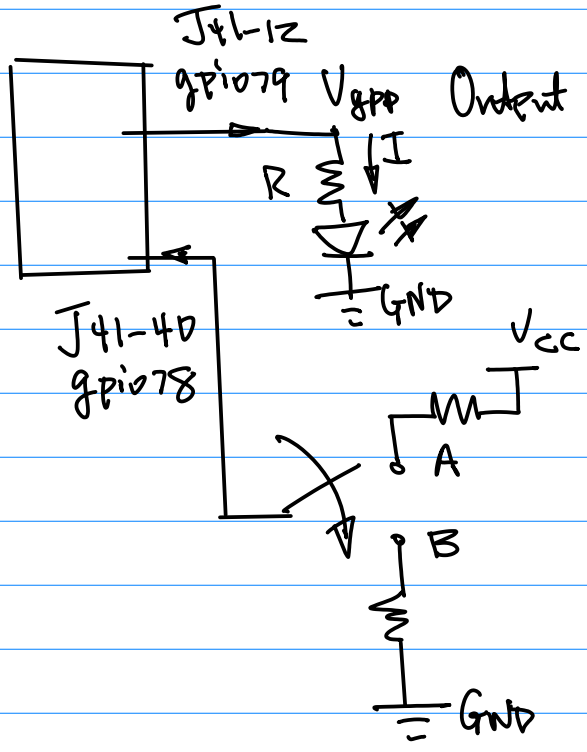


Note 4°: GPIO Input/Output Testing CKT

Build the following Testing CKT.





Let $I = 4mA$, $V_{LED} \simeq 1.8V$

$$V_{gpo,H} = IR + V_{LED} \quad \cdots (1)$$

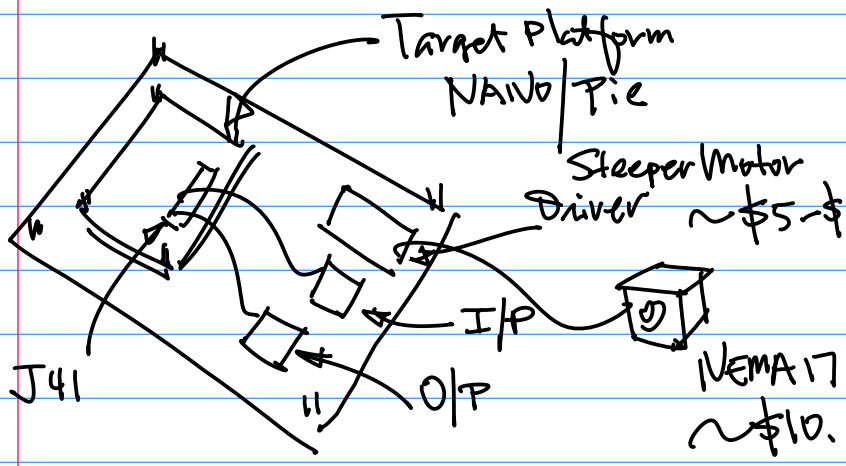
W/O Resistor with Proper Selected LED.

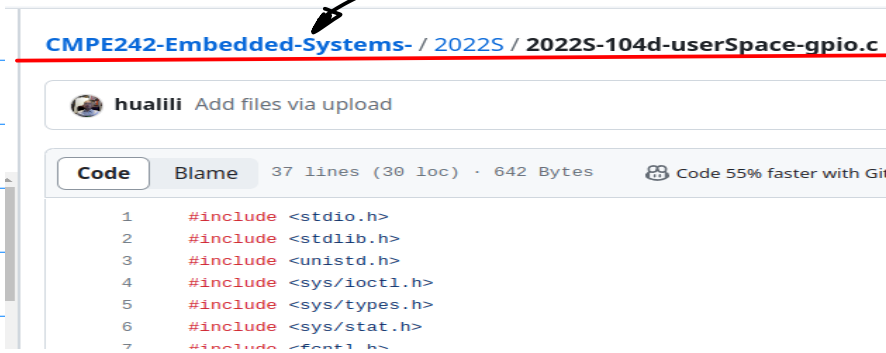
GPIO J41 Pins	CPU Functionality	Note
J41-12	gpio79	Output
J41-40	gpio78	Input

Code { User Space Code
Kernel Space Code

Take a Reference Design from ARM11, Samsung CPU.

Ref: Sample code has been posted on the github.





Note: Form 2-person Team for A Semester Long Project.

Scoop: Hardware Layer (Sensors/Actuators) "Secuator"

↓

Device Driver / Kernel Space Process Management

↓

Web Server

↓

Smartphone APPs.

Chat GPT 3.5 API + Python Interface

Example: Sample Code for GPP Device Driver