

Embedded Platform

Embedded Platform Selection:

1. 32 bit RISC, ARM CPU is recommended;
2. RTOS supported is desired and recommended;

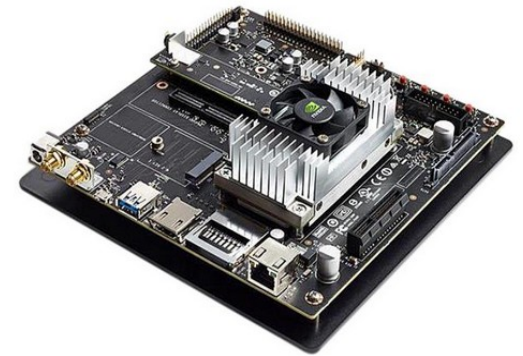
RF Module Selection:

1. PSK is desired to match up to IEEE 802.11x and industrial Commonly adopted RF modules, with balancing consideration of performance, cost, and educational/class usage; FSK and ASK are all ok for this class use. However, you may find ASK is the most popular low cost RF module without MAC (Media Access Layer) layer implementation (we will implement MAC layer in C/C++ in the class) ;

Industrial IoT Aspect:

1. Use this high end RF module. 4 person team will be formed , each team with one module. Hence, you will be required to work with other team for a project implementation.

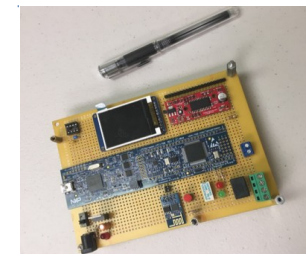
<https://www.digikey.com/product-detail/en/semtech-corporation/SX1276RF1IAS/SX1276RF1IAS-ND/4490401>



TX2 NVDA GPU



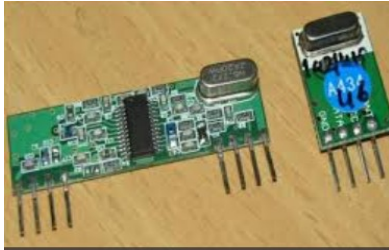
Raspberry Pie



NXP
LPC1769

Wireless Modules

Cat I



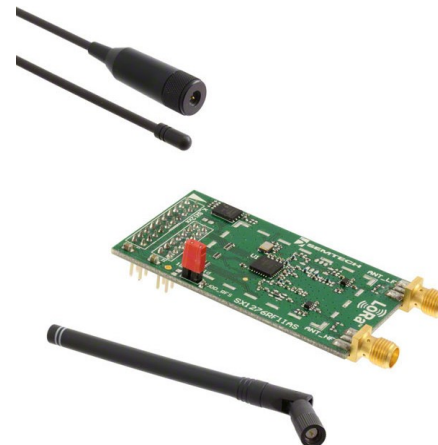
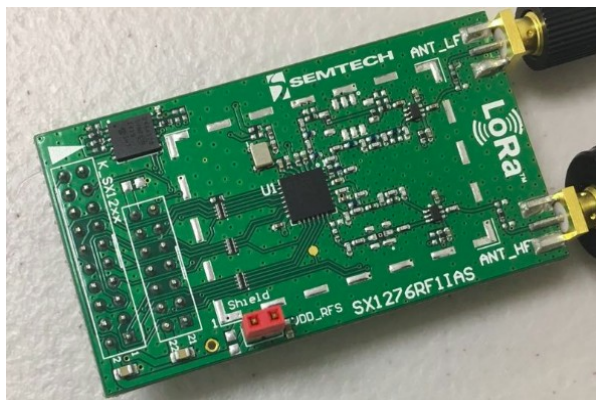
For Software Defined Radio and CR
(Cognitive Radio) Project Implementations

Google ASK RF module

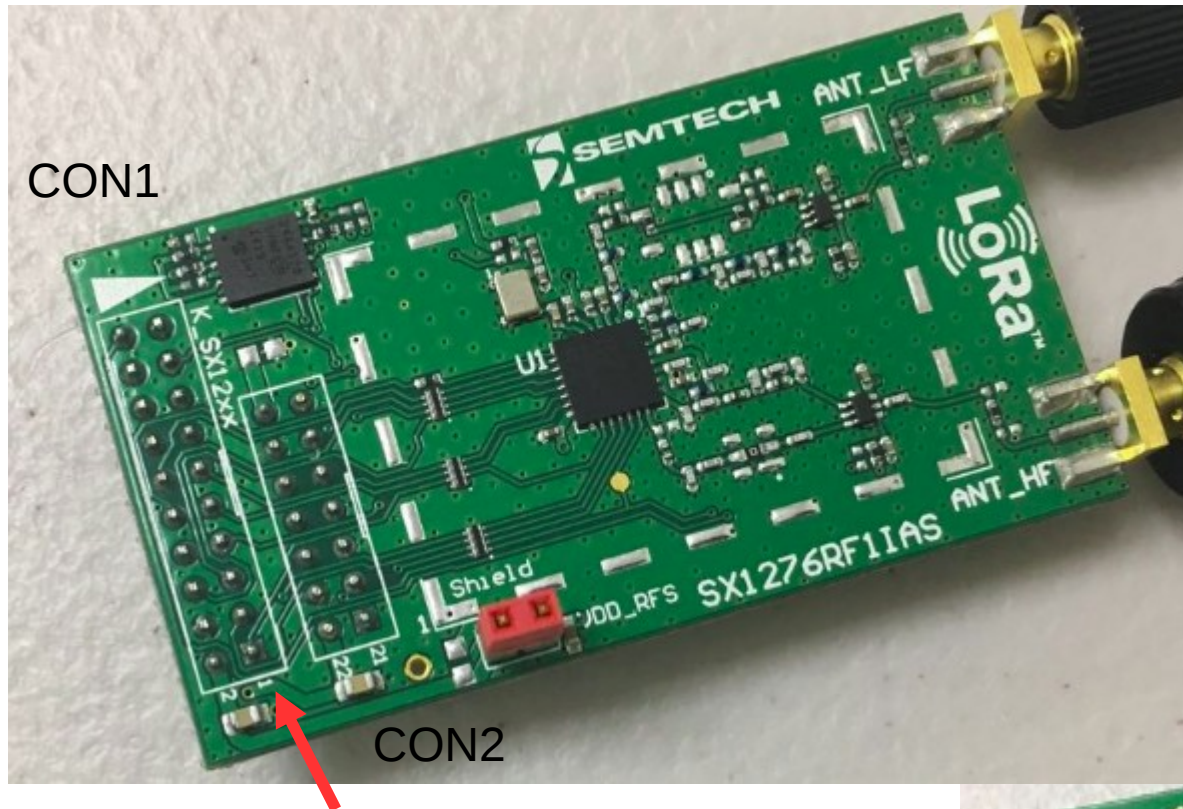
Cat II



For state-of-the-art
Industrial IoT applications



SX1276RF1IAS Modules I



For Real Industrial IoT Applications

For the design interface to embedded systems: SPI interface.

To Buy:

https://www.mouser.com/ProductDetail/Semtech/SX1276RF1IAS?qs=rBWM4%252bvDhleJeGldE033Lg%3D%3D&gclid=EAlaIqobChMI34irpMn_3AIVBMJkCh0e2gc8EAAYASAAEglWMPD_BwE



Document

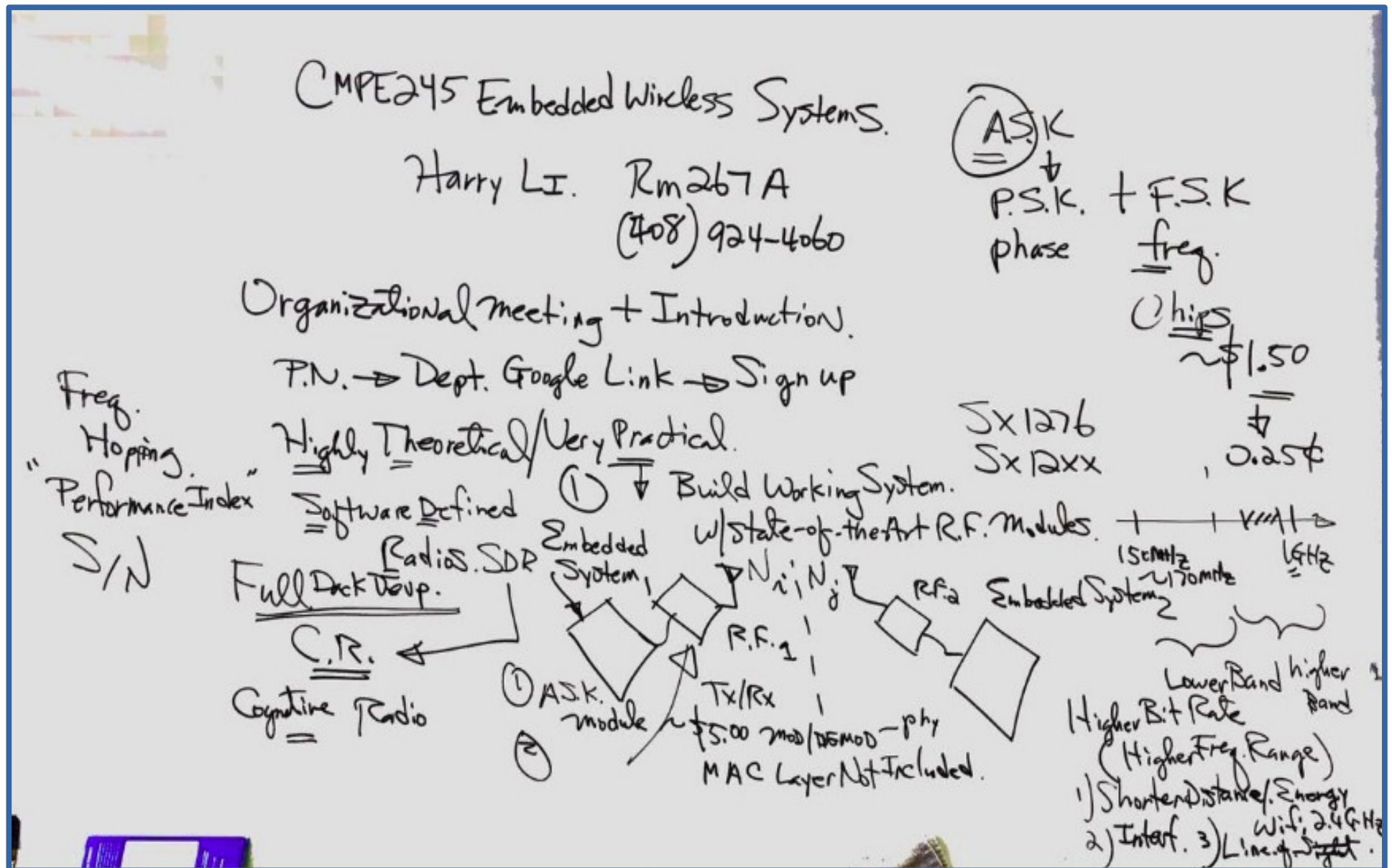
1. IEEE 802.11b Standard for Software Defined Radio and CR (Cognitive Radio) implementation, also for theoretical/mathematical discussion.
2. Datasheet of sx1276rf1ias for state-of-the-art industrial IoT implementation throughout the semester.
3. Check my github for document, references and design notes, lecture notes and sample code

<https://github.com/hualili>

Other resources

<http://www.ctione.com/>

8-22-2018 Organizational Meeting



8-27-2018 RF Module Requirements

CMPE245 Embedded Wireless.

August 27, 2018 1/.

Today's Topics:

1° Introduction. (Prototyping Board Design)

Objectives: IEEE 802.11x

① Embedded platform Software Defined Radios (SDR) → Smart

LPC1769

NXP
(OR Optional
Ras. Pie
ARM11)



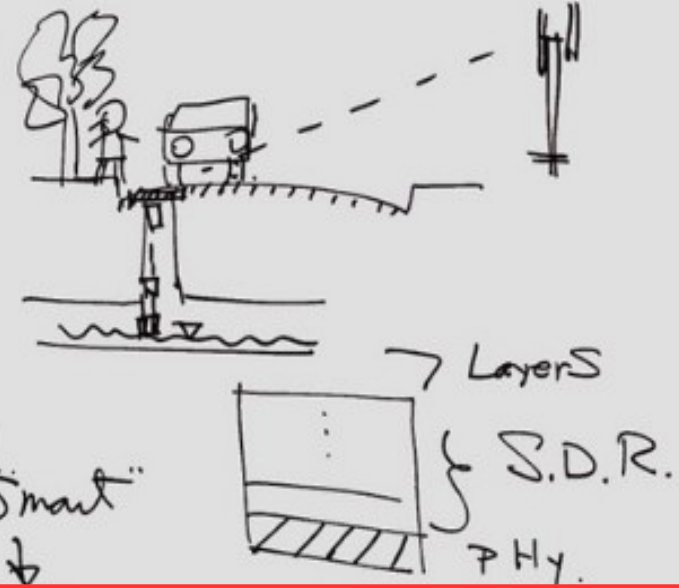
N_i
($N_i - N_2$)

② 1° R.F. (to Implement "all" MAC)

2° R.F. IOT "State-of-the-Art"

3° Debugging.
Wired (Cable) Communication

③ Tx/Rx C.S.R. (Low Cost Module) ④ F.C.C. 433MHz
ASK (Amp. Shift Keying) ⑤ Data sheet 315~
Microchips Wiring Diagram(s) < 1000mW
Sx1276. ⑥ S.P.I. ⑦ ANT Included
150MHz 1.4GHz (~1000MHz)



8-27-2018 Build Tech Spec For Prototype Design

CMPE245 August 27. Harry Li 2/.

Homework: Table(Tech. Spec) 1.
For Prototype Design.

No	Description	Notes
1.	RFxLPCxxx	<u>SXm+LRA+n76</u>
2.	RFxLPCxxx	
3.	RFxLPCxxx	

Naming Convention. 9 Letters.

Pref(3)+Root(3)+Post(3)

EMD

RFx + LPC + nnn → RFxLPCxxx

RFxASKTxφ, RFxASKRxφ

Option (Cognitive Radio Module):
CR0+LRA+IOT

Embedded System:
RF0+LPC+NOD

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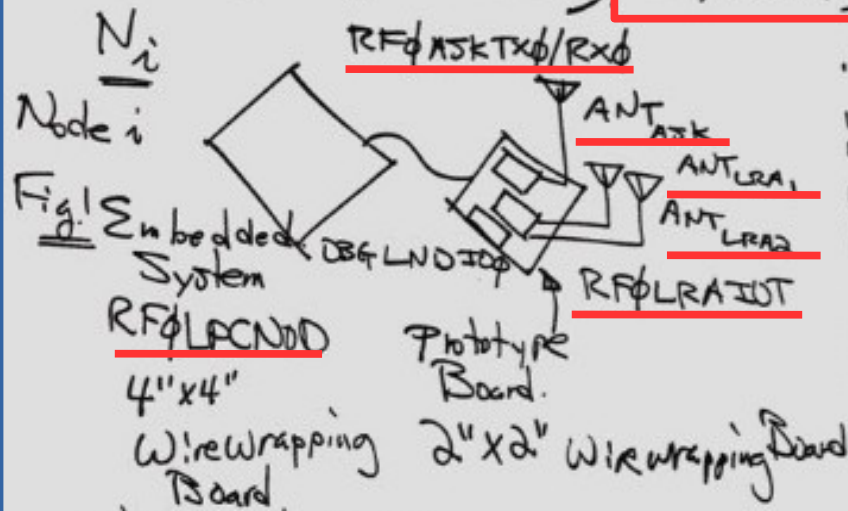
Embedded System:
RF0+LPC+NOD

8-29-2018 Prototype System Block Diagram

CMPE245 Embedded Wireless Aug 29, 2018
Harry Li 1/.

Today's Topics: 1° Tech. Spec. 2° Design Prototype System.

Example: (Homework) **System Block Diagrams**



a) Frey Electronics

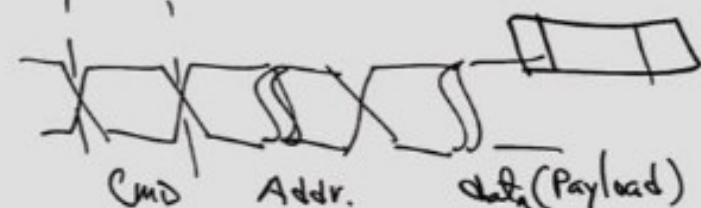
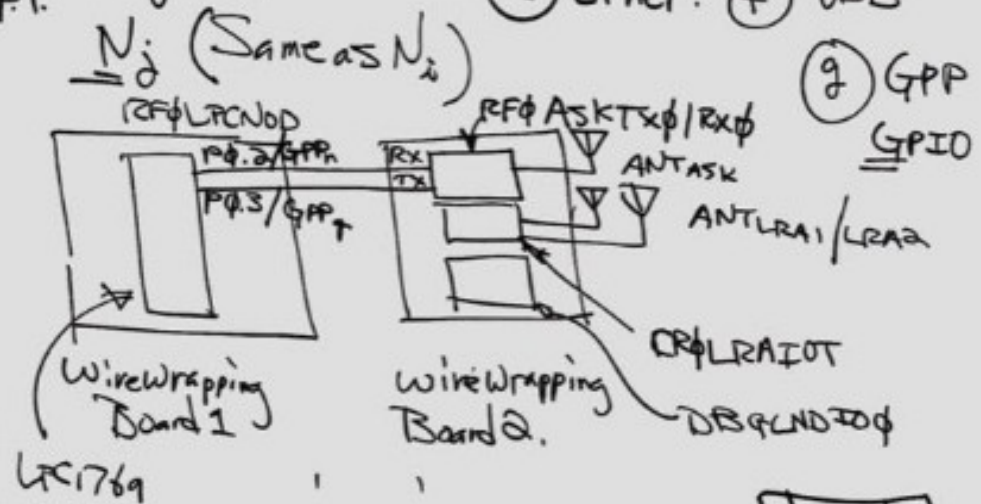
b) Halted Computers H.S.C. Central Expwy + Corwin

Pin Assignment of LPCNOD

ASK { TX I/P GPPn }
RX I/P GPPB

CPU ? RX TX ANT

Protocols: (a) SPI (b) Serial Peripheral I2C (3+1) (c) UART (3) (d) CAN (2) (e) Ether. (f) USB



8-29-2018 Prototype System Block Diagram

CMPE245 Embedded Wireless 2/
Homework: Harry LI

Table 2 Pin Assignment (RF0LPCNOD w/
RF0ASK TX ϕ /RX ϕ)

\sim ASK \sim	RF0LPCNOD	Note
RX (?)	GPP _n / P ϕ .2	I/P
Tx (?)	GPP _g / P ϕ .3	O/P

Prototype System	
RF0LPCNOD	Embedded System
RF0ASKTX0 RF0ASKRX0 ANT0_ASK ANT1_ASK	Tx for RF module 0 Rx for RF module 0 ANT for the Tx ANT for the Rx
CR0LRAIOT ANT0_LRA ANT1_LRA2	RF module for CR ANT0 for the RF module ANT1 for the RF module

Note: 1. Naming ON SCH of the LPC1769 module. CPU Datasheet \rightleftharpoons Protocol \rightleftharpoons 3rd Party

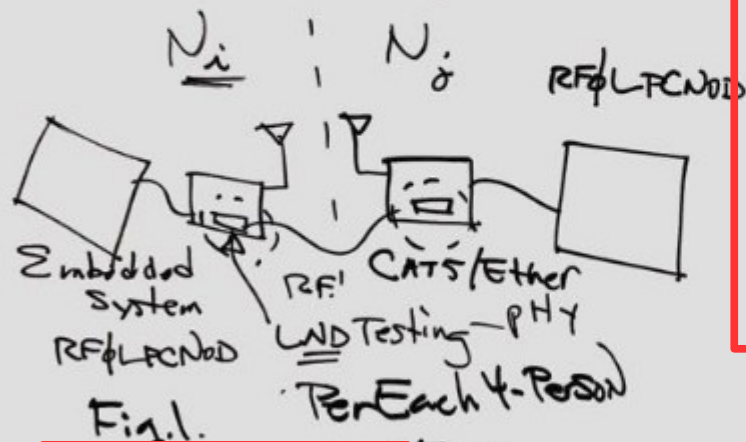
9-5-2018 Feature List

CMPE245 Embedded Wireless

Sept. 5, 2018 Harry LI 1/.

Today's Topics: 1st Prototype Board Design.
for Sync. Implementation.

System Block Diagram Table(s) → LND Testing Unit (1) Homework



Note: Use SW to Switch
ON/OFF Testing Ckt
Homework: Block Diagram.

Feature List Table 1

No.	Description	Notes
1. Cable	CATS	
2. RJ45	Ethernet Connector	8 Pins. Colour Coded
3. Cable(s)	RF/LPC Node B/w RF Board. (LND)	Soldering.
4. O/P.T.	2x GPP x GPP, LED ON for "1", off for "0"	Output Testing
5. I/P.T.	Input Testing, SW Toggle	Vcc → "1" GND → "0"
6. SW unit	Turn ON/OFF OPT./IPT	LND Comm. ON/OFF.

Build table 1 feature list for the RF prototype board

9-5-2018 Timing Information

CMPE245 Embedded Wireless 2/
Sept. 5th 2018

Naming Convention: 245rep-LW+HL+2018-09-05.
① ② ③ ④

lec 1-3-4-7-9-0-

RJ45 Connector (Right Angle) H.S.C. Halted Computer

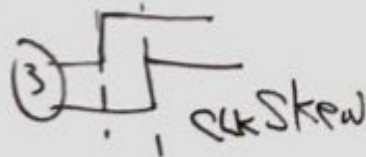
Sync Algorithm Development

Central Expwy+Lawrences.
CORVINDRI.

Objectives: To Establish Hand Shaking
B/W 2 Nodes

Technical Challenges:

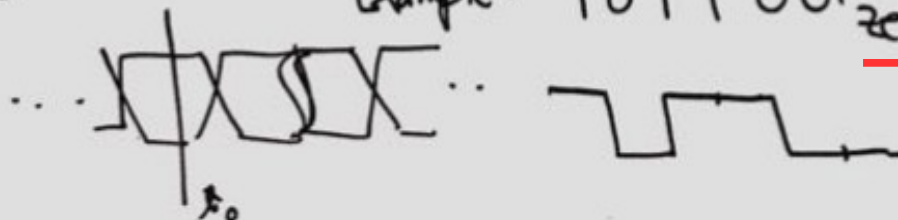
① N_i N_j ② bitRate
Digital Comm. "1" & "0"



Observation 1:
Same bit Rate
But always w/
Clock skew.

Question: Given a sequence
of digital signal, "0's and "1's",
which part(s) carries Timing
information? → Change of
the State

Example: 101100 "zero crossing"



Observation 2: Timing information
is embedded in the "zero-crossing"
Change of the State.

Observation 3: For N-bit
Sequence, we can have as
many as N-1 Change-of-State
as possible to maximize
Timing information