

August 25 (Wed)

CMPE245

Introduction.

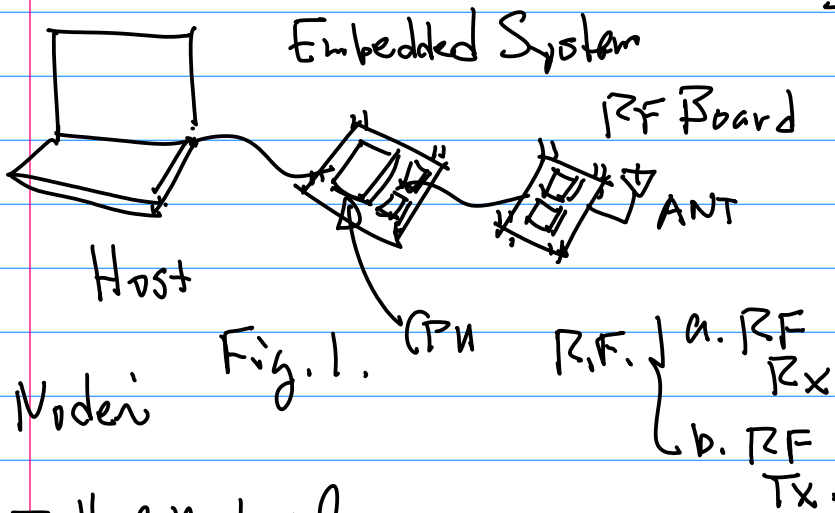
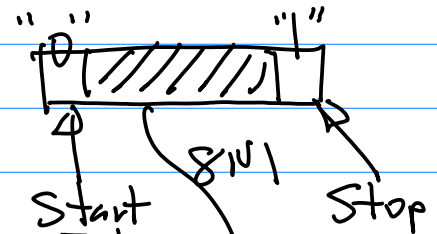
Today's Topics

Bill of Materials
Target platform
For Prototyping

Note: Your RF module(s)
is to be interfaced to GPIO
of your target Board.

Why? General Purpose \rightarrow No
Data Framing.

for UART, Data Frame



Node

Bill of Material

1. Target CPU NXP LPC1769
OR NAND (NVD)

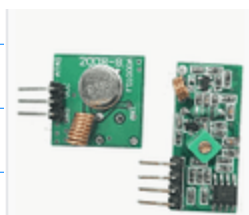
2. RF modules, physical layer only.

(2) ASK R.F. module, frequency $\sim 433\text{MHz}$
F.C.C. Certified

Amplitude Switching

(3) Open Spectrum.
Power $\leq 1000\text{mW. (1W)}$
Tx: Transmitter

(4) No MAC (media Access Control)
Needed



Note: CPU Target

Option to use NVD Jetson
NANO

Guide Line for Selection
of target Platform.

1. Register Level Control
of GPIO, SPI Controllers

For LPC1769 ✓

For NAND \rightarrow Devices
Drivers.

(1) Datasheet + root pages

(2) Software Dev.
Environment, tools.

Jetpack (OS +
Libs)

(3) O.S. Distr.

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Note: ON your RF Board.

2

2^o Access to CPU pins, e.g.
GPIO pins, SPI pins.

Homework: Purchase ASK RF
Module By Sept. 8th (Wed)
OR ideally Sept 3rd (Fri)

Note: To provide Hardware Debugging CKT. on
the RF Board

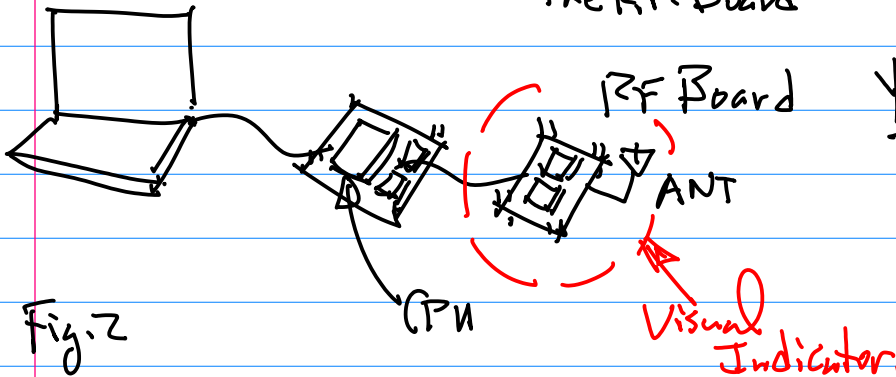


Fig. 2

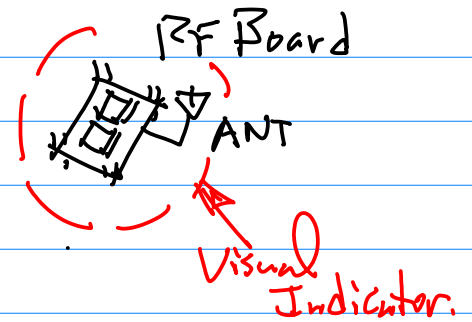


Fig. 3.

2 Blocks { Rx
Tx
Both Need to Be Powered.

You may want to have the
DC PWR Delivered via
CAT5 Cable from your
Embedded Board.

RJ45 Pins (Pin): 8

Debugging Capability on the R.F.
Board:

(1) Objective: To visualize/observe
GPIO output.

Means: LED.

Material:

a LED (Red, Green), 4~10mA

Connectors (to cable to RF Board)

b RJ45 Right Angle Connectors

(2)

A piece of CAT5 Cable (Ethernet)

c Components { Resistors
Chps.

(1117?)

7805, 7812 OR

August 30th.

RF module, to Build
RF Board.

1^o ASK RF.

Amplitude Switch Keying

2^o Rx: Receiving

TX: Transmission

3^o GPIO J/F

Regulator Data Pin

Homework: Identify/Bring Your Wire Wrapping Board for RFB Design. 4x3 Inch;

To Build RFB

1° Board

2° 4 standoffs

3° Build I/O I/F Testing CKT.

To Light up LED when CPU output "1"

To Turn off LED when CPU output "0"

Output Testing

SW Toggles to Vcc, when Vcc, CPU Reads as "1"

SW " " to GND, CPU Reads as "0"

Input Testing

4° CAT-5 Ethernet Cable

RJ45 Right Angle Connectors (2)

One for Embedded;
One for RF Board,

5. Power Distribution to RF Board:

a 5VDC is adequate
But R.F. module can be operated with

Bigger Power, 9VDC

OR 7.5VDC may be needed during Debugging;

ing;

Sept 1. (Wed)

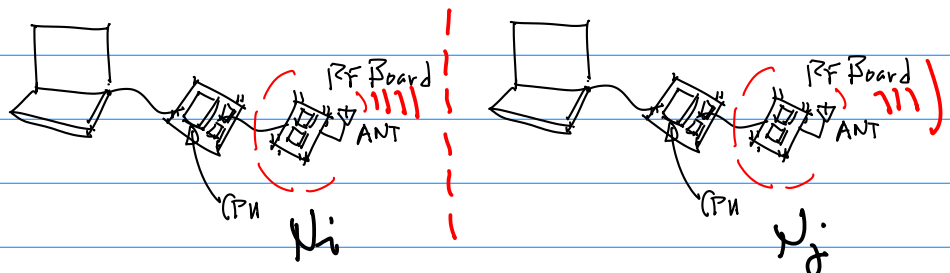
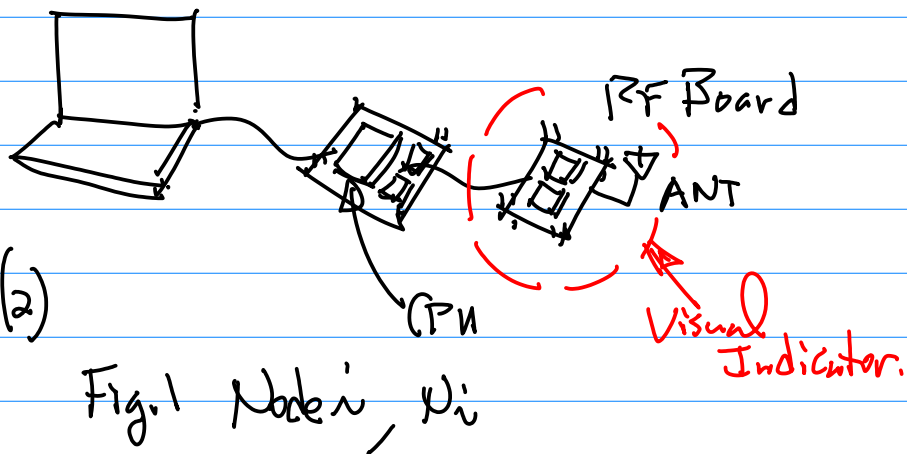
Ref: IEEE 802.6

1. github/Rualili/cmpe245/2018F

"2021F-"

2. Topics: Design R.F. Board for the 1st homework. 2pts. (Hardware)

From PP.2. System View



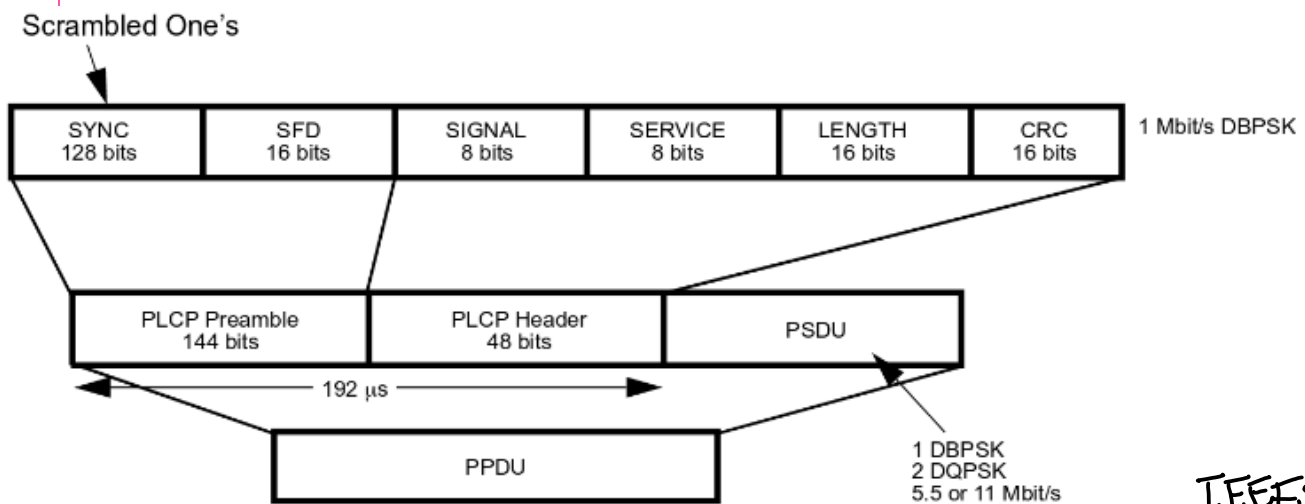
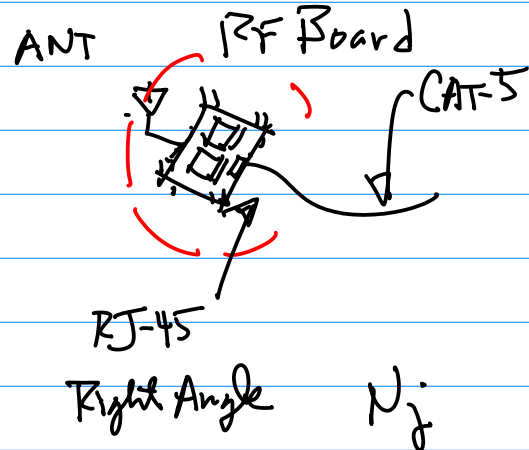
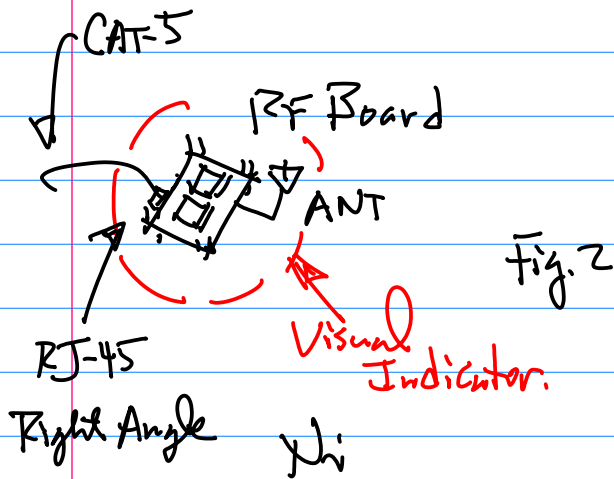


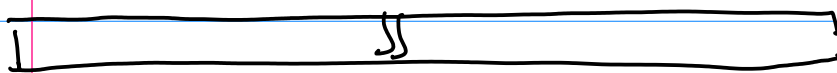
Figure 127 - Long PLCP PDU format

IEEE 802.6

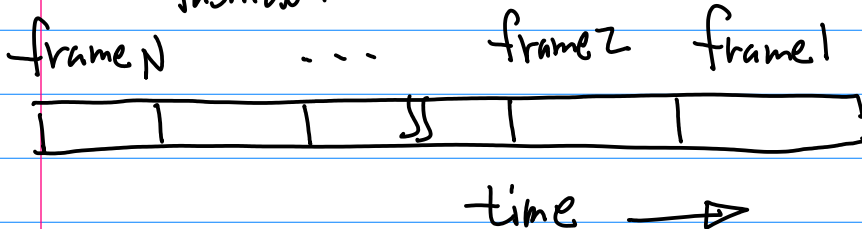
Fig. 3. TP.13

Node N_i , Node N_j , Each Node is illustrated in Fig. 1.

Sending Stream of Data from N_i to N_j



String of Bits Sent in A "Framed" fashion.



Note: Consider the Construction of Each frame, frame i , $i=1, 2, \dots, N_j$

What are the Contents to be placed into A Frame?

Like start bit(s) → to Mark the Beginning of the Communication.
→ Timing/Sync.

C.R. (Cognitive Radio), SDR (Software Defined Radio)

multiple Bits in Sync. Design \rightarrow more Reliable \rightarrow "Robust" performance
Maybe

Question: What is the general guideline in terms of designing "Sync" Field?

The Objective for R.F. Board Framework/Design: To Allow N_i, M_j to Sync.

multiple Bits of what?

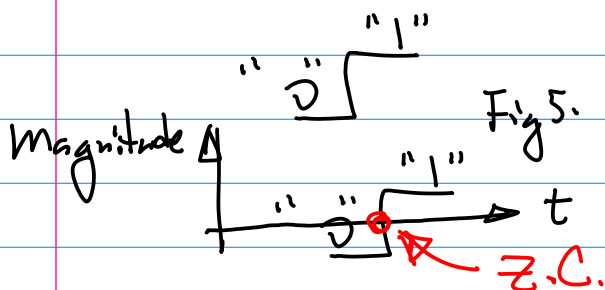
3 bits Example: $2^3 = 8$

b2	b1	b0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Transition \rightarrow Change of State

"Zero Crossing" \rightarrow

for Example "1" \rightarrow "0" or



To provide best possible "Transitions", e.g. "Z.C."

Pick 0x5 Binary: 101

2-Step Approach:

Step 1. Based on Land Line;

Step 2. then R.F. (Wireless)

Hence, R.F. Board will have to Support 2 Options.

