

August 25 (Wed)

CmPE245

## Introduction.

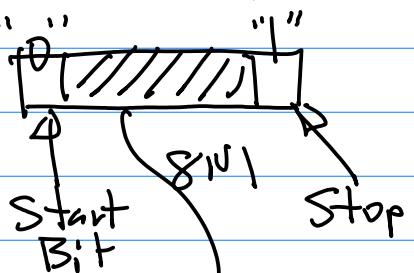
Today's Topics

Bill of Materials  
Target platform  
For Prototyping

Note: Your RF module(s) is to be interfaced to GPIO of your target Board.

Why? General Purpose  $\rightarrow$  No Data Framing.

for UART, Data Frame



Payload, Data, 8 Bit

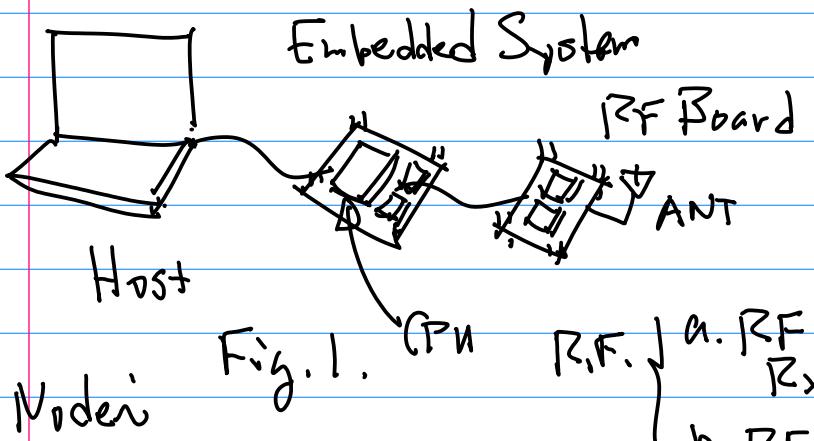


Fig. 1.

## Bill of Material

1. Target CPU NXP LPC1769  
OR NAND (NVDA)

2. RF modules, physical Layer only.

(1) ASK RF module, frequency  $\sim 433\text{MHz}$   
FCC Certified

Amplitude Switching

(2) Power  $\leq 1000\text{mW. (1w)}$   
Tx: Transmitter

(3) No MAC (media Access Control)  
Needed



Note: CPU Target

Option to use NVDA Jetson  
NANO

Guideline for Selection  
of target platform.

1. Register Level Control  
of GPIO, SPI Controllers

For LPC1769 ✓

For NAND  $\rightarrow$  Devices  
Drivers.

(1) Datasheet 400+ pages

(2) Software Dev.  
Environment, tools.

Jetpack (OS +

(3) O.S. Distr. Libs)

August 25 (Wed)

2° Access to CPU pins, e.g.  
GPIO pins, SPI pins.

Homework: Purchase ASK RF

Module By Sept. 8th (Wed)

OR ideally Sept 3rd (Fri)

Note: On your RF Board.

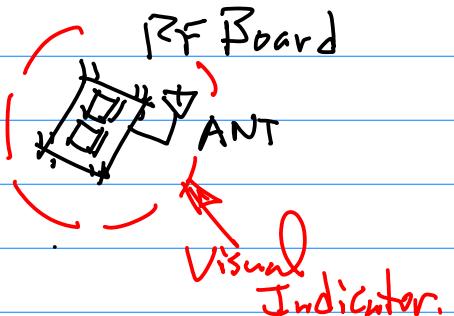


Fig. 3.

2 Blocks { Rx  
Tx

Both Need to Be Powered.

You may want to have the DC PWR Delivered via CAT5 Cable from your Embedded Board.

RJ45 Pairs (Pin): 8

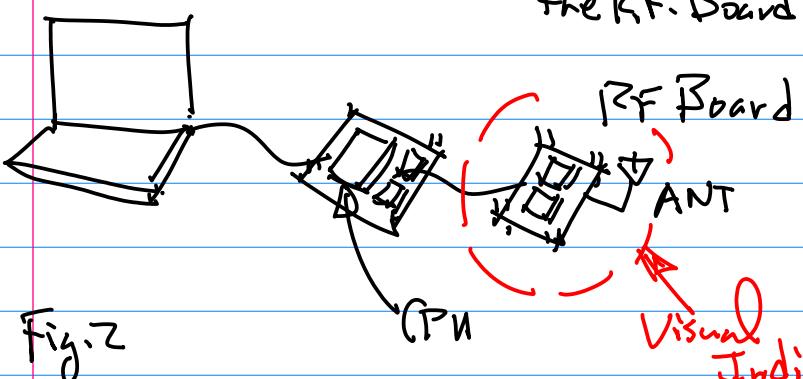


Fig. 2

Debugging Capability on the RF Board:

① Objective: To visualize/observe GPIO output.

Means: LED.

Material:

a LED (Red, Green),  $I \approx 10\text{ mA}$

Connectors (to cable to RF Board)

b RJ45 Right Angle Connectors (2)

A piece of CAT5 Cable (Ethernet)

Components { Resistors  
Capacitors

1° ASK RF.

Amplitude Switch/Keying

2° Rx: Receiving

TX: Transmission

3° GPIO I/F

Regulator Data Pin

(111?)

7805, 7812 OR

August 30th.

RF module to Build  
RF Board.

Homework: Identify/Bring Your  
Wire Wrapping Board for RFIB  
Design. 4x3 Inch ;

To Build RFIB

1° Board

2° 4 standoffs

3° Build I/O I/F Testing CKT.

To Light up LED when CPU Output "1"

To Turn off LED when CPU Output "0"

Output Testing

SW Toggles to V<sub>cc</sub>, when V<sub>cc</sub>, CPU  
Reads as "1"

SW " to GND, CPU  
Reads as "0"

Input Testing

4° CAT-5 Ethernet Cable

RJ45 Right Angle Connectors (2)  
One for Embedded ;  
One for RF Board ,

5. PWR Distribution to RF  
Board :

= 5VDC is adequate  
= But RF module can

be operated with  
Bigger Power, 9VDC  
or 7.5VDC may be  
needed during Debugg  
ing;

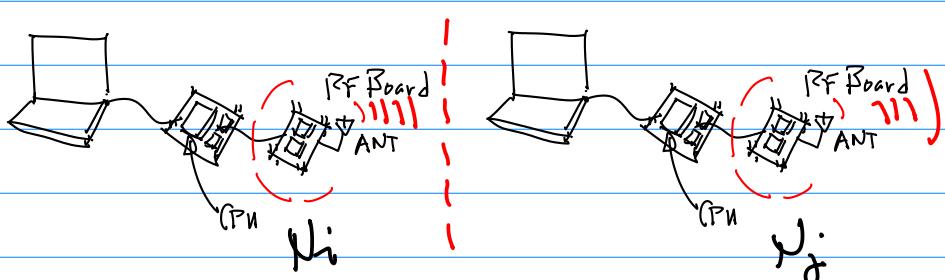
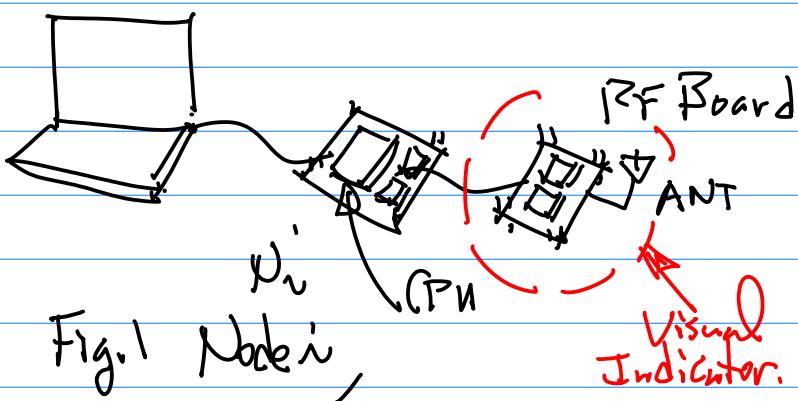
Sept 1. (wed)

Ref: IEEE802.6

1. [github.com/alili/cmpe245/2018F](https://github.com/alili/cmpe245/2018F)  
"2021F -"

2. Topics: Design R.F. Board for the  
1st homework. Zpts (Hardware)

From PP.2. System View



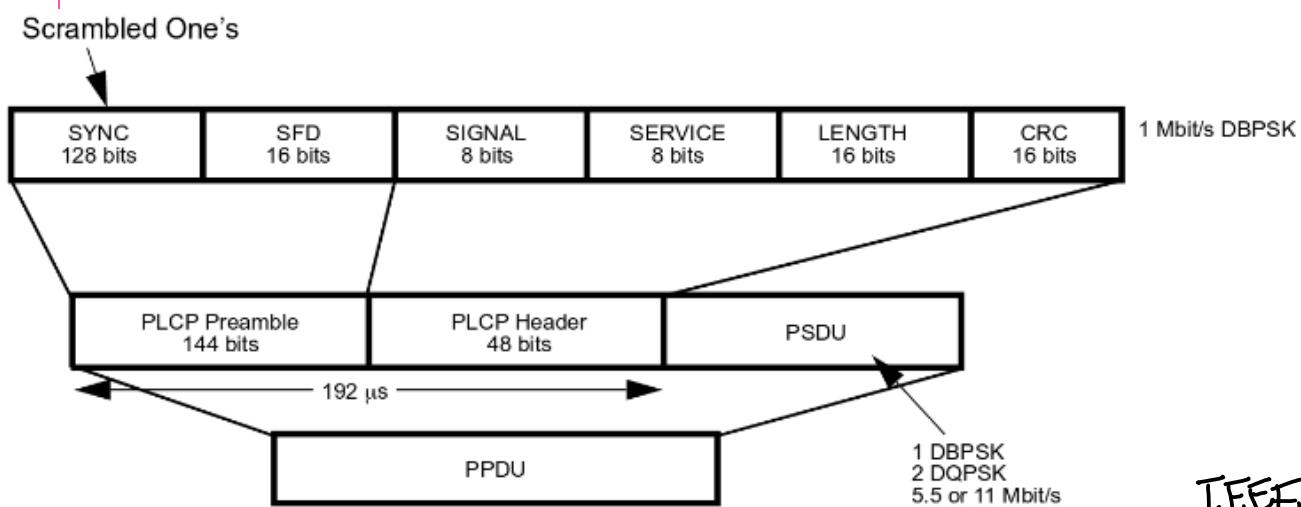
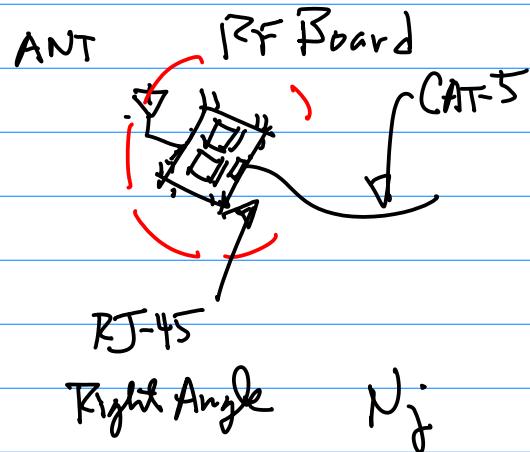
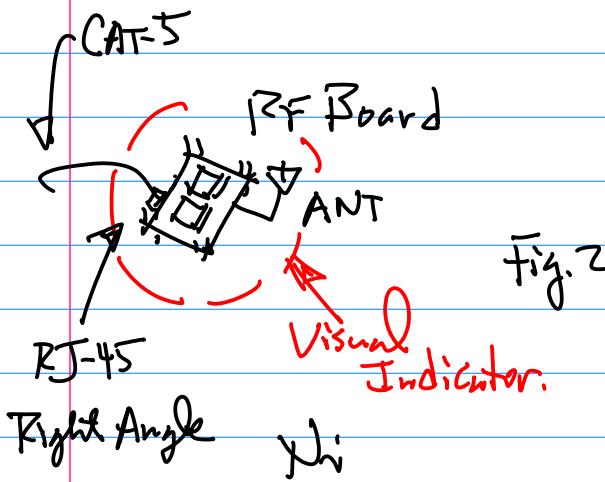


Figure 127—Long PLCP PPDU format

IEEE802.11

Fig. 3. TR.13

Node  $N_i$ , Node  $N_j$ , Each Node  
is illustrated in Fig 1.

Sending Stream of Data from  $N_i$  to  $N_j$



String of Bits Sent in "Framed" fashion.

frame $N$  ... frame $2$  frame $1$



time  $\rightarrow$

Note: Consider the construction of each frame, frame $i$ ,  $i=1, 2, \dots, N_j$

What are the contents to be placed into a frame?

like start bit(s)  $\rightarrow$   
to mark the beginning of the communication.  
 $\rightarrow$  Timing/Sync.

C.R. (Cognitive Radio), SDR (Software Defined Radio)

multiple Bits in Sync. Design  $\rightarrow$  more Reliable  $\rightarrow$  "Robust" performance  
Maybe

Question: What is the general guideline in terms of designing "Sync" Field?

multiple bits of what?

3 bits Example: b2 b1 b0

$2^3 = 8$	$\begin{array}{c} 0 \ 0 \ 0 \\ 0 \ 0 \ 1 \\ 0 \ 1 \ 0 \\ \vdots \\ , \ , \ , \end{array}$

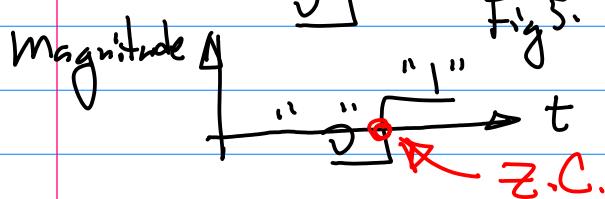
Transition  $\rightarrow$  Change of State

"Zero Crossing"

for example "1"

[ "D" ] OR

[ "0" ] [ "1" ]



To provide best possible

"Transitions", e.g. Z C

Pick OX5 Binary: 101

The Objective for R.F.

Board framework/Design:

To Allow Ni, Nj to Sync.

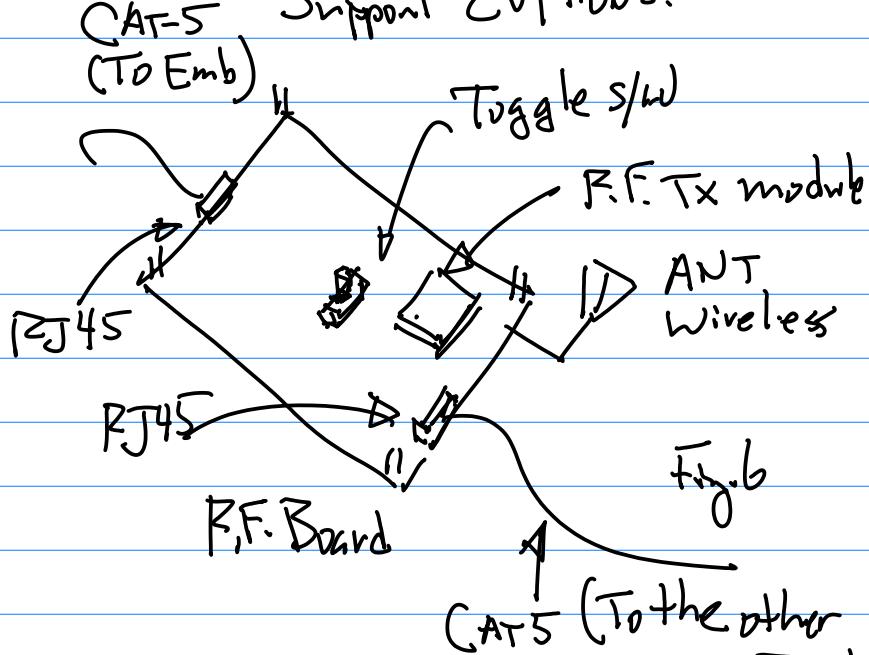
2-Step Approach:

Step 1. Based on Land Line;

Step 2. then R.F (Wireless)

Hence, R.F. Board will have to

Support 2 OPTIONS.



Sept 8 (W)

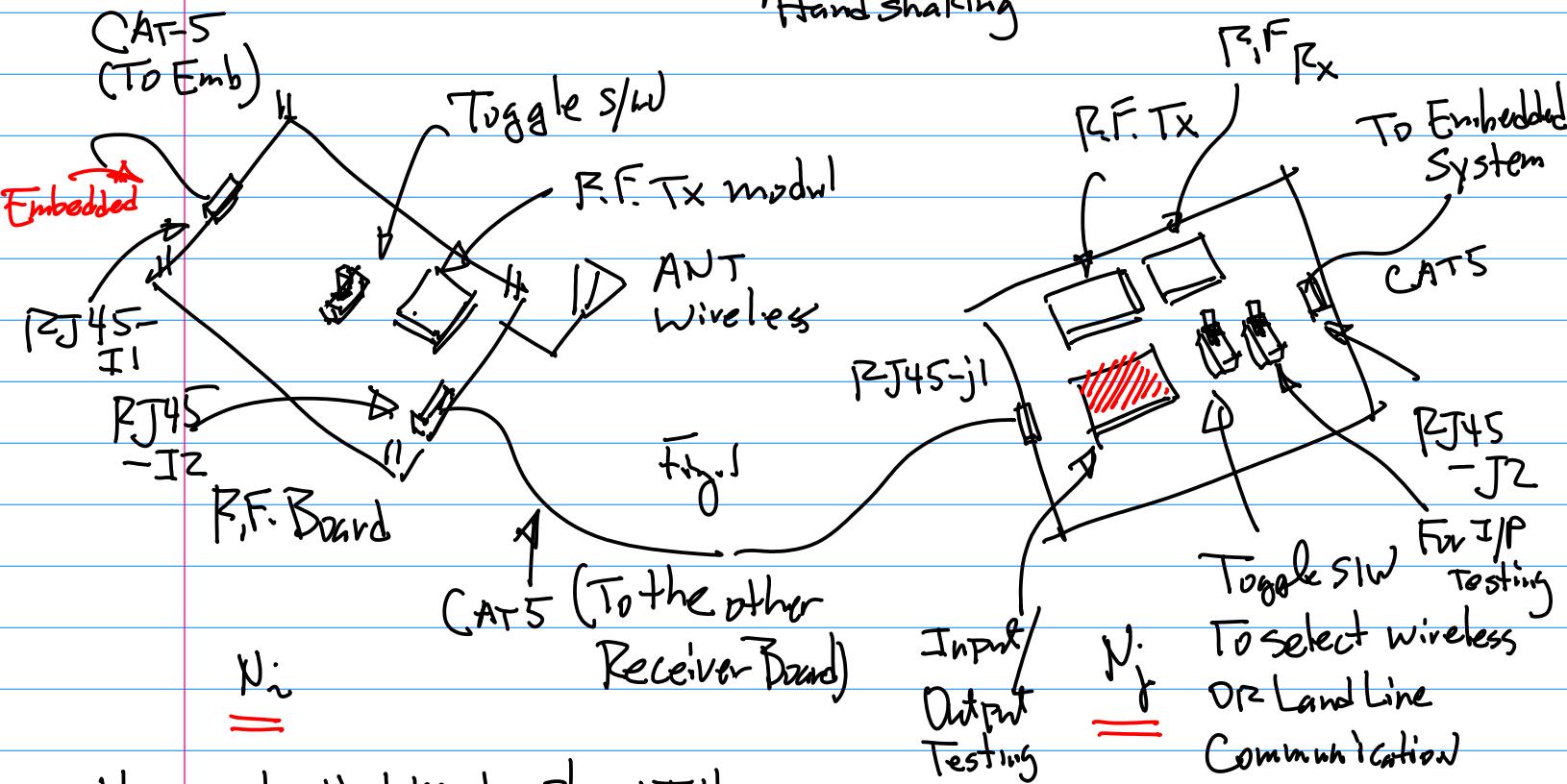
Topics: 1. Prototype for Handshaking (for URG17b9, NANO, OR your choice, such as Pie)

Note: NANO Boards are not delivered yet.  
So, please find your solution.

Note 2. Semester Long Project, please form

4 person team;

Example: "LAND-Line" Based Design for Handshaking



Homework: Next Monday, Show + Tell

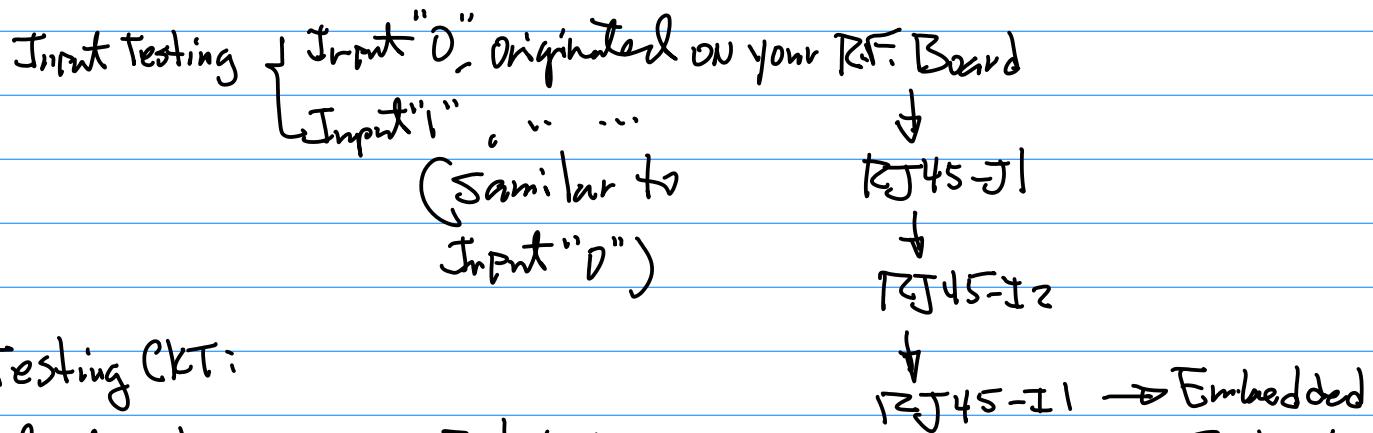
for each Person's R.F. Prototype Board.

Things to show for the next class: 1.  $4 \times 3$ " Prototype Board; the Bent Through-Hole; metal coating of the through-holes only; 2. Stand-offs  
3. RJ45 Connectors (2x), Right Angle; Mounted on the Board;  
4. Testing Circuit

Output Testing { Output "1" from the Host/Embedd System  
                    Output "0" .. .. .. ..

Input Testing { Input "D" originated on your R.F. Board  
                    Input "I" .. .. .. ..  
                    ↓  
                    RJ45-J1  
                    ↓  
                    RJ45-I2

Continued,



Testing CKT:

Output Testing CKT → Red LED.

Embedded → RFB( $N_i$ ) → LED1 → RJ45-I2

via

RJ45-I1

On RFB( $N_i \neq N_j$ )

GPIOD output  
from LFC/NAND

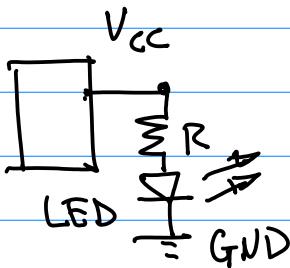


Fig. 2

$$V_{CC} = IR + V_{LED} \dots (1)$$

$$V_{CC} (\text{CMOS}) = 3.3 \text{ VDC}$$

$$V_{LED} = 1.8 \text{ VDC}; I = 10 \text{ mA};$$

Solve for  $R \sim 250 \pm \Omega$  or higher;

Input Testing CKT.

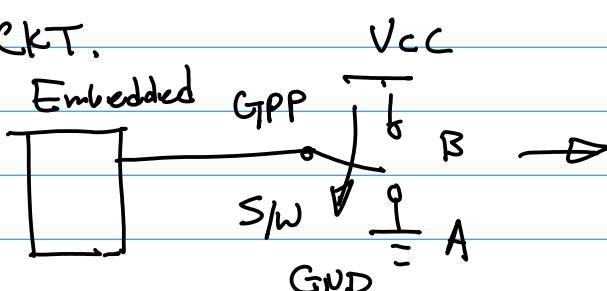
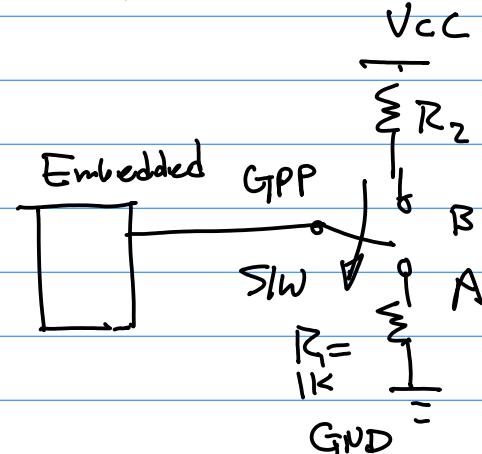


Fig. 3a



Sept 13 (Monday)

Todays Topics: 1° Hardware platform.

2° Sync Algorithm, LISA

(Linear Invariant Sync. Algorithm)

Ref: 1° ... github, ID: ~106...

2021F-106  
for target RISC-V  
(System On Chip)

2° github/finalisti/Cmpe245/...

2021F-105 ~ (NAND  
Connector)

FPGA Solution (RISC-V), Igloo2.

a Board from Future Electronics

b IP-Core for CPU in Verilog  
Can be downloaded ;

c TAP Plastic  
NAND Board. Connector J-41

Identify GPIO

Example: Let's consider the design  
of Sync Field in Wireless  
Communication

Consider 1° Place to define sync.  
Bits.



Suppose we have a letter  
in a Hex Number

$0x4f$   
 $0 \boxed{1} 00 : 1111$  Binary  
Equivalent  
"0"  
↑  
Due to Noise, the  
Corruption may lead  
to a failure

$0 \boxed{1} 00 : 11110$  ...  
↑  
Correct  
missing Sync. Bit

2° Sync is established  
Based on "2 C"

The change of the State of  
a Signal, For Example

"0" → "1" OR "1" → "0"

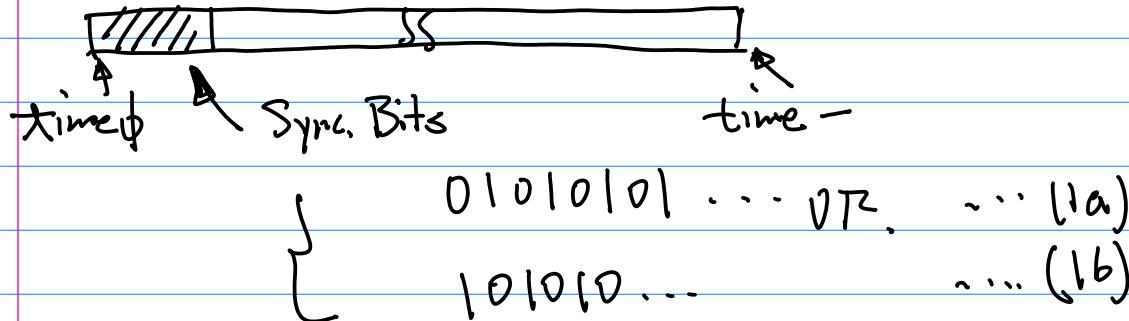
Preferred Change is to  
include "1".

Requirements:

1° Establish Sync with  
Change of State

01010101 ...

OR  
101010...



Consider Random Disturbances, alters one bit in the Sync field. (1a)

of the Sync Field,  
e.g. the Beginning  
of the payload.

010101...  
↓  
1 (Random Noise)

Suppose we know the Sync. field consists of 10 Bits.  $\rightarrow$  Discard the 1st 2 bits until we have 0101...

Pattern again, to satisfy the total Number of bits in the Sync. Definition.

Question: How to utilize the Sync Pattern even when this pattern is corrupted, And not to start over again?

- (1) The Need to Re-use the Sync Field Even if it is corrupted;
- (2) The Need to Known where is the end of

Sept 15 (W)

Homework: Due Next Wed.  
Official (2 pts) Sept. 22nd.

1° RF Board Prototype (finish this Prototype for Landline I/F).

2° Run a simple program C/C++ or Python to perform Testing of Input/Output function.

Input Testing : GPIO Reads Input "0" AND/OR "1", Note Toggle the Switch on the RF Board to produce "0", "1".

Output Testing: LED On when Output = "1"  
LED Off .. .. = "0"

2° To Establish Timing  
Even if Random disturbances  
Corrupted Some bits in  
Sync. Field, in addition to  
pin point to where the  
Corruption occurs.

What to Submit:

1° One description of your design implementation;

2° Photo of the System Set up

Host Laptop + Embedded Board + RF  
LPC / NANO Board

3° Source (Soft Copy) LPC1769

Export your work as a project

NANO, Python or C/C++ Code

4° Video Clip 5~10 Sec.

~~On CANVAS OR~~ Submit the Zip  
file via E-mail;

Embedding ID Index into  
Sync Field.

From 101010 ...

Change it to the following.

g Take 8 bits

10101010 at a time

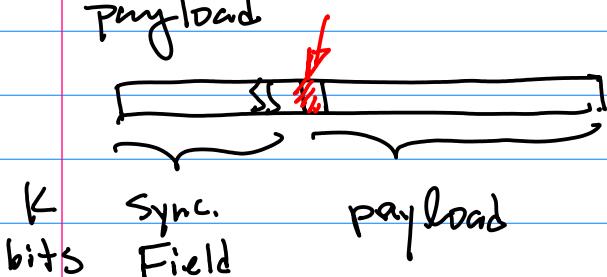
Taking the 1st 4 bits of this  
Segment (1 byte), preserve  
its pattern

prefix: 1010

Then, Taking the 2nd 4 bits  
modify it to make it as  
an index to reflect this

Byte position in the Sync

Field. e.g. 0 000 ... "0"  
0 001 ... "1"  
0 010 ... "2"  
0 011 ... "3"



# Cmpe245

11

0 0 0 0 ... "0"  
 0 0 0 1 ... "1"  
 0 0 1 0 ... "2"  
 0 0 1 1 ... "3"  
 ...

1 1 1 1 ... "f"

Assemble prefix and ID together

1 0 1 0 ; 0 0 0 0  
 1 0 1 0 ; 0 0 0 1

:

1 0 1 0 ; 1 1 1 1

a d i a l ; a z ; ... ; a f ... (1) 16 Bytes

Now, Change 1010 to 0101 = 0x5  
 Therefore,

50;51;52 ... ;5f ... (z) 256 bit.

Integrate (1) & (z) together, 16 Bytes Let's define Confidence level  $\eta$  as follows,  
 a d, a l, a z, ... , a f, 50, 51, ... , 5f

e.g.

0xa0, 0xa1, ... , ..., 0x5f ... (z)

32 Bytes (256 bits)

Design An Algorithm for Sync.  
 Extraction @ Rx End

Question: What is the minimum Number of Bits in (z) do we need to establish Sync.?

Remark 1: Minimum 8 consecutive Bits with first 4 bits from alternating Bit Pattern, e.g. DXA, or 0x5 is Needed to Establish Sync. Given

Question: Sync. Based 8 bits v.s. Sync. Based on 16 bits, which one gives higher confidence? Ans: 16 bits,

Question: What is the number bits that gives the highest confidence level?

$$\eta = \left( \frac{\text{Sync. Establish with } K \text{ bits}}{\text{Total No. of bit in Sync. Field}} \right)^{(4)}$$

Sept. 20 (Mon)

TOPICS : 1<sup>o</sup> LISA Conclusion  
2<sup>o</sup> Base Band Signals  
with Defintional Modulation  
Techniques, ASK, FSK, PSK.

3<sup>o</sup> Project 1. Assignment

Software Defined Radio  
Implementation of LISA.

The Oct. 8th (Fri), 11:59pm.

Written Requirements to Be

Posted on git & SJDE CANVAS.

Official (WRT5)

a. Land Line "LISA"  
(Based on Homework  
of Input/Output Testing)

b. RF. "LISA".

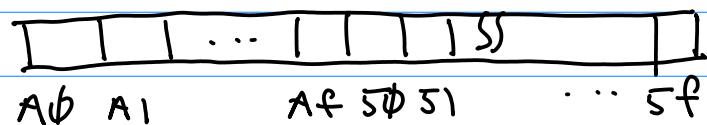
ASK RF Rx & Tx for the  
implementation.

Example: Compute  $n$  (confidence  
level, CL) for the sync  
established Based 8 bits  
data from the Sync. Field.

Sol. From Eqn(4),

$$\begin{aligned} n &= 8 \\ \text{Total Bits} &= 8/2 = 2^3/2 \\ \text{in the Sync} & \\ \text{Field} &= 2^{-5} = 1/32 \end{aligned}$$

Fig. 1



Linear: Index Arranged in a Linear  
fashion;

Invariant: Capture 8 bit sync  
pattern regardless of  
its/their position(s);

Conclusion: LISA algorithm  
Provides Robust, Versatile  
Sync. Scheme to Allow N<sub>i</sub>, N<sub>j</sub>  
to Establish Sync. (Handshaking).

Homework: Write C/C++ (or python)  
for your hardware platform, to Realize  
Baseline "LISA". (Due Sept. 27  
Monday) 1 pt.

a. Prompt the user for his/her  
Input for the Number of Bytes  
to establish Sync.

1 Byte, 2 Bytes, ... , 32 Bytes

b. Implementation for "the Base  
Line"

Baseline: Consecutive Bytes.

C. Creates A Test Pattern  
as follows, "testsync.txt"

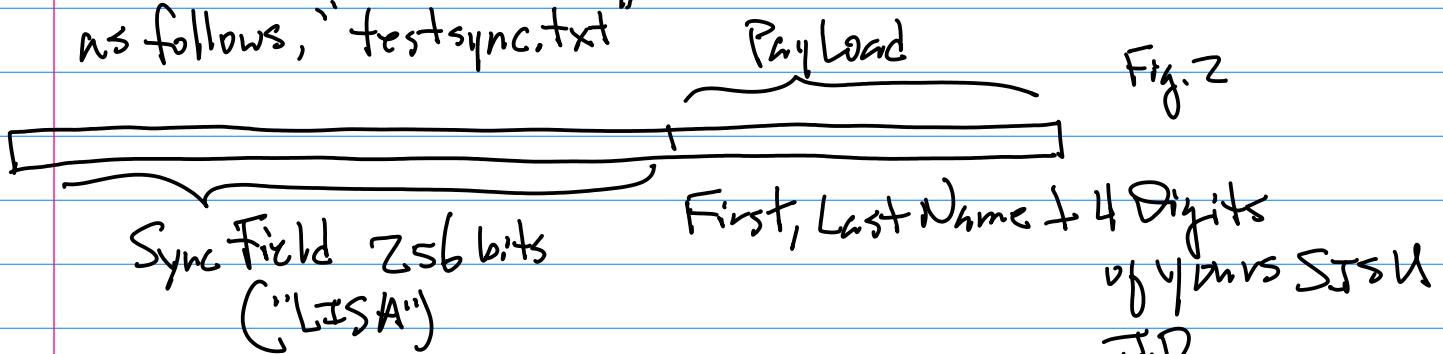


Fig. 2

Plaintext file.

d. Run your program to process  
the testSync.txt, to extract  
Sync. By Printing the payload.

Note, then future framework  
will allow the Bytes from  
Non-Consecutive order.

Note: Optional Requirements

Pseudo Code.

What to Submit:

a. Source Code (Indicate if  
on Linux, or Windows, or  
LPC, or NAND)

b. Binary Executable;

c. Optionally, Pseudo Code.

Base Band Signal:

Without

A Definition: Signal transmitted near zero frequency modulation.

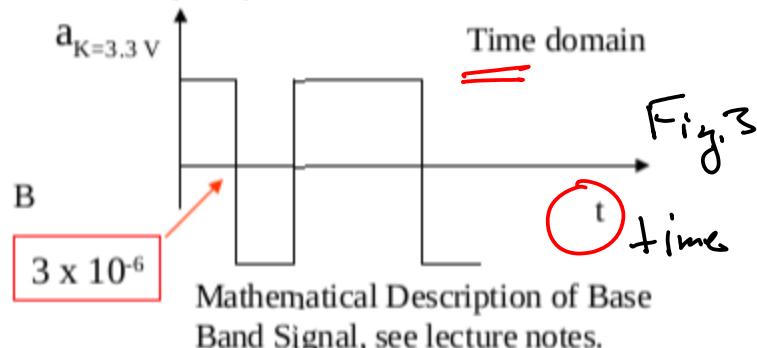
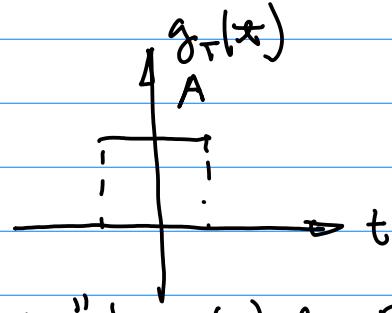


Fig. 3

Signds from GPIO, PWM, etc.  
for example.

Suppose the Signal is periodic  
Signal. Concentrate on a Single  
Bit.

Fig. 4



Subscript "T" in  $g_T(t)$  for One lat

# CmpE245

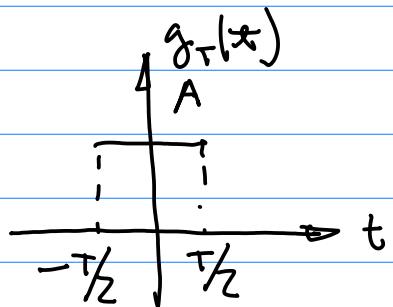
14

$$g_T(t) = \begin{cases} 1 & \text{for } t \in [-T/2, T/2] \\ 0 & \text{Otherwise} \end{cases} \quad \dots (1)$$

(bps - Bit per send)

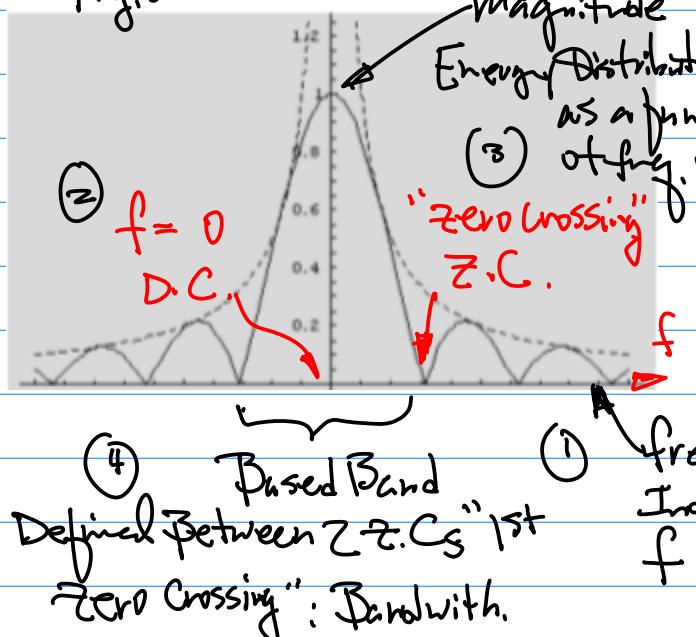
Sol:

Fig. b



Frequency Characteristics of the B.B. Signals:

Fig. 5



From the given bit rate,

$$f = 9600 \text{ Hz}$$

$$\text{Hence, } T = \frac{1}{f} = \frac{1}{9600}$$

$$= 1.04 \times 10^{-5} \text{ Sec}$$

$$= 1.04 \times 10^{-6} \text{ Sec (micro second)}$$

Consider Frequency Characteristics in Fig. 5,  
Define Bandwidth of the

$$g_T(t)$$

$$\bar{B}W =$$

(Between the 1st pair of Z.C.S)

Eye Pattern:  
Characterization of  
Base Band Signal

metric

IEEE 802.11b  
Standard pp. 56

Sept 22 (w)

Topics Today: Base Band Signal Analysis.

$g_T(t)$  from Eqn (1)

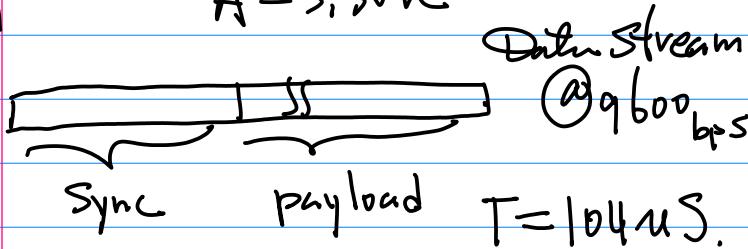
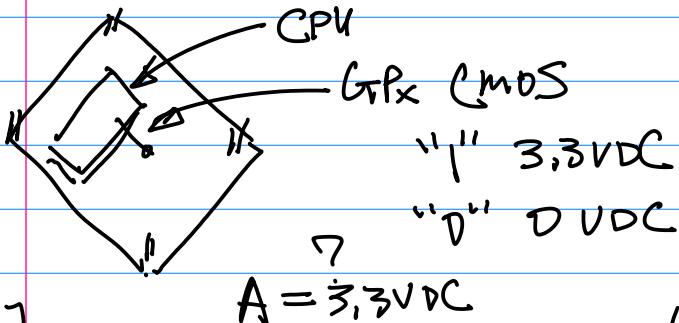
Example: Find  $T = ?$  for a  
Base Band Signal @ 9600 bps

By Fourier Transform,

$$g_T(t) \xleftrightarrow{F.T.} F[g_T(t)]$$

... (za)

$$F[g_T(t)] = A_T \frac{\sin \pi f T}{\pi f T} \dots (zb)$$



Find Bandwidth from the 1st pair of Z.C. in Eqn(zb)

$$AT \frac{\sin \pi f T}{\pi f T} \text{ set } 0$$

then  $\frac{\sin \pi f T}{\pi f T} = 0$ , Hence

$$\sin \pi f T = 0$$

$$\pi f T = n\pi$$

$$n = 0, 1, 2, \dots$$

$f T = n$ , where  $n = 1$  1st pair Z.C.

$$f T = 1, \therefore f = \frac{1}{T}$$

$$\text{Therefore, } B.W. = 2 \frac{1}{T} = 2 \frac{1}{f} \dots (3)$$

Example: Suppose a Baseband Signal is operating @ 9600 bps.

1. Find its Bandwidth?
2. If we double the Bit rate, find its new Bandwidth?

Sol.: For B.W., from eqn(3)

$$B.W. = 2 \frac{1}{f}$$

$$\text{and } T = \frac{1}{f}, \text{ or } f = 1/T$$

$$\text{hence: } B.W. = 2f = 19200 \text{ Hz}$$

When the bit rate is doubled, so is the B.W.

And  $T_{\text{new}}$  is the half of its original value.

PP60 IEEE 802.11b

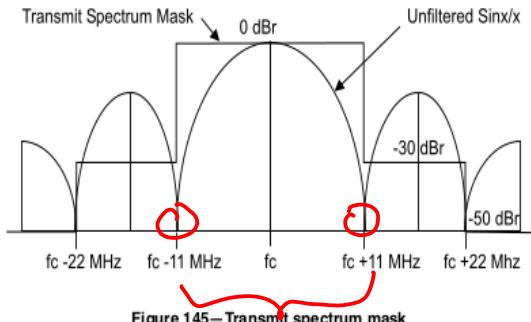
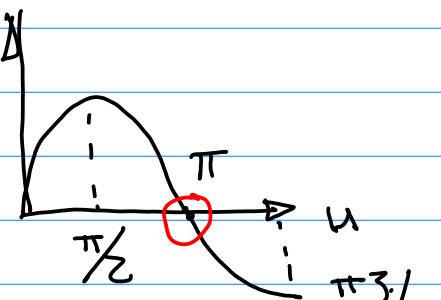


Figure 145 - Transmit spectrum mask

18.4.7.4 Transmit center frequency tolerance

$$\begin{aligned} B.W. &= f_c + 11 \text{ MHz} - (f_c - 11 \text{ MHz}) \\ &= 11 \text{ MHz} + 11 \text{ MHz} = 22 \text{ MHz} \end{aligned}$$

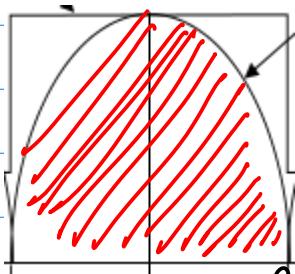
$f_c$  = Carrier frequency  $\approx 2.4$  GHz  
from the modulation  
Carrier Signal ( $R_c$ ) is modulated

# CmpE245

16

by a Base Band Signal.

80% of the total energy of the R.F. Signal (Base Band + Carrier) has to be captured within the Base Band



80% of the Energy.

This 80% Requirements has to Be Satisfied by F.C.C.

$$\frac{(\text{Energy of the})}{\text{Base Band}} \sqrt{\frac{(\text{Energy of the total})}{\text{Signal}}} = 80\%$$

or higher.

Question: How to Pack More energy into a Base Band (1st Part of the Z.C.)

Discrete Fourier Analysis Tool for the Design.

Sept. 27 (Mon)

Topics: 1<sup>o</sup> Analytic Tool for Base Band Signal (Spectrum) Analysis;

2<sup>o</sup> Semester Long Project (LoRaRF)

Team project (4 person)

Team, Each Team will have to Implement LoRaRF for C.R (Cognitive Radio)

Show+Tell "LISA" on NIAND

By Jonathan. Very Good

Note:

1<sup>o</sup> Header: Name of the code;

b. Coded by: c. Date

d. Version, OX1.0;

e. Status: Tested, Debugging

f. Note, Such as Version of the Python, or Compilation  
- (u) & Bind for C/C++;

2<sup>o</sup> Testing/Verification, to make sure the code works for All Possible Cases even when the Sync is corrupted;

Homework (1 pt). Continuation

of homework on pp. 12-13.

LAN Line Testing Between Ni & NJ Due A week from Today.

Oct. 11 (Monday) Before the Class.

Submission:

1<sup>o</sup> Sub: CmpE245 homework Sync. LAN Line



WIRELESS, SENSING &amp; TIMING



SX1276/77/78/79

DATASHEET

SX1276/77/78/79 - 137 MHz to 1020 MHz Low Power Long Range Transceiver

2. Sub. A photo of your testing result (Screen Capture); (where R.F. Tx module is connected to GPP of the target platform, LPC1769)
3. Submit A photo showing your testing environment. (N<sub>i</sub> & N<sub>j</sub>). Enhancement:
4. Source Code, and Binary;

Project 1. is Coming LISA  
ON R.F. Board Communication

(10 pts) Due Oct 11th (Mon)

Before class, please have the R.F. Part ready when submission is done.

Note: Need Timer/Interrupt function on LPC1769.

Implementation: Timer  $\rightarrow$

Interrupt on a desired

Time Interval for a chosen Bit Rate,  $\rightarrow$  Lead to R.F.

Tx module to send a bit

1° Due to Off-Campus Program, Change Office Hours to M, Tue, 3:40-4:40 pm.

2. Semester Long Project. Kit, start prepare purchasing

Discussion On Spectrum Analysis Tool.

Discrete Fourier Transform  $\rightarrow$

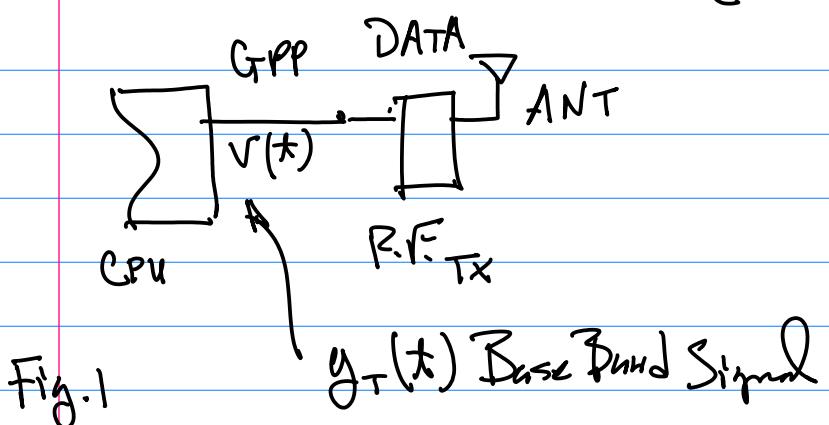
Compute Spectrum  $\rightarrow$  Evaluate the

Energy of the Signal  $\rightarrow$  To Modify

Improve the Energy ( $\delta\sigma^2$ )

Distribution Requirements.

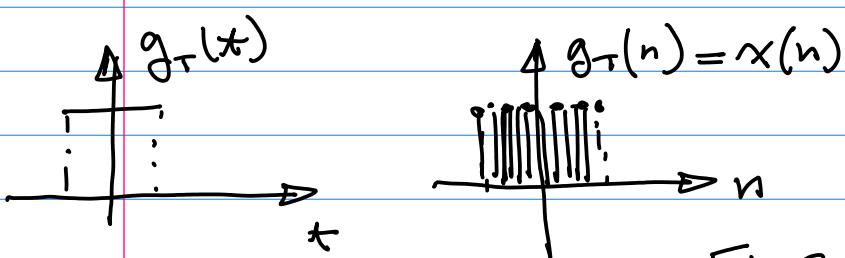
Example: Suppose A Base Band Signal  $y_r(t)$ , As An Output from GPP Port:



Base Band Signal  $y_T(t)$ .

Digitize the Signal  $y_T(n)$

$n$ : Time Index



Find its Fourier Transform.

Discrete

$$X(m) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) e^{-j 2\pi \frac{mn}{N}}$$

... (1)

$X(m)$ : Discrete Fourier

Transform;

$m$ : A Frequency Index

$m = 0, 1, 2, \dots, N-1$

$X(m)$  Digitized

$x(n)$  : Discrete Signal in

Time Domain, Base Band Signal for Example.

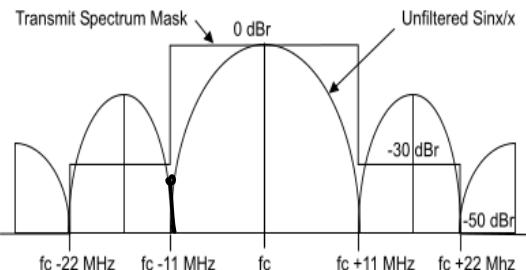
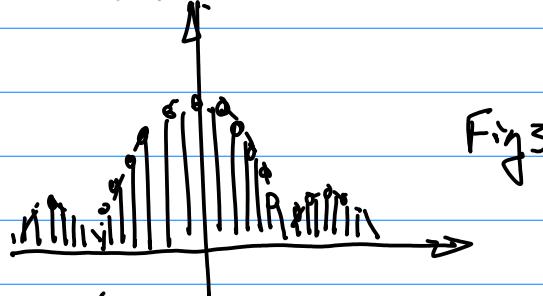


Figure 145—Transmit spectrum mask

#### 18.4.7.4 Transmit center frequency tolerance



Sept. 29 (Wed)

Announcement:

1. Project 1 (10 pts) Due 3 week  
at 8<sup>th</sup> Before 12:30 PM.

Requirements

(1) Individual Project, However working as team is required.

Report, Prototype Board, Programs have to be individual, Team work including discussions, debugging as a team is encouraged.

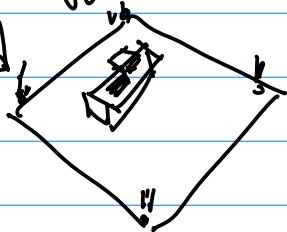
(2) Implement LISA for R.F. Communication. Based

on LISA

homework.

To have a toggle switch on

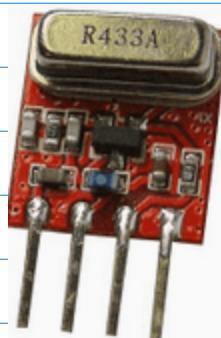
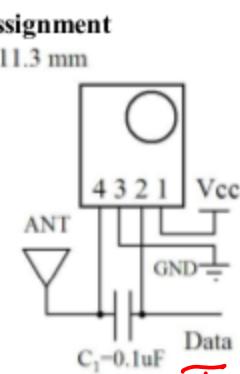
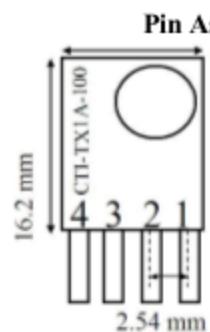
R.F Board,



Position A : For Land Line

Position B : For R.F. Wireless

Note: ASK R.F. module, From [github/kalilic/Cmpe245](https://github.com/kalilic/Cmpe245) ~ 2017 f... TX



Data sheet  
(Tech Spec)

$V_{cc} \in [3.3, 9]$

Pin Number	Label	
1	$V_{cc}$	Power
2	DATA	Data Input
3	GND	Ground
4	ANT.	Antenna

Table 2. Pin Assignment

Rf Solutions  
QAM-TX2-433

\$4.54

Newark

$330 \sim 450 \text{ MHz}$

$\sim 23 \text{ cm.}$

TO GPIO  
Pin

(3) On Receiver Side (R.F. Rx)

$430.5 \text{ MHz}$

$f_c$  Carrier frequency

a

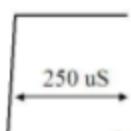
	Symbol	Test Condition	Parameter		
			Min	Typical	Max
Frequency	$F_c$		315 MHz	430.5 MHz	433.92 MHz
Modulation	ASK				

b R.F. Tx :

$$T = 1000 \mu\text{s} = 1 \text{ ms}, 1 \text{ kbps};$$

Logic "1"

When receiving signal high  $< 500 \mu\text{s}$



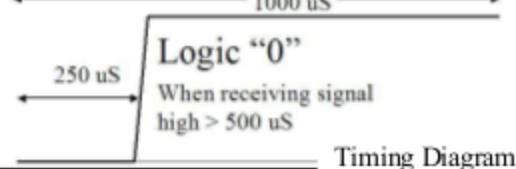
Over Sampling on Rx Side.

Determine R.F. Tx module Bit Rate

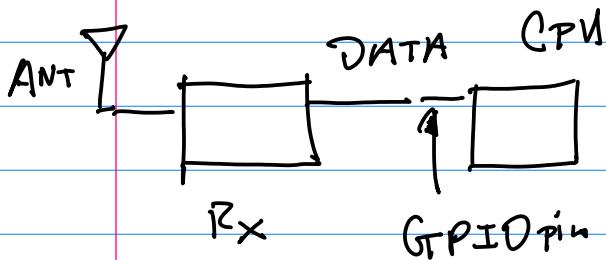
$$1 \text{ kbps} \rightarrow \text{Time per bit } T = \frac{1}{f} = 1 \times 10^{-3} \text{ s} \quad (f = 1 \text{ MHz})$$

Over Sampling +

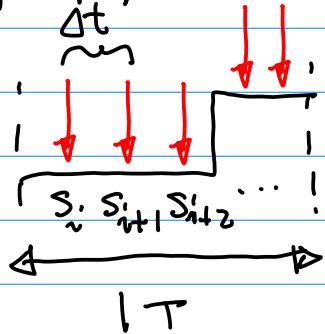
In One Period T, Sample K Times



On Rx Side



Triggered by System Clock



Over Sampling 5 Times per T

3 Votes (Readings) for "0"

2 Votes (Readings) for "1"

LPC1769

The Decision  
Based on the  
Majority

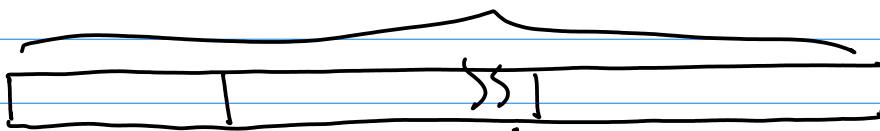
(4) Receiving Data from Rx, Read the Data

And place the Data

into A Buffer, 1 Kbits 1 kbit

Interrupt Timer to give the adequate Time Interval to Read.

Ref: INT-TIMER-HL ~  
(github)



Sync Field  
DXA0, ..., DXSF

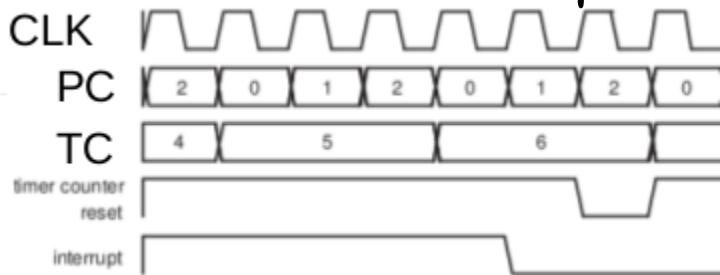
<input type="checkbox"/> 1	INT-TIMER-HL-2016--11-24.pdf	Add files via upload
<input type="checkbox"/> 2	INT-TIMER-Part2-HL-2016--12-4.pdf	Add files via upload
<input type="checkbox"/> 3	LPC1769_EINT_TIMER2016-4-19.zip	Add files via upload

Parse the Buffer to Extract Sync.

Objective: To Transmit Your Name (First, Last), plus 4 Digits

Student ID.

Timer Setup & Special Purpose Registers



Submission:

- 1º Report ( $2 \sim 5$  pages in IEEE)
- 2º Same Code + Binary.  
LPC1769 Zip. (Exported Project)
- 3º photos in Report  
 $\cong$  Entire System, Host + Embedded  
+ R.F.
- 4º Video Clips < 10 Sec.  
5 Sec. Better

Shows the Result.

Continue the Discussion on Eqn(1), pp.18

$$\mathcal{X}(m) = \frac{1}{N} \sum_{n=0}^{N-1} X(n) e^{-j 2\pi \frac{mn}{N}}$$

... (1)

Properties & Physical meaning:

$$\mathcal{X}(m) = \mathcal{X}(m+kN) \dots \text{ (2)}$$

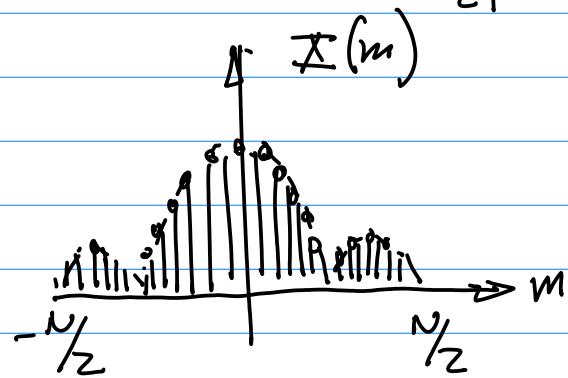
where  $k=0, 1, 2, \dots$

$N$  No. of points per one period.

e.g. Period.

$\mathcal{X}(m)$  is a periodical function.

Its period is equal to  $N$ .



Note: It is a plot of a Power Spectrum of  $X(m)$ .

Oct. 4 (Monday)

Today's Topic: Power Spectrum Analysis for Base Band Signal.

Q&A Session on Project 1.

1. Over-Sampling Implementation

(1) Bit Rate  $\rightarrow T$  Time Interval for Period;

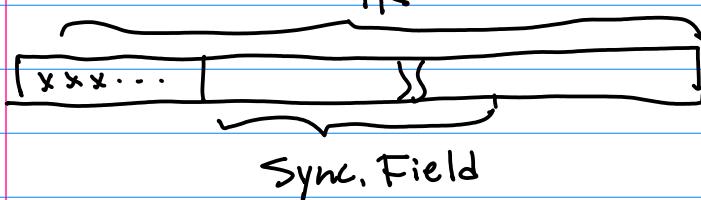
(2) Normal Sampling:

GPIO Read GPIO Pin  
is connected to Data Pin of Rx

Timing: Read once per  $T$   
Period

Timer (Interrupt)

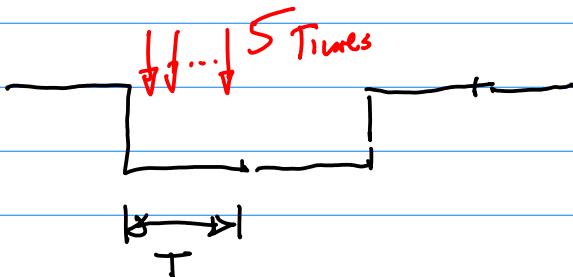
Software Side: Create a Buffer with size of 1k, Assuming the Communication @ Low bit rate ( $\sim 1024 \text{ bits/sec}$ , ...,  $9600 \text{ bits/sec}$ )



Parse the Buffer, find/Extract Sync Bytes.

③ Over Sampling: Keep the Same Bit Rate, RF Rx Output is presented to GPIO pin, GPIO Read

5 Times per period.



Read into A Buffer, 5K

Buffer  $\rightarrow$  Buffer 1K  
(After Preprocessing)

Preprocessing: Voting Algorithm. That is the real part

Interrupt Timer is the key

Continuation for DFT in Eqn(1)

Eqn. 2.1.  $\hat{x}(z)$

Define a Power Spectrum

$$P(m) \triangleq \sqrt{\operatorname{Re}[\hat{x}(m)]^2 + \operatorname{Im}[\hat{x}(m)]^2} \quad \dots (3)$$

$$\operatorname{Re}[\hat{x}(m)] = \operatorname{Re}\left[\frac{1}{N} \sum_{n=0}^{N-1} x(n) e^{-j 2\pi \frac{mn}{N}}\right]$$

$$= \frac{1}{N} \operatorname{Re}\left[\sum_{n=0}^{N-1} x(n) \left(\cos\left(-j 2\pi \frac{mn}{N}\right) + j \sin\left(j 2\pi \frac{mn}{N}\right)\right)\right]$$

where

$$\begin{aligned} e^{-j\omega} &= \cos(-j\omega) + j \sin(-j\omega) \\ &= \cos(j\omega) - j \sin(j\omega) \end{aligned}$$

Hence,

$$= \frac{1}{N} \sum_{n=0}^{N-1} x(n) \cos\left(-j 2\pi \frac{mn}{N}\right)$$

$$= \frac{1}{N} \sum_{n=0}^{N-1} x(n) \cos\left(j 2\pi \frac{mn}{N}\right)$$

Note: for Eqn(3), with the understanding of the Power Spectrum Definition, we can drop Square-root Computation for Simplicity.

Note:

$$P(m) = P(m + nN) \dots (4)$$

$$P_f^f = P(m) = \sqrt{R_e^2[\mathcal{X}(m)] + I_m^2[\mathcal{X}(m)]}$$

$$P(m + KN) = \sqrt{R_e^2[\mathcal{X}(m + KN)] + I_m^2[\mathcal{X}(m + KN)]}$$

where

$$\mathcal{X}(m) = \mathcal{X}(m + KN)$$

Therefore

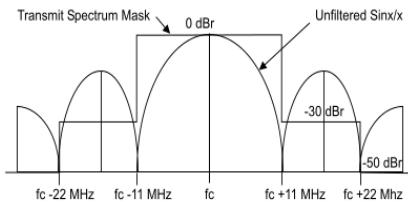
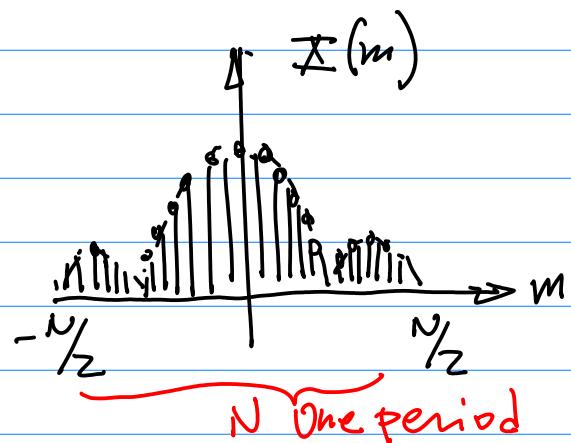
$$R_e^2[\mathcal{X}(m + KN)] + I_m^2[\mathcal{X}(m + KN)]$$

$$= R_e^2[\mathcal{X}(m)] + I_m^2[\mathcal{X}(m)]$$

So, we know this equal to  $P(m)$  Any One Period ( $N$ -Points)

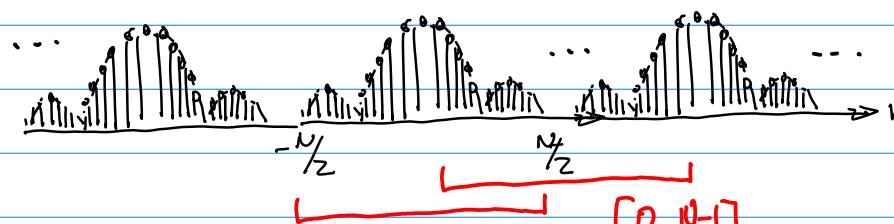
O.E.D.

Example:



18.4.7.4 Transmit center frequency tolerance

IEEE



$$[-\frac{N}{2}, \frac{N}{2}]$$

Fig.1a  
periodical function  
 $P(m)$ .

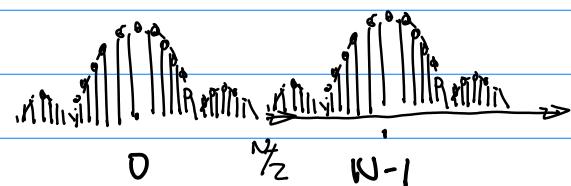


Fig.1b

$$[0, N-1]$$

Computation of  $X(m)$  and its Power Spectrum.

Hand Compute DFT. Eqn (1).

$$\begin{aligned} X(m) &= \frac{1}{N} \sum_{n=0}^{N-1} x(n) e^{-j \frac{2\pi}{N} mn} \\ &= \frac{1}{N} \left( x(0) e^{-j \frac{2\pi}{N} \cdot 0} + x(1) e^{-j \frac{2\pi}{N} \cdot 1} \right. \\ &\quad \left. + x(2) e^{-j \frac{2\pi}{N} \cdot 2} + \dots + x(N-1) e^{-j \frac{2\pi}{N} \cdot (N-1)} \right) \end{aligned}$$

$$= \frac{1}{N} \left( e^{-j \frac{2\pi}{N} \cdot 0}, e^{-j \frac{2\pi}{N} \cdot 1}, e^{-j \frac{2\pi}{N} \cdot 2}, \dots, e^{-j \frac{2\pi}{N} \cdot (N-1)} \right) \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ \vdots \\ x(N-1) \end{bmatrix}$$

$X(m)$  is D.F.T.  $m = 0, 1, 2, \dots, N-1$

$$X(m) = \frac{1}{N} \left( e^{-j \frac{2\pi}{N} \cdot 0}, e^{-j \frac{2\pi}{N} \cdot 1}, e^{-j \frac{2\pi}{N} \cdot 2}, \dots, e^{-j \frac{2\pi}{N} \cdot (N-1)} \right) \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ \vdots \\ x(N-1) \end{bmatrix}$$

for  $m=0$

$$X(0) = \frac{1}{N} \left( e^{-j \frac{2\pi}{N} \cdot 0}, e^{-j \frac{2\pi}{N} \cdot 0}, e^{-j \frac{2\pi}{N} \cdot 0}, \dots, e^{-j \frac{2\pi}{N} \cdot 0} \right) \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ \vdots \\ x(N-1) \end{bmatrix}$$

for  $m=1$ 

$$\mathcal{X}(1) = \frac{1}{N} \left( e^{-j\frac{2\pi \cdot 0}{N}}, e^{-j\frac{2\pi \cdot 1}{N}}, e^{-j\frac{2\pi \cdot 1 \cdot 2}{N}}, \dots, e^{-j\frac{2\pi \cdot 1 \cdot (N-1)}{N}} \right) \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ \vdots \\ x(N-1) \end{bmatrix}$$

for  $m=2$ 

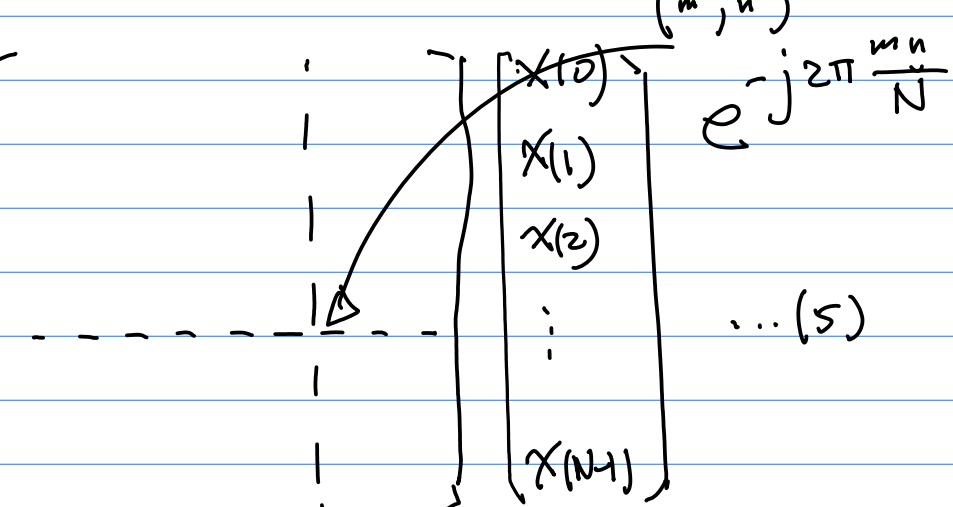
$$\mathcal{X}(2) = \frac{1}{N} \left( e^{-j\frac{2\pi \cdot 0}{N}}, e^{-j\frac{2\pi \cdot 2}{N}}, e^{-j\frac{2\pi \cdot 2 \cdot 2}{N}}, \dots, e^{-j\frac{2\pi \cdot 2 \cdot (N-1)}{N}} \right) \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ \vdots \\ x(N-1) \end{bmatrix}$$

 $\vdots$ for  $m=N-1$ 

$$\mathcal{X}(N-1) = \frac{1}{N} \left( e^{-j\frac{2\pi \cdot 0}{N}}, e^{-j\frac{2\pi \cdot N-1}{N}}, e^{-j\frac{2\pi \cdot (N-1) \cdot 2}{N}}, \dots, e^{-j\frac{2\pi \cdot (N-1) \cdot (N-1)}{N}} \right) \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ \vdots \\ x(N-1) \end{bmatrix}$$

Put these  $\mathcal{X}(0), \mathcal{X}(1), \mathcal{X}(2), \dots, \mathcal{X}(N-1)$  together,  
we have

$$\begin{bmatrix} \mathcal{X}(0) \\ \mathcal{X}(1) \\ \mathcal{X}(2) \\ \vdots \\ \mathcal{X}(N-1) \end{bmatrix} = \frac{1}{N} \begin{bmatrix} & & & & \\ & & & & \\ & & & & \\ & & & & \\ & & & & \end{bmatrix}$$



Oct 6 (Wed)

Q3 A session

Topics: 1° LTC1769 platform

Implementation of Sync

Algorithm Using Timing

Homework (Due Oct 11th) <sup>Monday</sup>

Purchase LoRa RF module

On-Line, [www.digikey.com](http://www.digikey.com)

monster.com.

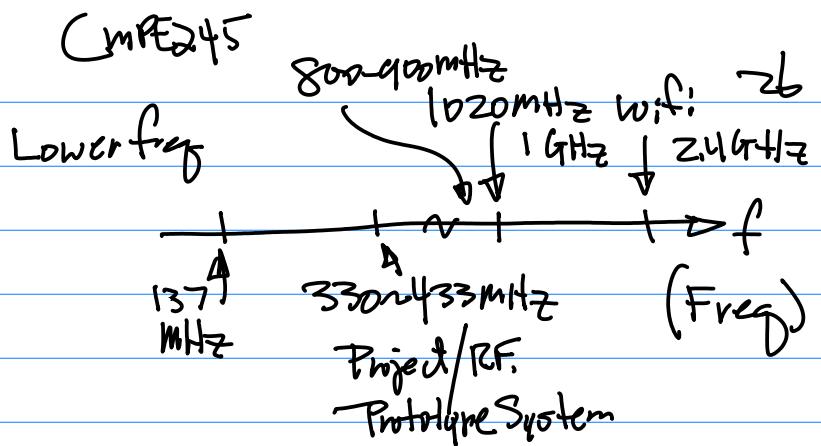


Fig. 1



**SX1276/77/78/79**

WIRELESS, SENSING & TIMING

DATASHEET

**SX1276/77/78/79 - 137 MHz to 1020 MHz Low Power Long Range Transceiver**

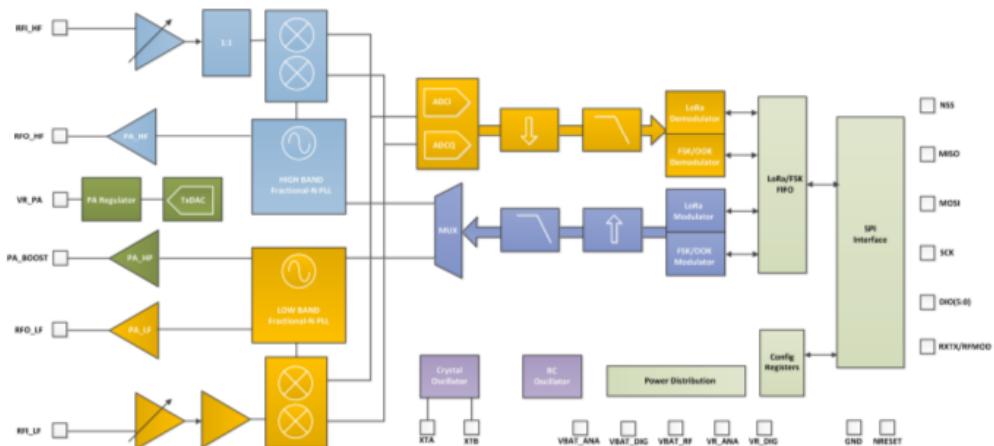
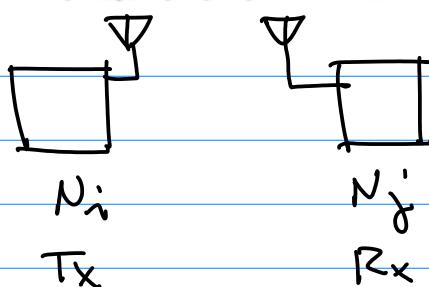


Fig. 2

Example:

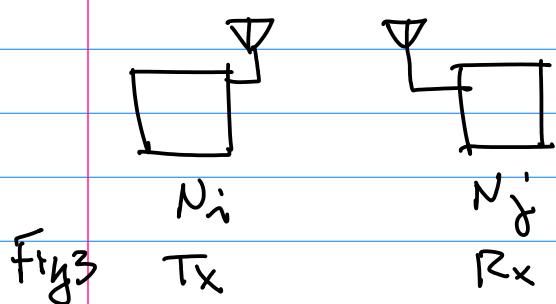
LTC1769 Platform. Regarding  
Project 1. Extension 1 week (at 25  
Monday)

Sampling Technique, GPIO Reading  
from Node j (Rx)



a. Bit Rate for Both Tx, Rx are the  
Same, e.g. 1kbp; 1024 bits/sec.

Fig. 3



Send "Hello, the world"

↓  
letter 'H', ASCII code

↓  
0x5f : 0101 1111

$$\begin{aligned} \text{Tx} &= \text{Bit Rate} \\ T_b &= \frac{1}{f} = 1 \times 10^{-3} \text{ Sec.} \\ f &= 1000 \end{aligned}$$

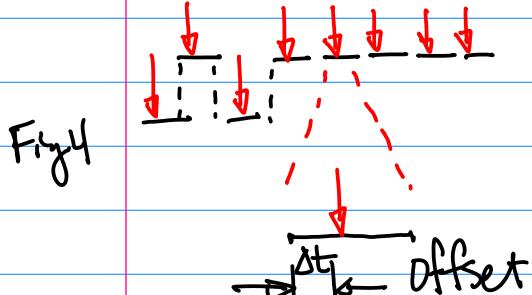
Sending (Tx).

↓  
Rx Knows the Bit Rate,

↓  
Rx "Normal Sampling"

| Read per |  $T_b$ .

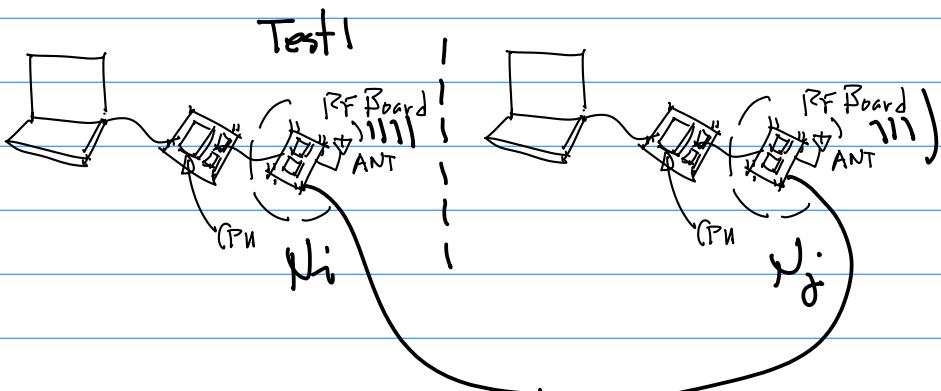
Rx:



b. The Read from GPIO  
Result is Saved into 1 K buffer  
OR 8K Buffer

Parsing the Buffer Content By "LISA" Algorithm.

C. Test on LandLine first



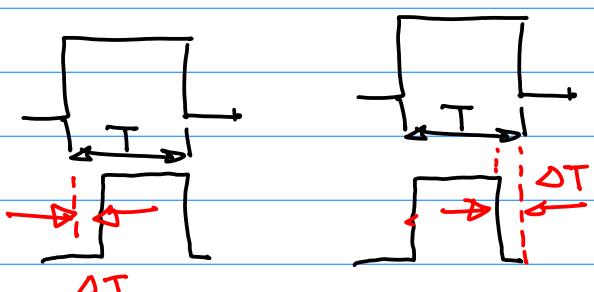
Test 1: Embedded @  $N_i \rightarrow$  RF Board ;

Test 2: Embed @  $N_i \rightarrow$  RF.B.  $\rightarrow$  R.F.B.  $j$

Test 3: Embed @  $N_i \rightarrow$  Embed @  $N_j$

— OverSampling Technique

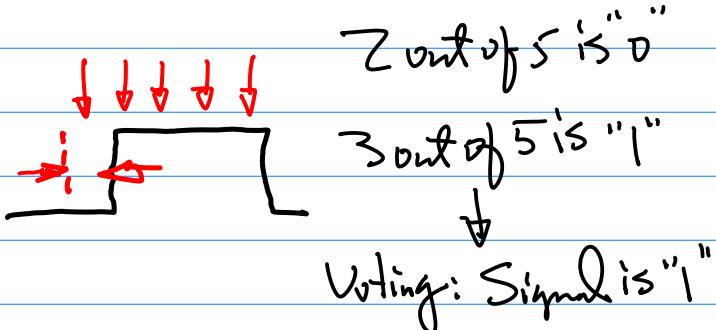
Why? Noisy Environment; Rx Data Distant Variation (From Data Sheet)



# CMPE245

28

Read more, Reliable, By "Voting"



Clock Rate for OverSampling:

5X faster than the Bit Rate

New Buffer is Needed, it is 5 times

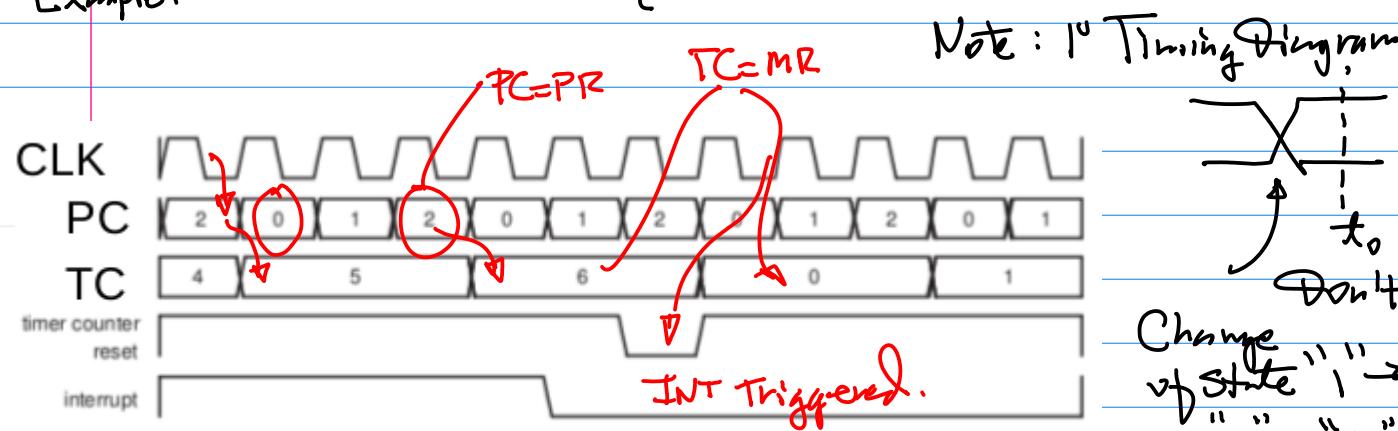
Bigger. Sample Code for LPC1769 Timer

[https://github.com/hualili/CMPE245-Embedded-Wireless/blob/master/LPC1769\\_EINT\\_TIMER2016-4-19.zip](https://github.com/hualili/CMPE245-Embedded-Wireless/blob/master/LPC1769_EINT_TIMER2016-4-19.zip)

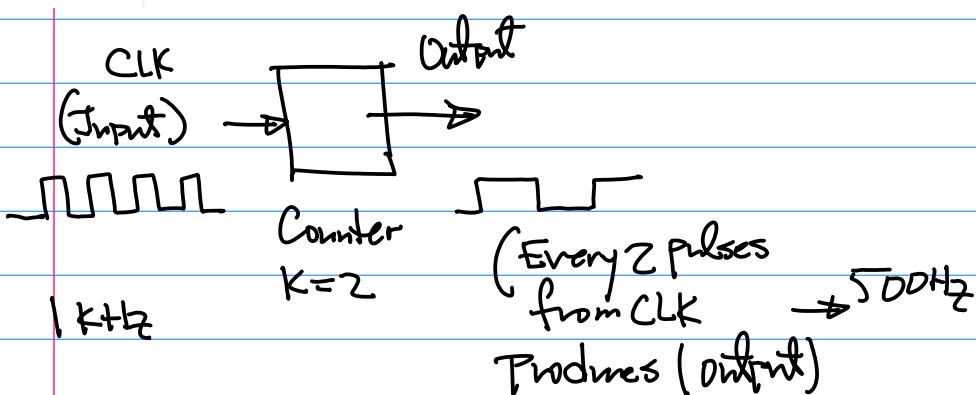
From Part 2 pdf on git

Example: INT Timer SPIRIS:

CLK  
PC: Prescaler Counter  
TC: Timer Counter



Change of State "1" → "0" or "0" → "1"



2° Marking on PC indicates PR=2;

$$MR = 6$$

2nd Counter with Input from the 1<sup>st</sup> Counter.

Example: INT TIMER Design for Sync. Project.

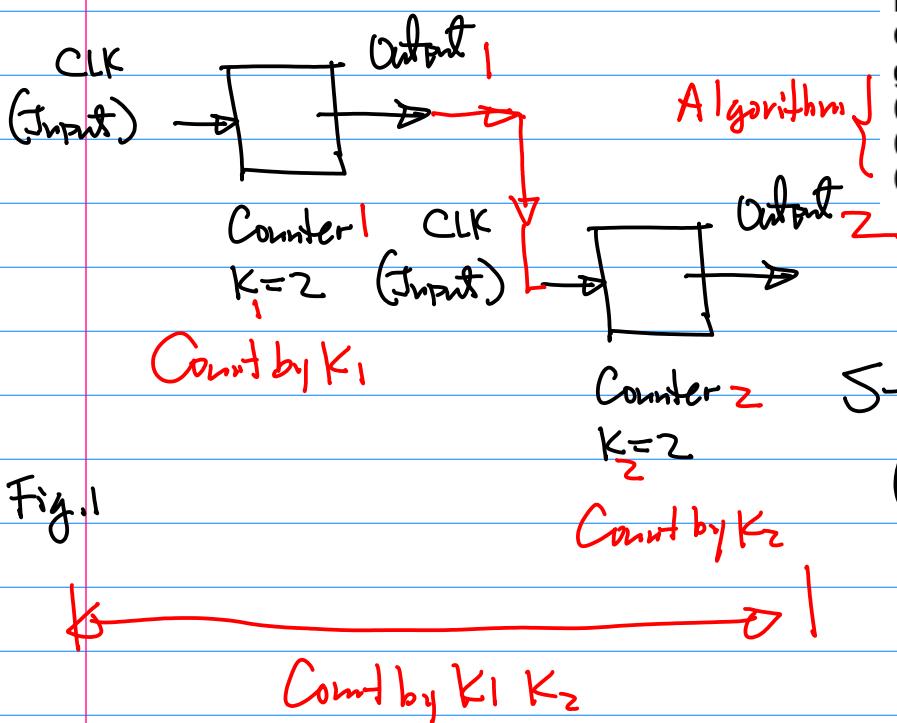


Fig.1

$\xrightarrow{K}$   $\rightarrow 1$

Count by  $K_1 K_2$

Oct 11 (Monday)

Update: 1<sup>o</sup> LISA Sync Project

Extension from Oct 18<sup>th</sup> to Oct

25<sup>th</sup> (Monday), 11:59 PM.

Submission on CANVAS

Z021F-108 for the Project

Requirements + Rubrics.

2<sup>o</sup> Timer Design Reference.

NXP UM.

Doc. ID  
please google it & Down



Load it as Ref.

Example:

Given PR = 2, MR = 6; An interrupt generated on match.

- (1) at every clock, PC  $\rightarrow$  PC+1;
- (2) when PC = PR, TC  $\rightarrow$  TC+1 ;
- (3) when TC = MR, INT generated.

Design Interrupt at every 20 ms.  $\Delta T = 20 \text{ msec}$

Step 1. Special Purpose Registers.

- (1) PC
- (2) PR
- (3) TC
- (4) MR

Table 426. TIMER/COUNTER0-3 register map

Generic Name	Description	PPSV1
IR	Interrupt Register. The IR can be written to clear it and can be read to identify which of eight possible interrupt pending.	
TCR	Timer Control Register. The TCR is used to control Counter functions. The Timer Counter can be controlled through the TCR.	
TC	✓ Timer Counter. The 32-bit TC is incremented by PCLK. The TC is controlled through the TCR.	
PR	✓ Prescale Register. When the Prescale Counter reaches this value, the next clock increments the TC.	
PC	✓ Prescale Counter. The 32-bit PC is a counter that is cleared to the value stored in PR. When the value in PC is incremented and the PC is cleared. The PC is controlled through the bus interface.	
MCR	Match Control Register. The MCR is used to generate a match signal and if the TC is reset when a Match occurs.	
MRO	Match Register 0. MRO can be enabled through the MCR.	
MR0	Match Register 0. MRO can be enabled if the TC, stop both the TC and PC, and/or every time MRO matches the TC.	
MR1	Match Register 1. See MRO description.	
MR2	Match Register 2. See MRO description.	

Step 2. Pre-requisite PCLK Rate

System Clock Rate  $\rightarrow$  Configured to Desired

PCLK  
By SPRs  
 $\downarrow \frac{1}{4}, \dots$

Assume PCLK = 10 MHz

OR,

$$N = \frac{T_{goal}}{T_{PCLK}} = \frac{20 \times 10^{-3}}{1 \times 10^{-7}} = 20 \times 10^4 \dots (3b)$$

$$N = N_1 N_2 = 20 \times 10^4 = \underbrace{2 \times 10^3}_{N_1} \times \underbrace{1 \times 10^2}_{N_2}$$

(Sample code on Class with wb, find PCLK)

Step 3 Find Timing Relationship

Between PCLK and your design

target. e.g.

$T_{PCLK}, T_{goal}$  where

$$T_{PCLK} = \frac{1}{f_{PCLK}} = \frac{1}{10 \times 10^6} = 1 \times 10^{-7} \text{ sec.} \dots (1)$$

$$T_{goal} = 20 \text{ ms} = 20 \times 10^{-3} \text{ sec.}$$

$$= 2 \times 10^{-2} \text{ sec.} \dots (2)$$

$$N_1 = 2 \times 10^3 \text{ so, set PR} = N_1 = 2 \times 10^3$$

$$N_2 = 1 \times 10^2, \text{ set MR} = N_2 = 1 \times 10^2$$

Note: 11Kbps (1024 bits/sec).

PCLK = 40 MHz

$$T_{PCLK} = \frac{1}{40 \times 10^6} ;$$

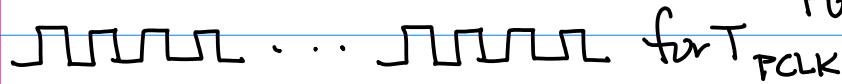
$$T_{goal} = \frac{1}{1024} \text{ sec.}$$

$$N = \frac{T_{goal}}{T_{PCLK}} = \frac{1}{1024} \times 40 \times 10^6$$

$$= N_1 N_2$$

For Oversampling 5X.

Fig.2



$$T'_{goal} = T_{goal} \times \frac{1}{5}$$

for  $T_{goal}$  Hence, New  $N_{oversampling}$

Either Edge Triggered or Level Triggered.

$$N_{over} = \frac{T'_{goal}}{T_{PCLK}}$$

Oct 13 (Wed)

Homework On Base Band Signal  
and Spectrum Analysis.

Note:  $\eta = \frac{\text{Energy in Freq Range}}{\text{Entire Energy}}$

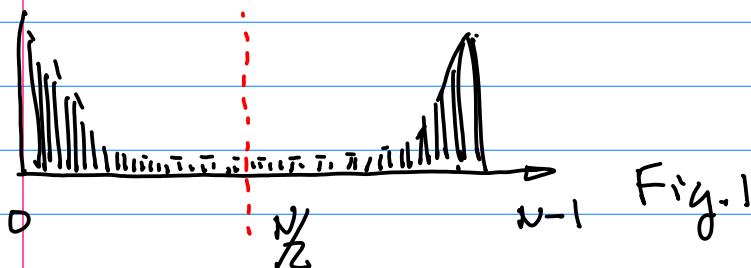
$$= \frac{P(0) + P(1)}{\sum_{i=0}^{N-1} P(i)} = \frac{P(0) + P(1)}{P(0) + \dots + P(N-1)} \dots (1)$$

Power Spectrum Calculation

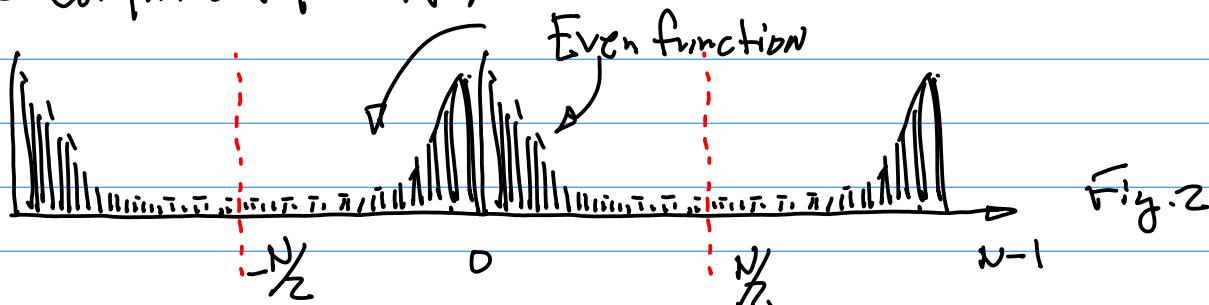
$$P(m), m=0, 1, 2, \dots, N-1$$

(make  $N$  for Computation)

512 points  $\rightarrow$  fft.c  
make sure  
 $N = 512$



You may want to Remove  $P(0)$   
D.C. Component from  $P(m)$ .



$P(m) = P(-m)$  Even function ... (za)

$P(m) = P(m + PN)$ ,  $P=0, 1, 2, \dots$  Periodical Function ... (zb)

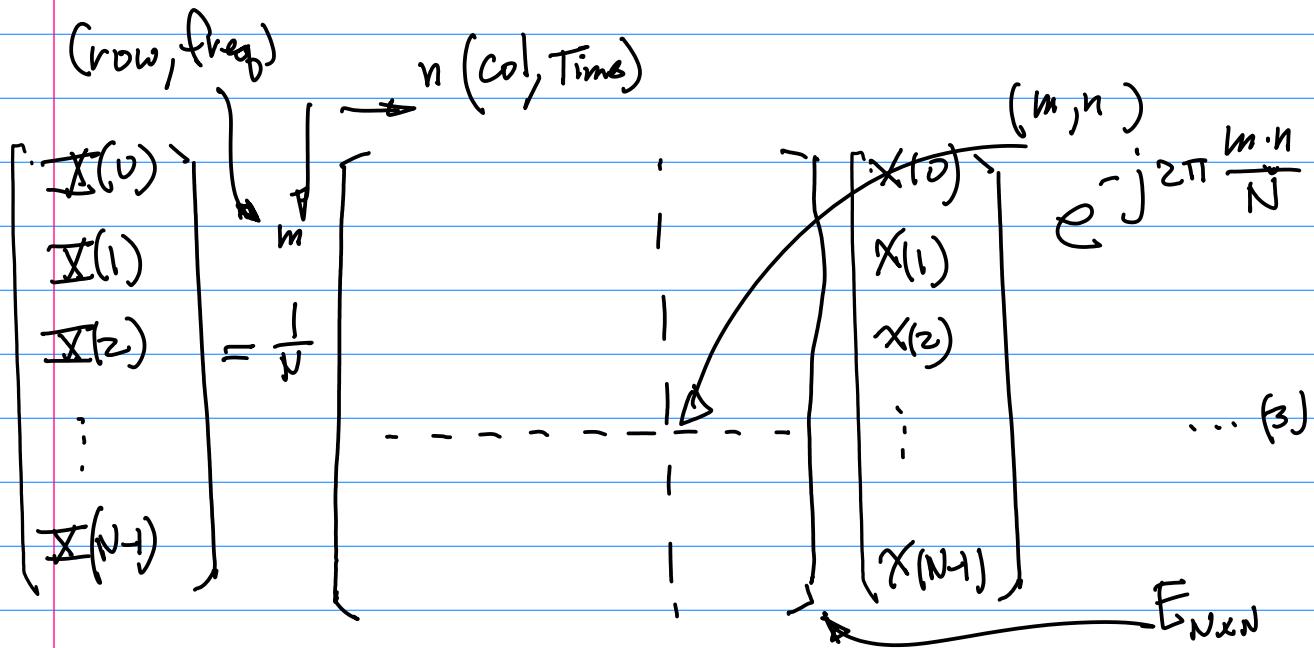
Presentation (Show+Tell)

Bring your Project 1 (on-going work)  
to the Class, make Demo.

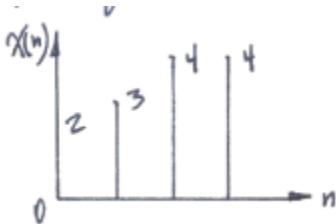
Example:

Given Base Band Signal  $x(0), x(1)$   
 $x(2), x(3)$ , Find Power Spectrum.

Sol:



from Handout Example on the Class github.



given condition

$$1^{\circ} \quad x(0)=2, x(1)=3, x(2)=x(3)=4$$

From the

$$\sum x(n)$$

First, find  $E_{N \times N}$ , e.g.  $E_{4 \times 4}$

Based Eqn(3), we can define  
Eqn(4)

$$e^{-j2\pi \frac{m \cdot n}{N}} =$$

$$\cos 2\pi \frac{m \cdot n}{N} - j \sin 2\pi \frac{m \cdot n}{N} \dots (4)$$

at 1st Row, 1st col.

$$m=0, n=0$$

$$e^{-j2\pi \frac{0 \cdot 0}{N}} = 1,$$

at 1st Row, 2nd col.

$$m=0, n=1$$

$$e^{-j2\pi \frac{0 \cdot 1}{N}} = 1$$

$$4^{\circ} \quad \text{Highest Frequency Component}$$

the Highest Frequency Index

$$M = \frac{N}{2} - 1$$

# Cmpe245

33

for 1st Row  $m=0$ , therefore the entries are always Equal to 1 ( $m=0$  Always)

Consider 1st col.

for 1st col. 2nd Row  
 $\downarrow n=0 \quad \downarrow m=1$

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{1 \cdot 0}{N}} = 1$$

for 1st col, 3rd Row.

$$n=0, m=2$$

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{0 \cdot 2}{N}} = 1$$

;

All the Entries on the 1st Col. is always equal to 0.

Secondly, for the Rest of the entries (Not the 1st Row, Not the 1st col.), just use Eqn(4) to Evaluate.

$$\begin{bmatrix} I(0) \\ I(1) \\ I(2) \\ I(3) \end{bmatrix} = \frac{1}{4} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -j & -1 & j \\ 1 & -1 & 1 & -1 \\ 1 & j & -1 & -j \end{bmatrix} \begin{bmatrix} 2 \\ 3 \\ 4 \\ 4 \end{bmatrix}$$

Main Diagonal

Symmetric w.r.t.

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{n \cdot m}{N}}$$

(Symmetric).

Oct 18th (Monday)

1. Review & Master Copy of Homework Assignment Since the Beginning of the Semester. Will be Posted on CANVAS please Check. Submission Requirements
  - a. Based on the List, you put them together into one zip file, then Submit to CANVAS.
  - b. Please observe the time Line, Due in 1 week. Oct. 25 (Monday)

2. Midterm, Nov. 3rd (Wed), 1 hour, Close Book, Close Notes, 1 page formula Sheet is allowed.

Format : On-Line, 1<sup>o</sup> Video On all the time, 2<sup>o</sup> Scan the papers, and Put them into One pdf file, Submit One pdf file on CANVAS.

Naming Convention : First\\_Last\\_4Digits-

Cmpe245\_mi.d.pdf

Example: Continuation of Power Spectrum Analysis.

Consider for 1st Row, 2nd col.

$$m=0, n=1$$

from

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{0 \cdot 1}{N}} = 1$$

for 2nd Row, 2nd col.

$$m=1, n=1$$

hence

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{1 \cdot 1}{4}}$$

$$= \cos 2\pi \frac{1}{4} - j \sin 2\pi \frac{1}{4}$$

$$= \cos \frac{\pi}{2} - j \sin \frac{\pi}{2}$$

$$= 0 - j = -j$$

.....

for  $m=3$  (Last Row),  $n=2$   
(3rd col)

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{3 \cdot 2}{4}}$$

$$= e^{-j2\pi \frac{3}{2}} = e^{-j3\pi}$$

$$= \cos 3\pi - j \sin 3\pi = -1$$

Therefore, the entire matrix

can be evaluated.  $E_{N \times N}$

Note: Symmetric property of  $E_{N \times N}$

e.g.

$$e^{-j2\pi \frac{m \cdot n}{N}} = e^{-j2\pi \frac{n \cdot m}{N}} \dots (1)$$

Then, Compute D.F.T.

2017F-109-1D-DFTv2.pdf

2017F-109-FFT program 20

$$\begin{bmatrix} \mathbf{x}(0) \\ \mathbf{x}(1) \\ \mathbf{x}(2) \\ \mathbf{x}(3) \end{bmatrix} = \frac{1}{4} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -j & -1 & j \\ 1 & -1 & 1 & -1 \\ 1 & j & -1 & -j \end{bmatrix} \begin{bmatrix} z \\ 3 \\ 4 \\ 4 \end{bmatrix}$$

So, ... (3\*)

$$\mathbf{x}(0) = \frac{1}{4}(z+3+4+4) = 3.25$$

$$\mathbf{x}(1) = \frac{1}{4}(z-3j-4+j) = \frac{1}{4}(-2+j)$$

$$\mathbf{x}(2) = \frac{1}{4}(z-3+4-4) = \frac{1}{4}(-1)$$

$$\mathbf{x}(3) = \frac{1}{4}(z+3j-4-4j) = \frac{1}{4}(-2-j)$$

Then, Power Spectrum,

$$P(m) = \sqrt{R_e^2[\mathbf{x}(m)] + I_m^2[\mathbf{x}(m)]} \dots (2)$$

For Simplification purpose, use Eqn (2) w/o Square,

$$P(m) \cong \sqrt{R_e^2[\mathbf{x}(m)] + I_m^2[\mathbf{x}(m)]} \dots (2b)$$

for  $m=0$  (DC Component),

$$\left. P(m) \right|_{m=0} \stackrel{\cong}{=} \text{Re}[X(0)] + \text{Im}[X(0)]$$

$$= (3.25)^2 + (0)^2 = (3.25)^2$$

with  $\sqrt{3.25^2} = 3.25$

$$(\text{Total Energy}) = \sum_{m=0}^{n-1} P(m)$$

$$= P(0) + P(1) + \dots + P(n-1)$$

$$= P(0) + \dots + P(3)$$

So, we can finish the power spectrum computation as,

$$= 3.25 + \frac{\sqrt{5}}{4} + \frac{1}{4} + \frac{\sqrt{5}}{4} = 4.6180$$

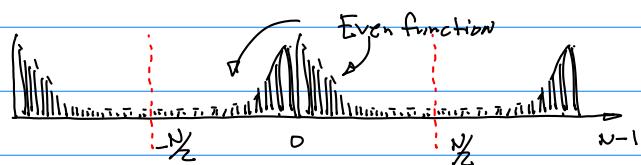
$$P(m) \stackrel{m=0}{=} 3.25$$

$$P(1) = \frac{1}{4} \sqrt{2^2 + 1^2} = \sqrt{5}/4$$

$$P(2) = \frac{1}{4} \sqrt{(-1)^2 + 0^2} = 1/4$$

$$P(3) = \frac{1}{4} \sqrt{(-2)^2 + (1)^2} = \sqrt{5}/4.$$

$$\therefore n = \frac{3.25 + \frac{\sqrt{5}}{4}}{3.25 + \frac{1}{4} + \frac{\sqrt{5}}{2}} = \frac{3.8090}{4.6180} = 0.8248 \approx 82\%$$

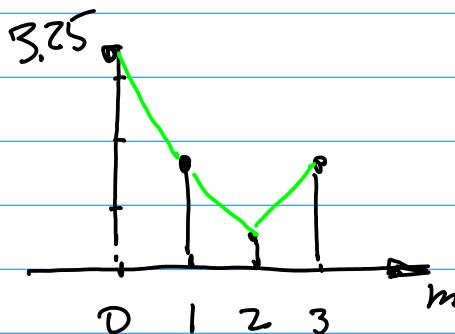


Then, finally the Energy Index

$$\eta = \frac{\underset{\text{Frequency Range}}{\text{Energy in the Selected}}}{\underset{\text{(Total Energy)}}{\text{}}}$$

... (3)

(From PP.31)

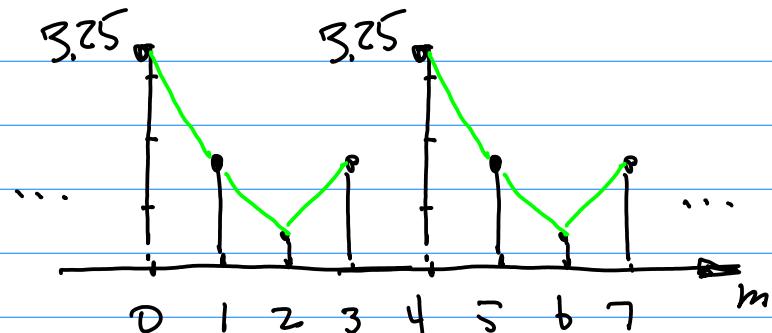


Suppose, m upper bound

$m=1$ , Find  $\eta = ?$

$$\left. \begin{array}{l} \text{Energy in the Selected} \\ \text{Frequency Range} \end{array} \right) = P(0) + P(1)$$

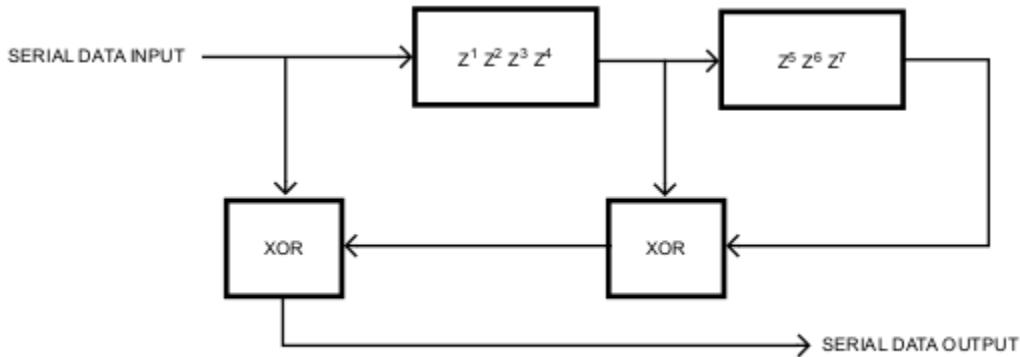
$$= 3.25 + \sqrt{5}/4 = 3.8090$$



IEEE Standard, 802.11b.

2021F-101-IEEE-802.11b.pdf

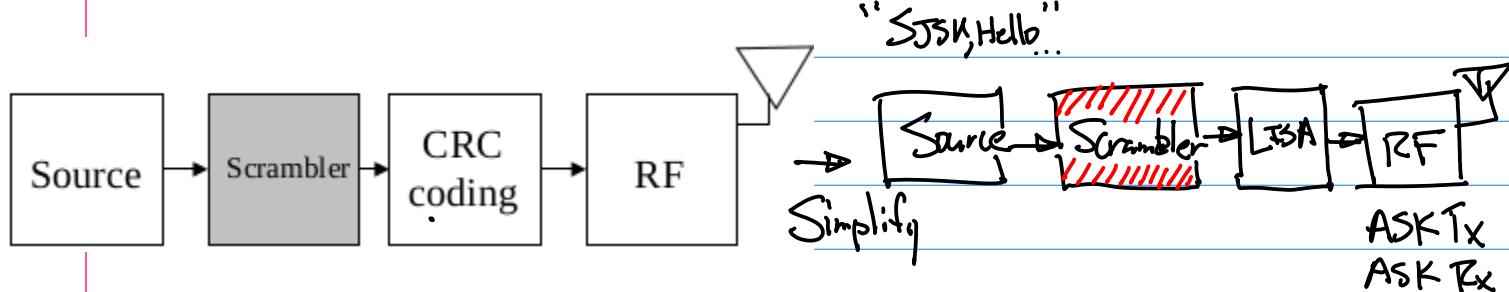
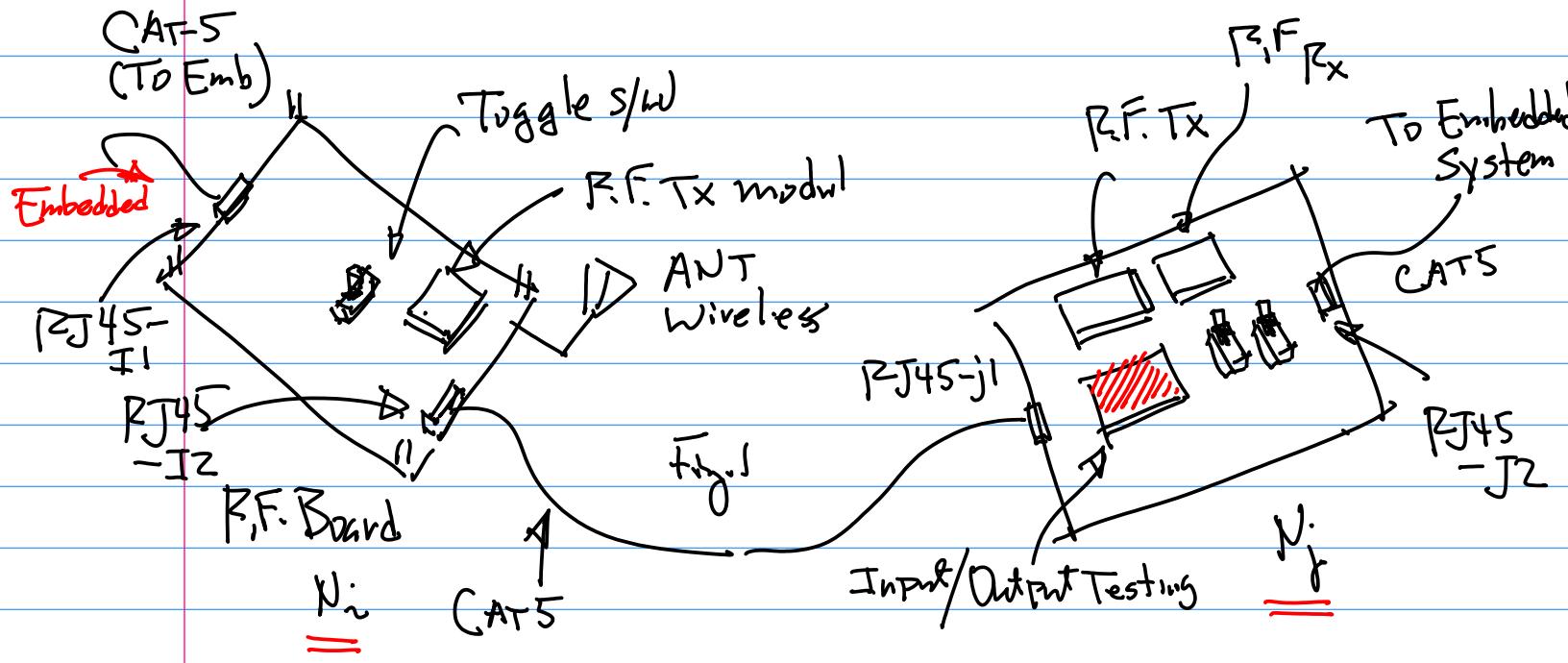
Example: Scrambling Algorithm



**Figure 132—Data descrambler**

#### **18.2.4 PLCP/High Rate PHY data scrambler and descrambler**

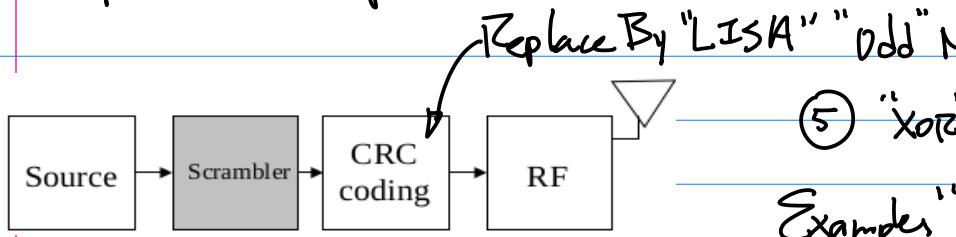
The polynomial  $G(z) = z^{-7} + z^{-4} + 1$  shall be used to scramble all bits transmitted.



Oct. 20 (Wed)

## Scrambler/Descrambler Design.

## Step 1. Block Diagram



We can have different orders of a Scrambler. 3, 5, 7, 9, ..., 13, 15, ...

(4) the order has to be  $2^n + 1$ ,  $n=1, 2, \dots$ 

(5) "XOR" Unit

Example "SJSU" string  $\rightarrow$  SASCII  
. ↓

0x f5 ?

bits  
"D's & I"  
1111 0101

Step 2. From IEEE 802.11b Fig 1

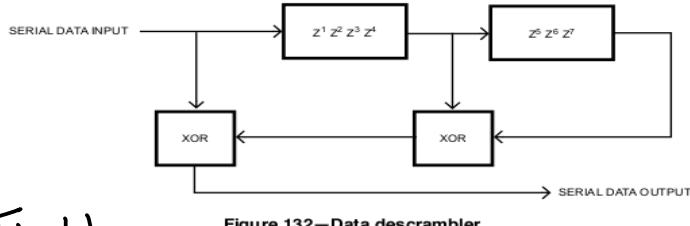


Figure 132—Data descrambler

Fig 1-b

Bit1 Bit2 : XOR

0 0 | 0

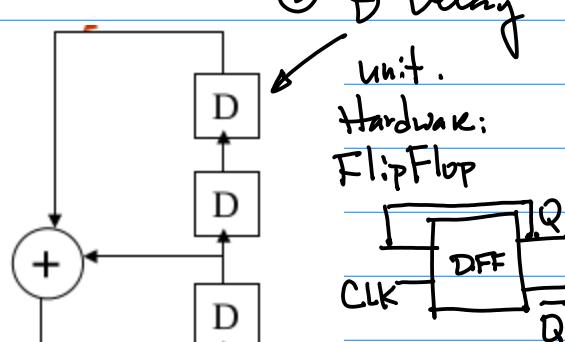
0 1 | 1

1 0 | 1

1 1 | 0

Fig. 2

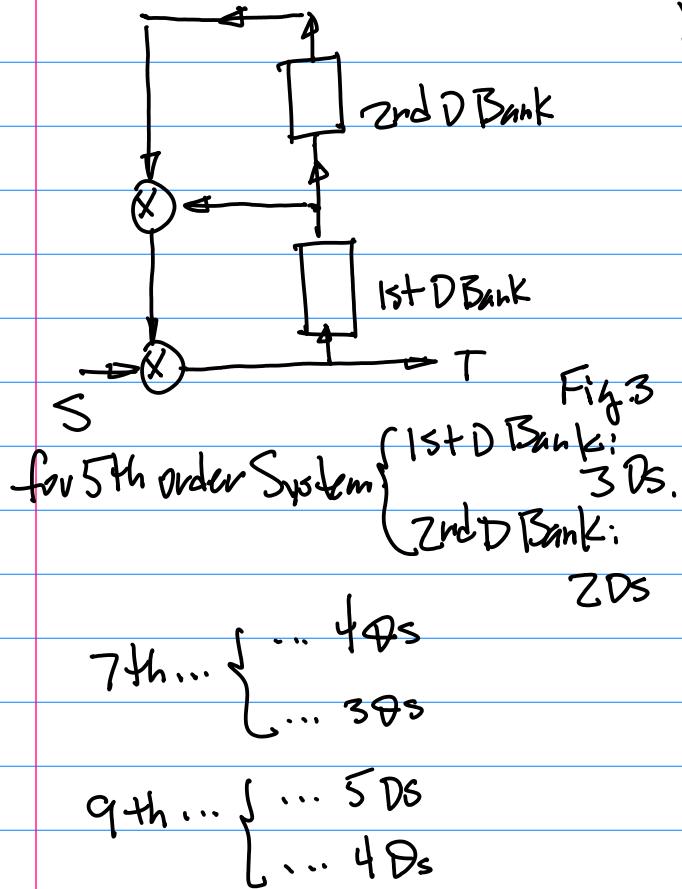
(5) .. "XOR" Unit

Input "S",  
Source

Transmission

C/C++ Implementation for "XOR" is Bitwise Operation.

(6) Two Delay Banks, the 1st Delay Bank is defined as the Bank tied to the Output  $T_1$ . And it is always 1 order higher than the 2nd Bank.(7) The Architecture of the Scrambler:  $\cong 2$  Banks↳ 2 feedbacks.  $\cong$  Two "XOR"Note: Total 5 Delays  $\rightarrow$  Defines the order of the scrambler, 5th Order Scrambler.



Note : 1. De-Scrambler Architecture :

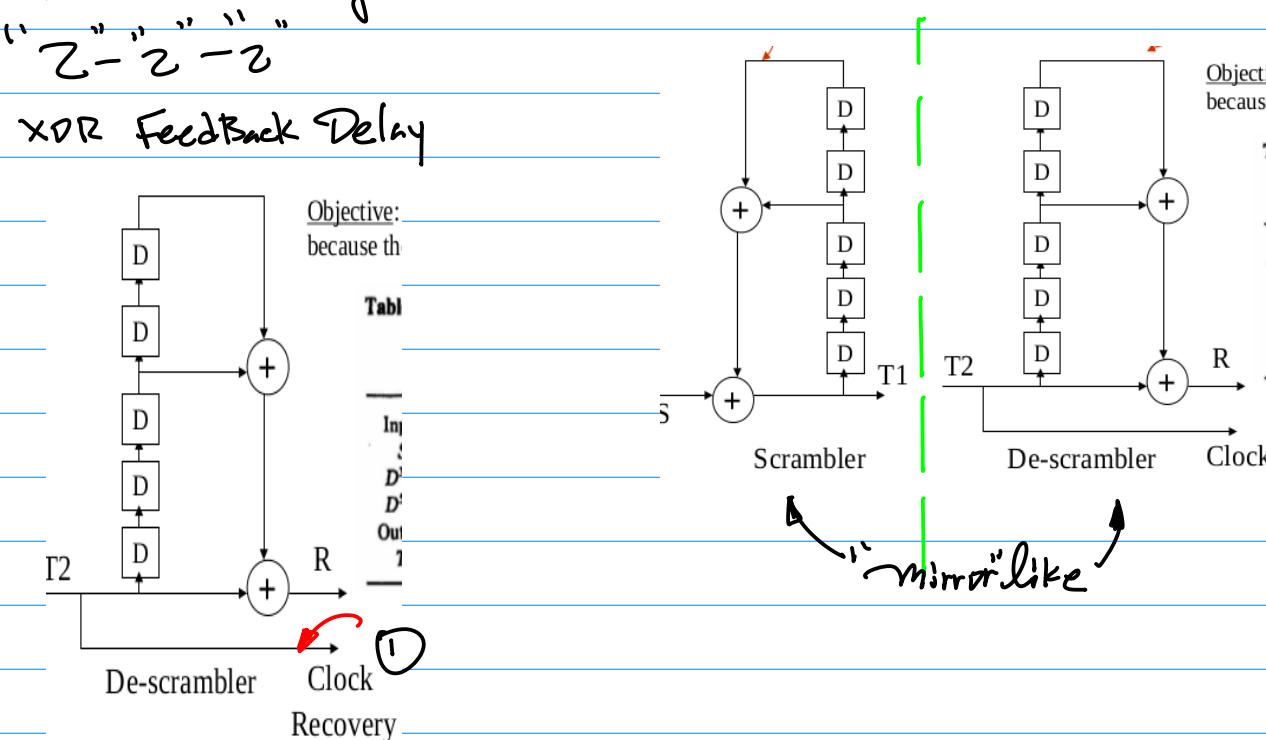
"Z-Z-Z" Z "XDR" units,  
Z D Banks, BANK1, Z ;  
Bank1 is 1 order higher  
2 feedforward Branches.

Note: Clock Recovery Output, to provide Timing Signal for Better Synchronization

Question: What is the general guideline for Timing Synchronization Preservation / Recovery?  
Ans: Alternating "0's & 1's.

Remark: The objective of Scrambler is  
to preserve timing information by Scrambling  
to alter long "0's and/or long "1's  
in the source in the communication.

Design of De-Scrambler :



Oct. 25 (Mon)

Note: Midterm Exam, Nov. 3rd  
(Wed) On Zoom. During

Zoom Examination: (1) Video of the entire session; if black screen, then red flag. Could lead to disqualification.  
if emergency, text me at (650) 410-1116.  
(2) 1 hr Exam (bornin), plus 5-10 minutes extra time, so you can scan your paper. Once it is done, convert all the papers (in Jpeg for example) into a single pdf document.

<https://www.google.com/search?client=ubuntu&channel=fs&q=convert+multiple+jpegs+to+pdf&ie=utf-8&oe=utf-8>

③ One exercise session on Next

Lecture, Scan multiple pages, put them together into one pdf, then submit to CANVAS.

Note New Homework Assignment

{ One on Scrambler/DeScrambler Design.

Review of All Homeworks.

Objective: Scrambler Design allows us to preserve timing/sync information by producing alternating patterns of long "0's" or long "1's"

Example: Scrambling/Desrambling Design.

Note: The De-Scrambler Output consists of Two Signals:

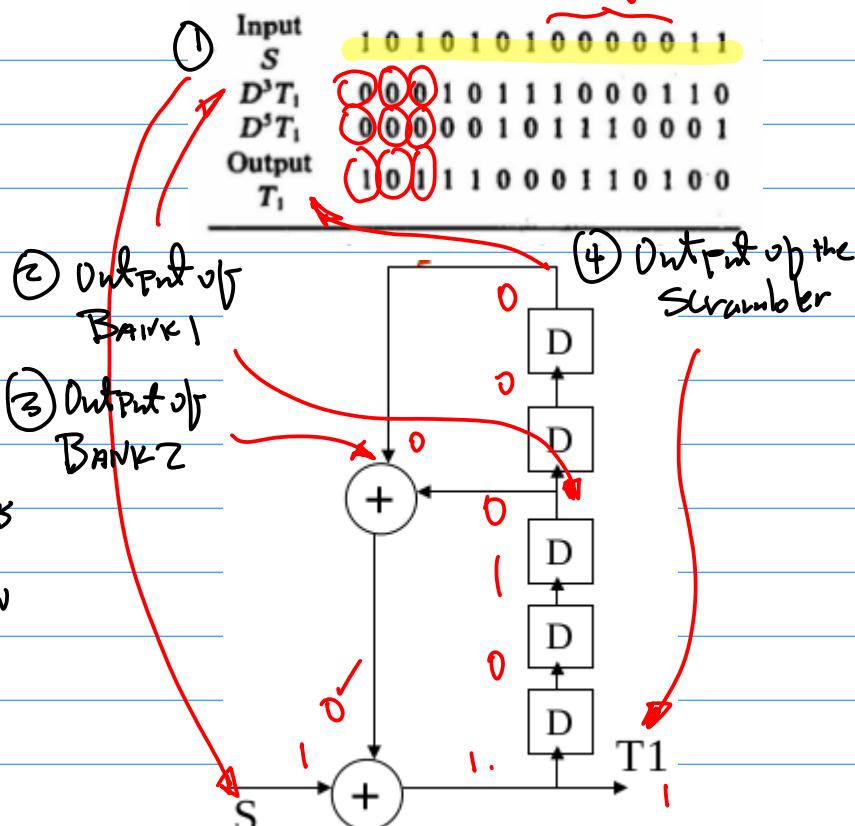
{ One is just for timing that the signal received without Desrambling.  
One is the output Signal "R" After Desrambling which is used to Transmitted Signal.

2018F-115-Lecture Scrambler Design HL.pdf

From PPT, the System Block Diagram of Node  $N_i$  (Transmission),  $N_j$  (Receiver)

Table 5.3. Input and output bit streams of the scrambler shown in Figure 5.24

long "0's



Construction of the Table :

- ① Input "S" (Source)
- ② Bank1's Output
- ③ Bank2's Output
- ④ Output of the Scrambler

Homework (Submission) on (CANVAS)

The A week from today. Nov. 1st, Monday

202

(END)

your first name + your last name + scrambler + yy/mm/dd.zip

1. Design a 5<sup>th</sup> order scrambler by

(1.1) drawing its block diagram;

(1.2) suppose input is 1 1 1 1 1 1 0 0 0 0 0, find its output after scrambling.

C/C++, Python Implementation

" ^ " Operator for XOR

3. Write a computer program (Use C/C++, or Python) to implement your design of scrambler and de-scrambler (for the 5<sup>th</sup> order) and verify your result in 1.

Bitwise "XOR" Sample.

temp\_buffer[i] = op1[i] ^ op2[i];

your first name + your last name + scrambler + yy/mm/dd.zip

(END)

" harry-li-Scrambler-2021-10-24.zip "

Another Homework (and Homework

This week) for Midterm Review. Due

2021F-109c-homework-scrambler-cmpe245...

2021F-109c-homework-review1-cmpe245...

1 week from today.  
Nov. 1st (Monday)

Submission on CANVAS

Requirements on Scrambling/De-Scrambling.  
Integration of Scrambling/De-Scrambling  
ON your R.F. Board, Implementation of  
Scrambler/De-Scrambler on your target  
platform.

<https://www.google.com/search?client=ubuntu&channel=fs&q=adafruit.com+product+3072&ie=utf-8&oe=utf-8>

Semester Long project  
on SX1276/.../79

