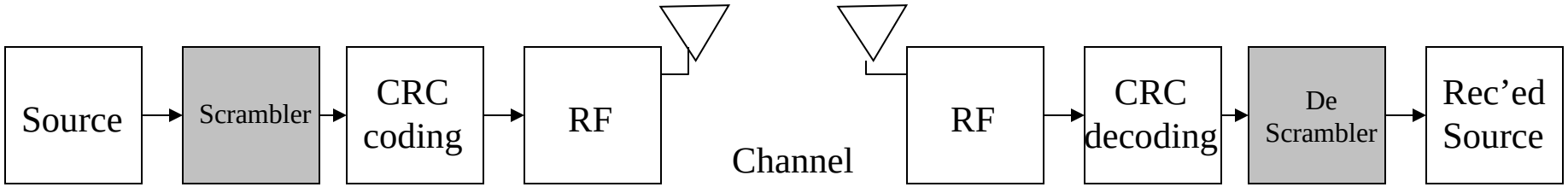
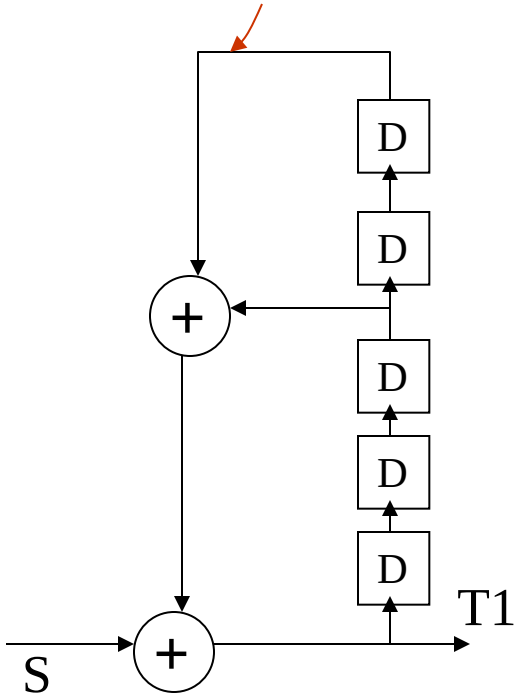
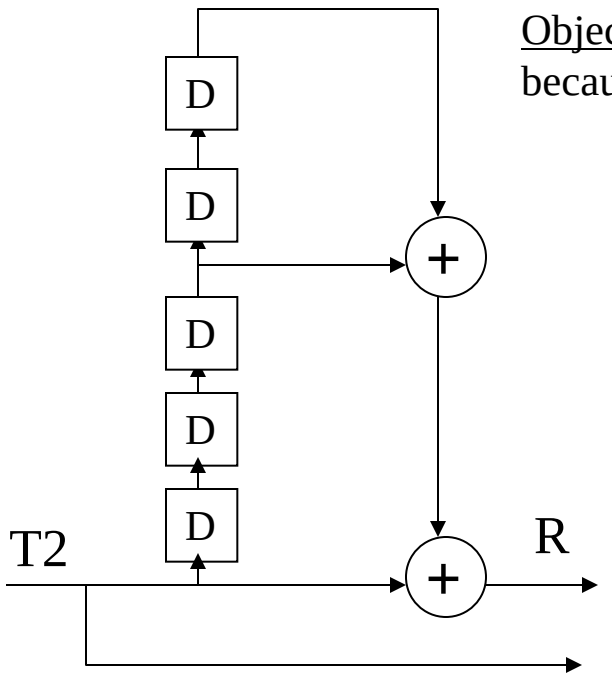
Scrambler Design





Scrambler



De-scrambler

Clock Recovery

Objective: to remove long "1s" or "0s" because they tend to lose timing

Table 5.3. Input and output bit streams of the scrambler shown in Figure 5.24

Input S	1 0 1 0 1 0 1 0 0 0 0 0 1 1
D^3T_1	0 0 0 1 0 1 1 1 0 0 0 1 1 0
D^5T_1	0 0 0 0 0 1 0 1 1 1 0 0 0 1
Output T_1	1 0 1 1 1 0 0 0 1 1 0 1 0 0

Reference: Digital and analog communication systems, by K. Sam Shannugam