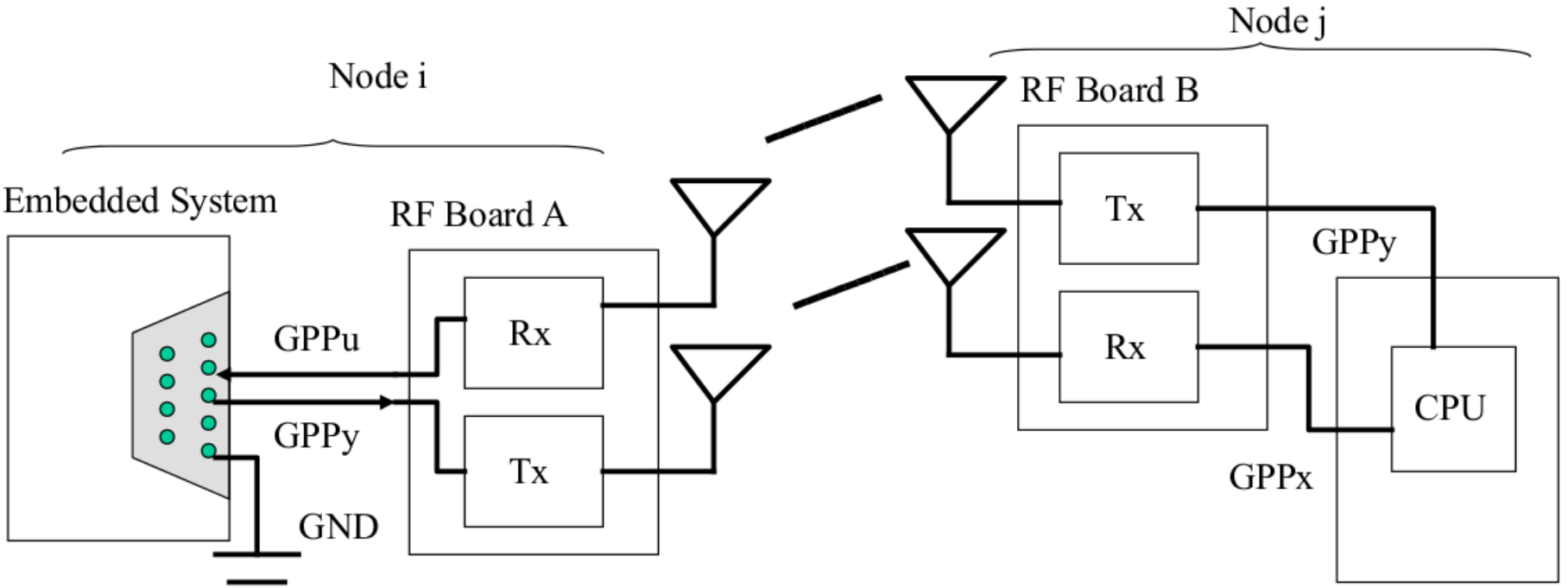
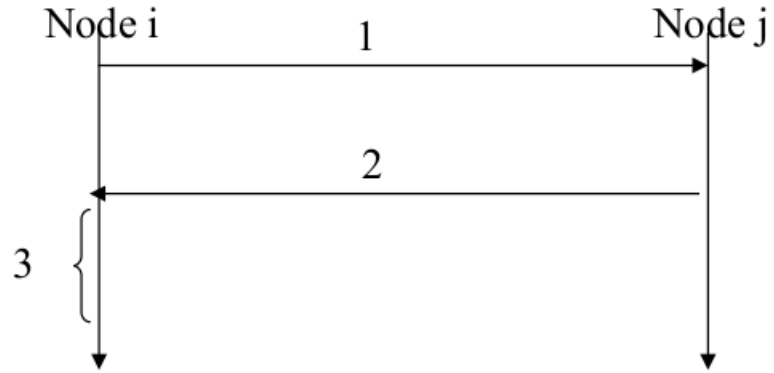
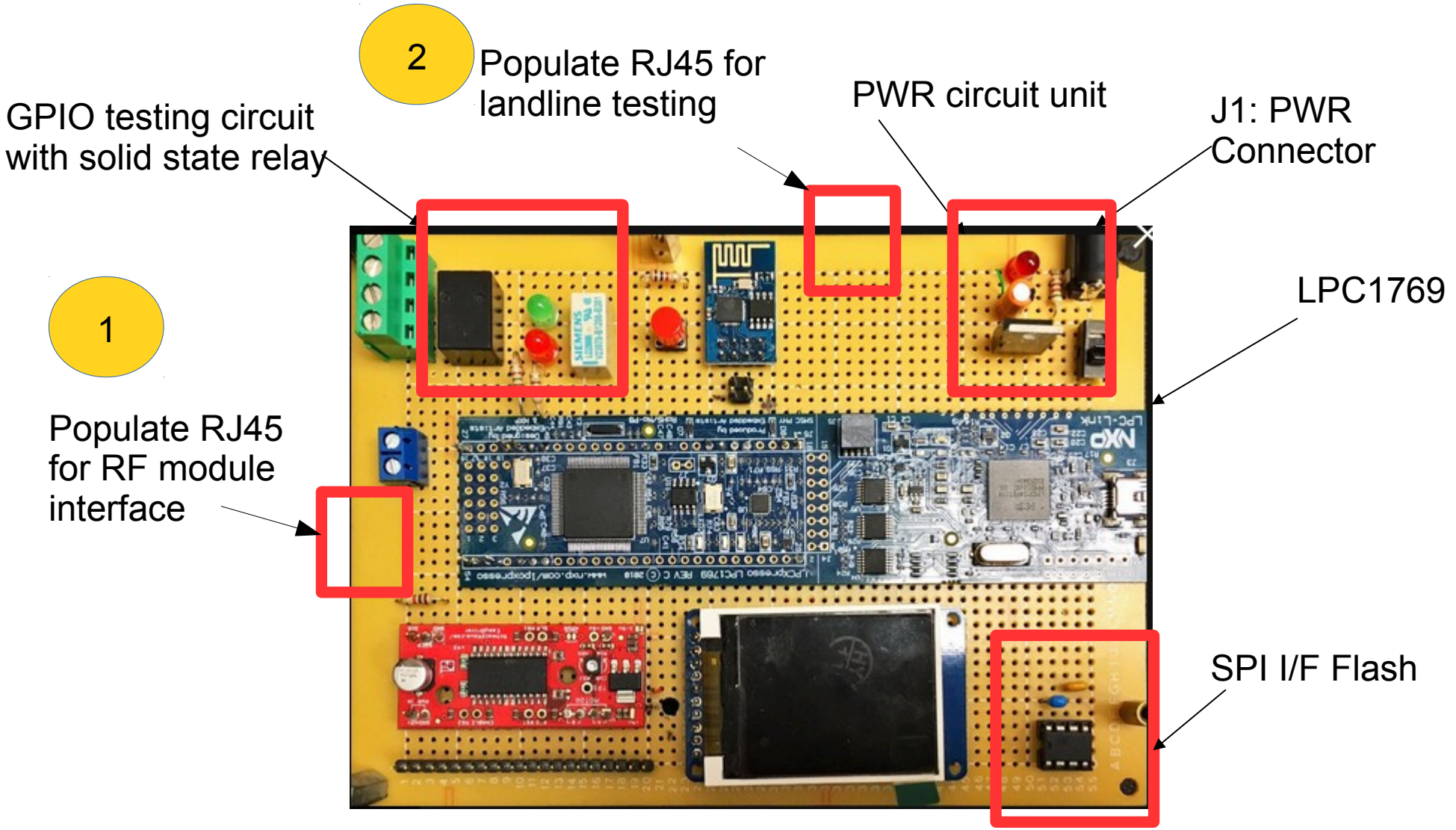
System Architecture





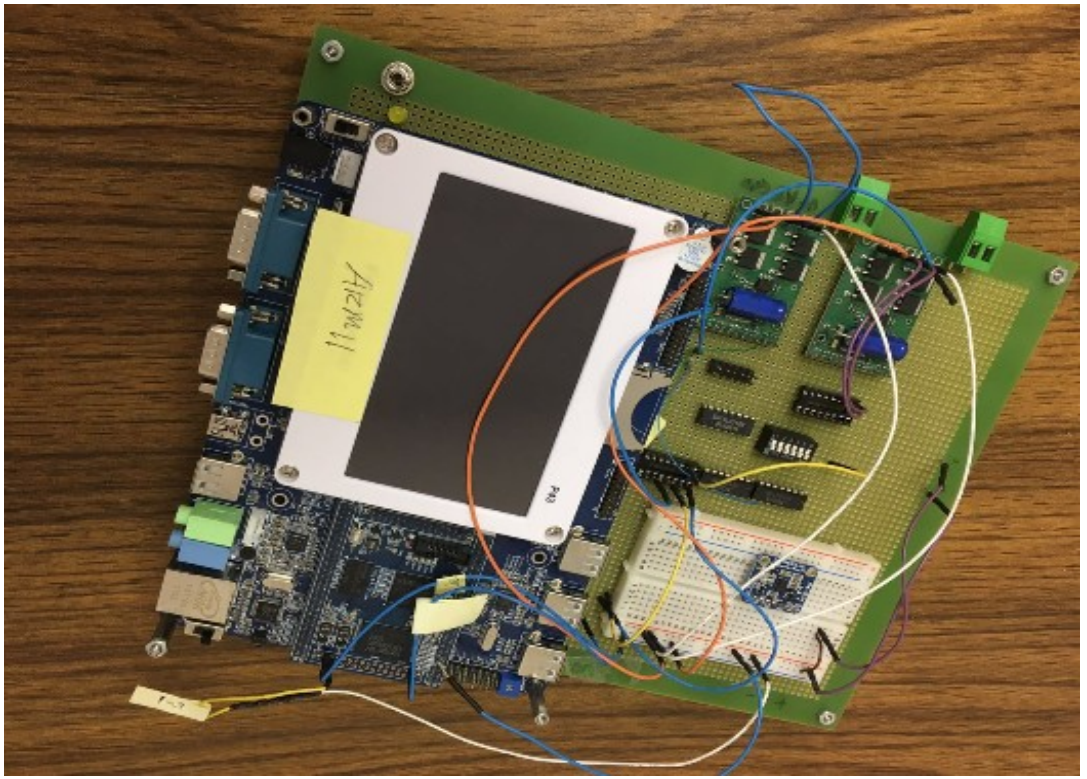
1	N_i send your name and day, hour, and min, second.
2	N_k send "hello xxx, D,H,M,S"
3	N_i process the response and calculate (1) the number of error bits; (2) the loop time

LPCNOD for RF Communications



Dimension: 16 x 11 mm or 6.25 x 4.50 inch

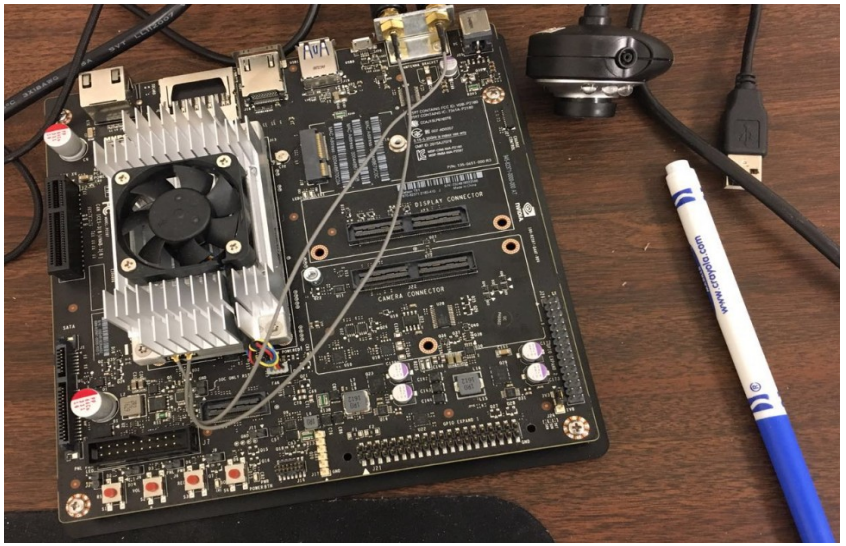
ARMSVR for RF communications



http://www.friendlyarm.net/

FriendlyARM

TX1SVR for RF communications

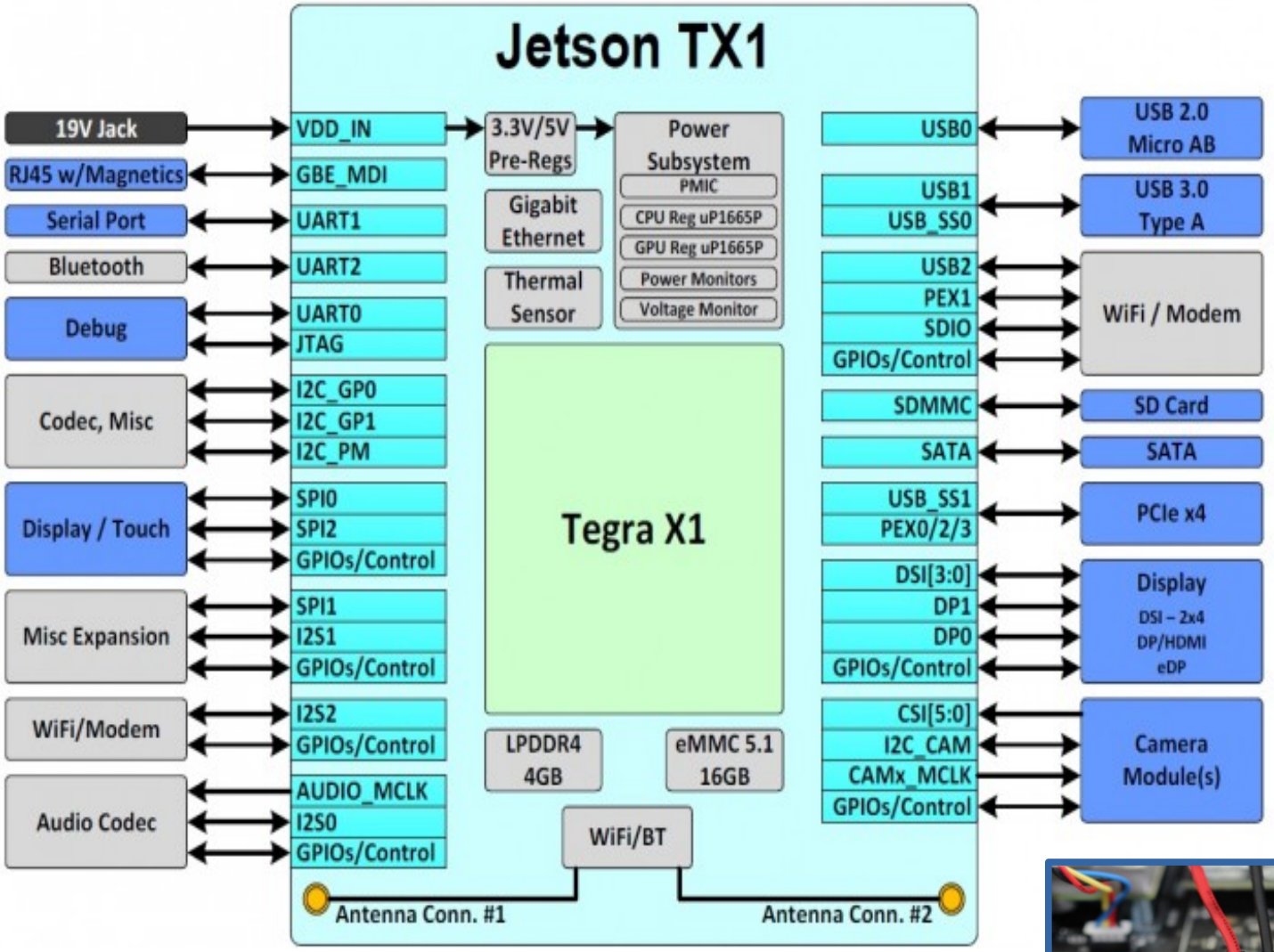


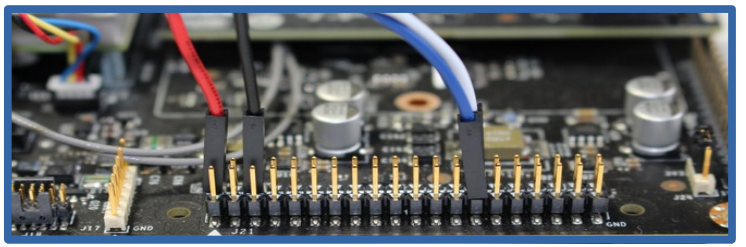
https://developer.nvidia.com/embedded/buy/jetson-tx2

http://elinux.org/Jetson/TX1_SPI

NVIDIA Maxwell ™, 256 CUDA cores
Quad ARM® A57/2 MB L2
video 4K x 2K 30 Hz Encode (HEVC) 4K x 2K 60 Hz Decode (10-Bit Support)
4 GB 64 bit LPDDR4 25.6 GB/s
2x DSI, 1x eDP 1.4 / DP 1.2 / HDMI
Up to 6 Cameras (2 Lane) CSI2 D-PHY 1.1 (1.5 Gbps/Lane)
Gen 2 | 1x4 + 1x1
16 GB eMMC, SDIO, SATA
UART, SPI, I2C, I2S, GPIOs

TX1SVR Architecture Overview





TX1SVR Pinout (1)

NVIDIA Jetson TX1 J21 Header Pinout

	3.3 VDC *Power*	1	2	**5.0 VDC** *Power*		**GPIO_EXP_P17_3V3** *From GPIO Expander (P17)*	15	16	**AO_DMIC_IN_DAT_LVL** *Unused*
	I2C_GP_DAT *General I2C #0 Data 3.3.V*	3	4	**5.0 VDC** *Power*		**3.3 VDC** *Power*	17	18	**GPIO16_MDM_WAKE_AP** *Modem Wake AP GPIO*
	I2C_GP_CLK *General I2C #0 Data 3.3.V*	5	6	**GND**		**SPI_MOSI** *SPI #1 Master Out/Slave In*	19	20	**GND**
	AUDIO_MCLK *Audio Master Clock (1.8/3.3.V)*	7	8	**UART0_TX** *UART #0 Transmit*		**SPI1_MISO** *SPI #1 Master In/Slave Out*	21	22	**GPIO_EXP_P16_3V3** *From GPIO Epander (P16)*
	GND	9	10	**UART0_RX** *UART #0 Receive*		**SPI_CLK** *SPI #1 Shift Clock*	23	24	**SPI1_CS0#** *SPI #1 Chip Select #0*
	UART0_RTS# *UART #0 Request to Send*	11	12	**I2S0_SCLK** *Audio I2S #0 Clock*		**GND**	25	26	**SPI1_CS1#** *SPI #1 Chip Select #1*
gpio38	**GPIO_PE6** *Audio Code Interrupt*	13	14	**GND**		**I2C_GP1_DAT** *General I2C #1 Data (3.3V)*	27	28	**I2C_GP1_CLK** *General I2C #1 Clock (3.3V)*
					gpio219	**GPIO19_AUD_RST** *Audio Reset (1.8/3.3V)*	29	30	**GND**

TX1SVR Pinout (2)

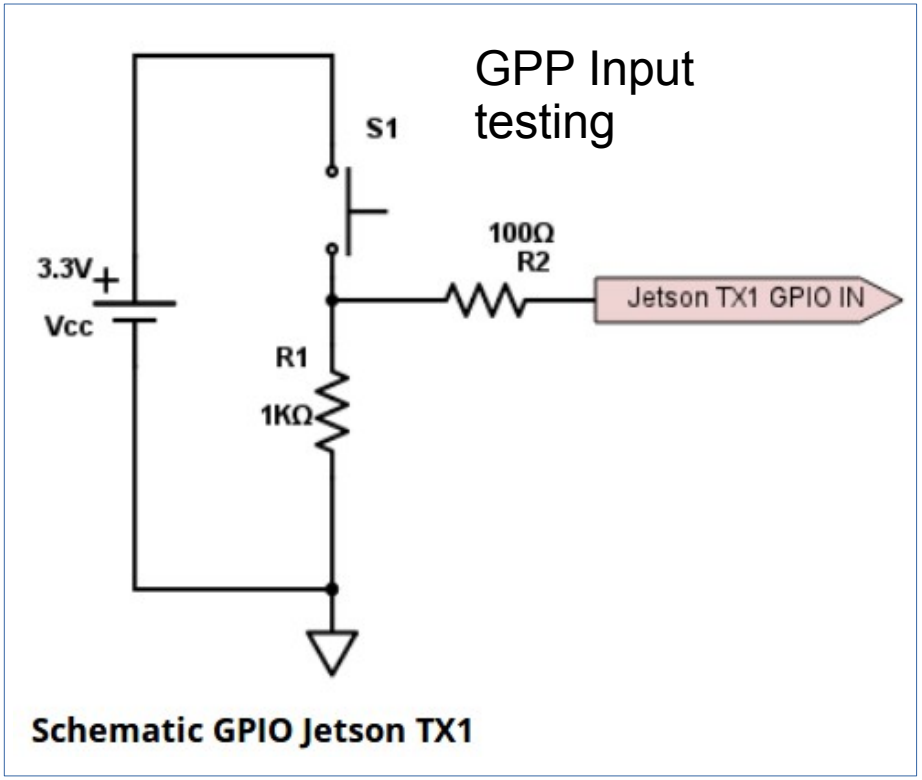
NVIDIA Jetson TX1 J21 Header Pinout

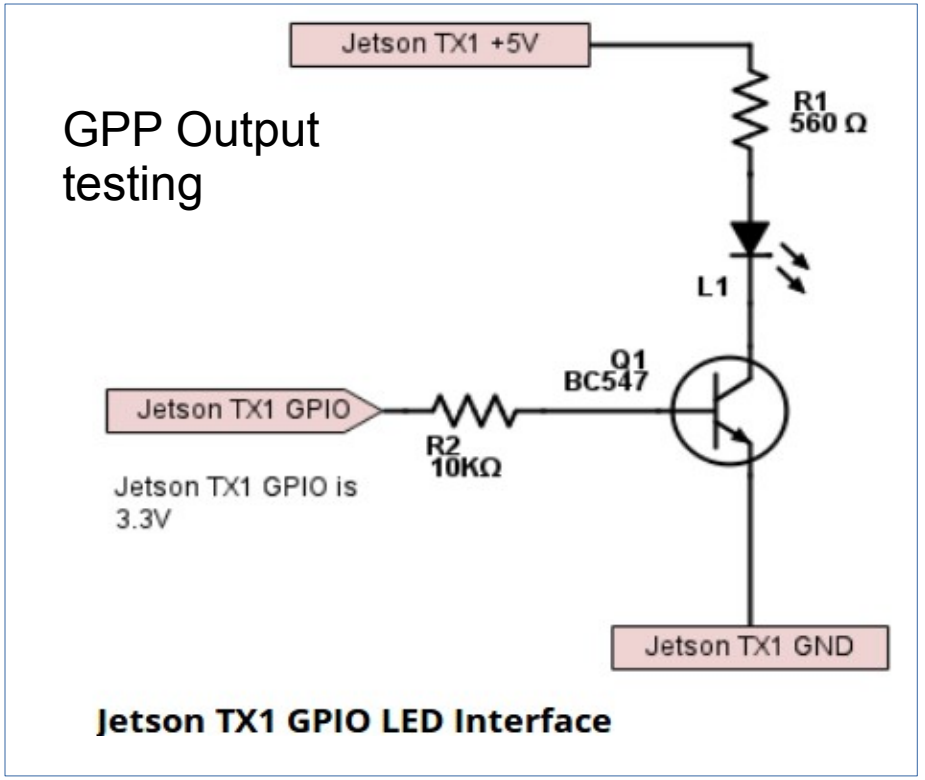
http://www.jetsonhacks.com/2015/12/29/gpio-interfacing-nvidia-jetson-tx1/

Sysfs GPIO	Pin	Jetson Signal Name	PUPD
gpio36	Pin 32	AO_DMIC_IN_CLK	PULL_DOWN
gpio37	Pin 16	AO_DMIC_IN_DAT	PULL_DOWN
gpio38	Pin 13	GPIO20/AUD_INT	PULL_DOWN
gpio63	Pin 33	GPIO11_AP_WAKE_BT	PULL_DOWN
gpio184	Pin 18	GPIO16_MDM_WAKE_AP	PULL_DOWN
gpio186	Pin 31	GPIO9_MOTION_INT	PULL_UP
gpio187	Pin 37	GPIO8_ALS_PROX_INT	PULL_DOWN
gpio219	Pin 29	GPIO19_AUD_RST	PULL_UP

Sysfs GPIO is the name of the virtual file that can be used to access the GPIO port. The file is accessed in the '/sys/class/gpio' directory. Signals on the header can be configured to run at 3.3V or 1.8V by shorting the appropriate pins on the J24 header. For this example, 3.3V is selected, which is the standard configuration. Signals on the J21 header can be configured with a resistor as a PULL_DOWN, PULL_UP, or NORMAL circuit. The standard configuration is noted in the table. The resistance value is 4KΩ.

TX1SVR Input/Output Testing



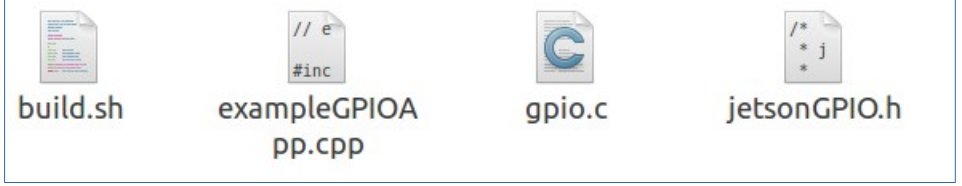


http://www.jetsonhacks.com/2015/12/29/gpio-interfacing-nvidia-jetson-tx1/

TX1SVR GPIO Driver

https://github.com/jetsonhacks/jetsonTX1GPIO

- LICENSE
- README.md
- build.sh
- exampleGPIOApp.cpp
- jetsonGPIO.c
- jetsonGPIO.h

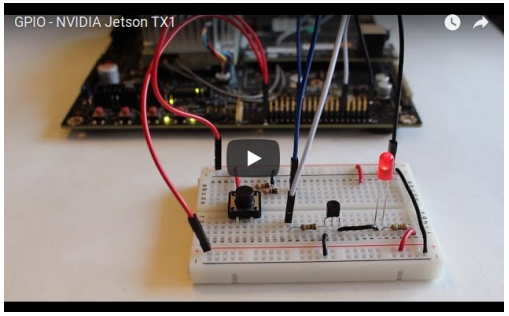


From gpio.h , see the GPIO pin selection

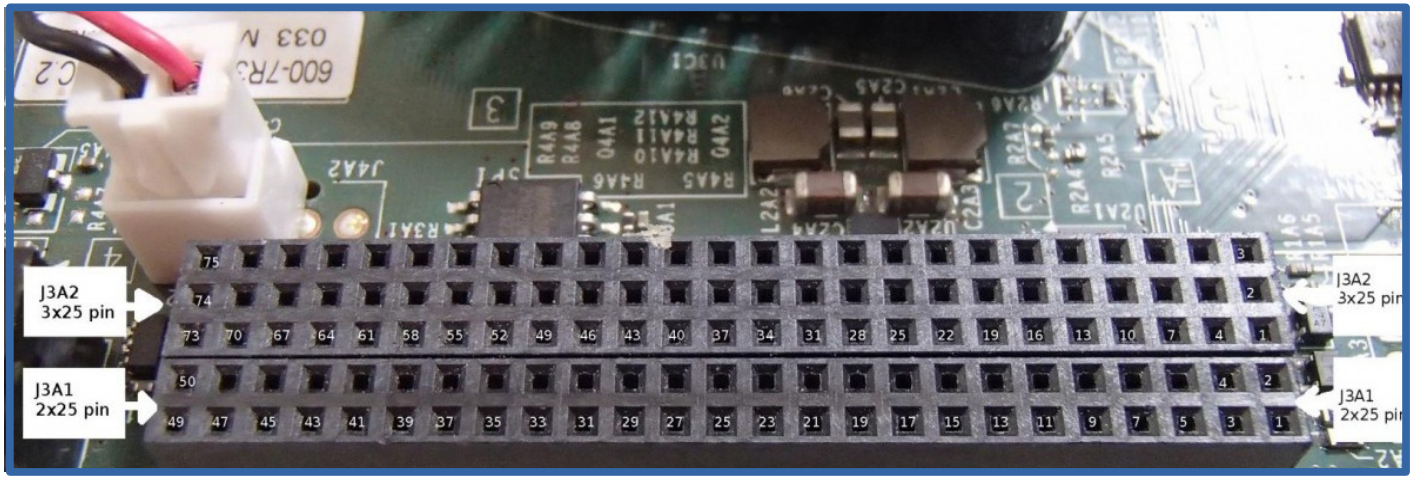
```
enum jetsonTX1GPIONumber {
        gpio36 = 36,      // J21 - Pin 32 - Unused - AO_DMIC_IN_CLK
        gpio37 = 37,      // J21 - Pin 16 - Unused - AO_DMIC_IN_DAT
        gpio38 = 38,      // J21 - Pin 13 - Bidir  - GPIO20/AUD_INT
        gpio63 = 63,      // J21 - Pin 33 - Bidir  - GPIO11_AP_WAKE_BT
        gpio184 = 184,    // J21 - Pin 18 - Input  - GPIO16_MDM_WAKE_AP
        gpio186 = 186,    // J21 - Pin 31 - Input  - GPIO9_MOTION_INT
        gpio187 = 187,    // J21 - Pin 37 - Output - GPIO8_ALS_PROX_INT
        gpio219 = 219,    // J21 - Pin 29 - Output - GPIO19_AUD_RST
} ;
```

TK1SVR Expansion Connectors

GPIO Interfacing – NVIDIA Jetson TX1



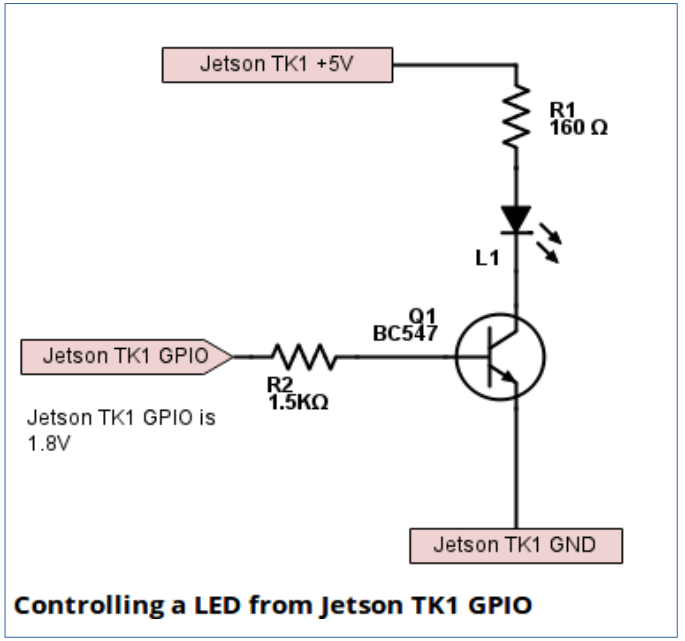
http://www.jetsonhacks.com/2015/12/29/gpio-interfacing-nvidia-jetson-tx1/



http://elinux.org/Jetson/GPIO#GPIO_on_Jetson_TK1

Disable by default

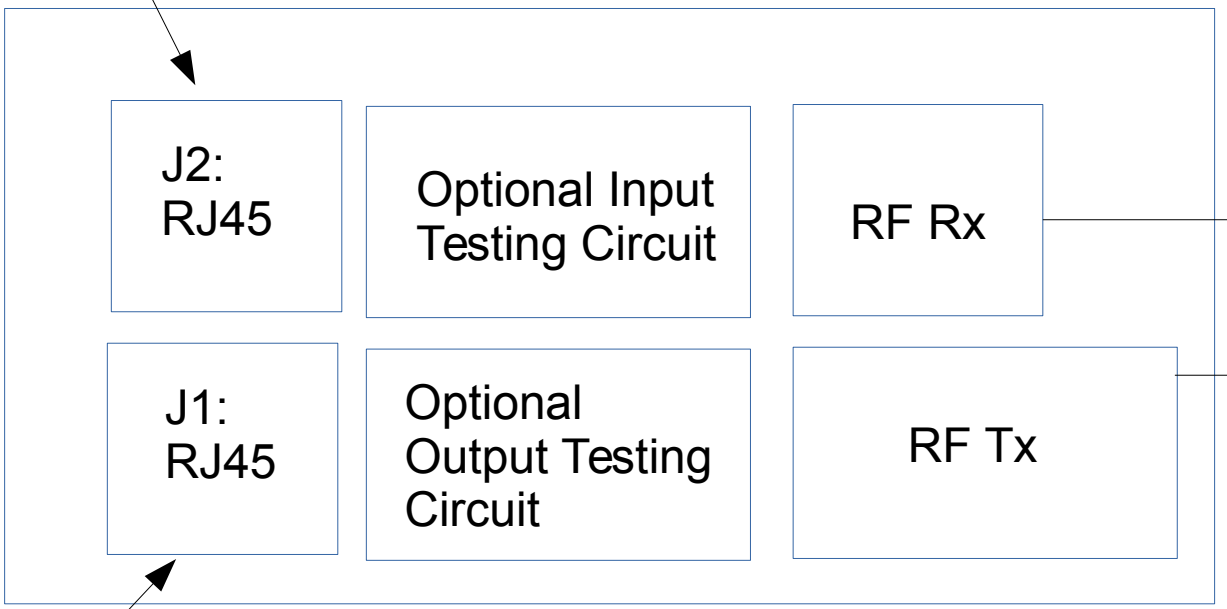
Port	sysfs filename	Physical pin
GPIO_PU0	gpio160	Pin 40 on J3A2
GPIO_PU1	gpio161	Pin 43 on J3A2
GPIO_PU2	gpio162	Pin 46 on J3A2
GPIO_PU3	gpio163	Pin 49 on J3A2
GPIO_PU4	gpio164	Pin 52 on J3A2
GPIO_PU5	gpio165	Pin 55 on J3A2
GPIO_PU6	gpio166	Pin 58 on J3A2
GPIO_PH1	gpio57	Pin 50 on J3A1



http://www.jetsonhacks.com/2015/09/17/gpio-nvidia-jetson-tk1/

RF Module Design

J2 connects to node N_j for landline based testing



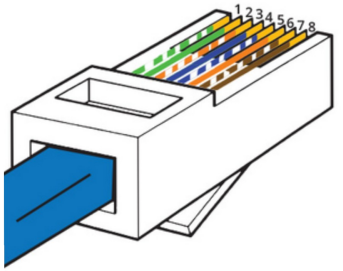
ANT1

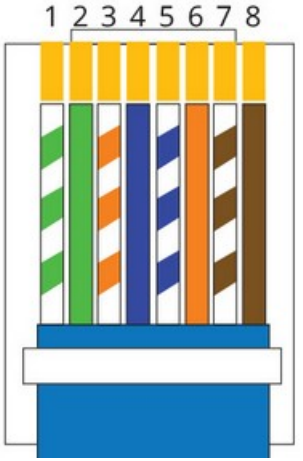
ANT2

J1 connects to LPCNOD or ARMSVR or TX2SVR

Note: 1. identify the data pin from the TX or RX module, and link it to the properly configured GPIO pins of the microprocessor

RJ45 Pinout
T-568A





1. White Green	5. White Blue
2. Green	6. Orange
3. White Orange	7. White Brown
4. Blue	8. Brown