



3-7-4-1-lpc-hardware-2019-3-18.odp

CTI One Corporation

Version: x0.4

Date: Sep 7, 2018

Project Lead: Harry Li, Ph.D.

Team members:

Company confidential

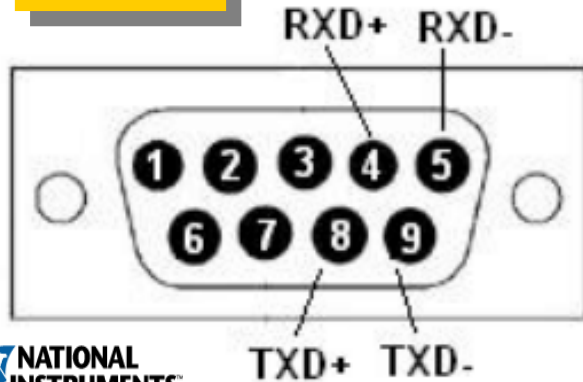


Mar-28-2019 MODBUS



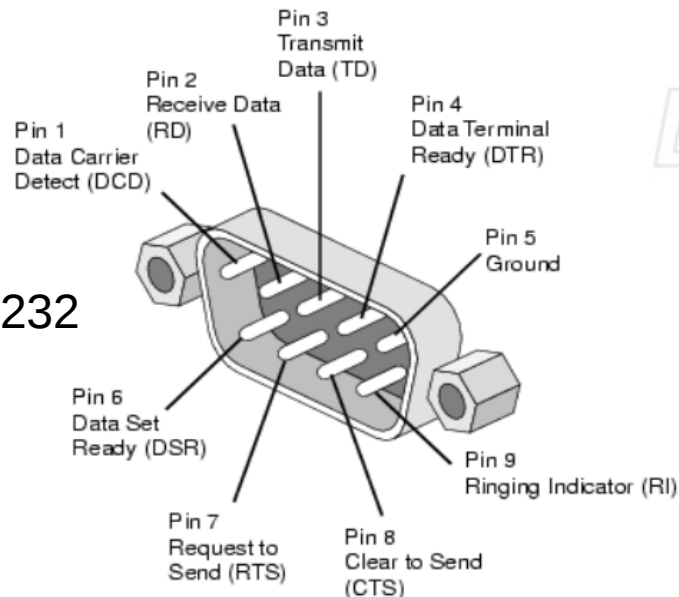
Mar-28-2019 Sierra Smart-Track-100 Compod

RS485



<https://knowledge.ni.com/KnowledgeArticleDetails?id=kA00Z000000P9E8SAK&l=en-US>

RS232



Male DB9



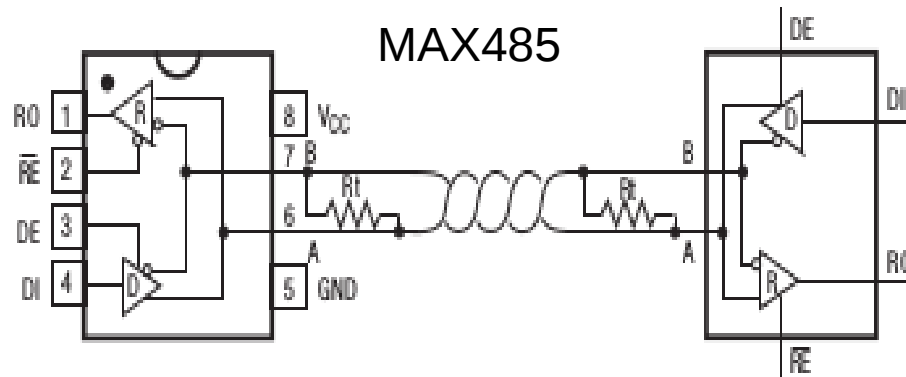
SmartTrak 100

■ RS-485 communication with MODBUS RTU protocol allows digital multi-drop networks

Note LPCNOD with DB9 Male connector for RS485 communication to Smart-track-100 compod DB9 Male connector, so we need DB9-DB9 female to female cable. See below:



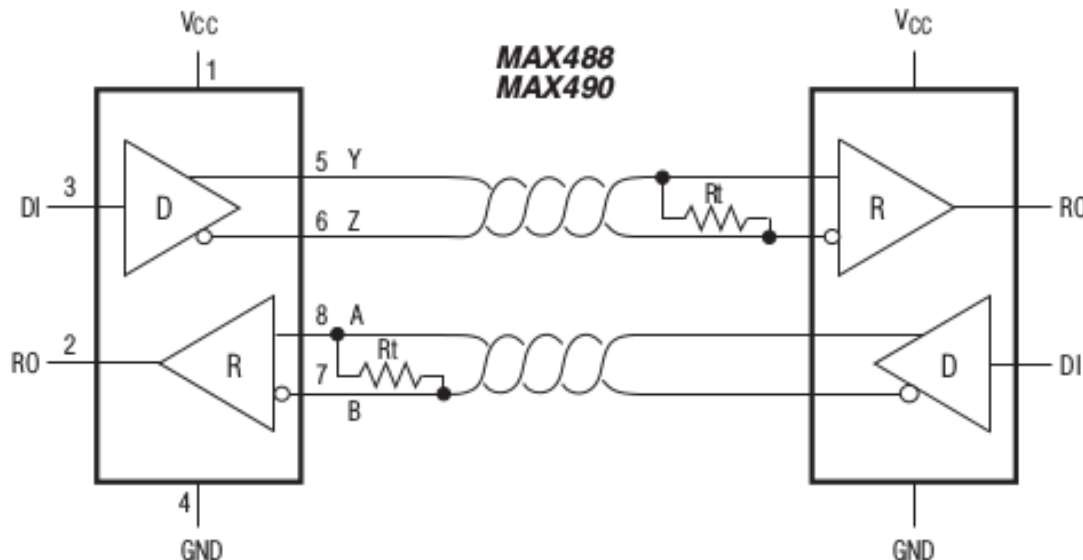
Mar-28-2019 RS485 Hardware



Need to verify Sierra Smart-Track-100
485 pin configuration

RO	Receiver Output: If $A > B$ by 200mV, RO will be high; If $A < B$ by 200mV, RO will be low.
\overline{RE}	Receiver Output Enable. RO is enabled when \overline{RE} is low; RO is high impedance when \overline{RE} is high.
DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if \overline{RE} is low.
DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.

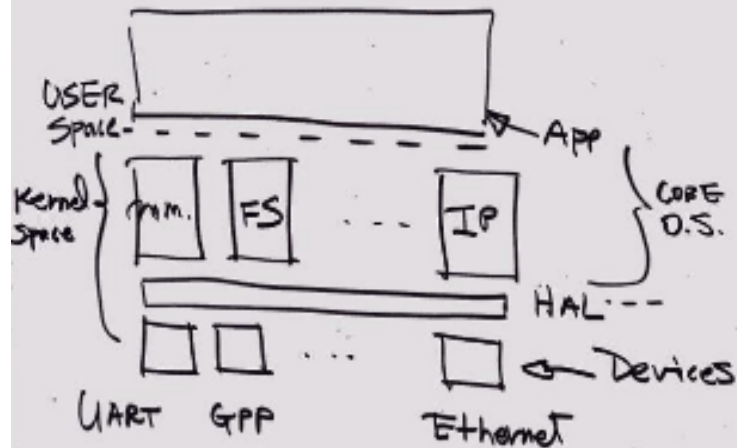
From MAX485 datasheet, pp. 7





Mar-28-2019 RS232 Hardware

March 22, 2019



RTOS
UART → RS232 → RS485 → MODBUS protocol.

Table 1

TX2 P0.10 J2-40
RX2 P0.11 J2-41

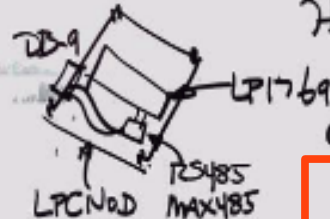
MNIJT

March 25, 2019

- 1) Barry ① PIT update;
- ② TCP/IP ③ User Guide to perform Pick & Place Job.
- ④ ARB

March 28. Flow Pharma Project ⊥ RS485. ① Reference CPU Datasheet

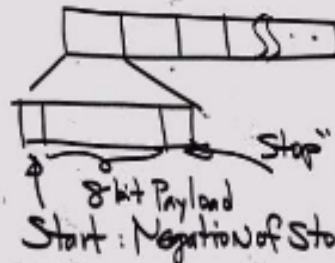
Hardware: UART → RS485 → 2Tins Dt & SCH Differential Pair



CPU UART → MAX

J2 CPU	DB-9
TX J2-9/P0.10	DB9-3
Rx J2-10/P0.11	DB9-2
GND J2-1/GND	DB9-5

⑤ RS232
Band Rate 9600
8N1



- ⑥ Carri: a freertos blanky
b UART w/o freertos
- ⑦ Max485 Hardware
a freertos with UART
April 9 Peter Loyd
d freertos-top-ip
e webserver
U.I.

② Special Purpose Registers (SPRs)
Init & Config.
LPC-GPIO2 → FIOSET
IO Controller (Peripheral) Prefix
Root

- ③ Hardware Dependant Software
a CMSIS-CORE-LPC17xx
b lpcboard-nxp-lpcexpresso-1769
c lpc_chip-175x-6x

④ DB-9 "male"





Mar-28-2019 Ethernet Hardware

TCP/IP Ethernet March 18, 19

1) RJ45, 2) Pin-Number LCNBD, SCH, 3) Physically Build By Soldering 4) TCP/IP Testing

① Mount RJ45
② CAT5-8 Position
③ Soldering.

Connectivity Table

Debugging
TCP/IP → GPIO
UART ← ADC
RS232

GPP ① PP9, CPU/PP13, References, memory map.
② SCH pdf

Table 1

RJ45			
RD- J2-32	ETH-LRXN	Pin 6	Green
RD+ J2-33	ETH-RXP	Pin 3	White/Green
TD- J2-34	ETH-TXN	Pin 2	Orange
TD+ J2-35	ETH-TXP	Pin 1	White

Orange

Table 2

RJ45	
P0.2 J2-21	Input
P0.3 J2-22	Output

Sample Code: [GPI1769 GPP.zip](#)?
[github/hualili](#)

$V_{CC} = IR + V_{LED}$
 $V_{CC} = 3.3V, V_{LED} = 1.8V_{DC}$
 $I = 4mA, R = 370\Omega$

CPU Data Sheet PP156

P0.3

GPIO



Mar-19-2019 TCP/IP Hardware

TCP/IP Ethernet March 18, 19

1) RJ45, 2) Pin-Number LCNOD, SCH, 3) Physically Build By Soldering 4) TCP/IP Testing

① Mount RJ45
② Cat 5-8 Position
③ Soldering.

RD- J2-32
RD+ J2-33
TD- J2-34
TD+ J2-35

Pos 1 Pin 1 ... Pos 8 Pin 8

J2-28
J2-1
J2
RJ45

≧ Debugging.
TCP/IP → GPIO
UART ← ADC
RS232

GPP ① PP9.CPU/PP13.
References:
Table ② SCH pdf
memory map.

Table 1

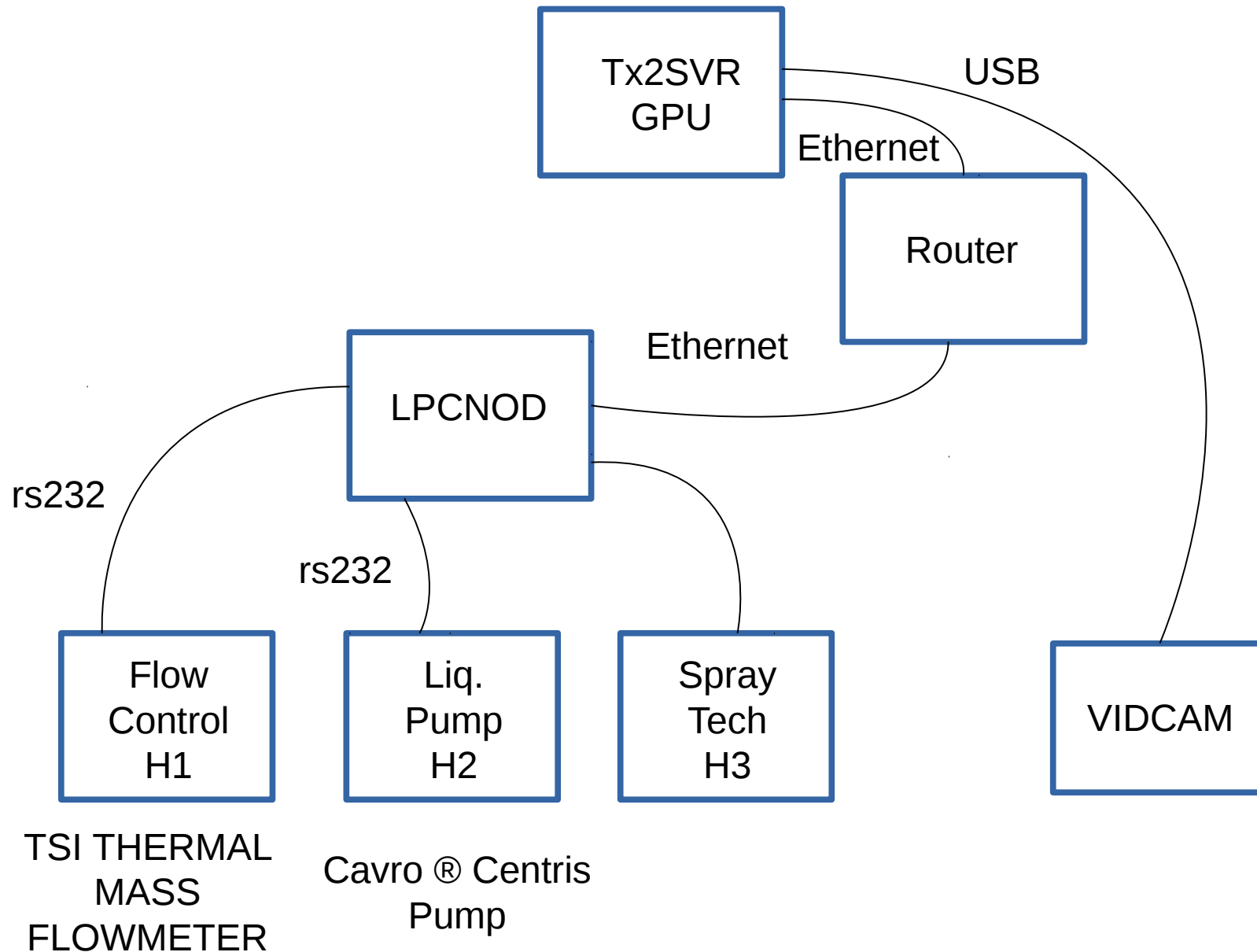
Pin	Signal	Color
RD- J2-32	ETH-RXN	Pin 6 Green
RD+ J2-33	ETH-RXP	Pin 3 White/Green
TD- J2-34	ETH-TXN	Pin 2 Orange
TD+ J2-35	ETH-TXP	Pin 1 White/Orange

$V_{CC} = IR + V_{LED}$
 $V_{CC} = 3.3V, V_{LED} = 1.8V_{CC}$
 $I = 4mA, R = 570\Omega$

P0.2 J2-21 Input
P0.3 J2-22 Output

Sample Code: uc1769GPP.zip?
github/hualili

TX2SVR System Architecture






Mar-19-2019 Prototype Design





Mar-28-2019 Intern Orientation

Bill of Material for Control Project and AGU2000.

- ✓ 1. Right Angle RJ45 Connector 5 March 20, 19
- ⊖ 2. DB-9 Right Angle Connector 2 (male)
- ✓ 3. PDIP (Packaging) Max232 3
- ⊖ 4. Right Angle RJ45 Connector and Plug.


Orientation Process.

- 1° Paper Works for ID/Authorization Verification;
 - 2° NDA,
 - 3° Professional Deck.
 - 4° Hours/Load
 - 5° Professionalism
- = By the End of 3 months Period;