3-7-4-1-lpc-hardware-2019-3-18.odp

CTI One Corporation

Version: x0.4
Date: Sep 7, 2018
Project Lead: Harry Li, Ph.D.

Team members:

May-14-2019 UART-232-485 Hardware

Board Layout

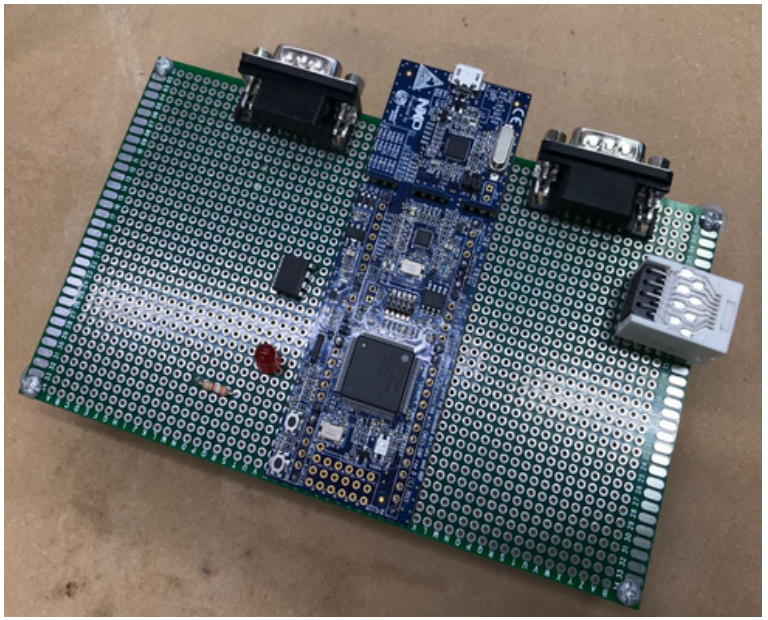
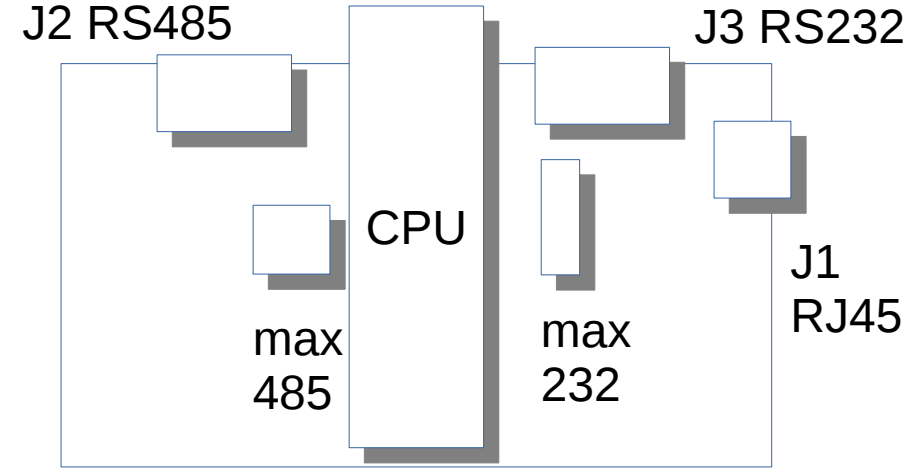


Table 1 connectors

J1	RJ45	TCP/IP
J2	RS485	Modbus
J3	RS232	debugging



May-14-2019 UART1 for 232 Hardware

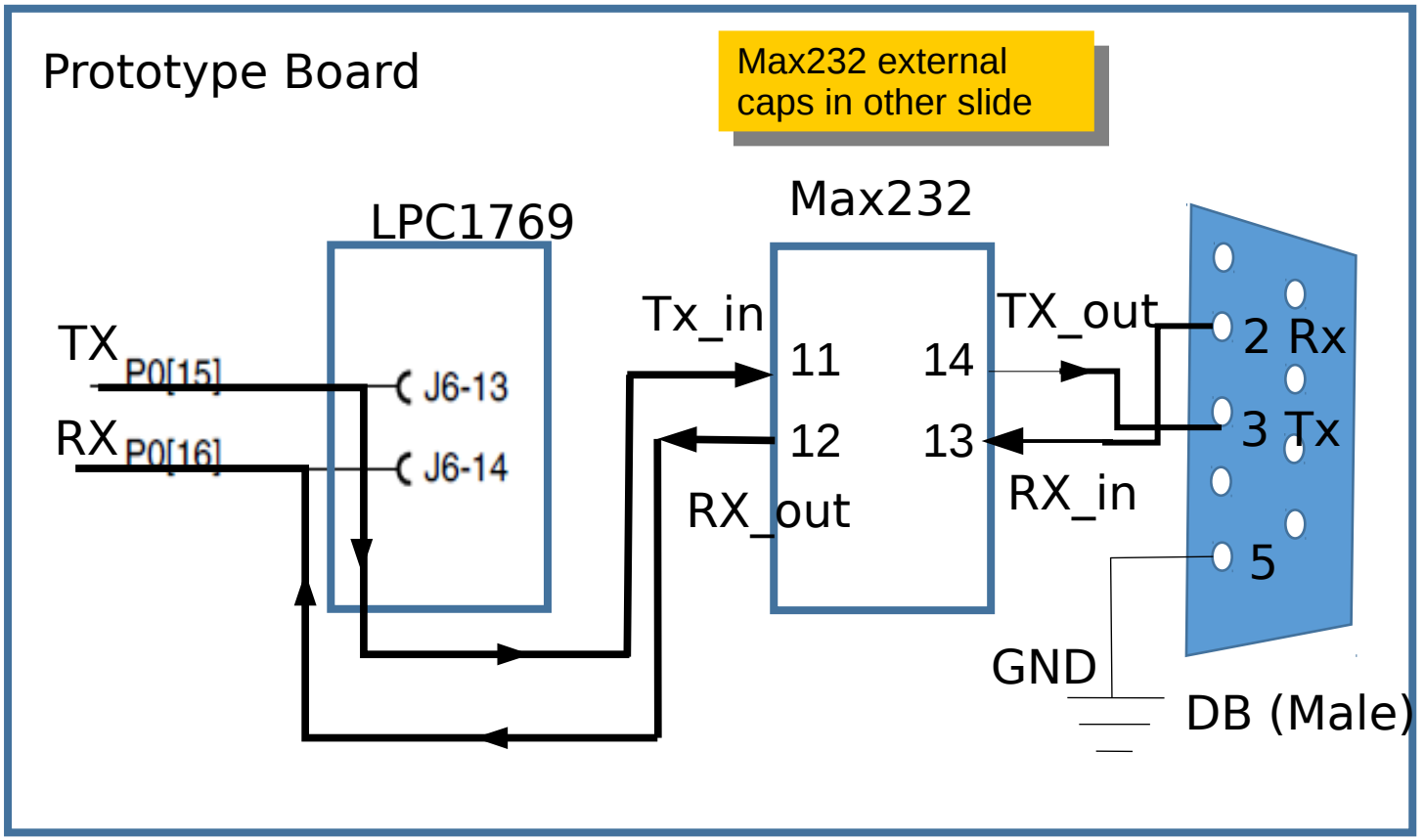
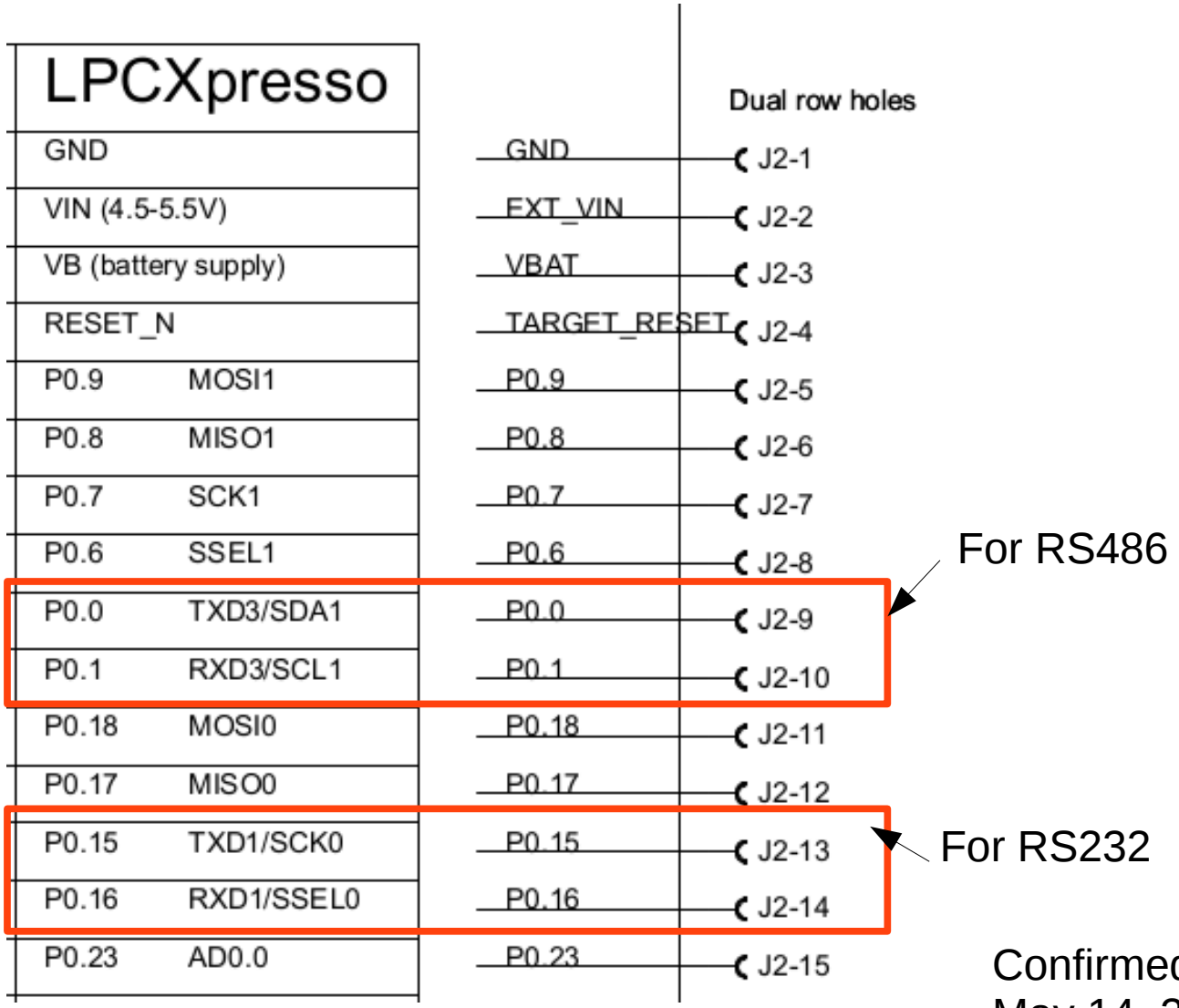


Table 2. CPU module pins for Max232 (RS232)

CPU Pin	Module Pin	MAX232	DB9 (Male) Pin
P0.15 TXD1/SCK0	J6-13 Tx	Tx1_in, 11	3 (from Tx1_out, 14)
P0.16 RXD1/SSEL0	J6-14 Rx	Rx1_out, 12	2 (to Rx_In, 13)

J6 and J2 (version D) are pin-to-pin compatible

May-14-2019 LPCNOD UART



For RS486

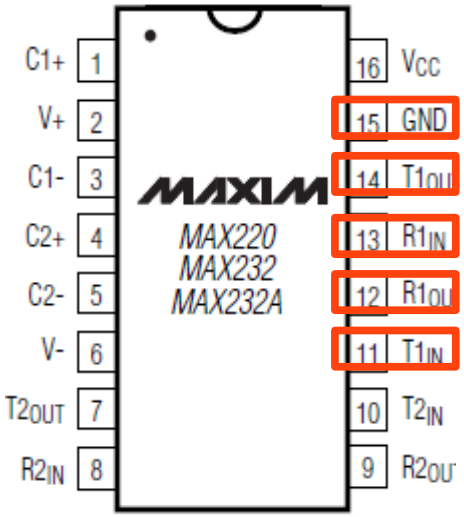
For RS232

Confirmed by HL
May 14, 2019

May-14-2019 UART-RS232 with Caps

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers



DIP/SO

Reference : from MAX232 Datasheet

Note: (1) external caps for low pass filter noise removal; (2) pay attention to the caps polarity.

External Capacitors

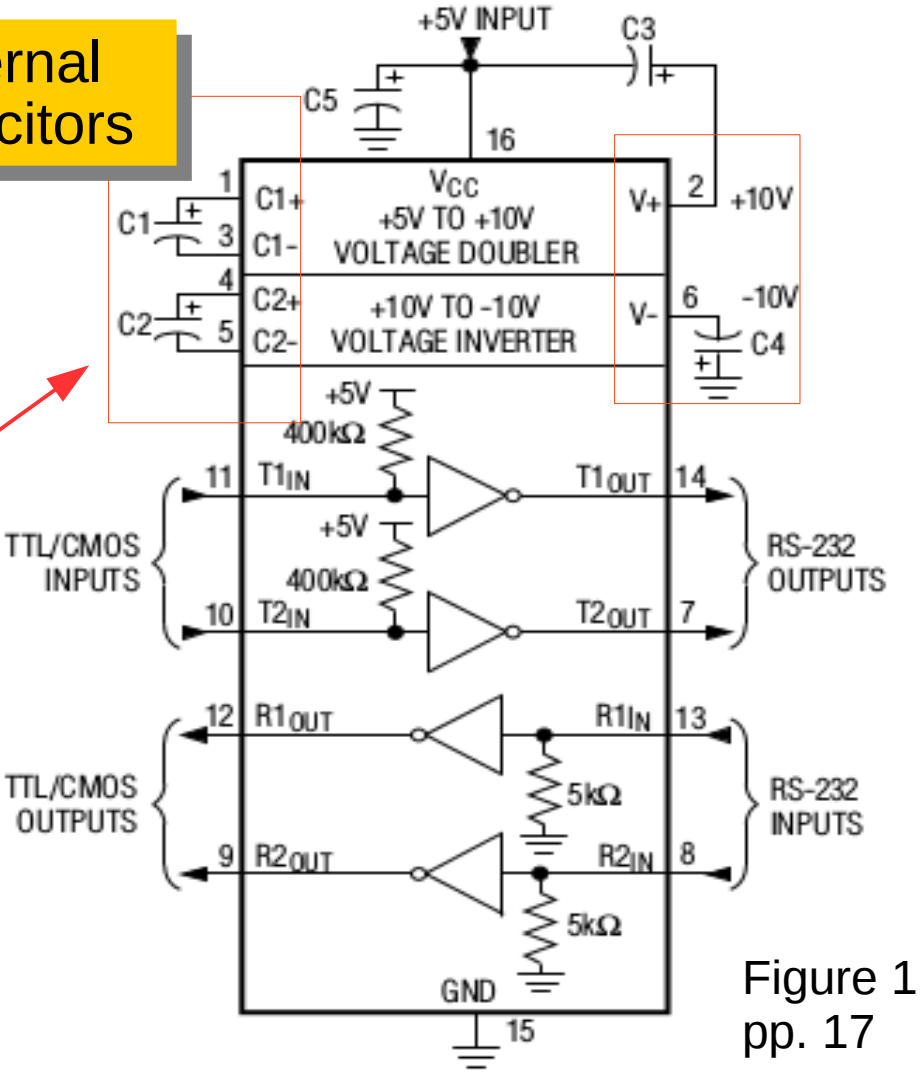


Figure 1. pp. 17

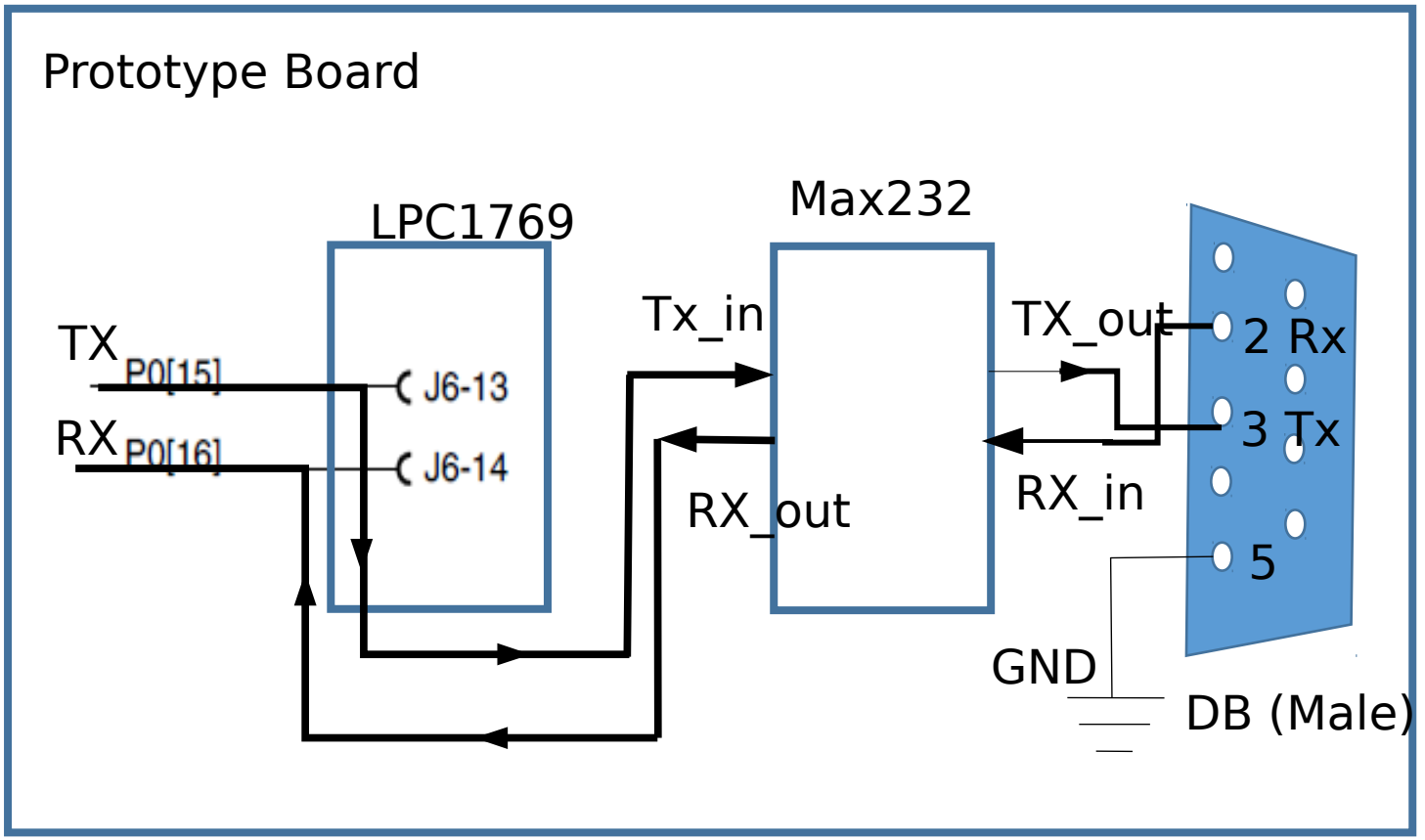
Table 1. Bill of Material

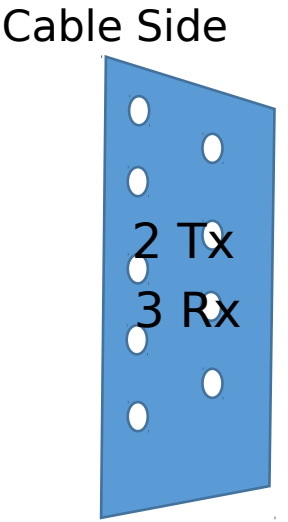
CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	0.047	0.33	0.33	0.33	0.33
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

Note: all these caps are polarity based capacitors, Figure 1

MAX220–MAX249

May-14-2019 UART2 for 485 Hardware





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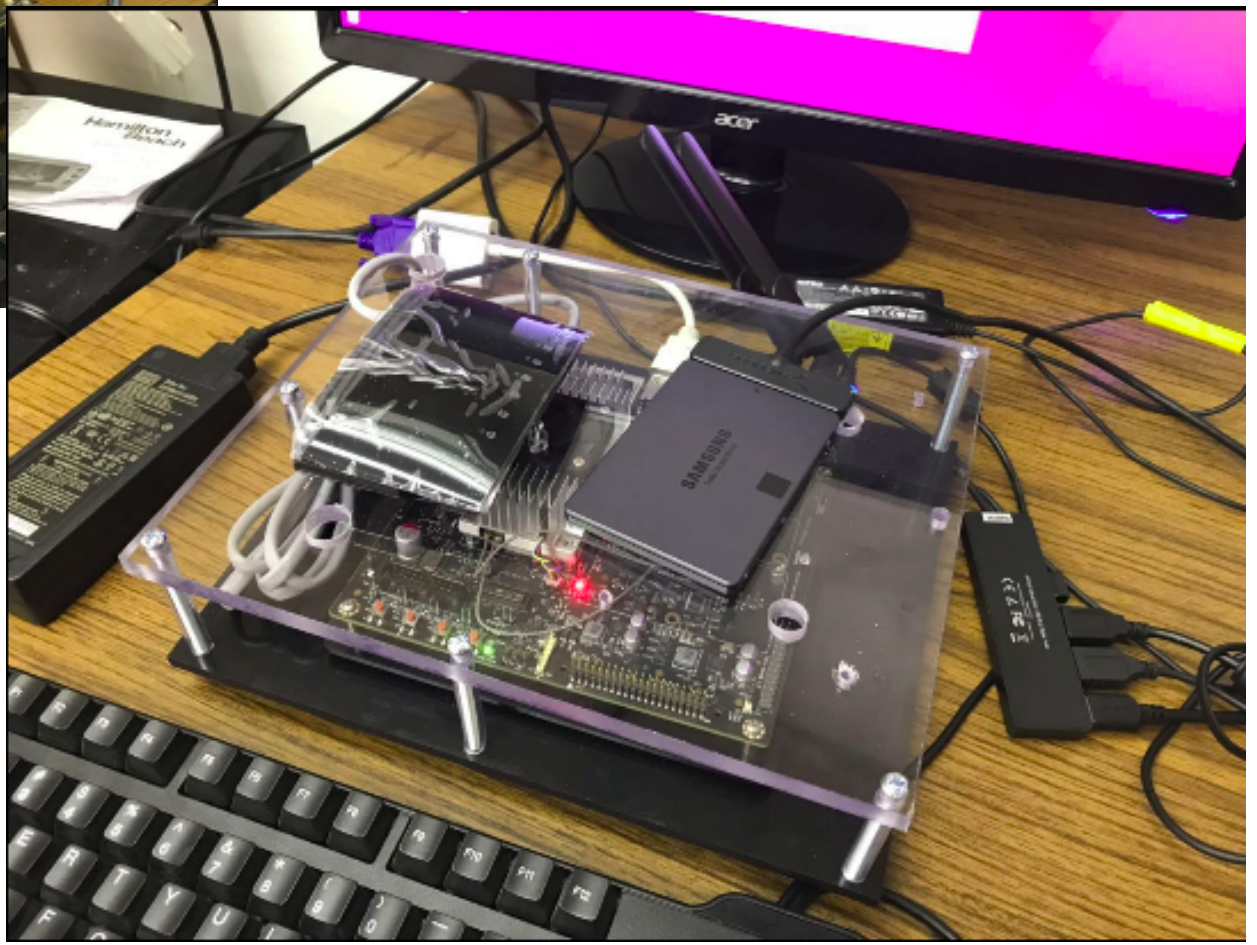
Mar-19-2019 Prototype Design



Mar-19-2019 TCP/IP Hardware