



3-7-4-1-lpc-hardware-2019-3-18.odp

CTI One Corporation

Version: x0.4

Date: Sep 7, 2018

Project Lead: Harry Li, Ph.D.

Team members:

Company confidential



May-14-2019 UART-232-485 Hardware

Board Layout

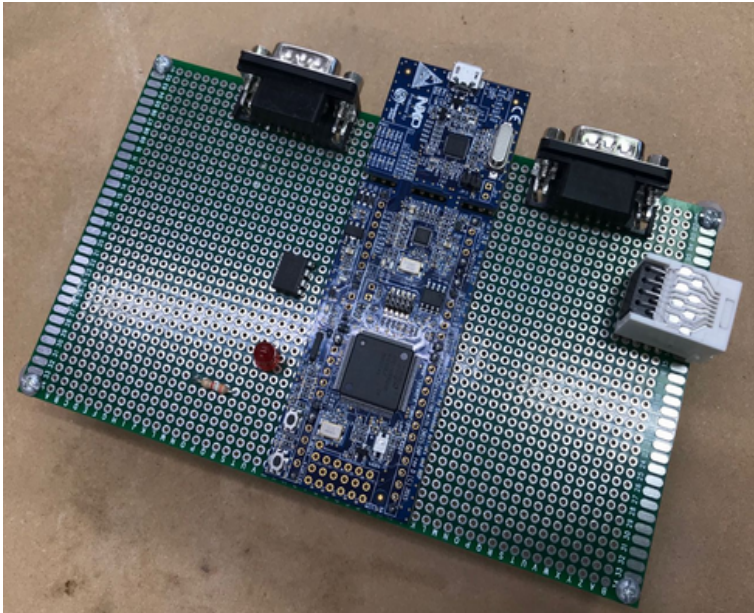
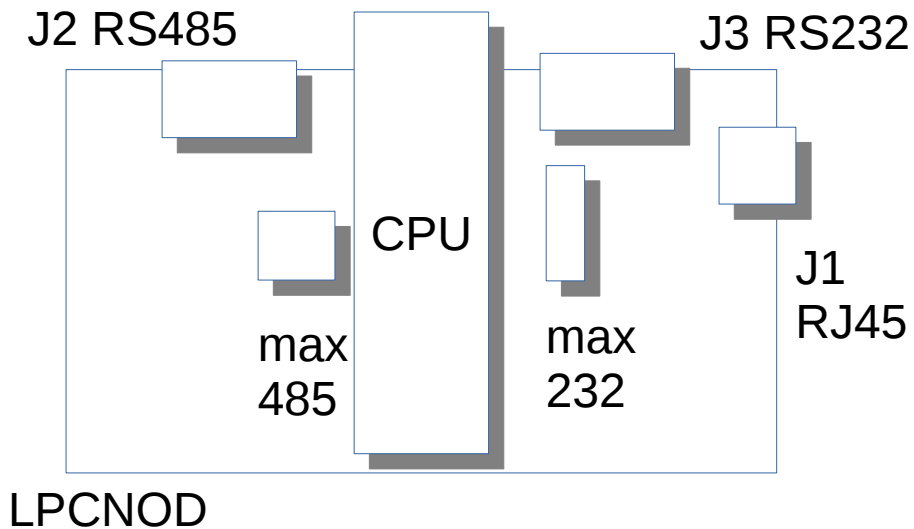


Table 1 connectors

J1	RJ45	TCP/IP
J2	RS485	Modbus
J3	RS232	debugging





May-14-2019 UART1 for 232 Hardware

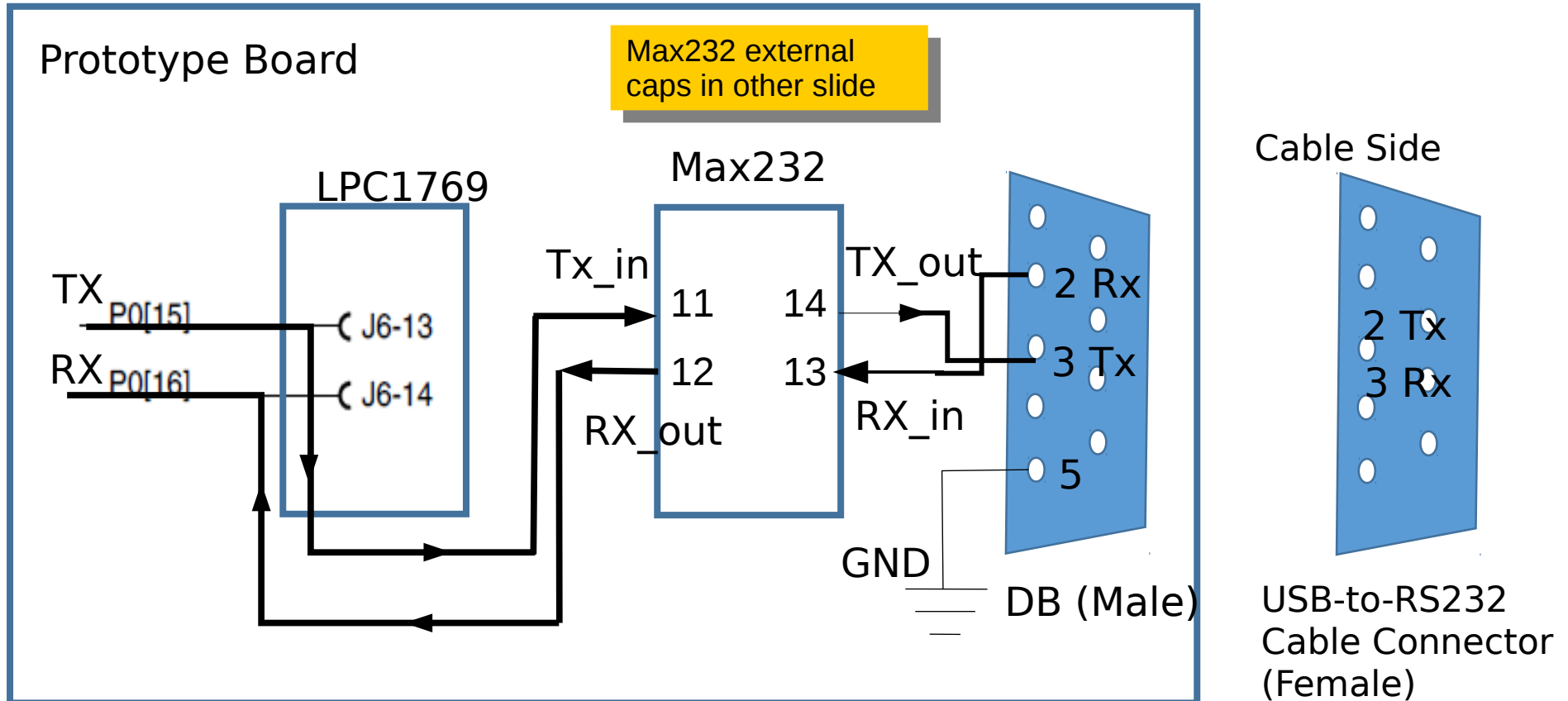


Table 2. CPU module pins for Max232 (RS232)

CPU Pin	Module Pin	MAX232	DB9 (Male) Pin
P0.15 <u>TXD1/SCK0</u>	J6-13 Tx	Tx1_in, 11	3 (from Tx1_out, 14)
P0.16 <u>RXD1/SSEL0</u>	J6-14 Rx	Rx1_out, 12	2 (to Rx_In, 13)

J6 and J2 (version D) are pin-to-pin compatible



May-14-2019 LPCNOD UART

LPCXpresso		Dual row holes	
GND		GND	⌋ J2-1
VIN (4.5-5.5V)		EXT_VIN	⌋ J2-2
VB (battery supply)		VBAT	⌋ J2-3
RESET_N		TARGET_RESET	⌋ J2-4
P0.9 MOSI1		P0.9	⌋ J2-5
P0.8 MISO1		P0.8	⌋ J2-6
P0.7 SCK1		P0.7	⌋ J2-7
P0.6 SSEL1		P0.6	⌋ J2-8
P0.0 TXD3/SDA1		P0.0	⌋ J2-9
P0.1 RXD3/SCL1		P0.1	⌋ J2-10
P0.18 MOSI0		P0.18	⌋ J2-11
P0.17 MISO0		P0.17	⌋ J2-12
P0.15 TXD1/SCK0		P0.15	⌋ J2-13
P0.16 RXD1/SSEL0		P0.16	⌋ J2-14
P0.23 AD0.0		P0.23	⌋ J2-15

For RS232

For RS486



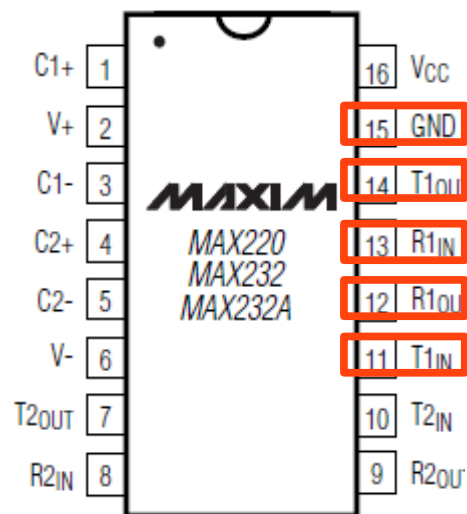
May-14-2019 UART-RS232 with Caps



+5V-Powered, Multichannel RS-232 Drivers/Receivers

Reference : from MAX232 Datasheet

Note: (1) external caps for low pass filter noise removal; (2) pay attention to the caps polarity.



DIP/SO

External Capacitors

Table 1. Bill of Material

CAPACITANCE (μF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	0.047	0.33	0.33	0.33	0.33
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

Note: all these caps are polarity based capacitors, Figure 1

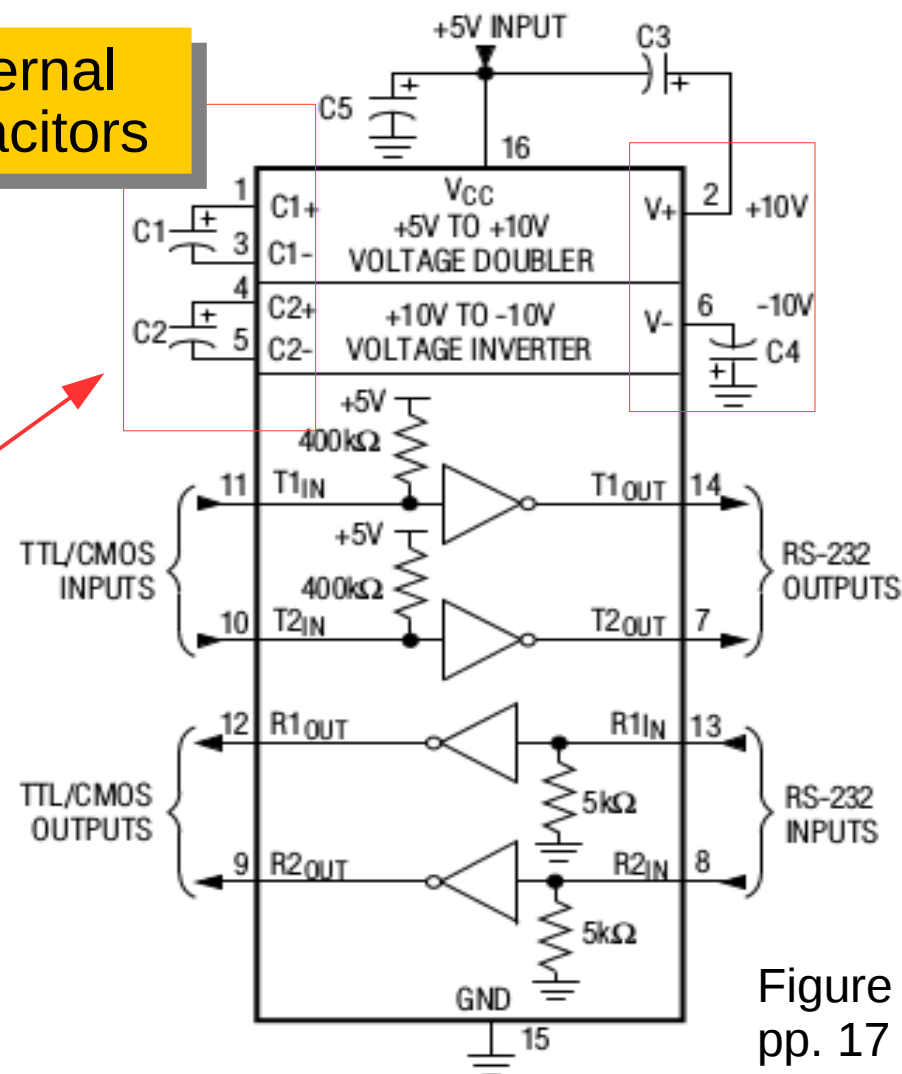


Figure 1.
pp. 17

MAX220-MAX249



May-14-2019 UART2 for 485 Hardware

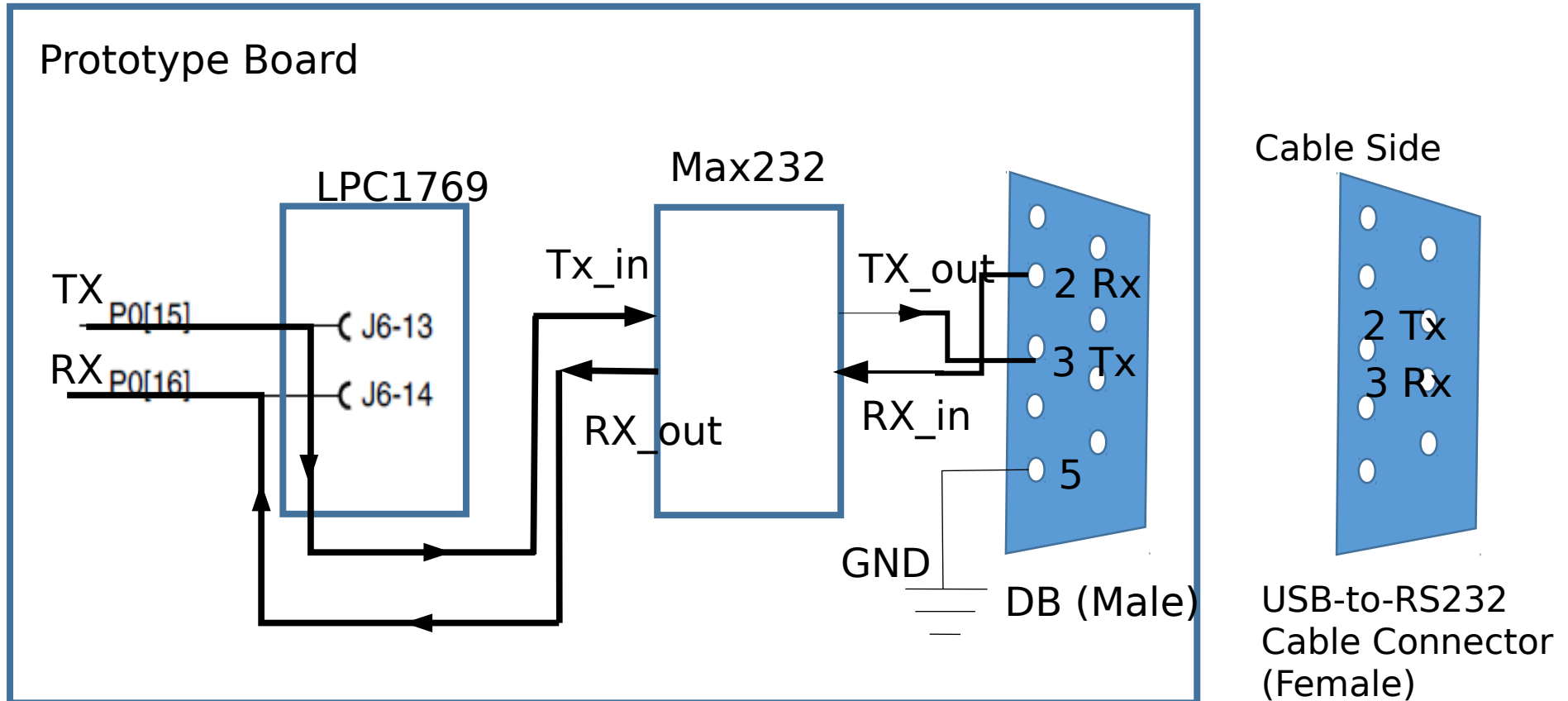


Table 2. CPU module pins for Max232 (RS232)

CPU Pin	Module Pin	MAX232	DB9 (Male) Pin
P0.15 <u>TXD1/SCK0</u>	J6-13 Tx	Tx1_in, 11	3 (from Tx1_out), 14
P0.16 <u>RXD1/SSEL0</u>	J6-14 Rx	Rx1_out, 12	2 (to Rx_in), 13



Mar-19-2019 Prototype Design





Mar-19-2019 TCP/IP Hardware

TCP/IP Ethernet March 18, 19

1) RJ45, 2) Pin-Number LCNOD, SCH, 3) Physically Build By Soldering 4) TCP/IP Testing

RD- J2-32 ① Mount RJ45
RD+ J2-33 ② CAT5-8 Position
TD- J2-34
TD+ J2-35

Pos1 Pin1 ... Pos8 Pin8

J2-28 J2-1 J2 RJ45

Connectivity Table
③ Soldering.

≧ Debugging.
TCP/IP → GPIO → UART ← ADC
RS232

GPP ① PP9.CPU/PP13.
References: memory map.
Table ② SCH pdf

Table 1

Pin	Signal	Color
RD- J2-32	ETH-RXN	Pin6 Green
RD+ J2-33	ETH-RXP	Pin3 White-Green
TD- J2-34	ETH-TXN	Pin2 Orange
TD+ J2-35	ETH-TXP	Pin1 White-Orange

P0.2 J2-21 Input
P0.3 J2-22 Output

Sample Code: uc1769GPP.zip?
github/hualili

$V_{CC} = IR + V_{LED}$
 $V_{CC} = 3.3V, V_{LED} = 1.8V_{CC}$
 $I = 4mA, R = 570\Omega$