Samantha Smith

Wenyi Chen

Huan Nguyen

Read ME:

1) What's working and what's not?

Everything worked!

2) Success rate

100% for int_float, float_int, and float_float.

With the exception for float_int where we get the correct output but the auto-grader graded us wrong.

3) How to run the bench?

All the components are in the root folder. All the test bench are in the bench folders separated by the function name

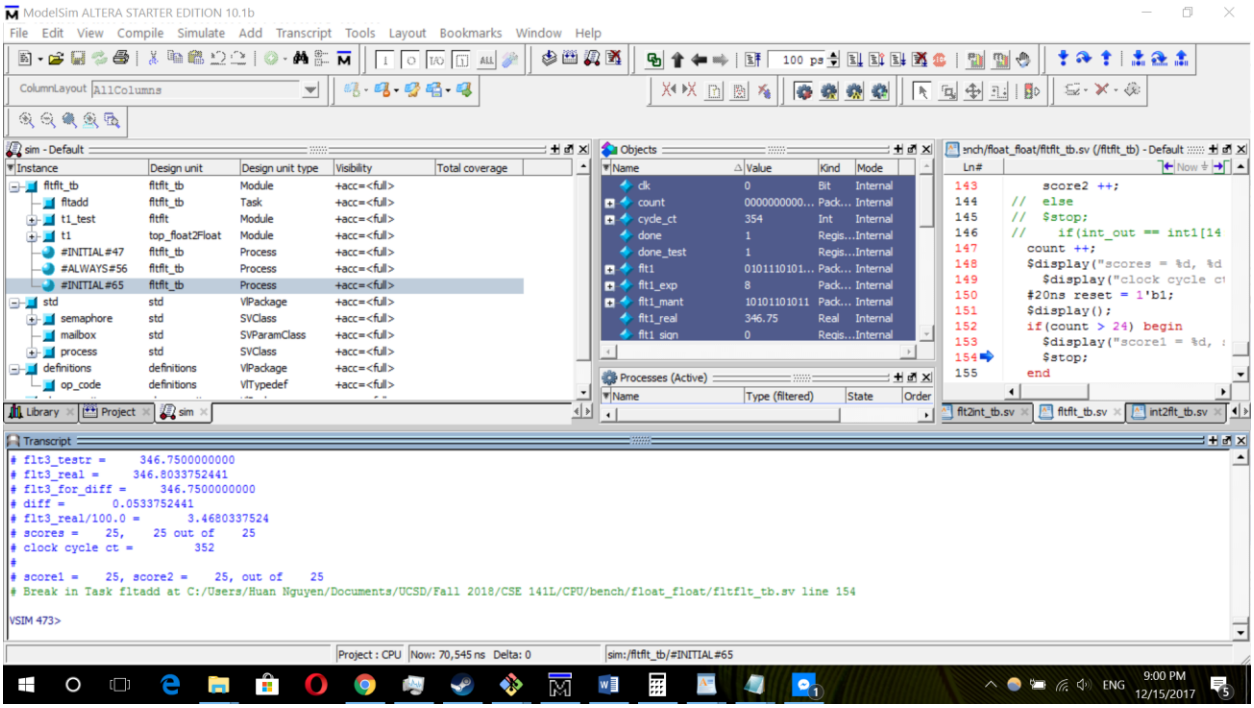
Just add everything to ModelSim, and add the benchs to it and run it. I also make separate ROMs for each function inside the bench folders.

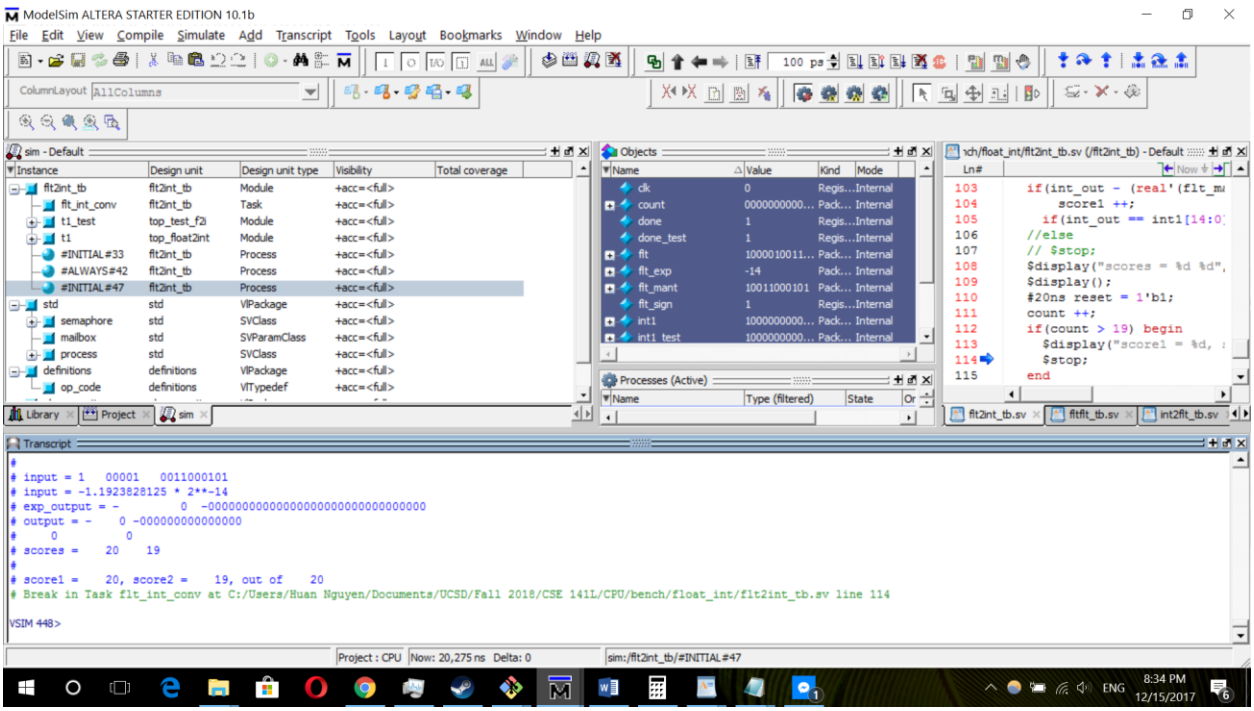
4) What I changed in the test bench?

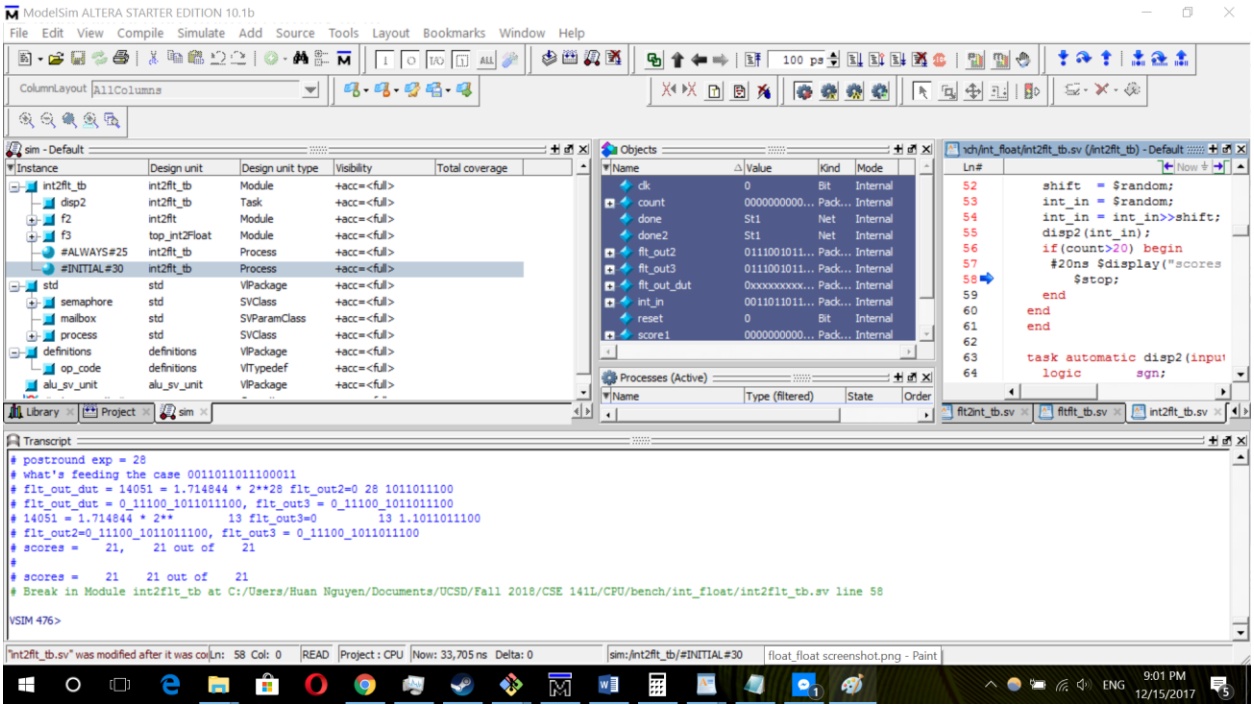
I modify the bench to use my top instead of the dummy. Also for int_float, I modified the input location from 1,2 to 0,1 because that is what we expected in our program.

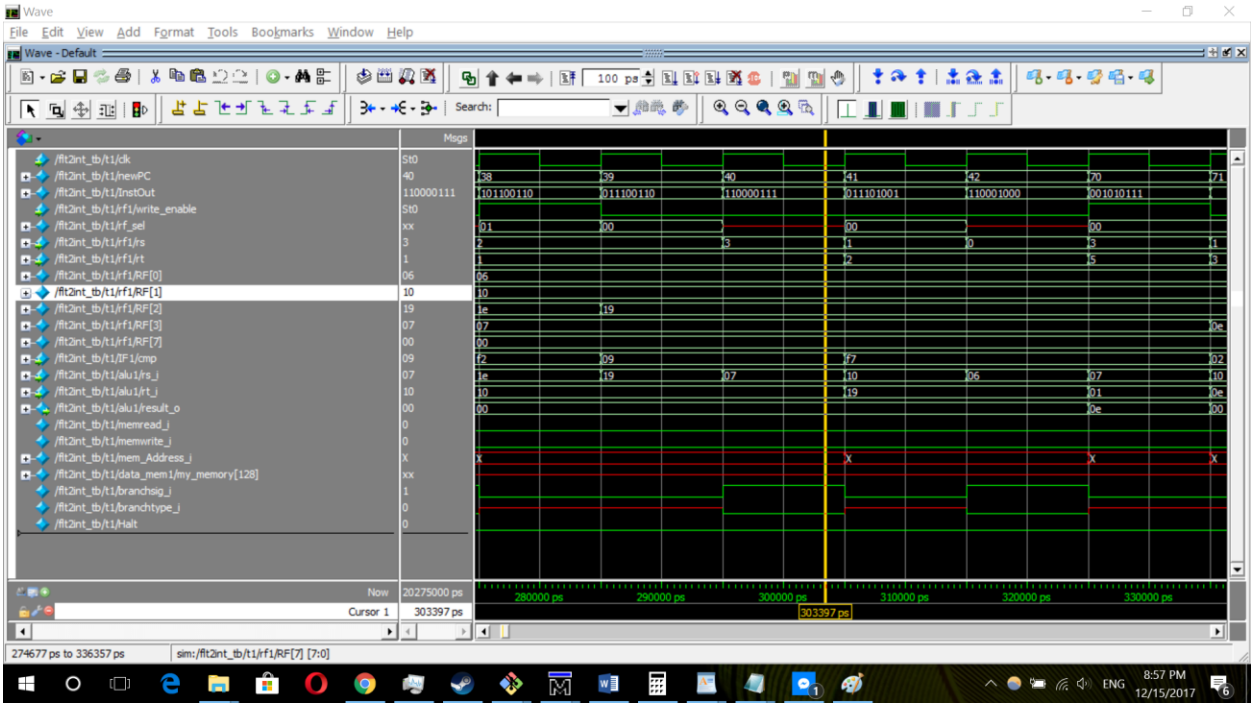
5) Assembler

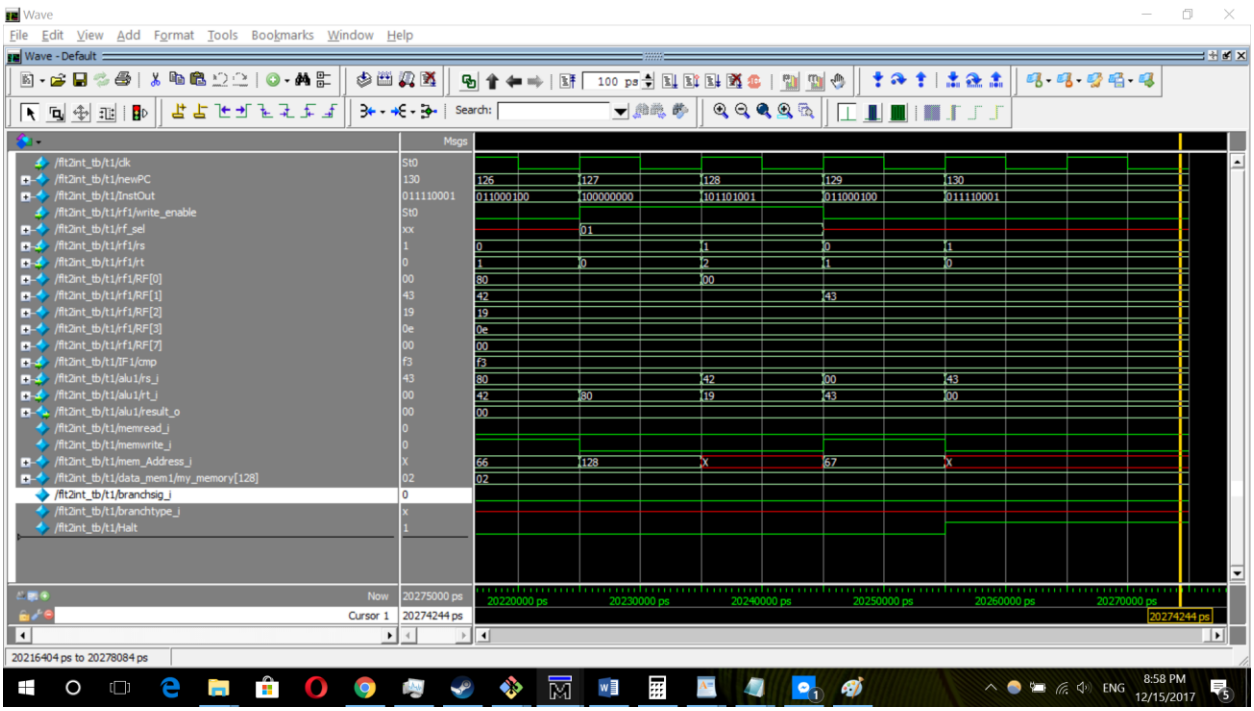
We have included the assembler inside java_things folder. Please compile first before use.


ModelSim ALTERA STARTER EDITION 10.1b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type Visibility Total coverage
fltflt_tb fltflt_tb Module +acc=<full>
fltadd fltflt_tb Task +acc=<full>
t1_test fltflt Module +acc=<full>
t1 top_float2Float Module +acc=<full>
#INITIAL#47 fltflt_tb Process +acc=<full>
#ALWAYS#56 fltflt_tb Process +acc=<full>
#INITIAL#65 fltflt_tb Process +acc=<full>
std std VlPackage +acc=<full>
semaphore std SVClass +acc=<full>
mailbox std SVParamClass +acc=<full>
process std SVClass +acc=<full>
definitions definitions VlPackage +acc=<full>
op_code definitions VlTypedef +acc=<full>
Objects
Name Value Kind Mode
clk 0 Bit Internal
count 0000000000... Pack... Internal
cycle_ct 354 Int Internal
done 1 Regis... Internal
done_test 1 Regis... Internal
flt1 0101110101... Pack... Internal
flt1_exp 8 Pack... Internal
flt1_mant 10101101011 Pack... Internal
flt1_real 346.75 Real Internal
flt1_sign 0 Regis... Internal
Processes (Active)
Name Type (filtered) State Order
nch/float_float/fltflt_tb.sv (/fltflt_tb) - Default
Ln#
143 score2 ++;
144 // else
145 // $stop;
146 // if(int_out == int1[14
147 count ++;
148 $display("scores = %d, %d
149 $display("clock cycle c
150 #20ns reset = 1'b1;
151 $display();
152 if(count > 24) begin
153 $display("score1 = %d,
154 $stop;
155 end
flt2int_tb.sv fltflt_tb.sv int2flt_tb.sv
Transcript
# flt3_testr = 346.7500000000
# flt3_real = 346.8033752441
# flt3_for_diff = 346.7500000000
# diff = 0.0533752441
# flt3_real/100.0 = 3.4680337524
# scores = 25, 25 out of 25
# clock cycle ct = 352
#
# score1 = 25, score2 = 25, out of 25
# Break in Task fltadd at C:/Users/Huan Nguyen/Documents/UCSD/Fall 2018/CSE 141L/CPU/bench/float_float/fltflt_tb.sv line 154
VSIM 473>
Project : CPU Now: 70,545 ns Delta: 0 sim:/fltflt_tb/#INITIAL#65
9:00 PM 12/15/2017


ModelSim ALTERA STARTER EDITION 10.1b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type Visibility Total coverage
flt2int_tb flt2int_tb Module +acc=<full>
flt_int_conv flt2int_tb Task +acc=<full>
t1_test top_test_f2i Module +acc=<full>
t1 top_float2int Module +acc=<full>
#INITIAL#33 flt2int_tb Process +acc=<full>
#ALWAYS#42 flt2int_tb Process +acc=<full>
#INITIAL#47 flt2int_tb Process +acc=<full>
std std VlPackage +acc=<full>
semaphore std SVClass +acc=<full>
mailbox std SVParamClass +acc=<full>
process std SVClass +acc=<full>
definitions definitions VlPackage +acc=<full>
op_code definitions VlTypedef +acc=<full>
Objects
Name Value Kind Mode
clk 0 Regis... Internal
count 0000000000... Pack... Internal
done 1 Regis... Internal
done_test 1 Regis... Internal
flt 1000010011... Pack... Internal
flt_exp -14 Pack... Internal
flt_mant 10011000101 Pack... Internal
flt_sign 1 Regis... Internal
int1 1000000000... Pack... Internal
int1_test 1000000000... Pack... Internal
Processes (Active)
Name Type (filtered) State
nch/float_int/flt2int_tb.sv (/flt2int_tb) - Default
Ln#
103 if(int_out - (real'(flt_m
104 score1 ++;
105 if(int_out == int1[14:0
106 //else
107 // $stop;
108 $display("scores = %d %d",
109 $display();
110 #20ns reset = 1'b1;
111 count ++;
112 if(count > 19) begin
113 $display("score1 = %d,
114 $stop;
115 end
flt2int_tb.sv fltflt_tb.sv int2flt_tb.sv
Transcript
#
# input = 1 00001 0011000101
# input = -1.1923828125 * 2**-14
# exp_output = - 0 -00000000000000000000000000000000
# output = - 0 -000000000000000
# 0 0
# scores = 20 19
#
# score1 = 20, score2 = 19, out of 20
# Break in Task flt_int_conv at C:/Users/Huan Nguyen/Documents/UCSD/Fall 2018/CSE 141L/CPU/bench/float_int/flt2int_tb.sv line 114
VSIM 448>
Project : CPU Now: 20,275 ns Delta: 0 sim:/flt2int_tb/#INITIAL#47
8:34 PM 12/15/2017


ModelSim ALTERA STARTER EDITION 10.1b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type Visibility Total coverage
int2flt_tb int2flt_tb Module +acc=<full>
disp2 int2flt_tb Task +acc=<full>
f2 int2flt Module +acc=<full>
f3 top_int2Float Module +acc=<full>
#ALWAYS#25 int2flt_tb Process +acc=<full>
#INITIAL#30 int2flt_tb Process +acc=<full>
std std VlPackage +acc=<full>
semaphore std SVClass +acc=<full>
mailbox std SVParamClass +acc=<full>
process std SVClass +acc=<full>
definitions definitions VlPackage +acc=<full>
op_code definitions VlTypedef +acc=<full>
alu_sv_unit alu_sv_unit VlPackage +acc=<full>
Objects
Name Value Kind Mode
clk 0 Bit Internal
count 0000000000... Pack... Internal
done St1 Net Internal
done2 St1 Net Internal
flt_out2 0111001011... Pack... Internal
flt_out3 0111001011... Pack... Internal
flt_out_dut 0xxxxxxxxx... Pack... Internal
int_in 0011011011... Pack... Internal
reset 0 Bit Internal
score1 0000000000... Pack... Internal
Processes (Active)
Name Type (filtered) State Order
Ln#
52 shift = $random;
53 int_in = $random;
54 int_in = int_in>>shift;
55 disp2(int_in);
56 if(count>20) begin
57 #20ns $display("scores
58 $stop;
59 end
60 end
61 end
62
63 task automatic disp2(input
64 logic sgn;
Library Project sim
flt2int_tb.sv fltflt_tb.sv int2flt_tb.sv
Transcript
# postround exp = 28
# what's feeding the case 0011011011100011
# flt_out_dut = 14051 = 1.714844 * 2**28 flt_out2=0 28 1011011100
# flt_out_dut = 0_11100_1011011100, flt_out3 = 0_11100_1011011100
# 14051 = 1.714844 * 2** 13 flt_out3=0 13 1.1011011100
# flt_out2=0_11100_1011011100, flt_out3 = 0_11100_1011011100
# scores = 21, 21 out of 21
#
# scores = 21 21 out of 21
# Break in Module int2flt_tb at C:/Users/Huan Nguyen/Documents/UCSD/Fall 2018/CSE 141L/CPU/bench/int_float/int2flt_tb.sv line 58
VSIM 476>
Ln: 58 Col: 0
READ
Project : CPU
Now: 33,705 ns Delta: 0
sim:/int2flt_tb/#INITIAL#30
float_float screenshot.png - Paint
ENG
9:01 PM
12/15/2017


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/fit2int_tb/t1/clk
/fit2int_tb/t1/newPC
/fit2int_tb/t1/InstOut
/fit2int_tb/t1/rf1/write_enable
/fit2int_tb/t1/rf_sel
/fit2int_tb/t1/rf1/rs
/fit2int_tb/t1/rf1/rt
/fit2int_tb/t1/rf1/RF[0]
/fit2int_tb/t1/rf1/RF[1]
/fit2int_tb/t1/rf1/RF[2]
/fit2int_tb/t1/rf1/RF[3]
/fit2int_tb/t1/rf1/RF[7]
/fit2int_tb/t1/IF1/cmp
/fit2int_tb/t1/alu1/rs_i
/fit2int_tb/t1/alu1/rt_i
/fit2int_tb/t1/alu1/result_o
/fit2int_tb/t1/memread_i
/fit2int_tb/t1/memwrite_i
/fit2int_tb/t1/mem_Address_i
/fit2int_tb/t1/data_mem1/my_memory[128]
/fit2int_tb/t1/branchsig_i
/fit2int_tb/t1/branchtype_i
/fit2int_tb/t1/Halt
Now
Cursor 1
303397 ps
274677 ps to 336357 ps
sim:/fit2int_tb/t1/rf1/RF[7] [7:0]
ENG
8:57 PM
12/15/2017


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/fit2int_tb/t1/clk
/fit2int_tb/t1/newPC
/fit2int_tb/t1/InstOut
/fit2int_tb/t1/rf1/write_enable
/fit2int_tb/t1/rf_sel
/fit2int_tb/t1/rf1/rs
/fit2int_tb/t1/rf1/rt
/fit2int_tb/t1/rf1/RF[0]
/fit2int_tb/t1/rf1/RF[1]
/fit2int_tb/t1/rf1/RF[2]
/fit2int_tb/t1/rf1/RF[3]
/fit2int_tb/t1/rf1/RF[7]
/fit2int_tb/t1/IF1/cmp
/fit2int_tb/t1/alu1/rs_i
/fit2int_tb/t1/alu1/rt_i
/fit2int_tb/t1/alu1/result_o
/fit2int_tb/t1/memread_i
/fit2int_tb/t1/memwrite_i
/fit2int_tb/t1/mem_Address_i
/fit2int_tb/t1/data_mem1/my_memory[128]
/fit2int_tb/t1/branchsig_i
/fit2int_tb/t1/branchtype_i
/fit2int_tb/t1/Halt
Now
Cursor 1
20274244 ps
20216404 ps to 20278084 ps
ENG
8:58 PM
12/15/2017