Computer Engineering Automation Project#2

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Here is your Python Project description, you are given the following technology and design data from 1) to 7).

1)

You have the following technology data from Foundry companies, they are located

at the specified paths.

tsmc45, 6ml:

**lef**: /A/B/C/tsmc/45nm/6ml/physical/tech.lef /A/B/C/tsmc/45nm/6ml/physical/macro.lef

**lib**: /D/E/F/tsmc/45nm/6ml/fast/corner.lib /D/E/F/tsmc/45nm/6ml/fast/stdcell.lib /D/E/F/tsmc/45nm/6ml/fast/io.lib

**sdc**: /D/E/F/tsmc/45nm/6ml/fast/timing/tapeout.sdc

**drc**: /A/B/C/tsmc/45nm/6ml/drc/tapeout.drc

**lvs**: /A/B/C/tsmc/45nm/6ml/lvs/tapeout.lvs

**synthesis**: /B/G/H/tsmc/6ml/45nm/syn.teh

tsmc45, 7ml:

**lef**: /A/B/C/tsmc/45nm/7ml/physical/tech.lef /A/B/C/tsmc/45nm/7ml/physical/macro.lef

**lib**: /D/E/F/tsmc/45nm/7ml/fast/corner.lib /D/E/F/tsmc/45nm/7ml/fast/stdcell.lib /D/E/F/tsmc/45nm/7ml/fast/io.lib

**sdc**: /D/E/F/tsmc/45nm/7ml/fast/timing/tapeout.sdc

**drc:** /A/B/C/tsmc/45nm/7ml/drc/tapeout.drc

**lvs**: /A/B/C/tsmc/45nm/7ml/lvs/tapeout.lvs

**synthesis**: /B/G/H/tsmc/7ml/45nm/syn.teh

tsmc65, 6ml:

**lef**: /A/B/C/tsmc/65nm/physical/tech.lef /A/B/C/tsmc/65nm/physical/macro.lef

**lib**: /D/E/F/tsmc/65nm/fast/corner.lib /D/E/F/tsmc/65nm/fast/stdcell.lib /D/E/F/tsmc/65nm/fast/io.lib

**sdc**: /D/E/F/tsmc/65nm/fast/timing/tapeout.sdc

**drc**: /A/B/C/tsmc/65nm/drc/tapeout.drc

**lvs**: /A/B/C/tsmc/65nm/lvs/tapeout.lvs

**synthesis**: /B/G/H/tsmc/65nm/syn.teh

umc45, 6ml:

**lef**: /A/B/C/umc/45nm/physical/tech.lef /A/B/C/umc/45nm/physical/macro.lef

**lib**: /D/E/F/umc/45nm/fast/corner.lib /D/E/F/umc/45nm/fast/stdcell.lib /D/E/F/umc/45nm/fast/io.lib

**sdc**: /D/E/F/umc/45nm/fast/timing/tapeout.sdc

**drc**: /A/B/C/umc/45nm/drc/tapeout.drc

**lvs**: /A/B/C/umc/45nm/lvs/tapeout.lvs

**synthesis**: /B/G/H/umc/45nm/syn.tec

2) **Your design data are listed below**:

**Top cell name**: TOP

**GDS**: /home/design/top.gds

**Schematic Netlist**: /home/design/top.sch

**DEF**: /home/design/top.def

**RTL** **verilog**: /home/design/top.v

**Power value**: 5 (volt.)

3) **The original PnR “dtmf.conf” file has the following content**:

set rda\_IASICt(ui\_qxconf\_file) {}

set rda\_IASICt(flip\_first) {1}

set rda\_IASICt(double\_back) {1}

set rda\_IASICt(ui\_timingcon\_file) "/home/NETLAB/ted.sun/Encounter/FEU\_4\_1/work\_fe/dtmf.sdc"

set rda\_IASICt(assign\_buffer) {0}

set rda\_IASICt(ui\_timelib,min) "/home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/fast.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/pllclk\_fast.lib

/home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/ram\_128x16A\_fast\_syn.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/ram\_256x16A\_fast\_syn.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/rom\_512x16A\_fast\_syn.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/tpz973gbc-lite\_fast.lib"

set rda\_IASICt(ui\_pg\_connections) ""

set rda\_IASICt(ui\_gen\_footprint) {1}

set rda\_IASICt(ui\_leffile) "./tech.lef ./macro.lef"

4) **The DRC run file has one example**:

drc -top\_cell TOP -gds ./TOP.gds -deck ./TOP.drc

5) **The LVS run file has one example**:

lvs -top dtmf -gds ./dtmf.gds -sch ./dtmf.sch -deck ./tapeout.lvs

6) **The Logic Synthesis file has the following statements**:

include /ee/setup/synopsys/synopsys\_setup\_ASIC018.inc

read -f verilog mux\_using\_assign.v

current\_design = mux\_using\_assign

link

compile

create\_schematic

plot -output mux\_using\_assign.ps

write -f verilog -o mux\_using\_assign.vs -hierarchy

exit

7) **The Power/IR/EM file has one example:**

power\_grid -lef "./tech.lef ./macro.lef" -gds "./test.gds" -sch "./test.sch" -dotlib "/home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/fast.lib

/home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/pllclk\_fast.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/ram\_128x16A\_fast\_syn.lib /NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/ram\_256x16A\_fast\_syn.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/rom\_512x16A\_fast\_syn.lib /home/NETLAB/ted.sun/Encounter/FEU\_4\_1/lib/tpz973gbc-lite\_fast.lib" -vdd 2.5 -sdc "./top.sdc" -def "./top.def"

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**Your task is to encode a PYTHON code with Object-Oriented Programming methodology to:**

**A)**

**Execute your code like:**

**./code.py -t Technology (tsmc65 or umc45) -p Process(6m) -g layout\_full\_path -s sch\_full\_path -n top\_cell\_name -r RTL\_verilog\_full\_path**

**-d DEF\_full\_path -v power\_value**

**And, it should include a “-h” to list the usage of your script.**

**B)**

**Automatically create 5 sub-directories under your current working directory:**

**pwr/ pnr/ drc/ lvs/ syn/**

**C)**

**Grep all required data listed from the 1) to 7) and construct required run file for each step (pnr, drc, lvs, syn, pwr) based upon the choice of technology and process when executing your script.**

**D)**

**Put your run file under each created sub-directory**

**E)**

**Put comment and explanation to each line of your script.**

**NOTE:**

**\*\*\* Your script and result will be presented, executed, displayed and explained in the last week of this semester (08/15/2015).**