Computer-Aided VLSI System Design
Lab10: Physical Verification System

TA: 邱仁皓 r12943008@ntu.edu.tw

Introduction

In this lab, you will perform Design Rule Checking (DRC) and Layout Versus Schematic (LVS) checking through Physical Verification System (PVS).

Environment Setup

1. Upload **PVS_RAK.tar.gz** and **innovus.cshrc** to your working directory
2. Source the licenses:

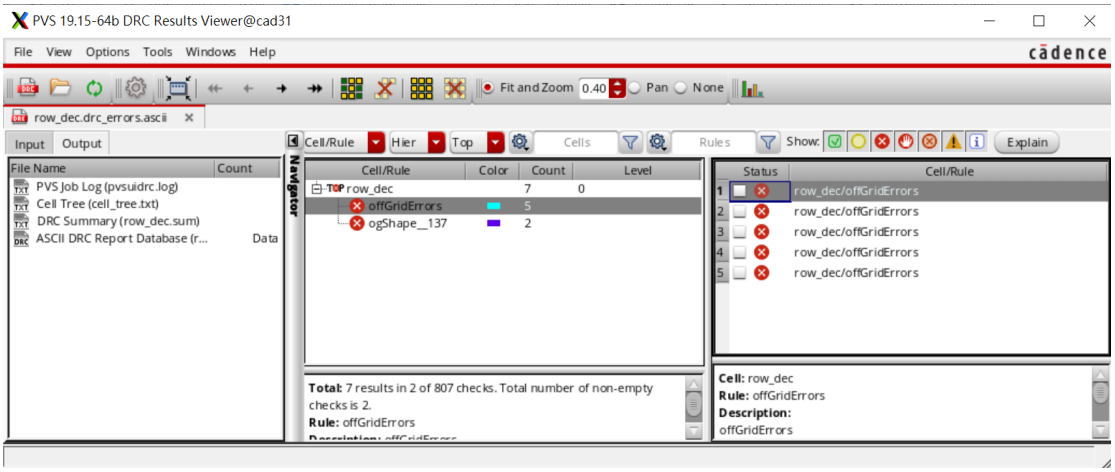
   % **source /usr/cad/innovus/CIC/license.cshrc**

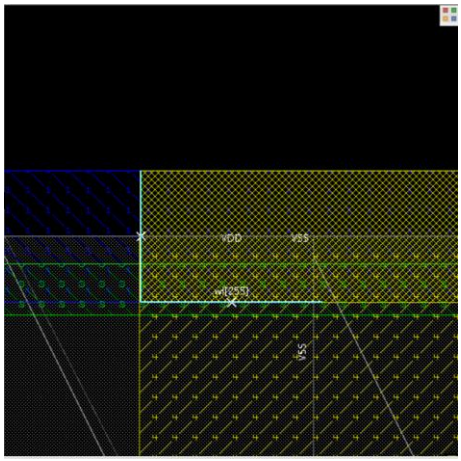
   % **source innovus.cshrc**

   % **source /usr/cad/cadence/CIC/pvs.cshrc**
3. Follow the instructions in **PVS_Innovus.pdf**

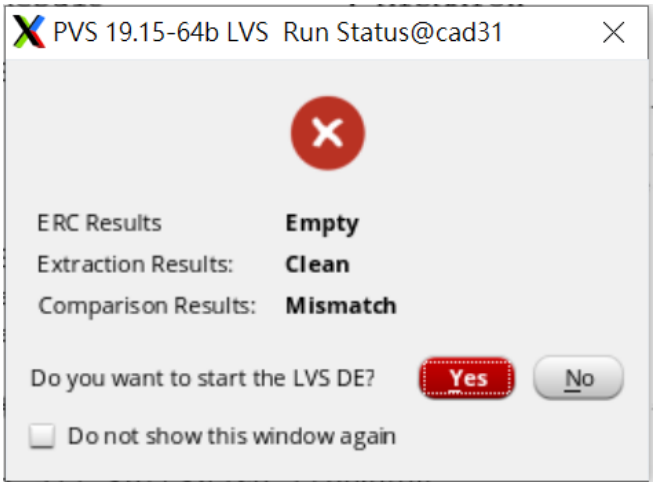
Checkpoints

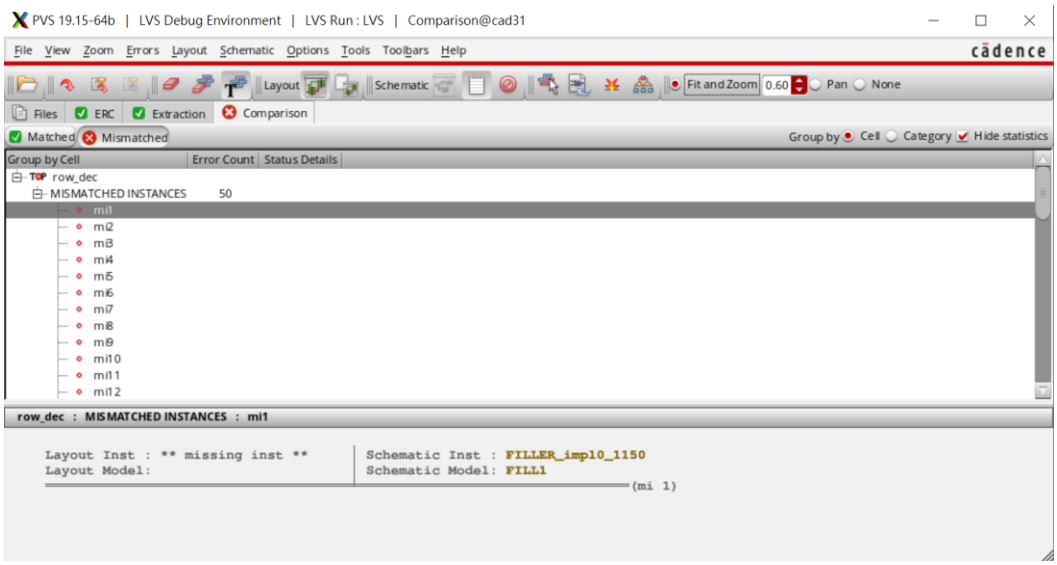
1. Take a screenshot of the DRC results viewer after the DRC run and show one of the offGridErrors.





2. Take a screenshot of the mismatch **before** using presets for LVS run and show the mismatched instances.





3. Take a screenshot of the match **after** using presets for LVS run

Submission

1. **Due Tuesday, Dec. 17, 19:00. No delay is allowed.**

2. Selected students need to take snapshots of the results shown in the previous section, record them into a PDF file, and submit it to NTU COOL.
   Title: CVSD_Lab10_studentID (E.g. CVSD_Lab10_r12943008.pdf)