Computer-Aided VLSI System Design
Lab8: Formal Verification

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Introduction

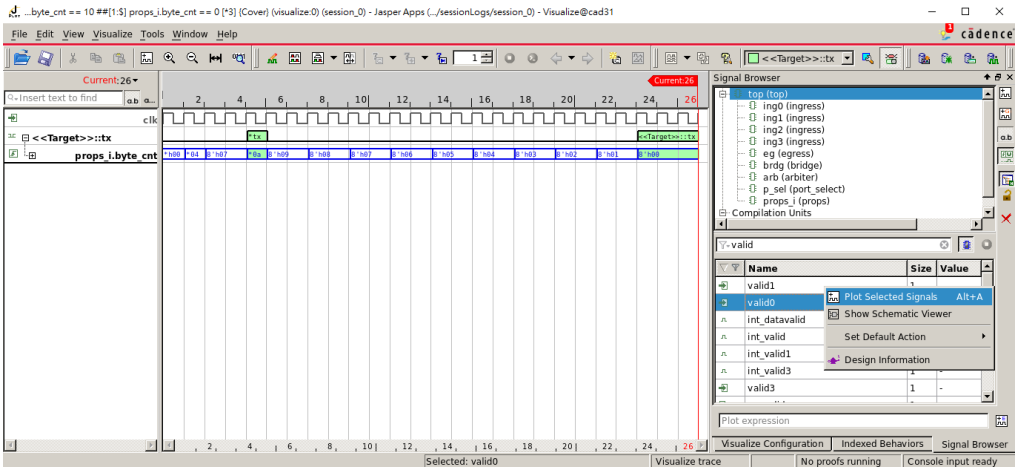
In this lab, you will perform verification using JasperGold with SystemVerilog assertions, and find bugs in the design.

Environment Setup

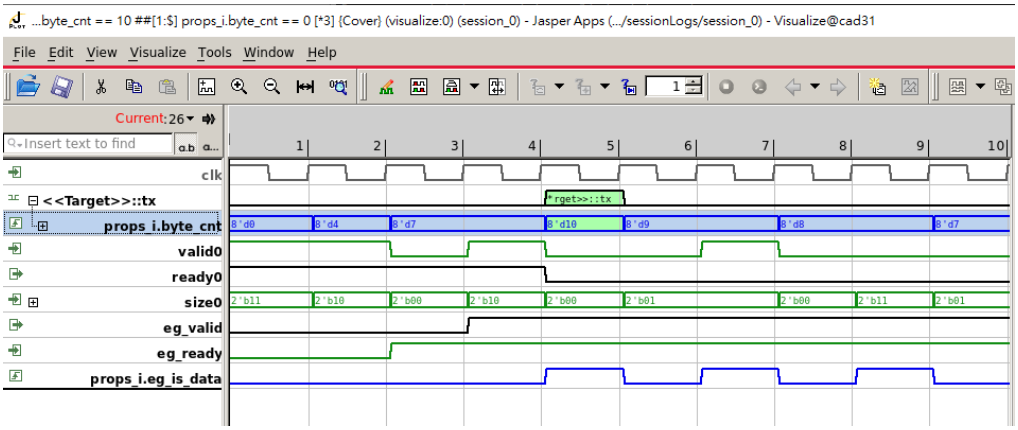
1. Upload **jasper_training.tgz** to your working directory.
2. Source the license:
   % **source /usr/cad/cadence/CIC/jasper.cshrc**
3. Follow the instructions in **Lab_SVA_and_Proof.pdf**

Checkpoints

1. Take a screenshot of the waveform from Visualize after running the visualize command. (You can select the useful signals on the right-hand side to inspect the byte_cnt behavior further, as shown in the following figure)

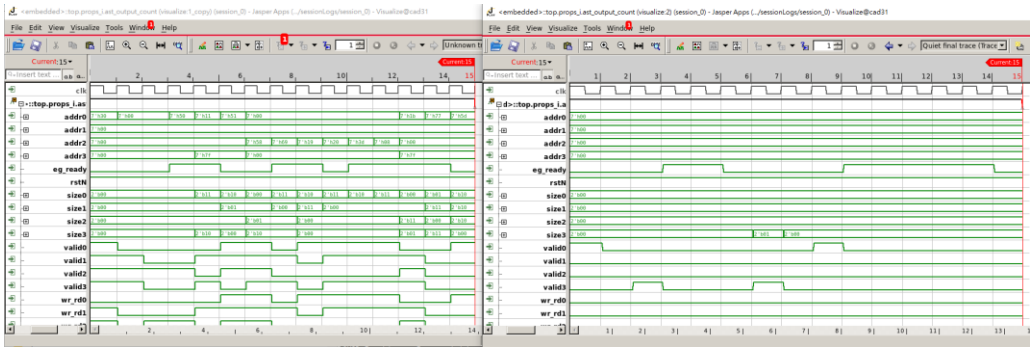


(The above image is for *Plot Selected Signals*, not for checkpoints.)

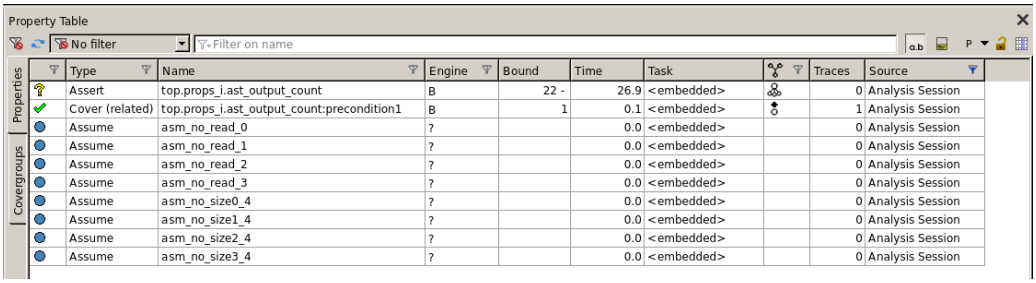


(This image is the first checkpoint.)

2. Take a screenshot of the comparison between non-quiet (left) and quiet (right) visualize windows.



3. Take a screenshot of the property table after disabling reads and running a formal proof.



	Type	Name	Engine	Bound	Time	Task		Traces	Source
	Assert	top.props_i.ast_output_count	B	22 -	26.9	<embedded>		0	Analysis Session
	Cover (related)	top.props_i.ast_output_count:precondition1	B	1	0.1	<embedded>		1	Analysis Session
	Assume	asm_no_read_0	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_read_1	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_read_2	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_read_3	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_size0_4	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_size1_4	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_size2_4	?		0.0	<embedded>		0	Analysis Session
	Assume	asm_no_size3_4	?		0.0	<embedded>		0	Analysis Session

Submission

1. **Due Tuesday, Dec. 3, 19:00. No delay is allowed.**

2. Selected students need to take screenshots of the results shown in the previous section, record them into a PDF file, and submit it to NTU COOL.
   Title: CVSD_Lab8_studentID (E.g. CVSD_Lab8_r12943008.pdf)