Computer-Aided VLSI System Design
Lab4: STA Lab: Static Timing Analysis

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Introduction

In this lab, you will learn:

1. How to use STA tools to analyze the timing of synchronous digital ASICs.
2. How to fix the problems of timing violations.

Environmental Setup

1. Source the license file:

```
source /usr/cad/synopsys/CIC/primetime.cshrc
```

2. Make a working directory:

```
mkdir Lab4
```

```
cd Lab4
```

Data Preparation

1. Upload Lab4.tar to your work directory.
2. Decompress Lab4.tar with the following command:

```
tar -xvf Lab4.tar
```

3. Check if you have these files (including hidden files):

Files/Folder	Description
`.synopsys_dc.setup`	Synopsys Design Compiler setup file
`ALU_syn.v`	Gate-level Verilog code for the simple ALU
`ALU.spef`	Timing and RC information file for the simple ALU
`ALU_pt.tcl`	Script to run PrimeTime
`ALU_syn.tcl`	Script to run Design Compiler (for ALU.spef)

4. Enter Lab4 directory:

```
cd Lab4
```

Invoking PrimeTime STA tool

1. To invoke PrimeTime, you can do either one:
   - pt_shell (command mode)
   - primetime & (GUI mode)

2. We encourage everybody to use command mode because:
   a. The command mode helps you keep a record of what you have done.
   b. The command mode runs more efficiently than the GUI mode.
   c. The command mode helps you look up the manual/reference quickly.

   In spite of the above advantages, command mode sometimes is not as good as GUI mode in terms of debugging the schematic problem. We will use command mode throughout this Lab. You are welcome to try the GUI mode by yourself.

Operating PrimeTime STA tool

STA Environment Setting for TSMC 0.13um Technology

1. Set search path (If it has not been set up yet).

```
set search_path ".
/home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db"
```

2. Set link library.

```
set link_path "* typical.db fast.db slow.db"
```

Reading Gate-Level Netlist Files

1. Type this line to read in CIC .18 library and your gate-level netlist:

```
read_verilog ./ALU_syn.v
```

2. Link all designs.

```
link_design ALU
```

Note that you have to check the search path and include library, if you get error messages after step 2.

Timing and RC information

Read leaf cell and net timing and RC information from a file in SPEF format and use that information to annotate the current design.

```
read_parasitics ALU.spef
```

Note: The file can be gotten during synthesis with “write_parasitics” command.

Operating Conditions

```
set_operating_conditions typical -library typical
```

Design Constraints

1. Specify the clock name, period, and clock characteristics.

```
create_clock -period 10 -waveform {0 5} [get_ports clk]
set design_clock [get_clock clk]
set_clock_uncertainty 0.5 $design_clock
set_clock_latency -min 1.5 $design_clock
set_clock_latency -max 2.5 $design_clock
set_clock_transition -min 0.25 $design_clock
set_clock_transition -max 0.30 $design_clock
report_timing
set_propagated_clock $design_clock
report_timing
```

2. Set wire load model:

```
set_wire_load_model -name "ForQA" -library "typical"
```

3. Set wire load mode:

```
set_wire_load_mode top
```

4. Report:

```
report_design
report_reference
```

Questions:

How many reference cells will you have? _____.

And total area size = _____

Timing analysis

1. Type the following commands to set the input/output delays:

```
set_input_delay 1.5 [get_ports inputA] -clock $design_clock
set_input_delay 1.5 [get_ports inputB] -clock $design_clock
set_input_delay 1.5 [get_ports instruction] -clock $design_clock
set_input_delay 1.5 [get_ports reset] -clock $design_clock
set_output_delay 1.5 [get_ports alu_out] -clock $design_clock
```

2. Check the timing:

```
check_timing
report_timing
report_bottleneck
```

Questions:

Does the design meet the timing requirement? _____.

Find the critical path: Start-point = _____

End-point = _____

3. Change the setting and check the timing again:

```
create_clock -period 2 -waveform {0 1.0} [get_ports clk]
report_timing
```

Questions:

Now, does the design meet the timing requirement? _____.

Is it the setup time violation or the hold time violation? _____.

If all other setting is the same, what is the minimum clock period for the design to meet the timing requirement (precision=0.1ns)? ___ ns.

Try to modify the setting and verify whether the clock period meets the timing requirement.

4. Change the setting and check the timing again:

```
create_clock -period 10 -waveform {0 5.0} [get_ports clk]
set_output_delay 8 [get_ports alu_out] -clock $design_clock
report_timing
```

Questions:

Now, does the design meet the timing requirement? _____.

Where is the new critical path:

Start-point = _____

End-point = _____

Reports

1. Show the types of checks being done (setup, hold, min pulse width, recovery, removal and so forth).

```
report_constraint
report_constraint -all_violators
report_analysis_coverage
```

Questions:

How many timing violations are there in the design? _____

2. Change the setting and check the report again:

```
set_clock_uncertainty 0.0 $design_clock
report_constraint
report_constraint -all_violators
report_analysis_coverage
```

Questions:

Why are the hold-time violations fixed? Think about the change in clock setting.

_____

_____

Checkpoints

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your final STA results as follows.

```
pt_shell> report_analysis_coverage
****************************************
Report : analysis_coverage
Design : ALU
Version: U-2022.12
Date   : Sat Oct 19 16:10:57 2024
****************************************

Type of Check         Total              Met          Violated        Untested
-------------------------------------------------------------------------------
setup                    28       28 (100%)         0 (  0%)       0 (  0%)
hold                     28       28 (100%)         0 (  0%)       0 (  0%)
recovery                 28       28 (100%)         0 (  0%)       0 (  0%)
removal                  28       28 (100%)         0 (  0%)       0 (  0%)
min_pulse_width          84       56 ( 67%)         0 (  0%)      28 ( 33%)
out_setup                 8        8 (100%)         0 (  0%)       0 (  0%)
out_hold                  8        8 (100%)         0 (  0%)       0 (  0%)
-------------------------------------------------------------------------------
All Checks              212      184 ( 87%)         0 (  0%)      28 ( 13%)
```

2. Show your answers of the questions in this lab document. There are 13 questions in total.

Submission

1. **Due Tuesday, Oct. 22, 19:00. No delay is allowed.**

2. Selected students need to take snapshots of the results shown in the previous section, record them into a PDF file, and submit it to NTU COOL.
   Title: CVSD_Lab4_studentID (E.g. CVSD_Lab4_r12943008.pdf)