Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 3, 13:59

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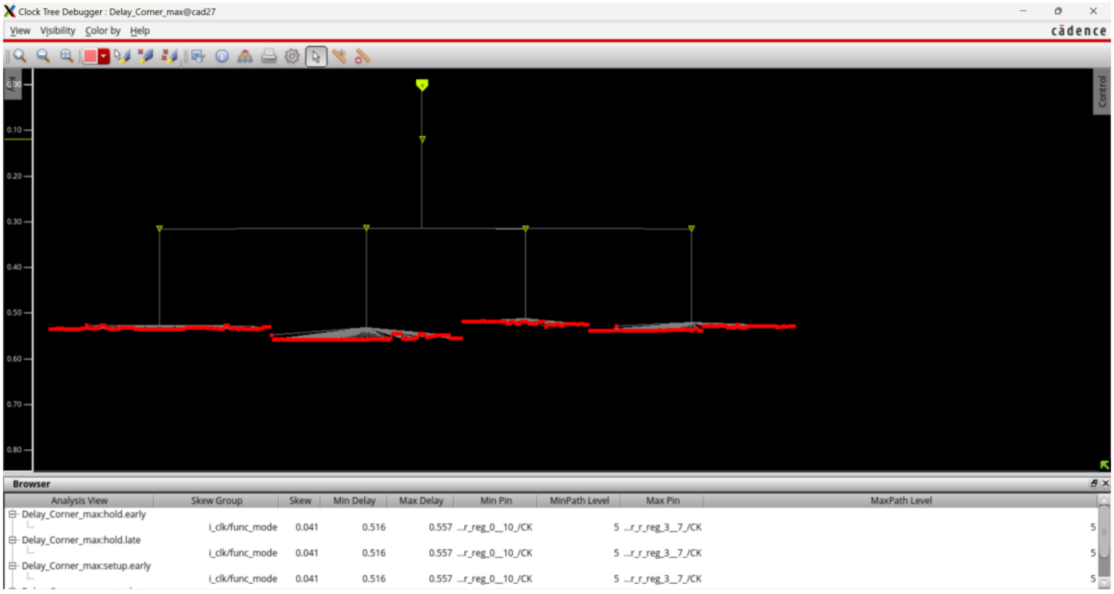
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	489062.43
	Core Area (um^2)	290445.51
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	5ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		From TA

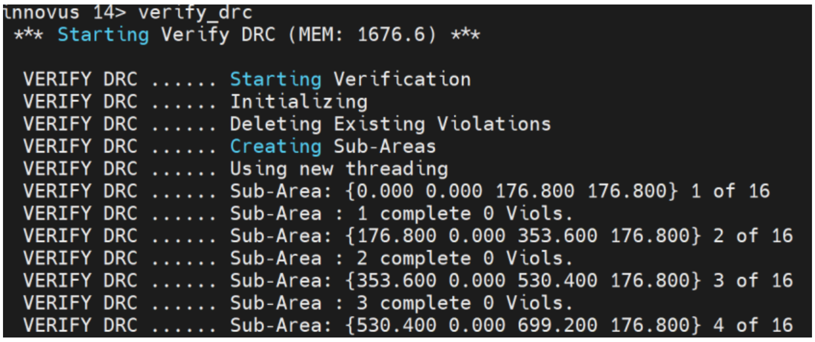
Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).

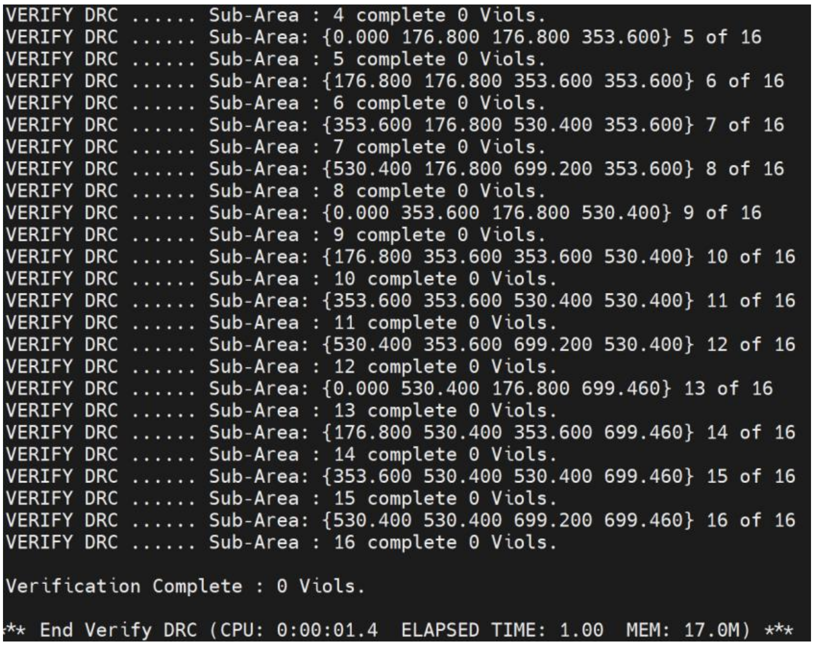


Analysis View	Skew Group	Skew	Min Delay	Max Delay	Min Pin	MinPath Level	Max Pin	MaxPath Level
Delay_Corner_max:hold.early								
	i_clk/func_mode	0.041	0.516	0.557	...r_reg_0__10_/CK	5	...r_r_reg_3__7_/CK	5
Delay_Corner_max:hold.late								
	i_clk/func_mode	0.041	0.516	0.557	...r_reg_0__10_/CK	5	...r_r_reg_3__7_/CK	5
Delay_Corner_max:setup.early								
	i_clk/func_mode	0.041	0.516	0.557	...r_reg_0__10_/CK	5	...r_r_reg_3__7_/CK	5

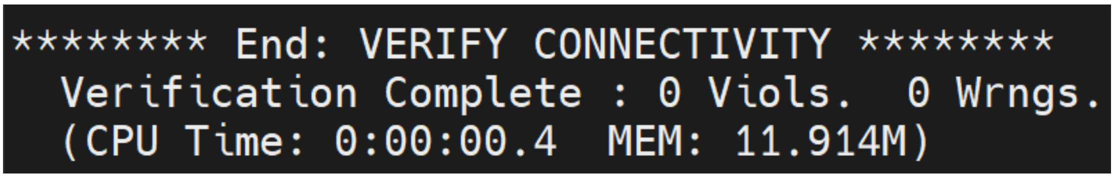
2. Attach the snapshot of DRC and LVS checking after routing. (5%)



```
innovus 14> verify_drc
 *** Starting Verify DRC (MEM: 1676.6) ***

  VERIFY DRC ...... Starting Verification
  VERIFY DRC ...... Initializing
  VERIFY DRC ...... Deleting Existing Violations
  VERIFY DRC ...... Creating Sub-Areas
  VERIFY DRC ...... Using new threading
  VERIFY DRC ...... Sub-Area: {0.000 0.000 176.800 176.800} 1 of 16
  VERIFY DRC ...... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ...... Sub-Area: {176.800 0.000 353.600 176.800} 2 of 16
  VERIFY DRC ...... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ...... Sub-Area: {353.600 0.000 530.400 176.800} 3 of 16
  VERIFY DRC ...... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ...... Sub-Area: {530.400 0.000 699.200 176.800} 4 of 16
```

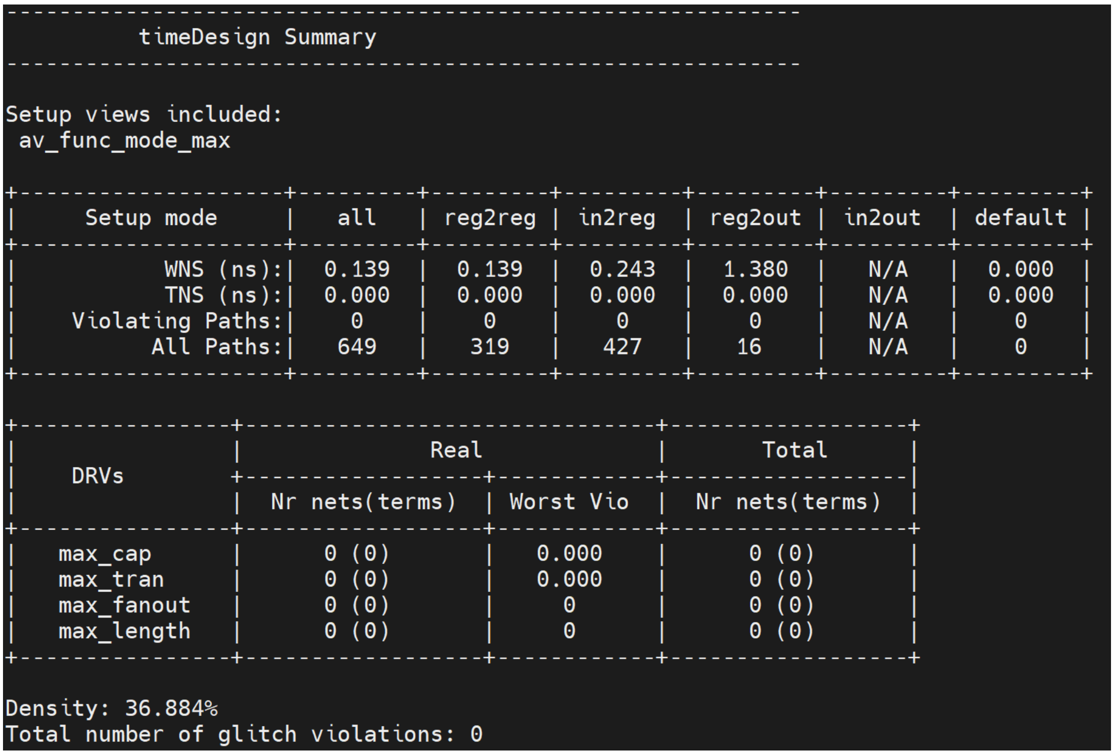


```
VERIFY DRC ...... Sub-Area : 4 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {0.000 176.800 176.800 353.600} 5 of 16
VERIFY DRC ...... Sub-Area : 5 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {176.800 176.800 353.600 353.600} 6 of 16
VERIFY DRC ...... Sub-Area : 6 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {353.600 176.800 530.400 353.600} 7 of 16
VERIFY DRC ...... Sub-Area : 7 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {530.400 176.800 699.200 353.600} 8 of 16
VERIFY DRC ...... Sub-Area : 8 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {0.000 353.600 176.800 530.400} 9 of 16
VERIFY DRC ...... Sub-Area : 9 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {176.800 353.600 353.600 530.400} 10 of 16
VERIFY DRC ...... Sub-Area : 10 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {353.600 353.600 530.400 530.400} 11 of 16
VERIFY DRC ...... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {530.400 353.600 699.200 530.400} 12 of 16
VERIFY DRC ...... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {0.000 530.400 176.800 699.460} 13 of 16
VERIFY DRC ...... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {176.800 530.400 353.600 699.460} 14 of 16
VERIFY DRC ...... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {353.600 530.400 530.400 699.460} 15 of 16
VERIFY DRC ...... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ...... Sub-Area: {530.400 530.400 699.200 699.460} 16 of 16
VERIFY DRC ...... Sub-Area : 16 complete 0 Viols.

Verification Complete : 0 Viols.

** End Verify DRC (CPU: 0:00:01.4  ELAPSED TIME: 1.00  MEM: 17.0M) ***
```

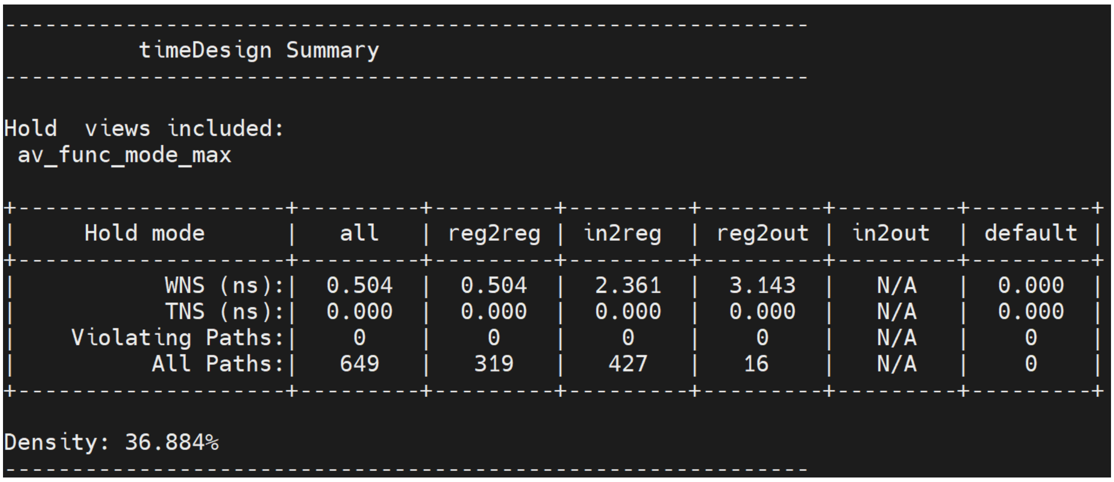


```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.4  MEM: 11.914M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

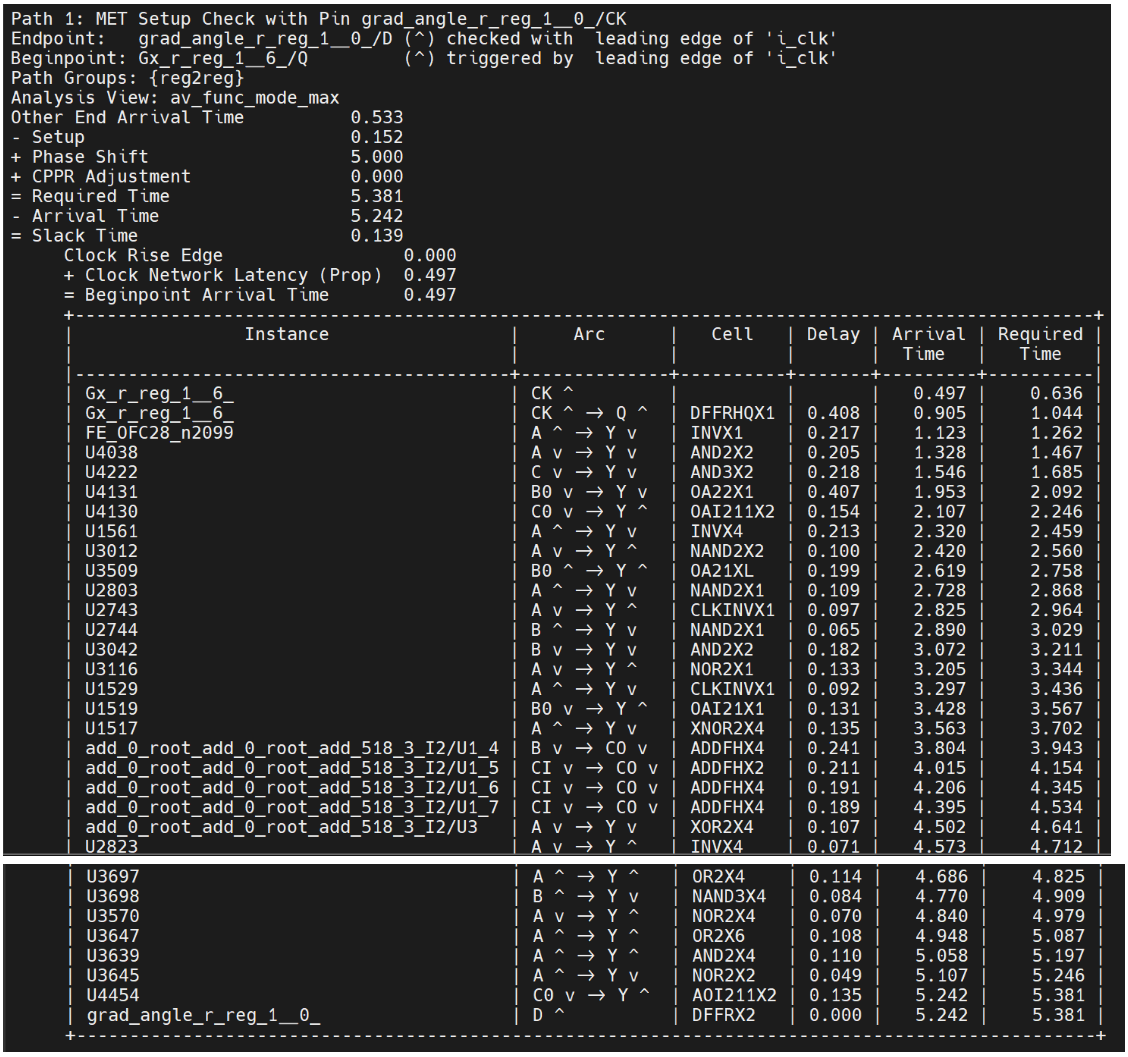


```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.139  |  0.139  |  0.243  |  1.380  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |     0 (0)        |   0.000    |     0 (0)        |
|   max_tran     |     0 (0)        |   0.000    |     0 (0)        |
|   max_fanout   |     0 (0)        |     0      |     0 (0)        |
|   max_length   |     0 (0)        |     0      |     0 (0)        |
+----------------+------------------+------------+------------------+

Density: 36.884%
Total number of glitch violations: 0
```



```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.504  |  0.504  |  2.361  |  3.143  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 36.884%
------------------------------------------------------------
```

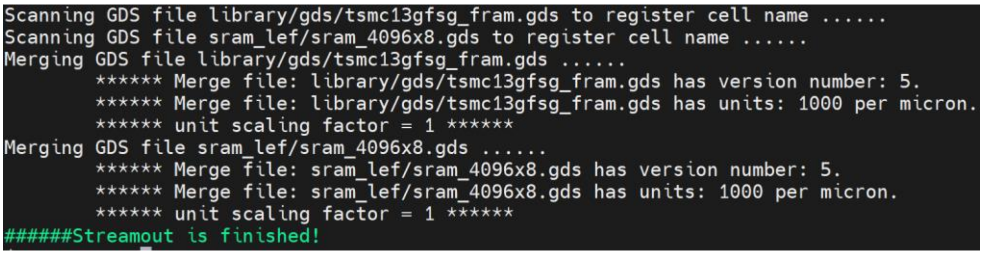
4. Show the critical path after post-route optimization. What is the path type? (10%) (The slack of the critical path should match the smallest slack in the timing report)



```
Path 1: MET Setup Check with Pin grad_angle_r_reg_1__0_/CK
Endpoint:   grad_angle_r_reg_1__0_/D (^) checked with  leading edge of 'i_clk'
Beginpoint: Gx_r_reg_1__6_/Q         (^) triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.533
- Setup                         0.152
+ Phase Shift                   5.000
+ CPPR Adjustment               0.000
= Required Time                 5.381
- Arrival Time                  5.242
= Slack Time                    0.139
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.497
     = Beginpoint Arrival Time       0.497
     +--------------------------------------------------------------------------------------------------------+
     |               Instance                 |     Arc      |   Cell    | Delay | Arrival | Required |
     |                                        |              |           |       |  Time   |   Time   |
     |----------------------------------------+--------------+-----------+-------+---------+----------|
     | Gx_r_reg_1__6_                         | CK ^         |           |       |   0.497 |    0.636 |
     | Gx_r_reg_1__6_                         | CK ^ → Q ^   | DFFRHQX1  | 0.408 |   0.905 |    1.044 |
     | FE_OFC28_n2099                         | A ^ → Y v    | INVX1     | 0.217 |   1.123 |    1.262 |
     | U4038                                  | A v → Y v    | AND2X2    | 0.205 |   1.328 |    1.467 |
     | U4222                                  | C v → Y v    | AND3X2    | 0.218 |   1.546 |    1.685 |
     | U4131                                  | B0 v → Y v   | OA22X1    | 0.407 |   1.953 |    2.092 |
     | U4130                                  | C0 v → Y ^   | OAI211X2  | 0.154 |   2.107 |    2.246 |
     | U1561                                  | A ^ → Y v    | INVX4     | 0.213 |   2.320 |    2.459 |
     | U3012                                  | A v → Y ^    | NAND2X2   | 0.100 |   2.420 |    2.560 |
     | U3509                                  | B0 ^ → Y ^   | OA21XL    | 0.199 |   2.619 |    2.758 |
     | U2803                                  | A ^ → Y v    | NAND2X1   | 0.109 |   2.728 |    2.868 |
     | U2743                                  | A v → Y ^    | CLKINVX1  | 0.097 |   2.825 |    2.964 |
     | U2744                                  | B ^ → Y v    | NAND2X1   | 0.065 |   2.890 |    3.029 |
     | U3042                                  | B v → Y v    | AND2X2    | 0.182 |   3.072 |    3.211 |
     | U3116                                  | A v → Y ^    | NOR2X1    | 0.133 |   3.205 |    3.344 |
     | U1529                                  | A ^ → Y v    | CLKINVX1  | 0.092 |   3.297 |    3.436 |
     | U1519                                  | B0 v → Y ^   | OAI21X1   | 0.131 |   3.428 |    3.567 |
     | U1517                                  | A ^ → Y v    | XNOR2X4   | 0.135 |   3.563 |    3.702 |
     | add_0_root_add_0_root_add_518_3_I2/U1_4 | B v → CO v   | ADDFHX4   | 0.241 |   3.804 |    3.943 |
     | add_0_root_add_0_root_add_518_3_I2/U1_5 | CI v → CO v  | ADDFHX2   | 0.211 |   4.015 |    4.154 |
     | add_0_root_add_0_root_add_518_3_I2/U1_6 | CI v → CO v  | ADDFHX4   | 0.191 |   4.206 |    4.345 |
     | add_0_root_add_0_root_add_518_3_I2/U1_7 | CI v → CO v  | ADDFHX4   | 0.189 |   4.395 |    4.534 |
     | add_0_root_add_0_root_add_518_3_I2/U3  | A v → Y v    | XOR2X4    | 0.107 |   4.502 |    4.641 |
     | U2823                                  | A v → Y ^    | INVX4     | 0.071 |   4.573 |    4.712 |
     | U3697                                  | A ^ → Y ^    | OR2X4     | 0.114 |   4.686 |    4.825 |
     | U3698                                  | B ^ → Y v    | NAND3X4   | 0.084 |   4.770 |    4.909 |
     | U3570                                  | A v → Y ^    | NOR2X4    | 0.070 |   4.840 |    4.979 |
     | U3647                                  | A ^ → Y ^    | OR2X6     | 0.108 |   4.948 |    5.087 |
     | U3639                                  | A ^ → Y ^    | AND2X4    | 0.110 |   5.058 |    5.197 |
     | U3645                                  | A ^ → Y v    | NOR2X2    | 0.049 |   5.107 |    5.246 |
     | U4454                                  | C0 v → Y ^   | AOI211X2  | 0.135 |   5.242 |    5.381 |
     | grad_angle_r_reg_1__0_                 | D ^          | DFFRX2    | 0.000 |   5.242 |    5.381 |
     +--------------------------------------------------------------------------------------------------------+
```

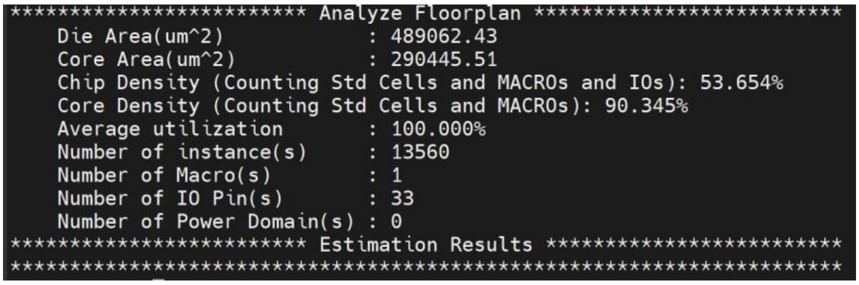
The path type is reg2reg

5. Attach the snapshot of GDS stream out messages. (10%)



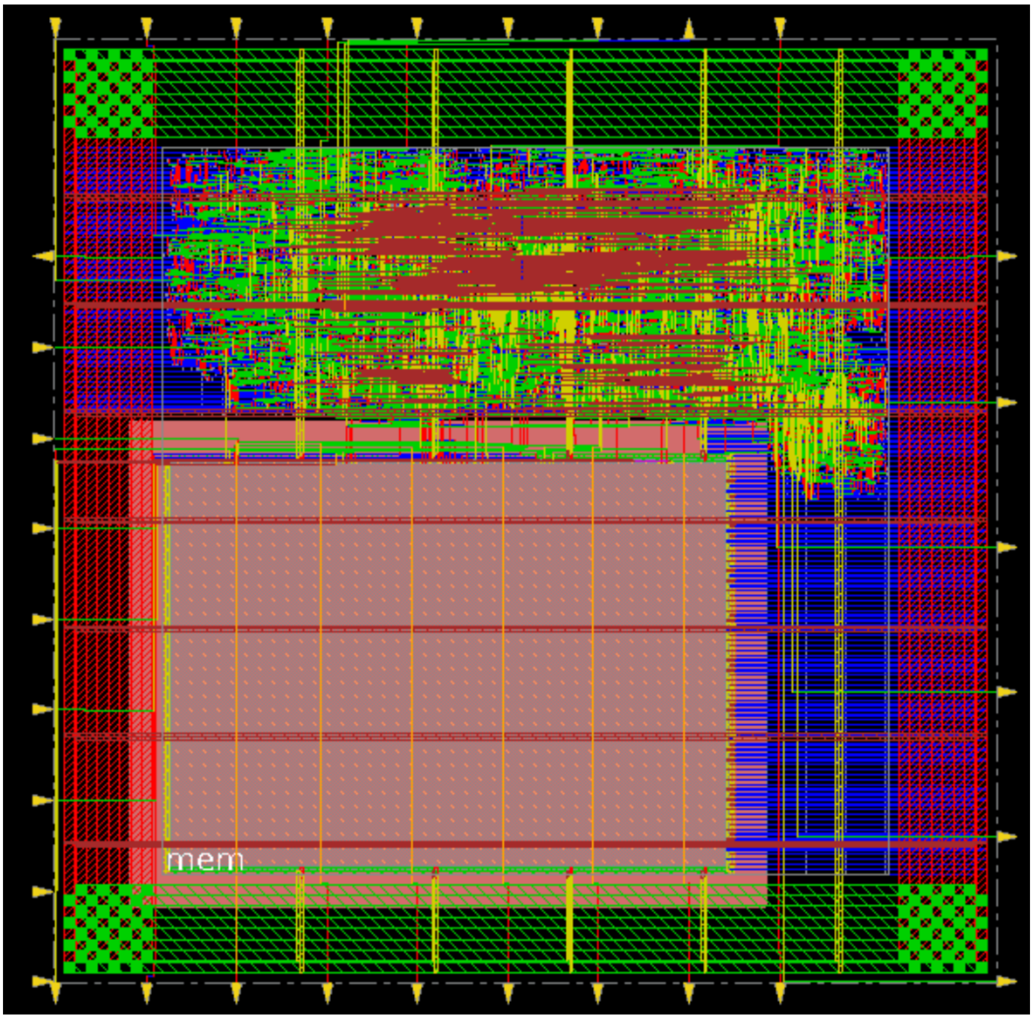
```
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file sram_lef/sram_4096x8.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file sram_lef/sram_4096x8.gds ......
        ****** Merge file: sram_lef/sram_4096x8.gds has version number: 5.
        ****** Merge file: sram_lef/sram_4096x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)



```
************************ Analyze Floorplan **************************
    Die Area(um^2)              : 489062.43
    Core Area(um^2)             : 290445.51
    Chip Density (Counting Std Cells and MACROs and IOs): 53.654%
    Core Density (Counting Std Cells and MACROs): 90.345%
    Average utilization         : 100.000%
    Number of instance(s)       : 13560
    Number of Macro(s)          : 1
    Number of IO Pin(s)         : 33
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
*********************************************************************
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

My strategy is to place the SRAM macro around the chip periphery to optimize its connections to fixed cells and minimize routing complexity. This placement reduces the wire lengths between the macro and logic gates, improving timing and lowering power consumption.

Placing the macro on the periphery ensures sufficient space for the central placement of standard cells, maintaining a clear and continuous area for random logic. This avoids fragmenting the layout and ensures signal routing paths are not overly constrained. Moreover, orienting the macro to minimize the distance between its pins further simplifies routing and reduces latency.

This approach is based on the concepts discussed in Chapter 7 part 1 of the lecture notes, particularly regarding macro placement strategies. By following these principles, the strategy ensures a balance between performance, power efficiency, and manufacturability, while supporting efficient chip design.