Computer-Aided VLSI System Design
Lab5: Innovus Lab (1/3)

TA：邱仁皓 r12943008@ntu.edu.tw

Introduction

In this lab, you will learn how to use Innovus to run the APR flow, and generate the required data for demonstration.

Data Preparation

1. **Innovus_Lab.zip** contains
   - **design_data**
     A. CHIP.v
     B. CHIP.ioc
     C. CHIP.sdc
     D. CHIP_scan_ideal.sdc
   - **library/celtic**
     A. fast.cdB
     B. slow.cdB
   - **library/tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **library/gds**
     A. tsmc13gfsg_fram.gds
     B. tpz013g3_v2.0.gds
   - **library/lef**
     A. tsmc13fsg_8lm_cic.lef
     B. tpz013g3_8lm_cic.lef
     C. RF2SH64x16.vclef
     D. antenna_8.lef
   - **library/lib**
     A. slow.lib
     B. fast.lib
     C. tpz013g3wc.lib
     D. tpz013g3lt.lib
     E. RF2SH64x16_slow_syn.lib
     F. RF2SH64x16_fast@0C_syn.lib
   - **library**
     A. streamOut.map
     B. tsmc013.capTbl
     C. addIoFiller_tpz.cmd
   - mmmc.view

Data Preparation (Library)

1. Extract data from **Innovus_Lab.zip** and change the directory to **Innovus_Lab**:
   1.1 % **unzip Innovus_Lab.zip**
   1.2 % **cd Innovus_Lab**
2. Start Innovus:
   2.1 % **innovus** (remember do not use background execution)
   2.2 Fail to open Innovus:
   % **source /usr/cad/innovus/CIC/license.cshrc**
   % **source innovus.cshrc**
   2.3 % **innovus** (successfully provoke Innovus)
3. Design Import
   3.1 ***File → Import Design…***
   3.2 Verilog
   - Files: **design_data/CHIP.v**
   - Top Cell: ◆ By User: **CHIP**

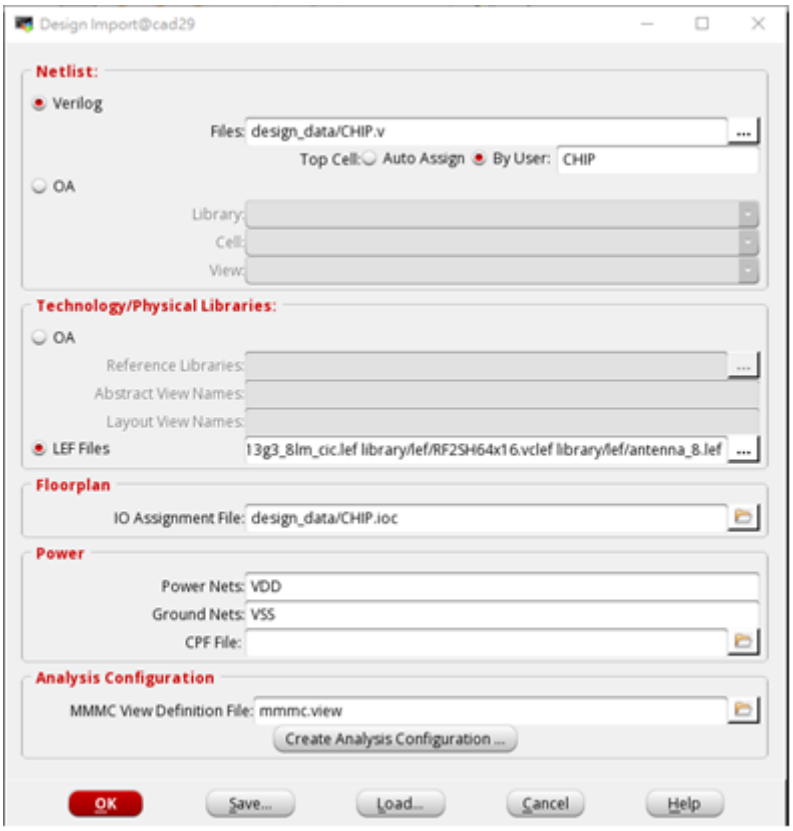
   3.3 Technology/Physical Libraries
   - LEF Files: **library/lef/tsmc13fsg_8lm_cic.lef (must be in first order)**
     library/lef/tpz013g3_8lm_cic.lef
     library/lef/RF2SH64x16.vclef
     library/lef/antenna_8.lef

   3.4 Floorplan
   - IO Assignment Files: **design_data/CHIP.ioc**

   3.5 Power
   - Power Nets: **VDD**
   - Ground Nets: **VSS**

   3.6 Analysis Configuration
   - MMMC View Definition File: **mmmc.view**

   3.7 Save current settings:
   - Click Save… button
   - File name: **CHIP.conf**
   - Click Save button
   - Click OK button



Connecting Global Net

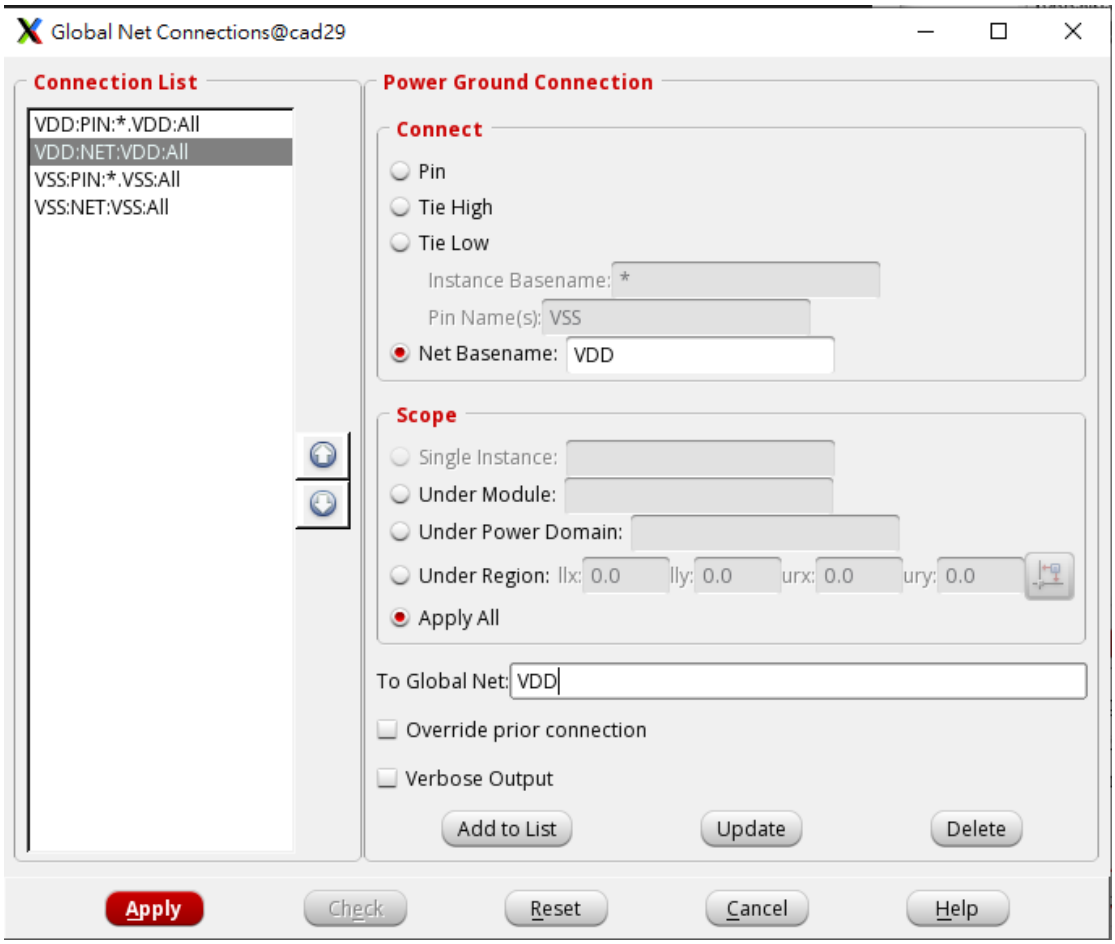
1. Open ***Power → Connect Global Nets…***
2. Add all VDD pins to Connection List:
   - Connect ◆ Pin ◆ Pin Name(s): **VDD**
   - Scope ◆ **Apply All**
   - To Global Net: **VDD**
   - Click Add to List button
3. Add all VDD nets to Connection List:
   - Connect ◆ Net Basename: **VDD**
   - Scope ◆ **Apply All**
   - To Global Net: **VDD**
   - Click Add to List button
4. Add all Tie High pins to Connection List:
   - Connect ◆ **Tie High**
   - Scope ◆ **Apply All**
   - To Global Net: **VDD**
   - Click Add to List button

Skip step 4 and step 7 here. We will add tie high and tie low cells later.

5. Add all VSS pins to Connection List:
   - Connect ◆ Pin ◆ Pin Name(s): **VSS**

- Scope ◆ **Apply All**
- To Global Net: **VSS**
- Click Add to List button

6. Add all VSS nets to Connection List:
   - Connect ◆ Net Basename: **VSS**
   - Scope ◆ **Apply All**
   - To Global Nets: **VSS**
   - Click Add to List button
7. Add all Tie Low pins to Connection List:
   - Connect ◆ **Tie Low**
   - Scope ◆ **Apply All**
   - To Global Net: **VSS**
   - Click Add to List button



8. Apply the connection list and check:
   - Click Apply button
   - Click Check button
   - Click Cancel button

```
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_5_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_5_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_4_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_4_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_3_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_3_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_2_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_2_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_1_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_1_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_0_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_0_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S17_reg is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S17_reg is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S16_reg is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S16_reg is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/Finish_reg is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/Finish_reg is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_1_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_1_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_0_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_0_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_0_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_0_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_1_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_1_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_2_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_2_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_3_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_3_ is not connect to global special net.
```

9. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/init**
   - Click OK button

```
Generated self-contained design init.dat
#% End save design ... (date=11/20 22:08:02, to
*** Message Summary: 0 warning(s), 0 error(s)
```

10. Restore file
    - Open ***File → Restore Design…***
    - Choose ◆ Innovus
    - Restore Design File: **DBS/init**
11. Set process node
    - innovus #> **setDesignMode -process 130**

Specifying Scan Chain

1. innovus # > **specifyScanChain scan1 -start ipad_SCAN_IN/C -stop opad_SCAN_OUT/I**
2. innovus # > **scanTrace**

```
*** Scan Trace Summary (runtime: cpu: 0:00:00.0 , real: 0:00:00.0):
Successfully traced 1 scan chain  (total 1574 scan bits).
*** Scan Sanity Check Summary:
*** 1 scan chain  passed sanity check.
```

Floorplan

1. Open ***Floorplan → Specify Floorplan…***
2. Specify core size:

- Ratio (H/W): Set any as your wish. It is set to 1 in Lab5.
- Core Utilization: Set any as your wish. It is set to 0.7 in Lab5.

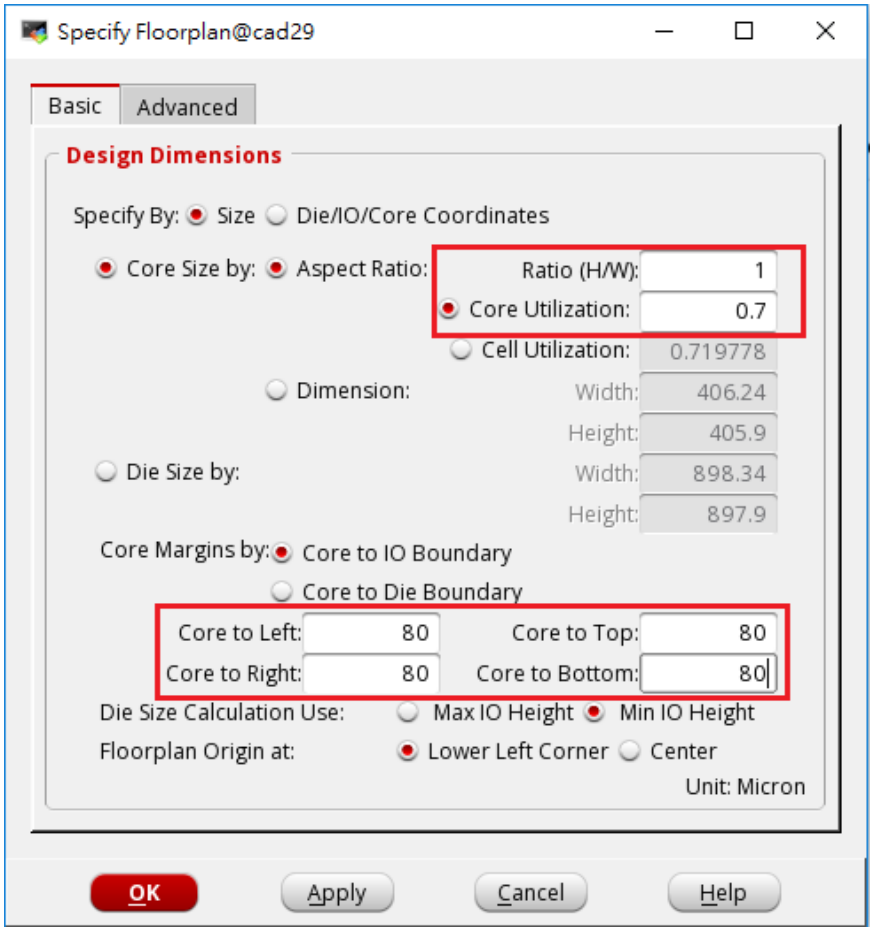
3. Specify core margin:
   - Core to IO Boundary

     Core to Left: **80**

     Core to Right: **80**

     Core to Top: **80**

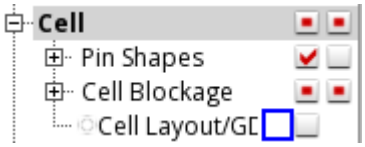
     Core to Bottom: **80**
4. Click OK button



Plan Design

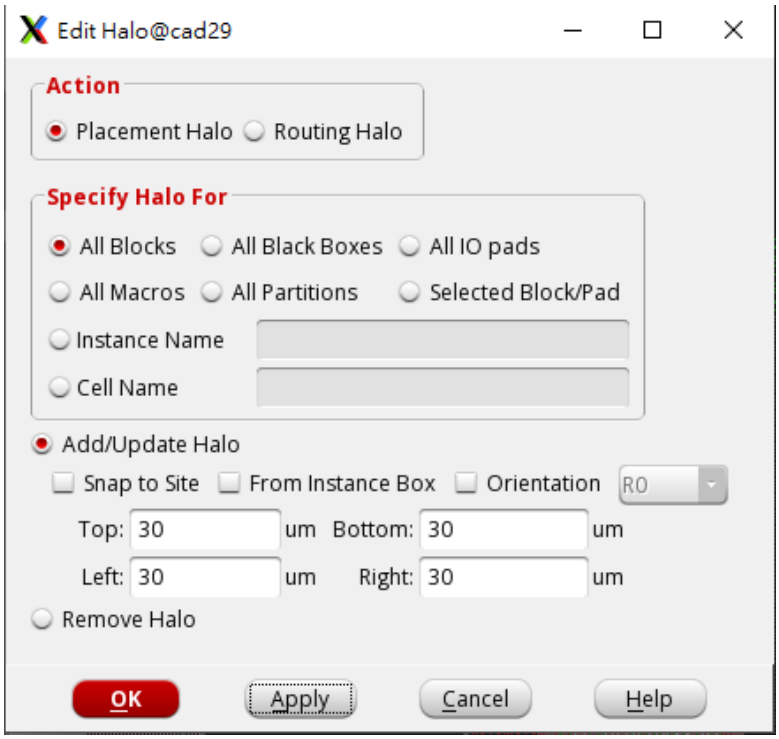
1. Change to **floorplan view** 
2. Open ***Floorplan → Automatic Floorplan → Plan Design…***

   Note: Option ***Plan Design…*** does not exist in latest Innovus but in Innovus v17. Latest Innovus is provoked by cvsd.cshrc, while v17 by innovus.cshrc of this lab.
3. Click OK button
4. Set **Visible** to Cell/Pin Shapes in color control



Edit Halo

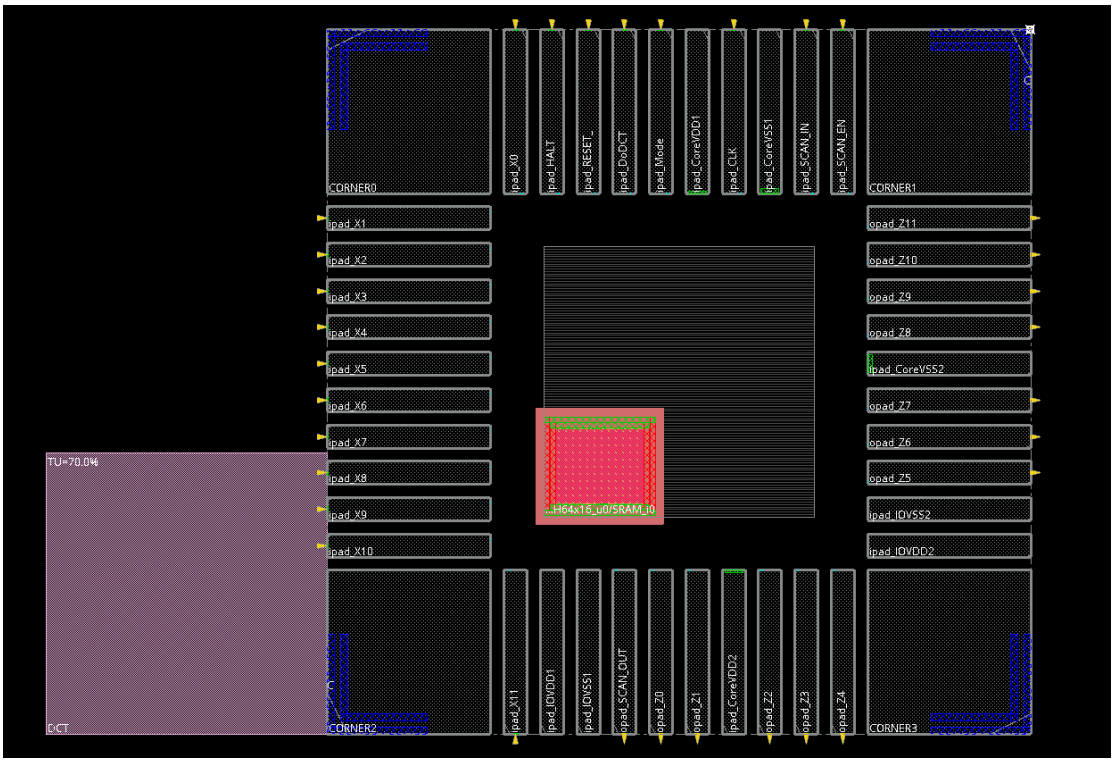
1. Open ***Floorplan → Edit Floorplan → Edit Halo…***
2. Choose ◆ **All Blocks**
3. Add/Update Halo
   - Top: **30 um**
   - Bottom: **30 um**
   - Left: **30 um**
   - Right: **30 um**
4. Click OK button
5. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/floorplan**



Checkpoints

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Take a snapshot after floorplan.



Submission

1. **Due Tuesday, Nov. 12, 19:00. No delay is allowed.**

2. Selected students need to take snapshots of the results shown in the previous section, record them into a PDF file, and submit it to NTU COOL.
   Title: CVSD_Lab5_studentID (E.g. CVSD_Lab5_r12943008.pdf)

Appendix 1: Multi-Mode-Multi-Corner (MMMC)

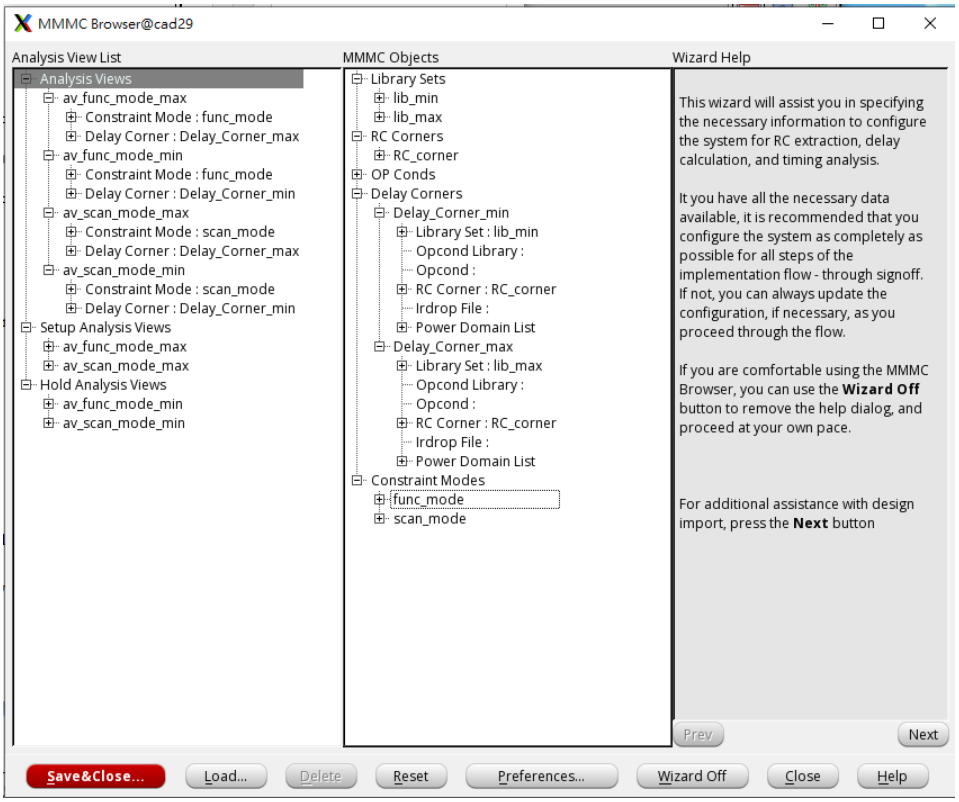
1. Open ***File → Import Design…***
2. Press Create Analysis Configuration …
3. Click Library Sets and include the max and min delay library:
   - Max delay
     Name: **lib_max**
     (containing the worst-case conditions for setup-time analysis)
     Timing Library:
     slow.lib, tpz013g3wc.lib, RF2SH64x16_slow_syn.lib
     SI Library: **slow.cdB**
   - Min delay
     Name: **lib_min**
     (containing the best-case conditions for hold-time analysis)
     Timing Library:

fast.lib, tpz013g3lt.lib, RF2SH64x16_fast@0C_syn.lib
SI Library: **fast.cdB**

4. Click RC Corners to include the RC corner library:
   - Name: **RC_Corner**
   - Cap Table: **tsmc013.capTbl**
   - QRC Technology File: **icecaps_8lm.tch**
5. Click Delay Corners and create max and min delay constraints:
   - Max delay
     Name: **Delay_Corner_max**
     RC Corner: **RC_Corner**
     Library Set: **lib_max**
   - Min delay
     Name: **Delay_Corner_min**
     RC Corner: **RC_Corner**
     Library Set: **lib_min**
6. Click Constraints Modes and create a function mode/scan mode:
   - Function mode
     Name: **func_mode**
     SDC Constraint Files: **CHIP.sdc**
   - Scan mode
     Name: **scan_mode**
     SDC Constraint Files: **CHIP_scan_ideal.sdc**
7. Click Analysis Views to create max and min delay analysis
   - Max delay (function mode)
     Name: **av_func_mode_max**
     Constraint Mode: **func_mode**
     Delay Corner: **Delay_Corner_max**
   - Min delay (function mode)
     Name: **av_func_mode_min**
     Constraint Mode: **func_mode**
     Delay Corner: **Delay_Corner_min**
   - Max delay (scan mode)
     Name: **av_scan_mode_max**
     Constraint Mode: **scan_mode**
     Delay Corner: **Delay_Corner_max**
   - Min delay (scan mode)
     Name: **av_scan_mode_min**
     Constraint Mode: **scan_mode**

Delay Corner: **Delay_Corner_min**

8. Click Setup Analysis View and specify the max analysis mode
   - Choose: **av_func_mode_max**, **av_scan_mode_max**
9. Click Hold Analysis View and specify the min analysis mode
   - Choose: **av_func_mode_min**, **av_scan_mode_min**
10. Click Save&Close… button and name the configuration as "**mmmc.view**"



Appendix 2: Generate CHIP.ioc

1. Open ***File → Save → I/O File…***
   - Save IO ◆ sequence
   - To File: **CHIP.ioc**
   - ◆ Generate template IO File
   - Click OK button
2. Open ***File → Load → I/O File…***
   - Choose **CHIP.ioc**
   - Click Open button

Do after Import Design