Computer-Aided VLSI System Design
Lab7: Innovus Lab (3/3)

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Introduction

In this lab, you will learn how to use Innovus to run the APR flow, and generate the required data for demonstration.

Data Preparation

1. **Innovus_Lab** from Lab5 contains
   - **design_data**
     A. CHIP.v
     B. CHIP.ioc
     C. CHIP.sdc
     D. CHIP_scan_ideal.sdc
   - **library/celtic**
     A. fast.cdB
     B. slow.cdB
   - **library/tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **library/gds**
     A. tsmc13gfsg_fram.gds
     B. tpz013g3_v2.0.gds
   - **library/lef**
     A. tsmc13fsg_8lm_cic.lef
     B. tpz013g3_8lm_cic.lef
     C. RF2SH64x16.vclef
     D. antenna_8.lef
   - **library/lib**
     A. slow.lib
     B. fast.lib
     C. tpz013g3wc.lib
     D. tpz013g3lt.lib
     E. RF2SH64x16_slow_syn.lib
     F. RF2SH64x16_fast@0C_syn.lib
   - **library**
     A. streamOut.map
     B. tsmc013.capTbl
     C. addIoFiller_tpz.cmd
     D. mmmc.view

Clock Tree Synthesis (CTS)

1. Start Innovus:
   1.1 Source the licenses:
   % **source /usr/cad/innovus/CIC/license.cshrc**
   % **source innovus.cshrc**
   (In this Lab, source innovus.cshrc from NTU COOL instead)
   1.2 % **innovus** (remember do not use background execution)
2. Restore file
   - Open ***File*** → ***Restore Design…***
   - Choose ◆ Innovus
3. Restore Design File: **DBS/place**
4. Create new sdc files for CTS (use the terminal and text editors)
   4.1 Copy **CHIP.sdc** and **CHIP_scan_ideal.sdc** (in the **design_data** directory)
   - % **cp design_data/CHIP.sdc CHIP_cts.sdc**
   - % **cp design_data/CHIP_scan_ideal.sdc CHIP_scan_cts.sdc**

   4.2 Remove **set_clock_latency** & **set_clock_uncertainty** that estimate clock network delay
   4.3 Remove **set_ideal_network**

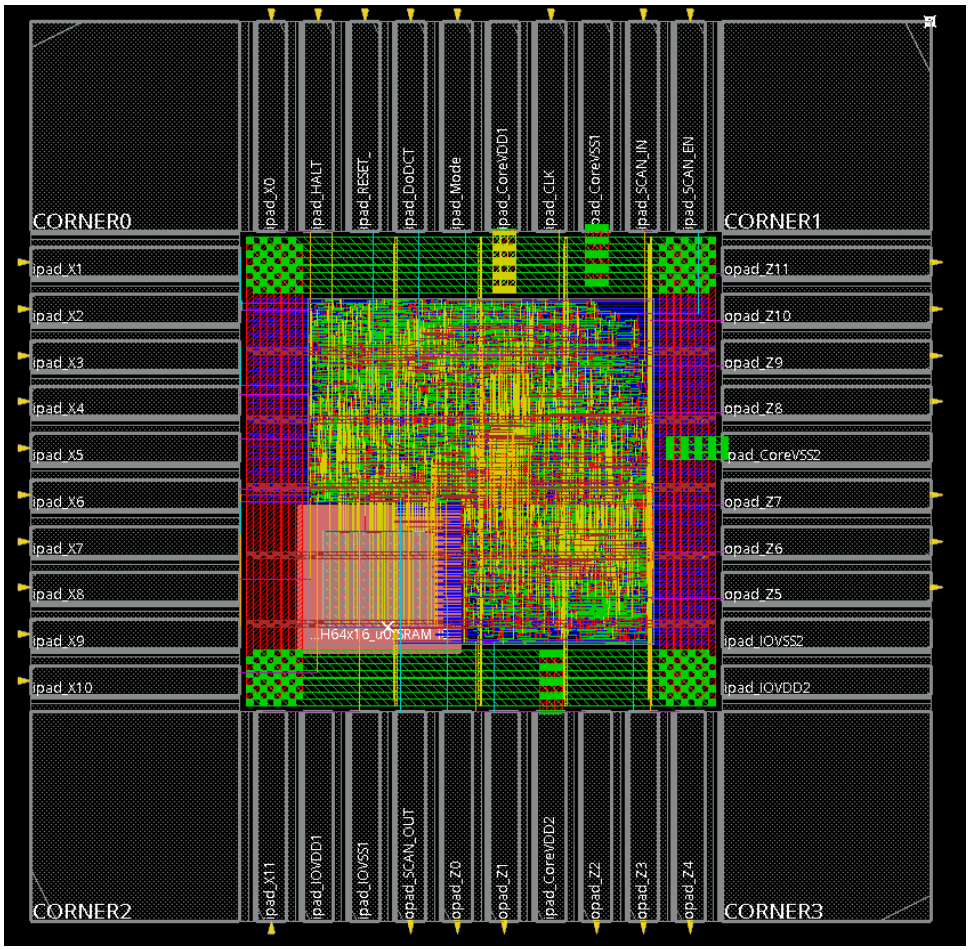
```
set sdc_version 1.2
current_design CHIP
create_clock [get_ports {CLK}] -name CLK1 -period 10 -waveform {0 5}
set_case_analysis 0 [get_ports {SCAN_EN}]
set_max_fanout 15 [current_design]
set_max_transition 2.7 [current_design]

#set_clock_latency 2 [get_clocks {CLK1}]

set_input_delay     1 -clock CLK1 \
                      [remove_from_collection [all_inputs] [get_ports CLK]]
set_output_delay    1 -clock CLK1 [all_outputs]

set_drive 0.1 [all_inputs]
set_load -pin_load 1 [all_outputs]

set_false_path  -from [get_ports {DoDCT}]
set_false_path  -from [get_ports {RESET_}]
set_false_path  -from [get_ports {Mode}]
```

5. Update sdc file
   5.1 innovus #> **update_constraint_mode -name func_mode -sdc_files design_data/CHIP_cts.sdc**
   5.2 innovus #> **update_constraint_mode -name scan_mode -sdc_files design_data/CHIP_scan_cts.sdc**
6. Create spec file for CTS
   6.1 innovus #> **create_ccopt_clock_tree_spec -file ./ccopt.spec**
   6.2 innovus #> **source ./ccopt.spec**

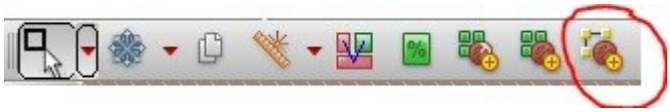
6.3 innovus #> **ccopt_design -cts**

```
# Skew group to balance non generated clock:i_clk in timing_config:func_mod
create_ccopt_skew_group -name i_clk/func_mode -sources i_clk -auto_sinks
set_ccopt_property include_source_latency -skew_group i_clk/func_mode true
set_ccopt_property extracted_from_clock_name -skew_group i_clk/func_mode i_
set_ccopt_property extracted_from_constraint_mode_name -skew_group i_clk/fu
set_ccopt_property extracted_from_delay_corners -skew_group i_clk/func_mode


check_ccopt_clock_tree_convergence
# Restore the ILM status if possible
```

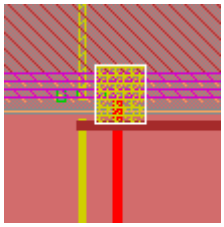
7. Find DRC errors



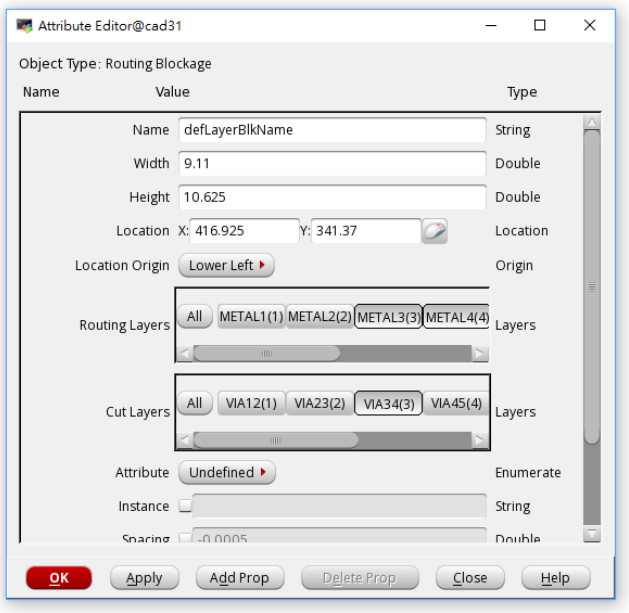
7.1 Create Routing Blockage



- Block the place appear DRC violation
- Select the blockage and press q to set **Routing Layers** and **Cut Layers**

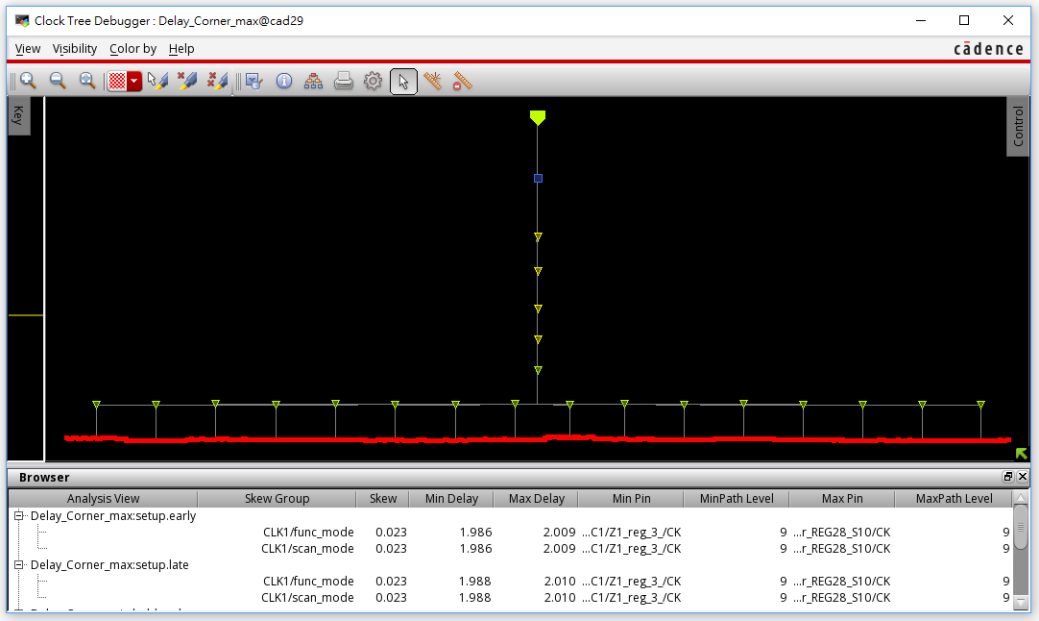


You can also create the blockage with commands:
innovus #> createRouteBlk -box 416.34550 338.51000 425.76600 351.46300



7.2 innovus #> **ccopt_design -cts**

8. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/cts
9. CCOpt clock tree debugger
   - Open ***Clock → CCOpt Clock Tree Debugger…***
   - Click OK button

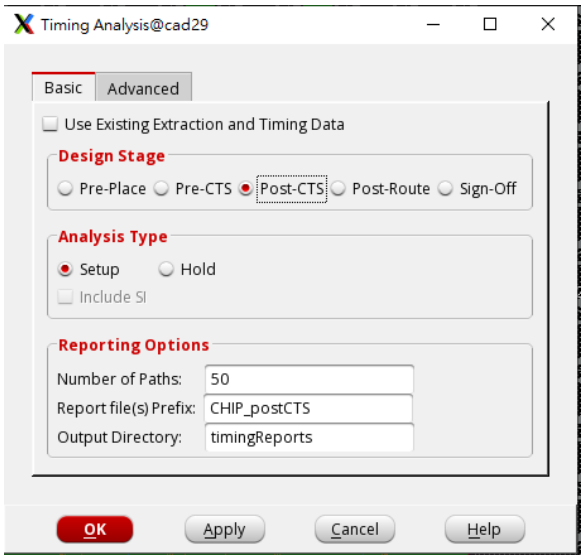


10. In-Place Optimization – After Clock Tree Synthesis

    10.1 Open ***Timing → Report Timing…***

    10.2 Perform First Encounter trial route to model the interconnection RC effects
    - Design Stage ◆ post-CTS

- Analysis Type ◆ Setup
- Click OK button



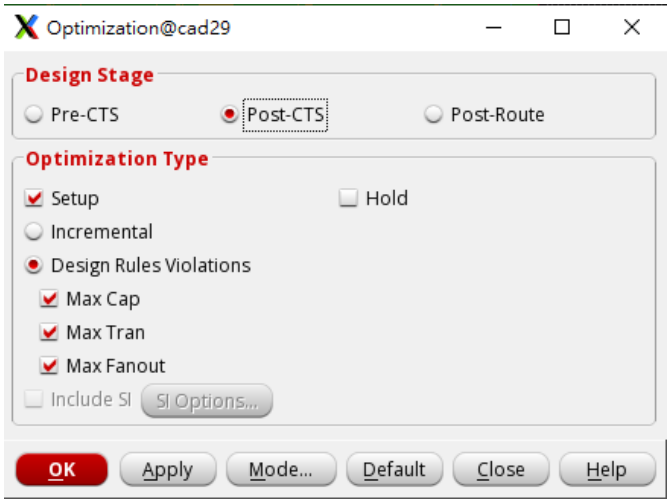

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -0.022  | -0.022  |  3.522  |  0.233  |   N/A   |  0.000  |
|           TNS (ns):| -0.022  | -0.022  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    1    |    1    |    0    |    0    |   N/A   |    0    |
|         All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |     17 (17)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

10.3 After CTS, further timing optimization is performed to meet timing constraints if there is negative timing slack or DRVs. Open ***ECO → Optimize Design…***

10.4 Perform post-CTS IPO

- Design Stage ◆ post-CTS
- Optimization Type
  - Setup
  - Design Rule Violations
  - Max Cap
  - Max Tran
  - Max Fanout

- Click OK button




```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.002  |  0.002  |  3.527  |  0.233  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |     17 (17)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

10.5 Verify if the hold time constraints are satisfied or not. Open ***Timing → Report Timing…***

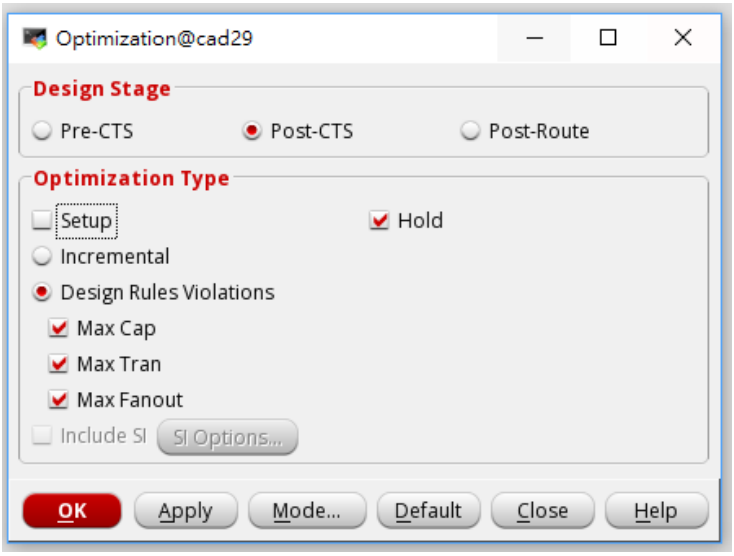
- Design Stage ◆ post-CTS
- Analysis Type ◆ Hold
- Click OK button

10.6 If hold time slack is negative, open ***ECO → Optimize Design…***

10.7 Perform post-CTS IPO

- Design Stage ◆ post-CTS
- Optimization Type
  - **Hold**
  - Design Rule Violations
  - Max Cap
  - Max Tran
  - Max Fanout

- Click OK button

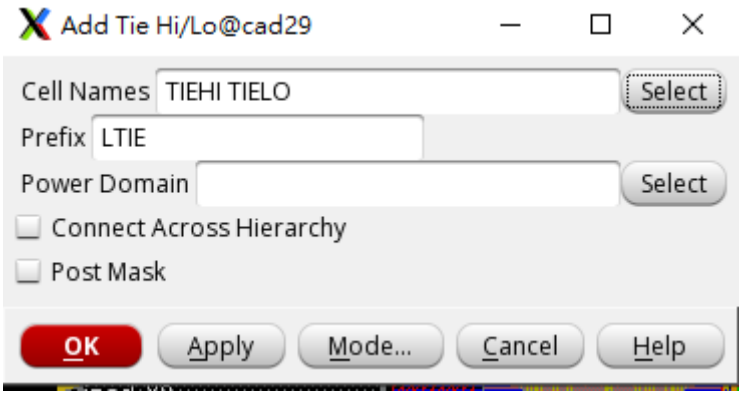


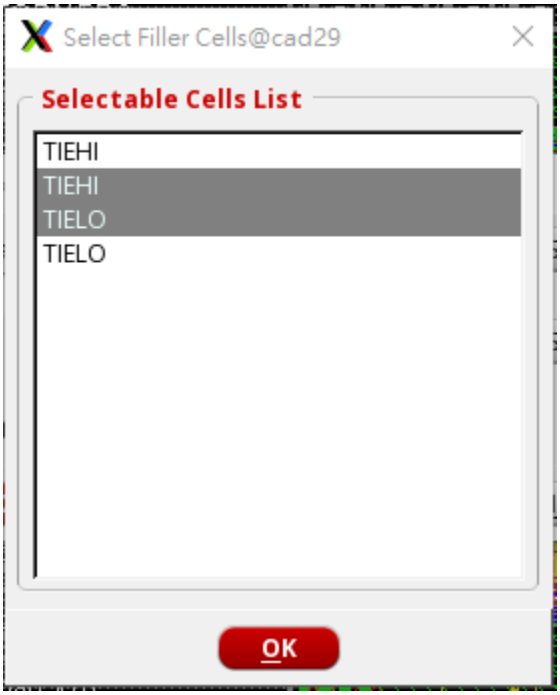
10.8 See timing reports in **timingReports** directory. For detail path report, see **CHIP_postCTS_reg2reg.tarpt.gz** (setup time check) and **CHIP_postCTS_reg2reg_hold.tarpt.gz** (hold time check).
DRV violations report files: ***.cap.gz** , ***.fanout.gz** , and ***.tran.gz**

11. Save file
    - Open ***File → Save Design…***
    - Choose ◆ Innovus
    - File Name: DBS/cts

Add Tie Hi/Lo Cells

1. Open ***Place → Tie Hi/Lo Cell → Add…***
2. Click Select button next to **Cell Names**
3. Choose one **TIEHI** and one **TIELO**, click OK button
4. Click OK button





Routing

1. Open ***Route*** → ***NanoRoute*** → ***Route…***
2. Nanoroute can prevent crosstalk effects and fix antenna rule violations, also it routes design to meet timing constraints
   2.1 Routing Phase
   - ◆ **Optimize Via** and ◆ **Optimize Wire**

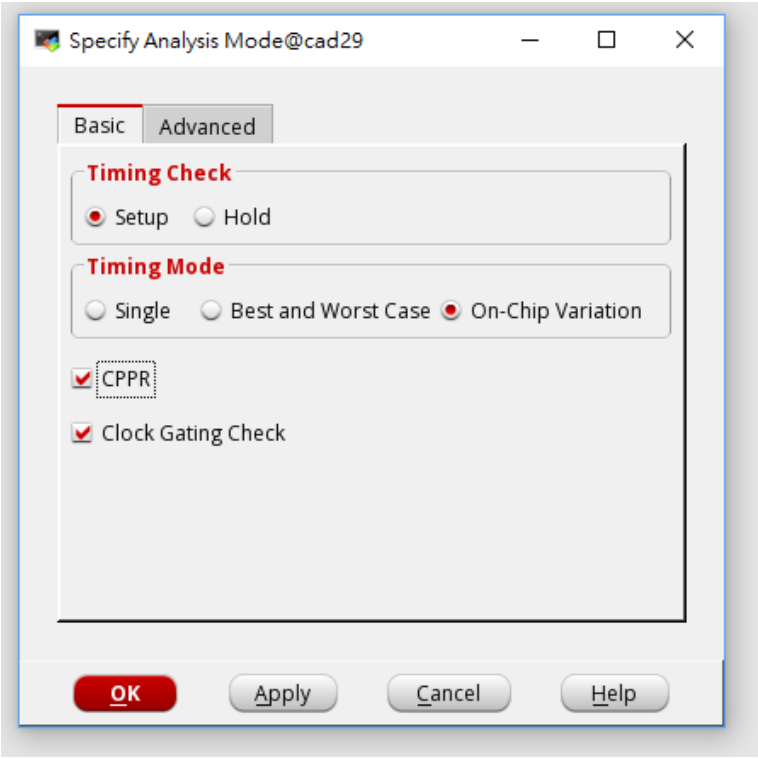
   2.2 Concurrent Routing Features
   - ◆ Fix Antenna
   - ◆ Insert Diodes — Diode Cell Name: **ANTENNA**
   - ◆ Timing Driven — Effort: **10**
   - ◆ SI Driven

   2.3 Click OK button

If Innovus crashes, cancel **Timing Driven**.

3. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/route
4. In-Place Optimization – After Detail Route

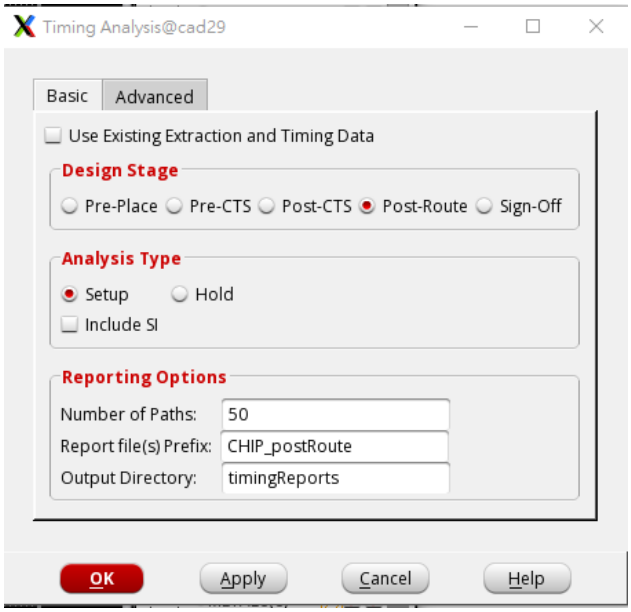
   4.1 Open ***Tools → set Mode → Specify Analysis Mode…***
   - Timing Mode ◆ On-Chip Variation
   - ◆ CPPR
   - Click OK button



4.2 Open ***Timing → Report Timing…***

4.3 Verify the setup time constraints and DRVs

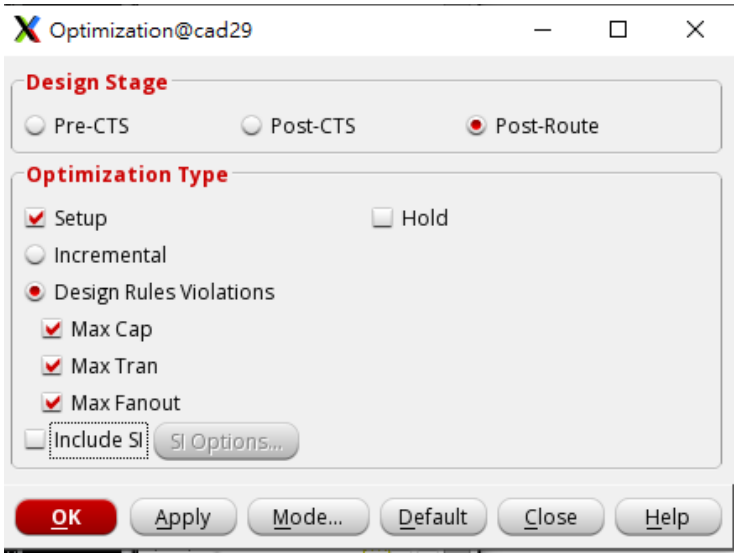
- Design Stage ◆ Post-Route
- Analysis Type ◆ Setup
- Click OK button



4.4 Further timing optimization is performed to meet timing constraints if there is negative timing slack or DRVs. Open ***ECO → Optimize Design…***

4.5 Perform post-Route IPO

- Design Stage ◆ post-Route
- Optimization Type
  - ◆ Setup
  - ◆ Design Rule Violations
  - ◆ Max Cap
  - ◆ Max Tran
  - ◆ Max Fanout
  - ◇ Include SI
- Click OK button



4.6 Verify if the hold time constraints are satisfied or not. Open ***Timing → Report Timing…***

- Design Stage ◆ Post-Route
- Analysis Type ◆ Hold
- Click OK button

4.7 If hold time slack is negative, open ***ECO → Optimize Design…***

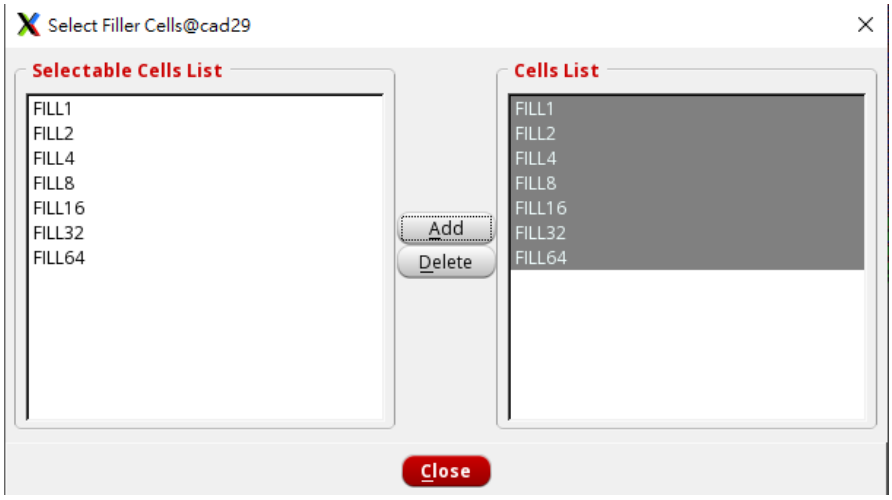
4.8 Perform post-Route IPO

- Design Stage ◆ Post-Route
- Optimization Type
  - ◆ **Hold**
  - ◆ Design Rule Violations
  - ◆ Max Cap
  - ◆ Max Tran
  - ◆ Max Fanout
  - ◇ Include SI
- Click OK button

5. Save file
   - ➢ Open ***File → Save Design…***
   - ➢ Choose ◆ Innovus
   - ➢ File Name: DBS/route

Add Core Filler Cells

1. Open ***Place → Physical Cell → Add Filler…***
2. Add core filler to improve electric effects of NWELL and PWELL:
   Cell Names:
   2.1 Click Select button
   2.2 Select all core filler cells
   2.3 Click Add button
   2.4 Click Close button
3. Click OK button




```
*INFO: Adding fillers to top-module.
*INFO:   Added 15 filler insts (cell FILL64 / prefix FILLER).
*INFO:   Added 48 filler insts (cell FILL32 / prefix FILLER).
*INFO:   Added 161 filler insts (cell FILL16 / prefix FILLER).
*INFO:   Added 516 filler insts (cell FILL8 / prefix FILLER).
*INFO:   Added 1400 filler insts (cell FILL4 / prefix FILLER).
*INFO:   Added 1515 filler insts (cell FILL2 / prefix FILLER).
*INFO:   Added 1593 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 5248 filler insts added - prefix FILLER (CPU: 0:00:00.6).
```

Verify Geometry & Connectivity & Process Antenna

1. Verify geometry
   1.1 innovus # > **verify_drc**
2. Verify connectivity
   2.1 Open ***Verify → Verify Connectivity …***
   2.2 Net Type ◆ **All**
   2.3 Nets ◆ **All**

If there are dangling wires, use hot key T (shift + t) to fix it.

2.4 Click OK button

3. Verify process antenna

3.1 Open ***Verify → Verify Process Antenna…***

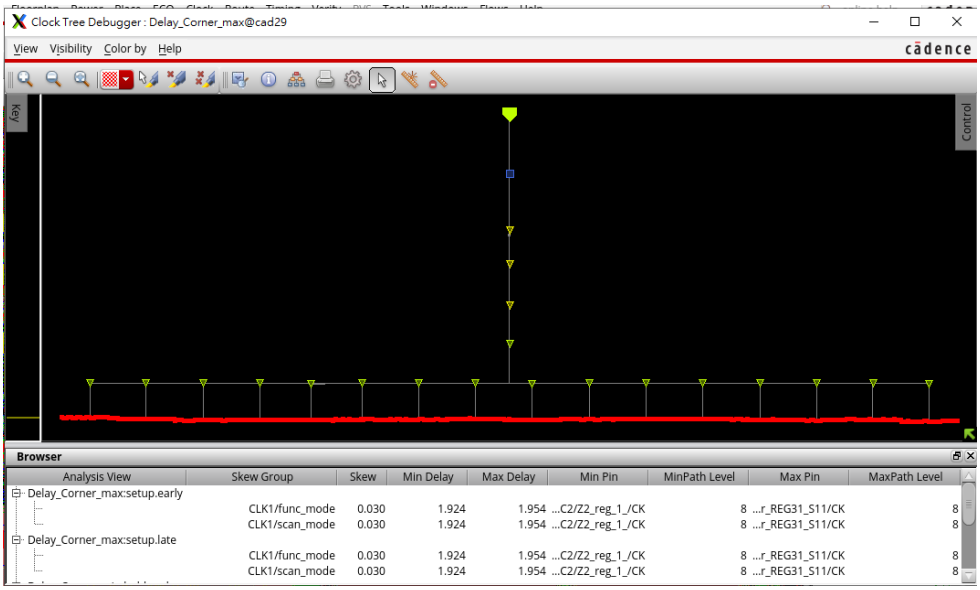
3.2 Click OK button

Output Data

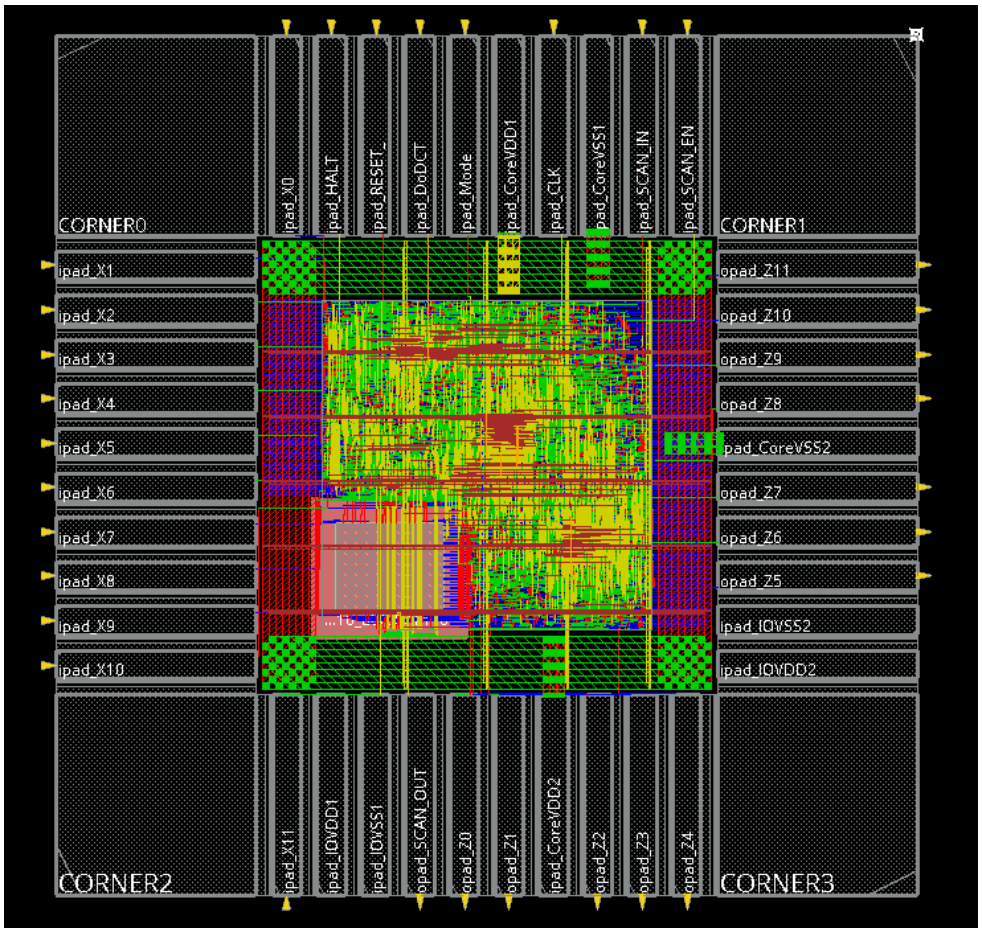
1. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/final
2. Open ***File → Save → Netlist…***
   - ⬧Include Intermediate Cell Definition
   - ⬧Include Leaf Cell Definition
   - Netlist File: CHIP_pr.v
   - Click OK button
3. In Innovus command prompt, execute the following commands:
   - innovus #> **setAnalysisMode -analysisType bcwc**
   - innovus #> **write_sdf -max_view av_func_mode_max **
     **-min_view av_func_mode_min **
     **-edges noedge **
     **-splitsetuphold **
     **-remashold **
     **-splitrecrem **
     **-min_period_edges none **
     CHIP.sdf
4. In Innovus command prompt, execute the following commands:
   - innovus #> **setStreamOutMode -specifyViaName default -SEvianames false -virtualConnection false -uniquifyCellNamesPrefix false -snapToMGrid false -textSize 1 -version 3**
   - innovus #> **streamOut CHIP.gds -mapFile library/streamOut.map **
     **-merge {library/gds/tsmc13gfsg_fram.gds **
     **library/gds/tpz013g3_v1.1.gds } **
     **-stripes 1 **
     **-units 1000 **
     -mode ALL

Checkpoints

1. Take a screenshot of the CCOpt clock tree debugger view.



2. Take a screenshot of the layout after routing (in physical view) and show post-route setup time and hold time analysis reports (ensure the slack of setup time and the slack of hold time >= 0)



```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.373  |  1.889  |  5.385  |  0.373  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |     17 (17)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 75.612%
Total number of glitch violations: 0
------------------------------------------------------------
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_min av_scan_mode_min

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.152  |  0.152  |  0.681  |  1.971  |  7.922  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |    0    |    0    |
|          All Paths:|  5436   |  3450   |  2636   |   13    |   12    |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 75.612%
------------------------------------------------------------
```

Submission

1. **Due Tuesday, Nov. 26, 19:00. No delay is allowed.**

2. Selected students need to take snapshots of the results shown in the previous section, record them into a PDF file, and submit it to NTU COOL.
   Title: CVSD_Lab7_studentID (E.g. CVSD_Lab7_r12943008.pdf)