Politecnico di Milano

Dipartimento di Elettronica, Informazione e Bioingegneria

prof. Fabrizio Ferrandi

Parallel Computing–I part–Thursday, January 12th, 2023

Polimi ID _____ _____

Surname _____ _____ **Name** _____

- This is a closed-book examination. You cannot use computers, phones, or laptops during the exam.
- Paper will be provided, but you should bring and use writing instruments that yield marks dark enough to be read easily. Erasable pens can be used.
- Total available time: 1h:30m.

Exercise 1 (4 points) _____

Exercise 2 (4 points) _____

Exercise 3 (4 points) _____

Exercise 3 (4 points) _____

Exercise n. 1

Answer the following questions about PRAM models and briefly explain (without an explanation, the answer will be considered invalid)

A. Describe the five phases followed during the PRAM computation. (1)

B. Write the general definition of the Speedup on p processors. (1)

C. Is the PRAM algorithm of the sum of a vector using concurrent reads? (1)

D. Write the definition of speedup according to Gustafson (definition, assumption, motivation). (1)

Exercise n. 2

Answer the following questions about different forms of parallel executions and briefly explain (without an explanation, the answer will be considered invalid).

A. Briefly describe how a SIMD execution may deal with conditional instructions. (1)

B. Is the latency of the memory operation changed by a multi-threading execution? True/False. (1)

C. Can a program with a small number of arithmetic operations and a large number of memory accesses be a problem for a multi-threaded processor? True/False. Why? (1)

D. Write a short description of "interleaved multi-threading processing." (1)

Exercise n. 3

Answer the following questions about programming models plus CUDA and briefly explain (without an explanation, the answer will be considered invalid).

A. CUDA __syncthreads() is a barrier, and it is waiting for all threads in execution. What is wrong or missing from the previous sentence? (1)

B. Briefly describe how CUDA threads-block are assigned to hardware. (1)

C. Please elaborate on why CUDA synchronization is required when applying the tiling technique. (2)

Exercise n. 4

Answer the following questions about memory and heterogeneous systems and briefly explain (without an explanation, the answer will be considered invalid).

A. Please briefly describe how DRAM bursting is working. (1)

B. Please explain what is meant by the "Corner Turning" technique. (1)

C. Please explain the difference between the Sequential consistency and the Total store ordering memory system. (1)

D. Please discuss the following statement: "Energy-optimized CPU consumes less than an ASIC." True/False? (1)