BROADCOM®

# BCM89820

# BroadR-Reach® Single-Port Automotive Ethernet Transceiver

## GENERAL DESCRIPTION

The Broadcom® BCM89820 is a 100 Mb/s automotive Ethernet transceiver integrated into a single monolithic CMOS chip. The device performs all the physical layer (PHY) functions for BroadR-Reach®-encoded Ethernet packets over single-pair unshielded twisted-pair copper wire, such as FlexRay. The BCM89820 is designed to exceed automotive specifications for noise cancellation and transmission jitter, providing consistent and reliable operation over the broadest range of existing single-pair twisted-pair automotive cable plants.

The BCM89820 is based on Broadcom's proven digital-signal processor technology, combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders, echo cancelers, and all other required support circuitry. The BCM89820 is designed to be fully compliant with the SGMII interface specification, allowing compatibility with industry-standard Ethernet media access controllers (MACs) and switch controllers.

BroadR-Reach enables the BCM89820 to auto-negotiate and link up with BroadR-Reach-compliant link partners.

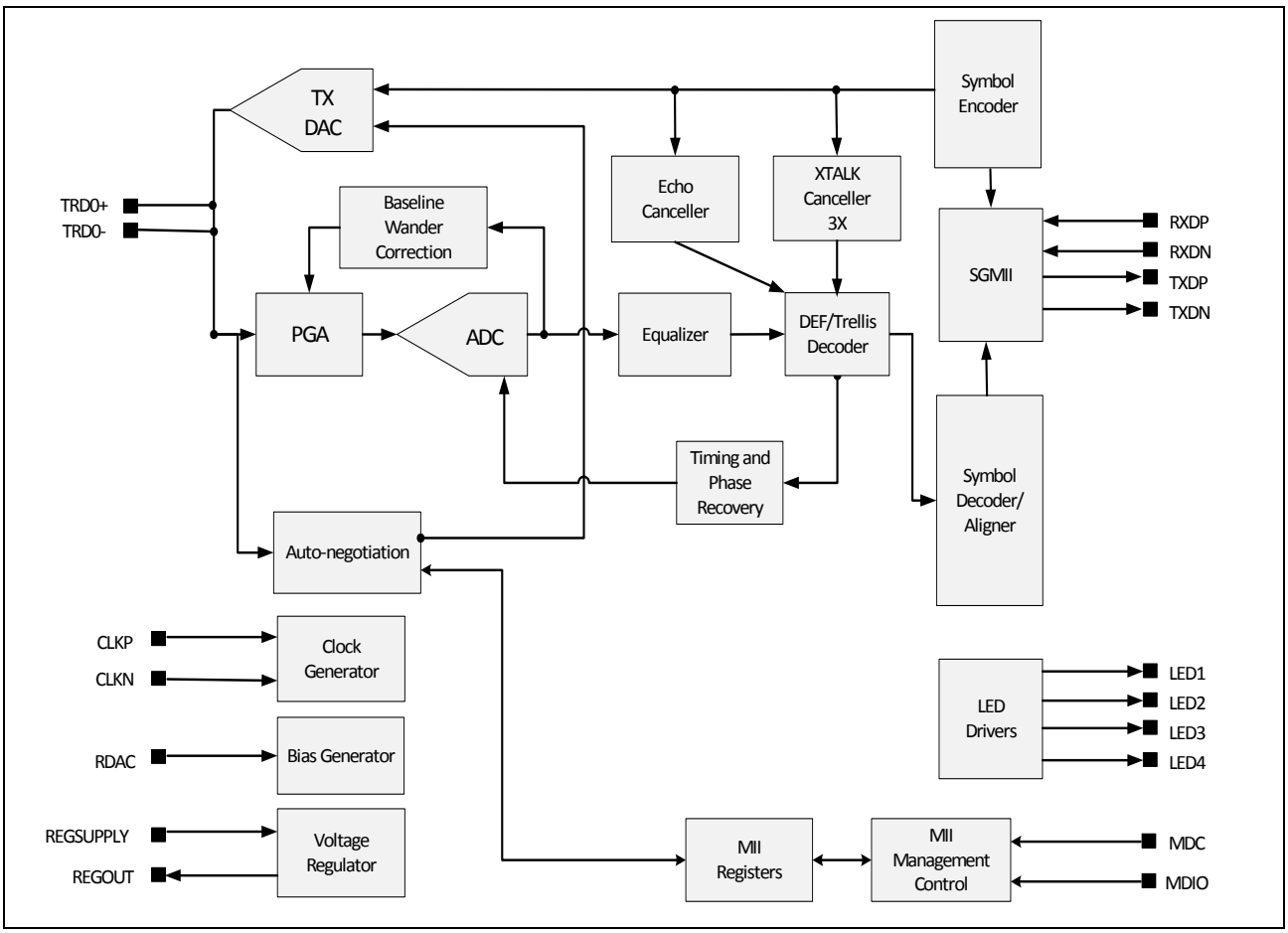
## FEATURES

- Single-chip integrated Ethernet transceiver
- Support for the following copper line interface: 100 Mb/s single-pair BroadR-Reach
- Integrated twisted-pair termination resistors
- Trace matched output impedance
- SGMII MAC interface
- Line loopback
- Low EMI emissions
  - High immunity
- Robust cable ESD (CESD) tolerance
- Support for jumbo packets up to 10 KB
- Advanced power management
- IEEE 1149.1 (JTAG) boundary scan
- Super Isolate mode
- 100-pin FBGA package
- Automotive Temperature Range: –40°C to +105°C ambient (Grade 2)

## APPLICATIONS

- Automotive Ethernet

**Figure 1: 100-ball FBGA Functional Block Diagram**



For a comprehensive list of changes to this document, see the Revision History.

# Table of Contents

# Section 1: Functional Description

## Overview

The Broadcom® BCM89820 is a single-chip BroadR-Reach® transceiver that performs all the physical layer (PHY) interface functions for Ethernet on unshielded twisted-pair (UTP) cabling. The BCM89820 connects to a MAC or switch controller through SGMII.

The device connects directly to the twisted-pair wiring of the network (through isolation transformers or common-mode choke using DC blocking capacitors) on the other side. It can be programmed to auto-negotiate its operating speed based on the capabilities of the link partner and the quality of the cabling plant.

The BCM89820 device adheres to Broadcom quality procedures and meets or exceeds the performance and functionality tested as part of our comprehensive product characterization, qualification, and functional verification process.

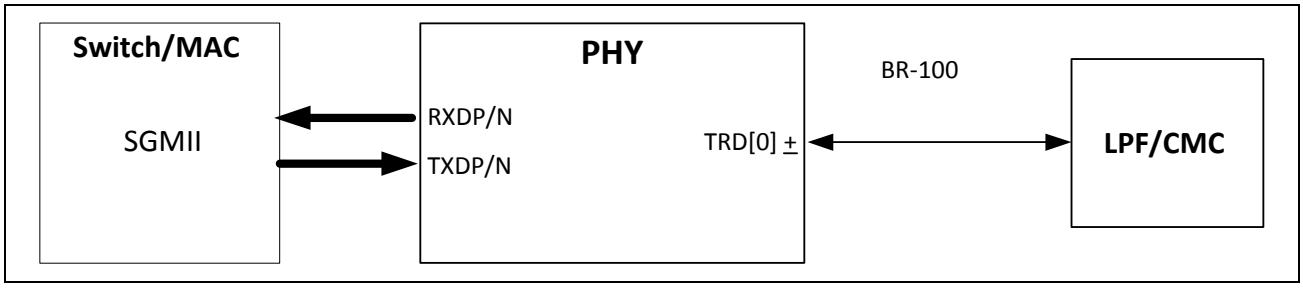
The BCM89820 is a single BroadR-Reach transceiver that performs all the PHY interface functions shown in the table below.

***Table 1: Supported Switch and MDI Interfaces***

| *Switch Interface* | *MDI* | *Protocol for MDI* | *Additional Features/Comments* |
|---|---|---|---|
| SGMII | Copper | BroadR-Reach BR-100 | 100 Mb/s operation using unshielded twisted-pair cable. |

A block diagram of a typical application is shown in the following figure.

**Figure 2: SGMII-to-BroadR-Reach 100 Mb/s Application**




## Serial Gigabit Media Independent Interface (SGMII)

The BCM89820 can communicate with Ethernet MACs that support the SGMII interface. The Serial GMII (SGMII) interface transmits serial data differentially at 1.25 Gbaud via the TXDP/TXDN pins and receives serial data differentially via the RXDP/RXDN pins, which includes an on-chip 100Ω differential termination resistor. Since the BCM89820 provides clock recovery on the SGMII input data, an input clock is not required.

# BroadR-Reach

The BCM89820 features the BroadR-Reach protocol on the MDI pins. BroadR-Reach enables the device to link up with BroadR-Reach-compliant link partners. BroadR-Reach mode operates only at full duplex.

The BroadR-Reach interface is configured by forcing link parameters at both ends of the link. Control of BroadR-Reach is achieved through a new set of registers, called LRE registers, that are overlaid on addresses 00–0Fh as described in “BroadR-Reach LRE Register Descriptions”.

# Management Interface

The BCM89820 contains a large set of management registers. The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3 Clause 22 and also support MDC clock rates up to 12.5 MHz. The management interface supports the defined Status and Control registers of IEEE 802.3, Clauses 22, 28, 37, and 40. In addition, the BCM89820 contains multipurpose registers for extended software control.

# Encoder

In BroadR-Reach mode, the BCM89820 simultaneously transmits and receives continuous data streams on one pair of the cable. PAM3 encoding is used for one-pair applications.

# Link Monitor

Following auto-negotiation or forced-mode link in BroadR-Reach, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver’s timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been stable for at least 1.8 µs, the link monitor enters the link-pass state and the transmission and reception of data packets are enabled. When the local receiver status is unstable for more than 1406 ms, the link monitor enters the link-fail state, and the transmission and reception of data packets are then disabled.

# Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM89820 achieves optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than $1 \times 10^{-12}$ for transmissions.

The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

# Echo Canceler

Due to the bidirectional nature of the channel in BroadR-Reach mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

# Analog-to-Digital Converter

Each receive channel has its own 66 MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

# Clock Recovery/Generator

In BroadR-Reach modes, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

# Baseline Wander Correction

BroadR-Reach data streams are not always DC-balanced. Because the receive signal must pass through a transformer or DC blocking capacitors, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM89820 automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

# Multimode Transmit Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM3 coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses voltage-driven output with internal terminations and hence does not require external components or magnetic supply for operation, thus reducing system complexity for routing and bill of materials.

# Forced BroadR-Reach Mode

To configure the PHY into forced one-pair 100 Mb/s BroadR-Reach mode, program the two PHYs in the link segment to set LRE register 00h to:

- 0200h for 100 Mb/s one-pair BroadR-Reach slave
- 0208h for 100 Mb/s one-pair BroadR-Reach master

Each BroadR-Reach link segment requires one link partner to be slave and one BroadR-Reach link partner to be master.

# Energy Detect

The energy-detect feature provides an output signal (Energy Detect) indicating the presence or absence of energy being received on the copper analog input pins of the chip. Additionally, the copper energy-detection status can be monitored from register 1Ch, shadow 11111, bit 5. See “Operational Description” for details.

# Power-Down Modes

Two low-power modes are supported in the BCM89820:

- Ultralow power-down mode (IDDQ)
- Standby power-down mode

# Jumbo Packets

In copper mode, packets up to 10 KB in length can be supported with the following register writes:

- Register 18h, shadow 000, bit 14 = 1 (default = 0)
- Register 10h, bit 0 = 1 (default = 0)

# Section 2: Hardware Signal Descriptions

The following conventions are used in Table 2:

- I: Input
- O: Output
- I/O: Bidirectional
- OD: Open-drain output
- OT: Tristateable signal
- B: Bias
- PU: Internal pull-up
- PD: Internal pull-down
- SOR: Sample on reset
- CS: Continuously sampled
- ST: Schmitt trigger

The following conventions are used to express the I/O types in Table 2. The I/O pin type is useful in referencing the DC pin characteristics contained in Section 7: “Electrical Characteristics”:

- A: Analog pin type
- D: Digital pin type
- DNC: Do not connect
- G: RGMII pin type
- GND: General ground
- PECL: Positive Emitter Coupled Logic
- S: SerDes pin type
- XT: Crystal inputs/outputs pin type

**Note:** Pin groups that are not found on a certain package are represented by an en dash (–)**.**

**Note:** Refer to the *BCM89820 Design Guide Application Note* for additional information regarding the configurations and bypassing of the power supply pins.

***Table 2: Hardware Signal Descriptions***

| *100-Pin FBGA* | *Label* | *I/O Type* | *Description* |
|---|---|---|---|
| Media Connections | | | |
| K3<br>K4 | TRD[0]± | A | Transmit/Receive Pairs<br>In BroadR-Reach mode, differential data from copper media is transmitted and received on the TRD± signal pair. There are 50Ω internal termination on each pin, so no external termination is required. |
| 3 | TVCOI | O | Copper PLL Test Clock Output |

***Table 2: Hardware Signal Descriptions (Cont.)***

| 100-Pin FBGA | Label | I/O Type | Description |
|---|---|---|---|
| SerDes/SGMII | | | |
| A2<br>A3 | TXDP<br>TXDN | O<br>S | SGMII Data Output<br>Differential serial data output. |
| A1<br>B1 | RXDP<br>RXDN | I<br>S | SGMII Data Input<br>Differential serial data input when BCM89820 is in SGMII mode. These pins have a 100Ω differential termination resistor on-chip. |
| Clocks | | | |
| D1 | CLK125 | O,G | MAC Reference Clock<br>Continuous 125 MHz output generated off the PLL (phase locked to the CLKP/CLKN input). This clock output remains active and stable during both hardware and software reset. This clock is powered by OVDD power. |
| F1<br>G1 | CLKP<br>CLKN | XT<br>XT | 25 MHz Clock Reference Pins for Entire Device.<br>Can be configured to either differential input or XTAL (crystal oscillator) type. |
| J3 | TVCOI | O | Copper PLL Test Clock Output. |
| Reference Clock Selection | | | |
| D9<br>C4 | REFCLK_SEL[0]<br>REFCLK_SEL[1] | $I_{PD}$<br>$I_{PD}$ | Clock Reference Selector<br>Allows user to select the type of input clock reference signal.<br>REFCLK_SEL[1]: REFCLK_SEL[0]: Clock Modes:<br>0 0 Selects differential reference clock inputs (CLKP, CLKN).<br>0 1 Selects single-ended CMOS.<br>1 0 Selects XTAL input.<br>1 1 Not allowed. |
| F7 | CLKSEL_125 | $I_{PD}$ | 125 MHz Input Reference Clock Enable<br>Allows user to supply a 125 MHz clock signal on pins CLKP/CLKN (F1/G1) instead of a 25 MHz clock.<br>0: 25 MHz input reference clock on pins CLKP/CLKN<br>1: 125 MHz input reference clock on pins CLKP/CLKN |
| MDIO | | | |
| B3 | MDC | $I_{PD}$, ST | Management Data Clock<br>The MDC clock input must be provided to allow MII management functions. When configured as BSC_SLAVE, this pin becomes the SCL pin of the BSC interface. |
| B2 | MDIO | $I/O_{PU}$, D, ST | Management Data I/O<br>This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC. When configured as BSC_SLAVE, this pin becomes the SDA pin of the BSC interface. |

*Table 2: Hardware Signal Descriptions (Cont.)*

| 100-Pin FBGA | Label | I/O Type | Description |
|---|---|---|---|
| Mode | | | |
| B5<br>G9<br>H8<br>H9<br>H7 | PHYA[0]<br>PHYA[1]<br>PHYA[2]<br>PHYA[3]<br>PHYA[4] | $I_{PD}$, SOR | PHY Address Selects<br>Active high. Sampled on reset. The PHY address selects the MII management PHY address. The device goes into isolate mode when the PHY address is strapped to 00000. To get out of isolate mode, write register 00h, bit 10 = 0. |
| A8<br>B7 | INTERF_SEL[0]<br>INTERF_SEL[1] | $I_{PD}$ | Interface Mode Selector.<br>Allows configuration of device to support SGMII to copper mode.<br>INTERF_SEL[1] INTERF_SEL[0] Interface Modes<br>0 0 Reserved<br>0 1 Reserved<br>1 0 SGMII-copper<br>1 1 Reserved |
| C2 | $\overline{\text{RESET}}$ | $I_{PU}$, CS, ST | $\overline{\text{RESET}}$<br>Active low, Schmitt Trigger Input. The BCM89820 requires a hardware $\overline{\text{RESET}}$ prior to normal operation. Configuration settings obtained via hardware strap option pins are latched on the rising edge of $\overline{\text{RESET}}$. |
| C3 | LED1 | $I_{PU}$, O | LED1/ANEN<br>This is a dual function pin.<br>Output polarity is determined at reset. See "Dual-Input Configuration/LED Output Function" for details. This pin can be programmed to alternate modes. See "General-Purpose LED Programmability" for details.<br>Copper Auto-Negotiation Enable Select. Active high. Sampled on reset. When this pin is high, copper auto-negotiation is enabled. When low, copper auto-negotiation is disabled. After reset, auto-negotiation configuration is under software control. |
| B4 | LED2 | $I_{PU}$, O | LED2/Full Duplex<br>This is a dual function pin.<br>Output polarity is determined at reset. See "Dual-Input Configuration/LED Output Function" for details. This pin can be programmed to alternate modes. See "General-Purpose LED Programmability" for details.<br>Full-duplex Select. Active high. Sampled on reset. When this pin is high, full-duplex is enabled. When low, full-duplex is disabled. After reset, full-duplex configuration is under software control. |
| E4 | LED3 | $I_{PU}$, O | LED3/LED4 |
| C5 | LED4 | $I_{PU}$, O, OD | Output polarity is determined at reset. See "Dual-Input Configuration/LED Output Function" for details.<br>Programmed to alternate modes. See "General-Purpose LED Programmability" for details.<br>If this pin is programmed to output interrupts, it becomes an open-drain output. |

***Table 2: Hardware Signal Descriptions (Cont.)***

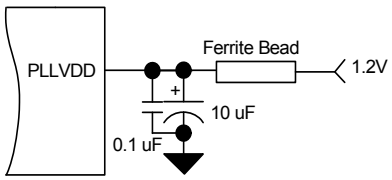
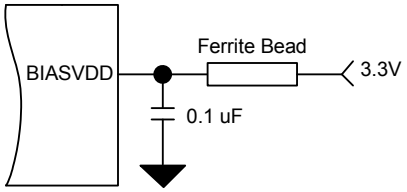
| *100-Pin FBGA* | *Label* | *I/O Type* | *Description* |
|---|---|---|---|
| G8 | LOWPWR | $I_{PD}$ CS | Low Power<br>Active high. If this pin is high, the device enters ultralow power-down mode (IDDQ-LP). This mode can also be entered through software by writing to register 1C, shadow 01100, bit 0 =1. To exit, set LOWPWR = 0 and issue a RESET. See "Ultralow Power-Down Mode". |
| Test | | | |
| D4 | TCK | $I_{PU}$ | Test Clock<br>JTAG serial clock. |
| A4 | TDI | $I_{PU}$ | Test Data Input<br>JTAG serial data input. |
| A5 | TDO | O, D | Test Data Output<br>JTAG serial data output. |
| A9 | TMS | $I_{PU}$ | Test Mode Select<br>JTAG mode select input. |
| H10 | $\overline{\text{TRST}}$ | $I_{PU}$ CS | JTAG Reset<br>Active low. Resets the JTAG controller. This signal must be pulled low during normal operation. |
| G4<br>F4 | TEST2<br>TEST3 | $I_{PD}$ CS | Test Mode Enables<br>Active high. These pins must always be pulled low during normal operation. These pins are used by Broadcom for test purposes only.<br>When TEST3/TEST2 = 01, the device enters a test mode where JTAG operations can be executed. |
| RDAC Bias | | | |
| J1 | RDAC | B | DAC Bias Resistor<br>Adjusts the reference current of the transmitter digital to analog converter. A 1.24 kΩ ±1% resistor is connected between the RDAC pin and GND. |
| Power | | | |
| D8, E9, D5, E1 | OVDD | PWR | 2.5V or 3.3V for the digital I/O pads. When 2.5V is selected, $\overline{\text{RESET}}$, MDIO, and LED pins are not 3.3V tolerant. |
| D7, E7, F5, G5 | DVDD | PWR | 1.2V power for digital core. |
| J5, J6 | AVDDL | PWR | 1.2V power for analog core. |
| J4, J10 | AVDD | PWR | 3.3V power for analog core. |
| K2 | PLLVDD | PWR | 1.2V PLL Supply to the AFE PLL<br>  |

***Table 2: Hardware Signal Descriptions (Cont.)***

| *100-Pin FBGA* | *Label* | *I/O Type* | *Description* |
|---|---|---|---|
| K1 | BIASVDD | PWR | Bias VDD<br>+3.3V. Normally filtered with a low resistance ferrite bead such as a Murata BLM11A601S or equivalent, as well as a 0.1 µF capacitor.<br>  <br> |
| F3 | PLLAVDD33 | – | 3.3V power supply to the reference clock (CLKP/CLKN pads). |
| H1 | TXVDD | – | 1.2V power supply to the transmitter and receiver of the SerDes (SGMII/ 1000BASE-X). |
| F2, G2 | SPLLVDD | – | 1.2V power supply to the SerDes PLL. |
| G3 | PLLAVSS | – | Ground for the SerDes PLL. |
| C1, H2 | TXVSS | – | Transmitter and receiver ground for the SerDes. |
| No Connect | | | |
| A6, A7, B6, B8, B9, C6, D3, D6, D10, E2, E10, F8, F9, F10, G10, H3, J2, K5, K6, K7, K8, K9, K10 | DNC | DNC | Do Not Connect Pins<br>Do not connect these pins to any other pin, and do not connect them together. |
| B10, C9, C10, D2, E3, E5, E6, E8, F6, G6, G7, H4, H5, H6, J7, J8, J9 | GND | GND | General Ground |

# Section 3: Pinout

**Figure 3: 100-Pin FBGA Ball Diagram, Top View**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | RXDP | TXDP | TXDN | TDI | TDO | DNC | DNC | INTERF_ SEL[0] | TMS | DNC | A |
| B | RXDN | MDIO | MDC | LED2 | PHYA[0] | DNC | INTERF_ SEL[1] | DNC | DNC | GND | B |
| C | TXVSS | $\overline{\text{RESET}}$ | LED1 | REFCLK _SEL[1] | LED4 | DNC | SCL | SDA | GND | GND | C |
| D | CLK125 | GND | REGOUT | TCK | OVDD | DNC | DVDD | OVDD | REFCLK _SEL[0] | DNC | D |
| E | OVDD | REGSUPPLY | GND | LED3 | GND | GND | DVDD | GND | OVDD | DNC | E |
| F | CLKP | SPLLVDD | PLLAVDD33 | TEST3 | DVDD | GND | CLKSEL_125 | DNC | DNC | DNC | F |
| G | CLKN | SPLLVDD | PLLAVSS | TEST2 | DVDD | GND | GND | LOWPWR | PHYA[1] | DNC | G |
| H | TXVDD | TXVSS | DNC | GND | GND | GND | PHYA[4] | PHYA[2] | PHYA[3] | $\overline{\text{TRST}}$ | H |
| J | RDAC | DNC | TVCOI | AVDD | AVDDL | AVDDL | GND | GND | GND | AVDD | J |
| K | BIASVDD | PLLVDD | TRD[0]+ | TRD[0]- | DNC | DNC | DNC | DNC | DNC | DNC | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

# Section 4: Operational Description

## Reset

The BCM89820 provides a hardware reset pin, $\overline{\text{RESET}}$, which resets all internal nodes to a known state. The reset pin must be asserted for at least 2.0 µs. Hardware reset should always be applied to the BCM89820 after power-up.

The BCM89820 also has a software reset capability. To enable the software reset, 1 must be written to bit 15 of the MII Control register (address 00h). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit.

Mode pins that are labeled sample on reset (SOR) are latched during hardware reset. Similarly, software resets also latch new values for some SOR mode pins, except for those pins that contain LED functions. SOR mode pins that contain LED functions during normal operation retain the values latched during the previous hardware reset.

During reset, the PHY output pins connected to MAC are driven low.

## PHY Address

The BCM89820 allows a unique PHY address for MII management. The address is set through the logic value of the PHYA[0] and TEST3/TEST2 pins, which are latched during reset. The address is set through the logic value of the PHYA[4:0] pins, which are latched during reset. The PHY checks each MII management read or write command on its MDIO pin and performs the operation only if the address in the command matches the

latched PHY address stored in the device.

Setting the PHY address to 00h puts the device into isolate mode during and after reset. To return to normal operation, write 0 to bit 10 of the MII Control register (address 00h).

## Standby Power-Down Mode

The BCM89820 can be placed into standby power-down mode using software commands. In this mode, all PHY functions, except the serial management interface and CLK125 output, are disabled. There are three ways to exit this mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software RESET bit 15, MII Control Register (address 00h).
- Assert the hardware $\overline{\text{RESET}}$ pin.

Reads or writes to any MII register other than MII Control register (address 00h) while the device is in the standby power-down mode may cause unpredictable results. Upon exiting standby power-down mode, the BCM89820 remains in an internal reset state for 40 µs and then resumes normal operation.

The DLL can be powered down by setting register 1Ch, shadow 00101, bit 1 = 0. These writes should be performed before enabling the standby power-down mode.

## Ultralow Power-Down Mode

The BCM89820 can be placed into ultralow power-down mode (IDDQ), consuming the lowest power possible while voltage is being supplied to the device.

Use the following method to enter and exit the ultralow power-down mode:

- To enter ultralow power-down mode, write register 1Ch, shadow 01100, bit 0 = 1.
- To exit ultralow power-down mode, issue a hardware reset by forcing the $\overline{\text{RESET}}$ pin low. See Table 57 for reset timing information.

## Internal Loopback Mode

An internal loopback mode is available on the BCM89820, where all packets sent through the SGMII TXD pins are internally looped back to the SGMII RXDP/N pins. The BCM89820 can be placed into internal loopback mode by setting bit 14 of the SerDes MII Control register.

Loopback mode can be cleared by writing 0 to bit 14 of the SerDes MII Control register or by resetting the chip.

## Line-Side (Remote) Loopback Mode

Line-side loopback mode allows the testing of the copper MDI interface from the link partner. This mode is enabled by setting bit 15 of the "Register 18h (Shadow 100): Miscellaneous Test Register". The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the MAC interface. The MAC interface can be tristated by setting bit 11 of the "Register 18h (Shadow 100): Miscellaneous Test Register".

# External Loopback Mode

External Loopback mode allows in-circuit testing of the BCM89820. External Loopback can be performed without a jumper block. External loopback without the jumper block tests the BCM89820's transmit and receive circuitry.

***Table 3: BroadR-Reach External Loopback without External Loopback Plug***

| *Register Writes* | *Comments* |
|---|---|
| Write 0x0208 to MII register 0x0 | Put PHY into 100 Mb/s master mode. |
| Write 0x8400 to MII register 0x18 | Enable external loopback mode. |

# Master/Slave Configuration

In BroadR-Reach mode, the BCM89820 and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave, as defined by IEEE 802.3ab. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. However, if both partners are configured with identical repeater/DTE settings, each generates an 11-bit random seed. The partner with the higher seed is configured as the master. If the local PHY and the link partner happen to generate the same random seed, auto-negotiation is restarted.

The link can be forced by writing the appropriate values in LRE Register 00h. However, if both ends of the link attempt to force the same manual configuration (both master or both slave) the PHY will not link up.

# SGMII Interface

The SGMII interface uses an onboard SerDes module to convey frame data information between the BCM89820 transceiver and an Ethernet MAC. Each pair of data signals operates at 1.25 Gbaud, and is realized as a differential pair because of the speed of operation, providing signal integrity while minimizing system noise. The SGMII signals use voltage levels similar to low voltage differential signaling (LVDS). The data are DC-balanced; therefore, implementations that meet the AC parameters, but fail to meet the DC voltage requirements, can be AC-coupled.

The 1.25 Gbaud transfer rate of the SGMII is greater than required for the BCM89820 transceiver operating at 100 Mb/s. When these situations occur, the BCM89820 elongates the frame by replicating each frame byte: 10 times for 100 Mb/s. This frame elongation takes place above the IEEE 802.3z PCS layer, making the start frame delimiter appear only once per frame.

In its receive path, the BCM89820 transceiver receives the signals from the copper interface through its PCS layer. The device serializes the PCS data to create a TXDP/TXDN signal pair and sends it to the MAC at 1.25 Gb/s.

In its transmit path, the BCM89820 deserializes the RXDP/RXDN pins to create parallel data. The device passes data through the PCS state machine to determine the appropriate transmit signals. The decoded transmit signals are passed through the transmit block and are output to the BCM89820 copper port at the predetermined speed.

# Control Information Exchange Between Links

The BCM89820 passes control information to the MAC to notify it of the change of the copper link status. The SGMII interface uses the auto-negotiation block to pass control information. If the device detects a copper link change, it restarts its SGMII auto-negotiation process, sending out the updated control information. The receive block in the MAC receives and decodes control information and transmits an acknowledgment of the link status change back to the device also using the auto-negotiation mechanism. Upon receiving the acknowledgment from the MAC, the BCM89820 finishes the auto-negotiation process and returns to the normal data mode. The following table summarizes the SGMII interface pins.

***Table 4: SGMII Interface Pins***

| *SGMII Signal Pin* | *Description* |
|---|---|
| RXDP/RXDN | SGMII differential data input pin with internal 100Ω termination (transmit path) |
| TXDP/TXDN | SGMII differential data output pin (receive path) |

# Signal Quality Indicator

The BCM89820 also provides a method for determining the quality of the link. This signal quality indicator (SQI) can be a valuable diagnostic tool. The final calculation results in a value ranging from 0 to 5 bars. An SQI indicator of one or higher allows for operation within the BroadR-Reach specification. At an SQI level of zero, errors are possible due to a lack of SNR margin. SQI is related to the SNR margin of a link and is only applicable when the link is up, with each step representing approximately 2 dB difference of margin. SQI is an indication of the quality of the link and not a measurement of the quality of the channel itself.

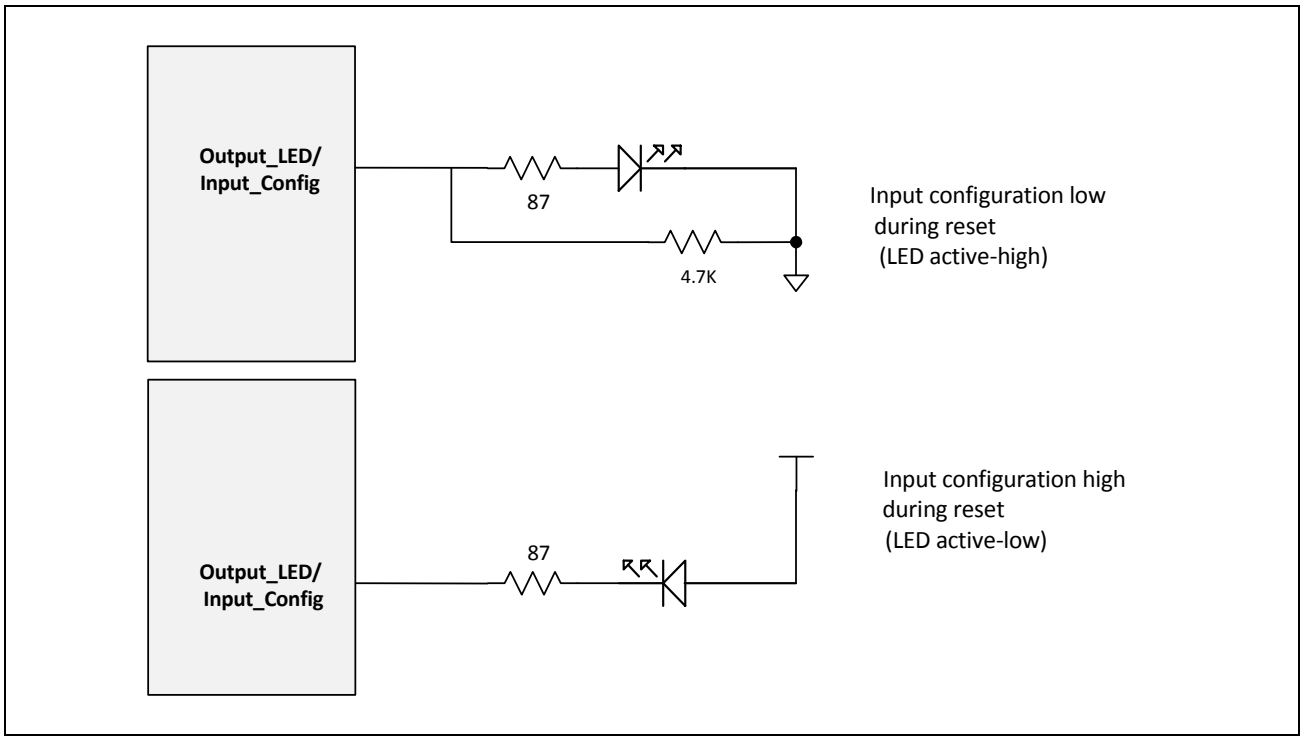
The algorithm is as follows:

1. Set up register access:
   Set bit 11 = 1 in register 18h
   Write 0002h to register 17h
2. Read register 15h
3. Convert resulting value to decimal (Q)
4. Convert Q to a logarithmic value D:
   $D = 10 \times \log_{10}(Q/32768)$
5. Average over 100 readings:
   A = avg(D[0:99])
6. Subtract baseline value:
   M = –20.0 – A
7. Calculate SQI according to the following ranges:
   - SQI = 0 when M is smaller than 0.0
   - SQI = 1 when M is between 0.0 and 2.0
   - SQI = 2 when M is between 2.0 and 4.0
   - SQI = 3 when M is between 4.0 and 6.0
   - SQI = 4 when M is between 6.0 and 8.0
   - SQI = 5 when M is greater than 8.0

# Dual-Input Configuration/LED Output Function

All four LEDs pins have secondary functions. These pins serve as an input pin during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active-low. The user must first decide, based on the individual application, the values of the input configuration pin shown in Table 14 to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or active-high LED output (see the figure below).

**Figure 4: LED Circuit for Dual-Input Configuration/LED Output Pins**



# General-Purpose LED Programmability

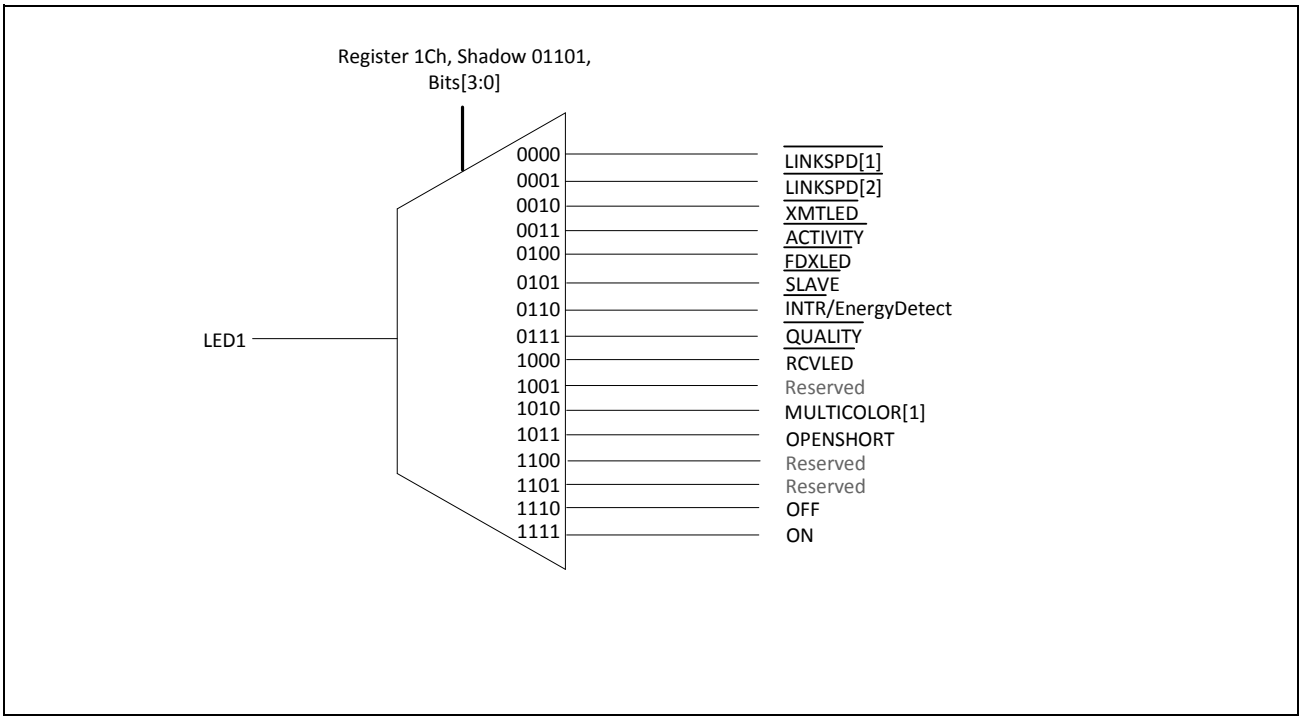
The BCM89820 has four LED pins that can be programmed to one of many useful LED functions. Four 4-bit control register words are provided to allow the user to select the LED function for each of the pins. These control words are located in register 1Ch, shadow 01101 and shadow 01110. The following table details each of the four programmable LEDs, their corresponding register bits, and default settings.

***Table 5: Programmable LEDs (100-ball FBGA)***

| *100-ball FBGA* | *Pin Name* | *Register Bits* | *Default Value* | *Default Function* |
|---|---|---|---|---|
| 45 | LED1 | Register 1C, Shadow 01101, Bits[3:0] | 0000 | LINKSPD[1] |
| 44 | LED2 | Register 1C, Shadow 01101, Bits[7:4] | 0001 | LINKSPD[2] |
| 43 | LED3 | Register 1C, Shadow 01110, Bits[3:0] | 0011 | ACTIVITY |
| 42 | LED4 | Register 1C, Shadow 01110, Bits[7:4] | 0110 | $\overline{\text{INTR}}$ |

Each of the output functions exists as an internal device signal that is multiplexed to a given general-purpose LED pin when the corresponding register bits are written with the appropriate register value. The figure below is a graphical representation of the multiplexer functionality of the programmable LED and uses LED1/ANEN as an example.

**Figure 5: Programmable LED Multiplexer**



When LEDs are programmed to $\overline{\text{LINKSPD[1]}}$ and $\overline{\text{LINKSPD[2]}}$ function, these indicate the link and speed status of the copper interface as shown in the following table.

***Table 6: LINKSPD[2:1] LED Function (Default-LED Mode/Non-LOM-LED Mode)***

| *LINKSPD[2]* | *$\overline{\text{LINKSPD[1]}}$* | *Link/Speed* |
|---|---|---|
| 0 | 0 | N/A |
| 0 | 1 | Linked @ 100 Mb/s BroadR-Reach |
| 1 | 0 | N/A |
| 1 | 1 | No link |

## Normal Operation Mode

When TEST3/TEST2 = 00, the device is in normal operational mode. When TEST3/TEST2 = 01, the device enters a test mode where JTAG operations can be executed. All other combinations are used by Broadcom for test purposes.

## PHY Address

The BCM89820 allows a unique PHY address for MII management. The address is set through the logic value of the PHYA[0] and TEST3/TEST2 pins, which are latched during reset. The address is set through the logic value of the PHYA[4:0] pins, which are latched during reset. The PHY checks each MII management read or write command on its MDIO pin and performs the operation only if the address in the command matches the latched PHY address stored in the device.

# Interrupt Function

The BCM89820 can be programmed to provide an interrupt output based on changes in the PHY status. Each individual interrupt condition is represented by a read-only bit in the "Interrupt Status Register (Address 1Ah)". Interrupts can be individually masked by setting or clearing bits in the interrupt mask register, in "Interrupt Mask Register (Address 1Bh)". When an unmasked interrupt condition occurs, programmed LED pins to $\overline{\text{INTR}}$ function are driven low until the interrupt is cleared. Most interrupts are automatically cleared by reading the Interrupt Status register.

The interrupt function can be globally disabled by setting the interrupt disable bit, register 10h, bit 12. The $\overline{\text{INTR}}$/EnergyDetect pin can be changed to indicate an energy-detect function by setting register 1Ch, shadow 00100, bit 1= 1.

# LED Modes

Many additional LED functions and modes are supported by the BCM89820. Table 7 describes many of these modes in detail. The LEDs can be forced on by setting bit 4 of register 10h. This forces all LEDs on continuously. Similarly, the LEDs can be forced off continuously by setting bit 3 of register 10h. This overrides all other LED modes except the force LEDs ON mode. Any LED output pin programmed to be in the INTR mode will be open-drain, in order to allow multiple devices to be connected in a wire-OR fashion. For all other LED modes, LED output pins are continuously driven.

Table 7 describes the different modes in which each individual pin can be programmed. For each pin, the modes are listed in order of priority. For example, when the receive LED is programmed to one of the link-utilization modes, the register bit enabling activity/link LED mode is not relevant. The last mode listed for each pin is the default mode.

## Multicolor LED

The MULTICOLOR mode uses two programmable LED output pins to control one single LED unit that is capable of producing three different colors: green, amber red. The multicolor LED mode is enabled by writing value B4AAh to "LED Selector 1 Register (Address 1Ch, Shadow 01101)". After this register write, the multicolor LED signals appear on LED1 and LED2. Alternatively, the multicolor LED can be output on LED3 and LED4 by writing B8AAh to "LED Selector 2 Register (Address 1Ch, Shadow 01110)". The subfunction and other parameters can be selected by setting control bits in "Expansion Register 05h: Multicolor LED Flash Rate Controls", and "Expansion Register 06h: Multicolor LED Programmable Blink Controls".

## Energy Link LED

When one of the programmable LED outputs is programmed in the ENERGYLNK mode, the LED uses blinking and solid on appearances to indicate energy detection and valid links. The ENERGYLNK LED is off when there is no link or energy detected. The LED blinks as soon as energy is detected on the wire. When the link is established, the LED remains continuously on for the duration. Shortly after a loss of energy is detected, the ENERGYLNK LED begins to blink and remains in this state for the length of the Disconnect Timer value, defined in Register 1Ch, Shadow 10000, bits 3:0. After the timer expires, the LED is turned off.

## Additional LED Modes

Some of the LEDs can also be programmed to additional modes. The different modes that each LED output can assume are described in Table 7. Because the modes are listed in the order of priority for each pin, the register bit enabling activity/link LED mode is not relevant when the receive LED is programmed to one of the link utilization modes. The last mode listed for each pin is the default mode. The table is valid for devices configured to RGMII/MII-lite to Copper mode only.

***Table 7: LED Modes***

| *LEDs* | *Description* |
|---|---|
| All LEDs (except for $\overline{\text{INTR}}$ mode) | Force LEDs:<br>• On (register 10h, bit 4 = 1): LED is on solid.<br>• Off (register 10h, bit 3 = 1): LED is off solid. |
| All LEDs | • General-purpose I/O input mode.<br>• General-purpose I/O output mode (default).<br>Register address 1Ch, shadow 01111, bits 3:0 = 0000. Each port can be individually programmed to input or output mode. |
| $\overline{\text{QUALITY}}$ LED | Remote fault (register 1Ch, shadow 01001, bit 2 = 1): LED is on when the Remote Fault bit (register 05h, bit 13) is set. The LED turns off if auto-negotiation is turned off, restarted, or if the Remote Fault bit is cleared. |
| $\overline{\text{ACTIVITY}}$ LED | Link utilization: This mode provides the estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by 10% increments. For duty cycles of 0.001 to 10%, the LED blinks at 3 Hz, for duty cycles of 10 to 20%, the LED blinks at 6 Hz, and for duty cycles of 90 to 96%, the LED blinks at 30 Hz. Though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. This LED mode is enabled to include all activity, transmit activity only, or receive activity only.<br>• Transmit (register 1Ch, shadow 01001, bits[1:0] = 01).<br>• Receive (register 1Ch, shadow 01001, bits[1:0] = 10).<br>• Activity (register 1Ch, shadow 01001, bits[1:0] = 11).<br>Activity/link LED (register 1Ch, shadow 01001, bits 4 = 1; register 10h, bit 5 = 0): LED is off when there is no link. The LED is on when there is a link. The LED blinks when the link is up and there is either transmit or receive activity. The LED blinks with a 167 ms cycle and a 50% duty cycle.<br>Receive (register 1Ch, shadow 01001, bit 3 = 0): This mode expresses receive activity in either of the two modes described as follows:<br>• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs.<br>• Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs.<br>Activity (default): This mode expresses both transmit and receive activity in either of the two modes described as follows.<br>• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs.<br>• Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs. |
| $\overline{\text{XMTLED}}$ LED | • Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for entire cycle if TX activity occurs.<br>• Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs. |
| $\overline{\text{RCVLED}}$ LED | • Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if TX activity occurs.<br>• Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs. |

***Table 7: LED Modes (Cont.)***

| *LEDs* | *Description* |
|---|---|
| $\overline{\text{INTR}}$ LED/Energy Detect (Open Drain) | • Force interrupt (register 10h, bit 11 = 1): LED is forced continuously on.<br>• Disable interrupt (register 10h, bit 12 = 1): LED is forced continuously off.<br>• Normal interrupt (default): LED is forced continuously on until interrupt is cleared. |

# Section 5: Register Summary

## MII Management Interface Register Programming

The BCM89820 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MII management interface registers are written and read serially, using the MDIO and MDC pins. A clock of up to 12.5 MHz must drive the MDC pin of the BCM89820. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

### Preamble (PRE)

To signal the beginning of an MII instruction after reset, at least thirty-two consecutive 1 bits must be written to the MDIO pin of the BCM89820. A preamble of thirty-two 1 bits is required only for the first read or write following reset. If bit 6 of MII register 01h is cleared, a preamble is always required. A preamble of fewer than thirty-two 1 bits causes the remainder of the instruction to be ignored.

### Start of Frame (ST)

A 01 pattern indicates that the start of the instruction follows.

### Operation Code (OP)

A read instruction is indicated by 10, while a write instruction is indicated by 01.

### PHY Address (PHYAD)

A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.

### Register Address (REGAD)

A 5-bit register address follows, with the MSB transmitted first. The addresses for the registers used by the BCM89820 are shown in Table 9.

### Turnaround (TA)

The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is performed, 10 must be sent to the BCM89820 chip during these two bit times. When a read operation is performed, the MDIO pin of the MAC must be put in a high-impedance state during these bit times. The BCM89820 transceiver drives the MDIO pin to 0 during the second bit time.

## Data

The last 16 bits of the instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first. During a read operation, the data bits are driven by the BCM89820 with the MSB transmitted first.

The complete management frame format is summarized in Table 8.

When writing to the MDIO pin, the bit value must be stable for 10 ns before the rising edge of the MDC and must be held valid for 10 ns after the rising edge of the MDC. When reading from the MDIO pin, the data bit is valid at the rising edge of the MDC until the next falling edge of the MDC.

***Example:*** To put a PHY with address 00001 into loopback mode, issue the following write MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111  0101 00001 00000 10 0100 0000 0000 0000

To determine if a PHY is in the link-pass state, issue the following read MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111  0110 00001 00001 *ZZ ZZZZ ZZZZ ZZZZ ZZZZ*

The BCM89820 drives the MDIO line during the last 17 bit times. If the link status is good, the third bit from the end (bit 2) is 1.

***Table 8: MII Management Frame Format***

| *Operation* | *PRE* | *ST* | *OP* | *PHYAD* | *REGAD* | *TA* | *Data* | *Direction* |
|---|---|---|---|---|---|---|---|---|
| Read | 1 ... 1 | 01 | 10 | AAAAA | RRRRR | ZZ<br>Z0 | Z ... Z<br>D ... D | Driven to BCM89820<br>Driven by BCM89820 |
| Write | 1 ... 1 | 01 | 01 | AAAAA | RRRRR | 10 | D ... D | Driven to BCM89820 |

# Register Map

The following table contains the set of registers for the BCM89820 transceiver.

***Table 9: Register Map***

| *Address* | *Register Table* |
|---|---|
| ***BroadR-Reach/100 Mb/s/10 Mb/s Registers*** | |
| 00h to 0Fh | “BroadR-Reach LRE Register Descriptions” |
| 0Ch to 0Eh | Reserved (do not read from or write to a reserved register) |
| 10h | “Register 10h: BroadR-Reach” |
| 11h | “Register 11h: BroadR-Reach PHY Extended Status” |
| 12h | “Register 12h: BroadR-Reach Receive Error Counter” |
| 13h | “Register 13h: BroadR-Reach False Carrier Sense Counter” |
| 14h | “Register 14h: BroadR-Reach Receiver NOT_OK Counter” |
| 15h to 16h | Reserved (do not read from or write to a reserved register except for accessing the Expansion registers through register 15h) |

***Table 9: Register Map (Cont.)***

| Address | Register Table |
|---|---|
| 17h | "Expansion Register Access Register (Address 17h)" |
| 18h | • "BroadR-Reach/100 Mb/s Auxiliary Control Shadows"<br>• "Register 18h (Shadow 010): Power/MII Control"<br>• "Register 18h (Shadow 100): Miscellaneous Test Register"<br>• "Register 18h (Shadow 111): Miscellaneous Control" |
| 19h | "Register 1Ah: Interrupt Status" |
| 1Ah | "Register 1Ah: Interrupt Status" |
| 1Bh | "Register 1Bh: Interrupt Mask" |
| 1Ch | • "Register 1Ch (Shadow 00010): Spare Control 1"<br>• "Register 1Ch (Shadow 00011): Clock Alignment Control"<br>• "Register 1Ch (Shadow 00100): Spare Control 2"<br>• "Register 1Ch (Shadow 01000): LED Status"<br>• "Register 1Ch (Shadow 01001): LED Control"<br>• "Register 1Ch (Shadow 01101): LED Selector 1"<br>• Register 1Ch (Shadow 01110): LED Selector 2<br>• "Register 1Ch (Shadow 01111): LED GPIO Control/Status"<br>• "Register 1Eh: Test Register 1" |
| 1Eh | "Register 1Eh: Test Register 1" |
| 1Fh | Reserved (do not read from or write to a reserved register) |
| ***Registers (Enabled by Register 1Ch, Shadow 11111, Bit 0 = 1)*** | |
| 07h to 0Eh | Reserved. (Do not read from or write to reserved register.) |
| ***Expansion Registers: Read/Write Through Register 15h (Accessed by Writing to Register 17h, Bits [11:0] = 1111 + Expansion Register Number)*** | |
| 00h | "Expansion Register 00h: Receive/Transmit Packet Counter" |
| 04h | "Expansion Register 04h: Multicolor LED Selector" |
| 05h | "Expansion Register 05h: Multicolor LED Flash Rate Controls" |
| 06h | "Expansion Register 06h: Multicolor LED Programmable Blink Controls" |
| 08h | "Expansion Register 0Eh: Synchronous Ethernet Controls" |
| 0Eh | "Expansion Register 0Eh: Synchronous Ethernet Controls" |
| 44h | "Expansion Register 70h: Soft Reset Register" |
| 70h | "Expansion Register 70h: Soft Reset Register" |
| 90h | "Expansion Register 90h: BroadR-Reach LRE Misc Control" |
| 91h | "Expansion Register 91h: BroadR-Reach LRE Misc Control" |
| 92h | "Expansion Register 92h: BroadR-Reach LRE Misc Control" |

# Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or write:

- R/W: Read or write
- RO: Read only
- LH: Latched high
- LL: Latched low
- H: Fixed high
- L: Fixed low
- SC: Self-clearing
- CR: Clear on reset

Reserved bits must be written as the default value and ignored when read.

# BroadR-Reach LRE Register Descriptions

The LRE register set contains control and status registers that are used during BroadR-Reach operation. These registers are overlaid on addresses 00-0Fh, thus special care must be taken to avoid confusion with the IEEE Register Set that reside at the same addresses. Access to the LRE Register Set is controlled by using Register 0Eh, which is available in both the LRE and the IEEE Register Sets.

## Register 00h: LRE Control

***Table 10: LRE Control Register (Address 00h)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| [15] | Reset | R/W SC | 1: PHY reset.<br>0: Normal operation. | 0 |
| [14] | Internal Loopback | R/W | 1: Loopback mode.<br>0: Normal operation. | 0 |
| [13] | Reserved | R/W | 1: Reserved. | 0 |
| [12] | Reserved | R/W | 1: Reserved.<br>0: Reserved. | 1 |
| [11] | Power Down | R/W | 1: Power down.<br>0: Normal operation. | 0 |
| [10] | Reserved | R/W | Reserved | 0 |
| [9:6] | Speed Selection | R/W | 1 0 0 0: 100 Mb/s.<br>Others: Reserved. | 0000 |

*Table 10: LRE Control Register (Address 00h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [5:4] | Pair Selection | R/W | 0 0: 1 pair connection.<br>0 1: Reserved.<br>1 0: Reserved.<br>1 1: Reserved. | 00 |
| [3] | Master Slave Selection | R/W | 1: Manually force local device to master, when Reg 0.12 = 0.<br>0: Manually force local device to slave, when Reg 0.12 = 0. | 0 |
| [2] | Reserved | R/W | Ignore on read. | 0 |
| [1:0] | Reserved | R/W | Write as 00, ignore on read. | 00 |

## Reset

To reset the BCM89820 by software control, 1 must be written to bit 15 of this register. This bit clears itself after the reset process is complete and does not require clearance using a second MII write. Writes to other MII Control register bits have no effect until the reset process is completed, which requires approximately 2.0 µs. Writing 0 to this bit has no effect. This bit returns 1 when it is read during the reset process; otherwise, it returns 0.

## Internal Loopback

The BCM89820 can be placed into internal loopback mode by setting bit 14 of this register. Loopback mode can be cleared by writing 0 to bit 14 of the MII Control register or by resetting the chip.

## Reserved

Bit 12 must be cleared in order to configure the PHY in forced mode.

## Power-Down

When bit 11 is set, the BCM89820 is placed into low-power standby mode.

## Reserved

Write bit 10 as 0, ignore on read.

## Speed Selection

Only one speed is supported on the BCM89820—1000 for 100 Mb/s operation. The default value for these bits is 0000.

## Pair Selection

Only one pair setting is currently supported: 00 for one-pair. The default value of these bits is 00.

## Master/Slave Selection

Bit 3 is used to manually select whether the device is configured as Master or Slave. For each pair of link partners, one node must be configured as Master, and one node must be configured as Slave. The default value of this bit is 0.

# Register 01h: LRE Status

***Table 11: LRE Status Register (Address 01h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:14] | Reserved | RO | Ignore on read. | 00 |
| [13] | 100 Mb/s One-pair Capable | ROH | 1: 100 Mb/s one-pair capable.<br>0: Not 100 Mb/s one-pair capable. | 1 |
| [12] | Reserved | ROH | Ignore on read. | 1 |
| [11] | Reserved | ROH | Ignore on read. | 1 |
| [10] | Reserved | ROH | Ignore on read. | 1 |
| [9] | Reserved | ROH | Ignore on read. | 1 |
| [8] | Extended Status | ROH | 1: Extended status information in reg 0Fh.<br>0: No extended status information in reg 0Fh. | 1 |
| [7] | Reserved | ROH | Ignore on read. | 1 |
| [6] | Management Frames Preamble Suppression | ROH | 1: Preamble can be suppressed.<br>0: Preamble always required. | 1 |
| [5] | Reserved | RO | Ignore on read. | 0 |
| [4] | Support IEEE 802.3 PHY | ROH | 1: Supports IEEE 802.3 PHY operation.<br>0: Does not support IEEE 802.3 PHY operation. | 1 |
| [3] | Reserved | ROH | Ignore on read. | 1 |
| [2] | Link Status | ROLL | 1: Link is up (Link-Pass state).<br>0: Link is down (link fail state). | 0 |
| [1] | Receive Jabber Detect | ROLH | 1: Receive Jabber condition detected.<br>0: No Receive Jabber condition detected. | 0 |
| [0] | Extended Capability | ROH | 1: Extended register capabilities.<br>0: No extended register capabilities. | 1 |

## 100 Mb/s One-Pair Capable

The BCM89820 is capable of 100 Mb/s one-pair BroadR-reach operation and returns 1 when bit 13 is read.

## Extended Status

The BCM89820 contains IEEE Extended Status register at address 0Fh and returns 1 when bit 8 is read.

## Support IEEE 802.3 PHY

The BCM89820 supports IEEE 802.3 PHY Operation, and returns 1 when bit 4 is read.

## Link Status

The BCM89820 returns 1 in bit 2 when the link monitor is in the link-pass state (indicating that a valid link has been established); otherwise, it returns 0. When a link failure occurs, the Link Status bit is latched at 0 and remains so until the bit is read and the device is in the link-pass state.

## Receive Jabber Detect

Receive jabber detection is performed within the PHY and the result is latched into this bit. When a jabber condition has been detected, the BCM89820 returns 1 in bit 1 of this register. The bit is cleared by reading.

## Extended Capability

The BCM89820 supports Extended Capability registers and returns 1 when bit 0 is read.

# Register 02h and 03h: LRE PHY Identifier

*Table 12: LRE PHY Identifier Register (Addresses 02h and 03h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:0] | Address 02: ID MSBs | RO | 16 MSBs of PHY Identifier. | 0362(hex) |
| [15:0] | Address 03: ID LSBs | RO | 16 LSBs of PHY Identifier. | 5CC*n*[a] (hex) |

a. The revision number (n) changes with each silicon revision.

The IEEE has issued an Organizationally Unique Identifier (OUI) to the Broadcom Corporation. This 24-bit number allows devices made by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], 6 Manufacturer's Model Number bits, and 4 Revision Number bits. The two least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-1B-E9, expressed as a hexadecimal value. The binary OUI is 0000-0000-1101-1000-1001-0111. The model number for the BCM89820 is 0Ch (001100 binary). Revision numbers start with 0h and are incremented by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision[3:0]

# Registers 04h–0Ah: Reserved

Registers 04h–0Ah are reserved.

# Register 0Fh: LRE Extended Status

*Table 13: LRE Extended Status Register (Address 0Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:10] | Reserved | RO | Ignore on read. | 000000 |
| [9] | Local Receiver Status | RO | 1: Local Receiver OK. | 0 |
| [8] | Remote Receiver Status | RO | 1: Remote Receiver OK. | 0 |
| [7:0] | Idle Error Count | RO | Number of Idle errors since last read. | 00h |

## Local Receiver Status

Bit 9 indicates the status of the local receiver.

## Remote Receiver Status

Bit 8 indicates the status of the remote receiver.

### Idle Error Count

The BCM89820 counts the number of idle errors received while the local receiver status is OK. Bits [7:0] return the number of idle errors counted since the last register read. The counter freezes at the maximum value (FFh) to prevent overflow.

# Auxiliary Register Descriptions

## Register 10h: BroadR-Reach

***Table 14: BroadR-Reach/100 Mb/s PHY Extended Control Register (Address 10h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Reserved | R/W | Write as zero. | 00h |
| [14] | Reserved | R/W | Write as zero. | 0 |
| [13] | Transmit Disable | R/W | 1: Transmitter outputs disabled.<br>0: Normal operation. | 0 |
| [12] | Interrupt Disable | R/W | 1: Interrupt status output disabled.<br>0: Interrupt status output enabled. | 0 |
| [11] | Force Interrupt | R/W | 1: Force interrupt status to active.<br>0: Normal operation. | 0 |
| [10:6] | Reserved | R/W | Write as zero. | 0 |
| [5] | Enable LED Traffic mode | R/W | 1: LED Traffic mode enabled.<br>0: LED Traffic mode disabled. | 0 |
| [4] | Force LEDs On | R/W | 1: Force all LEDs into on state.<br>0: Normal LED operation. | 0 |
| [3] | Force LEDs Off | R/W | 1: Force all LEDs into off state.<br>0: Normal LED operation. | 0 |
| [2:1] | Reserved | R/W | Write as 00, ignore on read. | 00 |
| [0] | BroadR-Reach PCS transmit FIFO Elasticity (copper mode) | R/W | 1: High latency.<br>0: Low latency. | 0 |

### MAC/PHY Interface Mode

Bit 15 selects the Interface mode between the MAC and the PHY. This bit must be set to 0 for normal operation.

### Transmit Disable

The transmitter can be disabled by setting bit 13. The transmitter outputs are forced into a high-impedance state.

### Interrupt Disable

When bit 12 is set, the interrupt pin is forced to its inactive state except when the Force Interrupt bit is set.

## Force Interrupt

When bit 11 is set, the $\overline{\text{INTR}}$ pin is forced to its active state.

## Enable LED Traffic Mode

When bit 5 is set, the BCM89820 enables the LED traffic mode for $\overline{\text{ACTIVITYLED}}$ and $\overline{\text{XMITLED}}$. When the bit is cleared, the device disables the LED traffic mode.

## Force LEDs On

When bit 4 is set, the BCM89820 forces all LEDs into the on state. When the bit is cleared, the device resets all LEDs to normal operation.

## Force LEDs Off

When bit 3 is set, the BCM89820 forces all LEDs into the off state. When the bit is cleared, the device resets all LEDs to normal operation.

## BroadR-Reach PCS Transmit FIFO Elasticity (Copper Mode)

When bit 0 is set, the BCM89820 sets the FIFO elasticity to high latency. In this mode, the device can transmit packets up to 9 kilobytes in length. When bit 0 is cleared, the FIFO elasticity is set to low latency. In this mode, the device can transmit packets up to 4.5 KB in length. Setting bit 0 to 1 adds 160 ns to the BroadR-Reach transmit latency.

# Register 11h: BroadR-Reach PHY Extended Status

***Table 15: BroadR-Reach/100 Mb/s PHY Extended Status Register (Address 11h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Auto-negotiation Base Page Selector Field Mismatch | RO<br>LH | 1: Link Partner Base Page Selector field mismatched Advertised Selector field since last read.<br>0: No mismatch detected since last read. | 0 |
| [14] | Reserved | RO | Write as 0, ignore on read. | 0 |
| [13] | MDI Crossover State | RO | 1: Crossover MDI mode.<br>0: Normal MDI mode. | 0 |
| [12] | Interrupt Status | RO | 1: Unmasked interrupt currently active.<br>0: Interrupt cleared. | 0 |
| [11] | Remote Receiver Status | RO<br>LL | 1: Remote receiver OK.<br>0: Remote receiver not OK since last read. | 0 |
| [10] | Local Receiver Status | RO<br>LL | 1: Local receiver OK.<br>0: Local receiver not OK since last read. | 0 |
| [9] | Locked | RO | 1: Descrambler locked.<br>0: Descrambler unlocked. | 0 |
| [8] | Link Status | RO | 1: Link pass.<br>0: Link fail. | 0 |
| [7] | CRC Error Detected | RO<br>LL | 1: CRC error detected.<br>0: No CRC error since last read. | 0 |
| [6] | Carrier Extension Error Detected | RO<br>LH | 1: Carrier extension error detected since last read.<br>0: No carrier extension error since last read. | 0 |
| [5] | Bad SSD Detected (False Carrier) | RO<br>LH | 1: Bad SSD error detected since last read.<br>0: No bad SSD error since last read. | 0 |
| [4] | Bad ESD Detected (Premature End) | RO<br>LH | 1: Bad ESD error detected since last read.<br>0: No bad ESD error since last read. | 0 |
| [3] | Receive Error Detected | RO<br>LH | 1: Receive error detected since last read.<br>0: No receive error since last read. | 0 |
| [2] | Transmit Error Detected | RO<br>LH | 1: Transmit error code received since last read.<br>0: No transmit error code received since last read. | 0 |
| [1] | Lock Error Detected | RO<br>LH | 1: Lock error detected since last read.<br>0: No lock error since last read. | 0 |
| [0] | Reserved | R | Ignore on read. | 0 |

## Auto-Negotiation Base Page Selector Field Mismatch

When bit 15 is set, a mismatch between the auto-negotiation base page selector and the Advertised Selector field has occur since the last register read.

## MDI Crossover State

When the BCM89820 is automatically switching the transmit and receive pairs to communicate with a remote device, the device returns 1 in bit 13. This bit returns 0 when the device is in normal MDI mode.

## Interrupt Status

The BCM89820 returns 1 in bit 12 when any unmasked interrupt is currently active; otherwise, it returns 0.

## Remote Receiver Status

When the remote receiver status is OK, the BCM89820 returns 1 in bit 11. When the device detects that the remote receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

## Local Receiver Status

When the local receiver status is OK, the BCM89820 returns 1 in bit 10. When the device detects that the local receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

## Locked

The BCM89820 returns 1 in bit 9 when the descrambler is locked to the incoming data stream; otherwise, it returns 0.

## Link Status

The BCM89820 returns 1 in bit 8 when the device has established a link; otherwise, it returns 0.

## CRC Error Detected

**The** BCM89820 returns 1 in bit 7 if a CRC error has been detected since the last time this register was read; otherwise, it returns 0.

## Carrier Extension Error Detected

The BCM89820 returns 1 in bit 6 if a carrier extension error has been detected since the last time this register was read; otherwise, it returns 0.

## Bad SSD Detected (False Carrier)

The BCM89820 returns 1 in bit 5 if a bad start-of-stream error has been detected since the last time this register was read; otherwise, it returns 0.

### Bad ESD Detected (Premature End)

The BCM89820 returns 1 in bit 4 if a bad end-of-stream error has been detected since the last time this register was read; otherwise, it returns 0.

### Receive Error Detected

The BCM89820 returns 1 in bit 3 if a packet was received with an invalid code since the last time this register was read; otherwise, it returns 0.

### Transmit Error Detected

The BCM89820 returns 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read; otherwise, it returns 0.

### Lock Error Detected

The BCM89820 returns 1 in bit 1 if the descrambler has lost lock since the last time this register was read; otherwise, it returns 0.

## Register 12h: BroadR-Reach Receive Error Counter

***Table 16: BroadR-Reach Receive Error Counter Register (Address 12h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:0] | Receive Error Counter | R/W CR | Number of non-collision packets with receive errors since last read. | 0000h |

#### Receive Error Counter

This counter increments each time the BCM89820 receives a noncollision packet containing at least 1 receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

## Register 13h: BroadR-Reach False Carrier Sense Counter

***Table 17: BroadR-Reach False Carrier Sense Counter Register (Address 13h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:8] | Reserved | R/W | Write as 00h, ignore on read. | 00h |
| [7:0] | False Carrier Sense Counter | R/W CR | Number of false carrier sense events since last read. | 00h |

#### False Carrier Sense Counter

The False Carrier Sense Counter increments each time the BCM89820 detects a false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

# Register 14h: BroadR-Reach Receiver NOT_OK Counter

*Table 18: BroadR-Reach Receiver NOT_OK Counter Register (Address 14h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:8] | Local Receiver NOT_OK Counter | R/W CR | Number of times local receiver was NOT_OK since last read. | 00h |
| [7:0] | Remote Receiver NOT_OK Counter | R/W CR | Number of times BCM89820 detected that the remote receiver was NOT_OK since last read. | 00h |

## Local Receiver NOT_OK Counter

This counter increments each time the local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

## Remote Receiver NOT_OK Counter

This counter increments each time the remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

# Register 17h: Expansion Register Access

*Table 19: Expansion Register Access Register (Address 17h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:12] | Reserved | R/W | Write as 0h, ignore on read. | 0h |
| [11:8] | Expansion Register Select | R/W | 1111: Expansion register selected.<br>1101: Top-level Expansion register selected.<br>0000: Expansion register not selected.<br>All others: Reserved (Do not use). | 0h |
| [7:0] | Expansion Register Address | R/W | Sets the Expansion register number accessed when read/write register 15h. | 00h |

## Expansion Register Select

Setting bits [11:8] to 1111 enables reading from and writing to the Expansion registers. These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. See “Expansion Registers” for details.

## Expansion Register Address

Bits [7:0] determine the Expansion register address. Once the access to Expansion register is completed, all reads and writes to register 15h access the required Expansion Register.

# Register 18h: Shadow Access

Register 18h contains several shadow registers that require special handling to access. The following table lists the 18h shadow registers.

***Table 20: BroadR-Reach/100 Mb/s Auxiliary Control Shadows***

| *Shadow Value* | *Register Name* |
|---|---|
| 000 | "Register 18h: Shadow Access" |
| 001 | "BroadR-Reach/100 Mb/s Auxiliary Control Shadows" |
| 010 | "Register 18h (Shadow 010): Power/MII Control" |
| 100 | "Register 18h (Shadow 100): Miscellaneous Test Register" |
| 111 | "Register 18h (Shadow 111): Miscellaneous Control" |

The following table describes how to read from one of the shadows of register 18h.

***Table 21: Reading Register 18h Shadows***

| *Register Reads/Writes* | *Description* |
|---|---|
| Write register 18h, with the following bit values: | This selects the Miscellaneous Control register, shadow 111. |
| • Bit [15] = 0 | This allows only bits [14:12] and [2:0] to be written. |
| • Bits [14:12] = yyy | This selects shadow value register yyy to be read. |
| • Bits [11: 3] = <don't care> | When bit [15] = 0, these bits are ignored. |
| • Bits [2:0] = 111 | This sets the Shadow Register Select to 111 (Miscellaneous Control register). |
| Read register 18h | Data read back is the value from shadow register yyy. |

The following table describes how to write register 18h, shadow yyy.

***Table 22: Writing Register 18h Shadows***

| *Register Writes* | *Description* |
|---|---|
| Bits [15:3] = Required value | Bits [15:3] contain the preferred bits to be written. |
| Bits [2:0] = yyy | This enables shadow register yyy to be written.<br>For shadow 111, bit 15 must also be written. |

# Register 18h (Shadow 000): Auxiliary Control Register

***Table 23: Auxiliary Control Register (Address 18h, Shadow 000)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| [15] | External Loopback | R/W | 1: External Loopback enabled.<br>0: Normal operation. | 0 |
| [14] | Extended Packet Length | R/W | 1: Allow reception of extended length packets.<br>0: Allow normal length Ethernet packets only. | 0 |

*Table 23: Auxiliary Control Register (Address 18h, Shadow 000) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [13:11] | Reserved | R/W | Write as 0, ignore on read. | 000 |
| [10] | Transmit Mode | R/W | 1: Normal operation.<br>0: Test mode. | 1 |
| [9:3] | Reserved | R/W | Write as 0, ignore on read. | 00h |
| [2:0] | Shadow Register Select | R/W | Shadow Value, see Table 20. | 000 |

## External Loopback

When bit 15 is set, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

## Extended Packet Length

When bit 14 is set, the BCM89820 is able to receive packets up to 18 KB in length. When the bit is cleared, the device can only receive packets up to 4.5 KB in length.

## Transmit Mode

Bit 10 must be set for normal PHY operation.

## Shadow Register Select

See Table 20.

# Register 18h (Shadow 010): Power/MII Control

*Table 24: BroadR-Reach/100 Mb/s Power/MII Control Register (Address 18h, Shadow 010)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:6] | Reserved | R/W | Write as 0000010011, ignore on read. | 0000010011 |
| [5] | Super Isolate | R/W | 1: Isolate mode with no link pulses transmitted.<br>0: Normal operation. | 0 |
| [4:3] | Reserved | R/W | Write as 00, ignore on read. | 00 |
| [2:0] | Shadow Register Select | R/W | Shadow Value, see Table 20. | 010 |

## Super Isolate

Setting bit 5 places the BCM89820 into the Super Isolate mode. Similar to the Isolate mode, all MAC inputs are ignored and all MAC outputs are tristated. All link pulses are suppressed.

## Shadow Register Select

See Table 20.

# Register 18h (Shadow 100): Miscellaneous Test Register

*Table 25: Miscellaneous Test Register (Address 18h, Shadow 100)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Line-side [Remote] Loopback Enable | R/W | 1: Enable line-side [remote] loopback from MDI (cable end) receive packet, through PCS and back to MDI transmit packet.<br>0: Disable loopback. | 0 |
| [14:12] | Reserved | R/W | Write as 100, ignore on read. | 100 |
| [11] | Line-side [Remote] Loopback Tri-state | R/W | 1: Tristate the receive MII pins (RXDV, RXD, and RXC) when line-side [remote] loopback is enabled.<br>0: Line-side [remote] loopback packets appear on MII. | 0 |
| [10:3] | Reserved | R/W | Write as 000000, ignore on read. | 00h |
| [2:0] | Shadow Register Select | R/W | Shadow Value, see Table 20. | 100 |

## Line-Side [Remote] Loopback Enable

Setting bit 15 enables line-side (remote) loopback of the copper receive packet back out through the MDI transmit path.

## Line-Side [Remote] Loopback Tristate

Setting this bit tri-states the receive MII pins when the device is in Line-side (remote) Loopback mode.

### Shadow Register Select

See Table 20.

## Register 18h (Shadow 111): Miscellaneous Control

*Table 26: Miscellaneous Control Register (Address 18h, Shadow 111)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable (Bits 11:3) | R/W<br>SC | 1: Write bits [14:0].<br>0: Only write bits [14:12] and [2:0]. | 0 |
| [14:12] | Shadow Register Read Selector | R/W | Shadow Value, see Table 20.<br>These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read. | 000 |
| [11] | Packet Counter Mode | R/W | 1: Receive packet counter.<br>0: Transmit packet counter. | 0 |
| [10] | Bypass Wirespeed Timer | R/W | 1: Link fail timer will clear as soon as link is up.<br>0: Link must be up for at least 2.5 seconds otherwise link fail timer will increment. | 0 |
| [9] | Reserved | R/W | Write as zero. | 0 |
| [8] | RGMII RXD to RXC Skew | R/W | 1: Enable skew.<br>0: Disable skew. | 1 |
| [7] | RGMII Enable | R/W | 1: RGMII mode.<br>0: GMII/MII mode. | 1 |
| [6:5] | Reserved | R/W | Write as 11, ignore on read. | 11 |
| [4:3] | Reserved | R/W | Reserved. | 00 |
| [2:0] | Shadow Register Select | R/W | Shadow Value, see Table 20. | 111 |

### Write Enable (Bits 11:3)

If bit 15 is set when writing to this register, then bits [11:3] of this register can be modified. Bits [2:0] and [14:12] can always be written regardless of the value of bit 15.

When this bit is set, bits [14:0] are written. When this bit is cleared, only bits [14:12] and bits [2:0] are written.

### Shadow Register Read Selector

Bits [14:12] are written, regardless of the value of bit 15. These bits determine the shadow value for an MII register 18h read operation. See the note in "Register 18h: Shadow Access" describing reading from and writing to register 18h.

### Packet Counter Mode

Bit 11 sets the packet counter mode in Expansion register 00h. The counter counts the receive packet when this bit is set; otherwise, it counts the transmit packet.

### Bypass Wirespeed Timer

When bit 10 is set, the link fail timer will clear as soon as link is up. If bit 10 is cleared, the link must be up for 2.5 seconds to clear the fail link timer.

### RGMII RXD to RXC Skew

Bit 8 allows the skew time from RXD to RXC to increase by approximately 4 ns for 100 Mb/s mode, and 50 ns for 10 Mb/s mode. Enabling this timing adjustment eliminates the requirement for board trace delays, as required by the RGMII specification. By default, this skew is always enabled.

### RGMII Enable

Bit 7 enables the RGMII mode of operation. Writing a 0 to this bit changes the MAC interface to GMII or MII mode of operation. The default value of this bit is 1 under most circumstances.

### Shadow Register Select

Shadow Value, see Table 20.

## Register 1Ah: Interrupt Status

*Table 27: Interrupt Status Register (Address 1Ah)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Energy Detect Change | RO<br>LH | 1: Filtered energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1).<br>0: Interrupt cleared. | 0 |
| [14] | Illegal Pair Swap | RO<br>LH | 1: Illegal pair swap detected.<br>0: Interrupt cleared. | 0 |
| [13] | Reserved | RO<br>LH | Ignore on read. | 0 |
| [12] | Exceeded High Counter Threshold | RO | 1: Value in one or more counters is above 32K.<br>0: All counters below 32K. | 0 |
| [11] | Exceeded Low Counter Threshold | RO | 1: Value in one or more counters is above 128K.<br>0: All counters below 128K. | 0 |
| [10:7] | Reserved | R | Ignore on read. | 0h |
| [6] | Scrambler Synchronization Error | RO<br>LH | 1: Scrambler synchronization error occurred since last read.<br>0: Interrupt cleared. | 0 |

*Table 27: Interrupt Status Register (Address 1Ah) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [5] | Remote Receiver Status Change | RO<br>LH | 1: Remote receiver status changed since last read.<br>0: Interrupt cleared. | 0 |
| [4] | Local Receiver Status Change | RO<br>LH | 1: Local receiver status changed since last read.<br>0: Interrupt cleared. | 0 |
| [3] | Duplex Mode Change | RO<br>LH | 1: Duplex mode changed since last read.<br>0: Interrupt cleared. | 0 |
| [2] | Link Speed Change | RO<br>LH | 1: Link speed changed since last read.<br>0: Interrupt cleared. | 0 |
| [1] | Link Status Change | RO<br>LH | 1: Link status changed since last read.<br>0: Interrupt cleared. | 0 |
| [0] | CRC Error | RO<br>LH | 1: CRC error occurred since last read.<br>0: Interrupt cleared. | 0 |

The $\overline{\text{INTR}}$ output is asserted when any bit in the Interrupt Status register is set and the corresponding bit in the Interrupt Mask register is cleared.

## Energy Detect Change

Bit 15 indicates that the copper Energy Detect status changed since the last time this register was read.

## Illegal Pair Swap

Bit 14 indicates an uncorrectable pair swap error on the twisted-pair cable has been detected since the last time this register was read.

## MDIX Status Change

Bit 13 indicates that a link pulse or 100 Mb/s carrier was detected on a different pair than previously detected since the last time this register was read.

## Exceeded High Counter Threshold

Bit 12 indicates that one or more of the counters in registers 12 to 14h is above 32 000.

## Exceeded Low Counter Threshold

Bit 11 indicates that one or more of the counters in registers 12 to 14h is above 128 000.

## Scrambler Synchronization Error

Bit 6 indicates that a scrambler synchronization error has been detected since the last time this register was read.

## Remote Receiver Status Change

Bit 5 indicates that the remote receiver status has changed since the last time this register was read.

## Local Receiver Status Change

Bit 4 indicates that the local receiver status has changed since the last time this register was read.

## Duplex Mode Change

Bit 3 indicates that the Duplex mode has changed since the last time this register was read.

## Link Speed Change

Bit 2 indicates that the link speed has changed since the last time this register was read.

## Link Status Change

Bit 1 indicates that the link status has changed since the last time this register was read.

## CRC Error

Bit 0 indicates that a receive CRC error has been detected since the last time this register was read.

# Register 1Bh: Interrupt Mask

*Table 28: Interrupt Mask Register (Address 1Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Energy Detect Change | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [14] | Illegal Pair Swap | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [13] | Reserved | R/W | Write as 1, ignore on read. | 1 |
| [12] | Exceeded High Counter Threshold | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [11] | Exceeded Low Counter Threshold | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [10:7] | Reserved | R/W | Write as 1111, ignore on read. | 1111 |
| [6] | Scrambler Synchronization Error | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [5] | Remote receiver status Change | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [4] | Local receiver status Change | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [3] | Duplex mode Change | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [2] | Link Speed Change | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [1] | Link Status Change | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |
| [0] | CRC Error | R/W | 1: Interrupt masked, status bits operate normally.<br>0: Interrupt enabled, status bits operate normally. | 1 |

### Interrupt Mask Vector

When bit *n* is written to 1, the interrupt corresponding to the same bit in the Interrupt Status register is masked. The status bits still operate normally when the interrupt is masked, but do not generate an interrupt output. When the bit is written to 0, the interrupt is unmasked.

## Register 1Ch Access

Register 1Ch contains several shadow registers that require special handling in order to access. The six MSBs of register 1Ch are special access control bits.

Bits [14:10] set the shadow value of register 1Ch, and bit 15 enables writing of bits [9:0]. To write to one of the shadow registers, set bit 15 =1 and bits [14:10] = shadow address value. All subsequent reads from register 1Ch will come from the chosen shadow register. If a read from a shadow of register 1Ch is required before a corresponding write to the same shadow, bit 15 =0 can be used to set access to the required shadow register, without writing bits [9:0]. The register 1Ch shadow address values are listed in the following table.

***Table 29: Register 1Ch Shadow Values***

| *Shadow Value* | *Register Name* |
|---|---|
| 00010 | “Register 1Ch (Shadow 00010): Spare Control 1” |
| 00011 | “Register 1Ch (Shadow 00011): Clock Alignment Control” |
| 00100 | “Register 1Ch (Shadow 00100): Spare Control 2” |
| 00101 | N/A |
| 01000 | “Register 1Ch (Shadow 01000): LED Status” |
| 01001 | “Register 1Ch (Shadow 01001): LED Control” |
| 01010 | N/A |
| 01101 | “Register 1Ch (Shadow 01101): LED Selector 1” |
| 01110 | “Register 1Ch (Shadow 01110): LED Selector 2” |
| 01111 | “Register 1Ch (Shadow 01111): LED GPIO Control/Status” |
| 01011 | “Register 1Ch (Shadow 01011): External Control” |

# Register 1Ch (Shadow 00010): Spare Control 1

The following register is enabled by accessing register 1Ch with shadow value 00010 in bits [14:10].

***Table 30: Spare Control 1 Register (Address 1Ch, Shadow 00010)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 00010 = Spare Control 1 register. | 00010 |
| [9:1] | Reserved | R/W | Write as 101h, ignore on read. | 101h |
| [0] | Link LED Mode | R/W | 1: Enable link LED mode.<br>$\overline{\text{LINKSPD}}$[2:1] = Speed.<br>00: N/A.<br>01: 100 BR link.<br>10: 10 BR link or no link.<br>$\overline{\text{SLAVE}}$ = Active low link.<br>0: Normal link LED mode. | 0 |

## Write Enable

During a write to this register, setting bit 15 to 1 allows writing to bits [9:0] of this register. For reading the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] of this register must be set to 00010 to enable read and write to the Spare Control 1 register address 1Ch.

## Link LED Mode

Bit 0 selects the link LED mode. When this bit is set, it enables the link LED mode. The $\overline{\text{LINKSPD2}}$/$\overline{\text{LINKSPD1}}$ are Link/Speed LED and $\overline{\text{SLAVE}}$ LED is $\overline{\text{LINK}}$ LED to indicate a link. When this bit is cleared, the $\overline{\text{LINKSPD2}}$, $\overline{\text{LINKSPD1}}$, and $\overline{\text{SLAVE}}$ are in normal mode.

# Register 1Ch (Shadow 00011): Clock Alignment Control

The following register is enabled by accessing register 1Ch with shadow value 00011 in bits [14:10].

***Table 31: Clock Alignment Control Register (Address 1Ch, Shadow 00011)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 00011: Clock Alignment Control register. | 00011 |
| [9] | GTXCLK Clock Delay Enable | R/W | 1: Enable GTXCLK delay.<br>0: Normal mode (bypass GTXCLK delay). | 1 |
| [8:0] | Reserved | R/W | Write as 000h, ignore on read. | 000h |

## Write Enable

During a write to this register, setting bit 15 to 1 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] of this register must be set to 00011 to enable read and write to the Clock Alignment Control register address 1Ch.

## GTXCLK Clock Delay Enable

Setting bit 9 enables the GTXCLK internal delay. When this bit is cleared, the GTXCLK delay is bypassed.

# Register 1Ch (Shadow 00100): Spare Control 2

The following register is enabled by accessing register 1Ch with shadow value 00100 in bits [14:10].

***Table 32: Spare Control 2 Register (Address 1Ch, Shadow 00100)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 00100: Spare Control 2 register. | 00100 |
| [9:5] | Reserved | R/W | Write as 00h, ignore on read. | 00h |
| [4:0] | Reserved | R/W | Write as 011, ignore on read. | 011 |

### Write Enable

During a write to this register, setting bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

### Shadow Register Selector

Bits [14:10] must be set to 00100 to enable read and write to the Spare Control 2 register.

### Energy Detect on $\overline{\text{INTR}}$ Pin

Bit 1 enables the signal detect or energy detect input on the $\overline{\text{INTR}}$ pin. Set the LED selector register to enable $\overline{\text{INTR}}$ LED mode (1Ch shadow 01101 or 01110 set bit [7:4]/[3:0] to 0110 depending on the LED).

## Register 1Ch (Shadow 01000): LED Status

The following register is enabled by accessing register 1Ch with shadow value 01000 in bits [14:10].

***Table 33: LED Status Register (Address 1Ch, Shadow 01000)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 01000: LED Status register. | 01000 |
| [9] | Reserved | RO | Write as 0, ignore on read. | 0 |
| [8] | $\overline{\text{Slave}}$ Indicator | RO | 1: Master mode.<br>0: Slave mode. | 1 |
| [7] | $\overline{\text{FDX}}$ Indicator | RO | 1: Half-duplex mode. | 0 |
| [6] | $\overline{\text{INTR}}$ Indicator | RO | 1: No active Interrupt.<br>0: Interrupt activated. | 1 |
| [5] | Reserved | RO | Write as 0, ignore on read. | 0 |
| [4:3] | $\overline{\text{LINKSPD}}$ Indicator | RO | 11: No link.<br>10: 10 Mb/s link.<br>01: 100 Mb/s link.<br>00: N/A. | 11 |
| [2] | $\overline{\text{Transmit}}$ Indicator | RO | 1: No transmit activity.<br>0: Transmit activity. | 1 |
| [1] | $\overline{\text{Receive}}$ Indicator | RO | 1: No receive activity.<br>0: Receive activity. | 1 |
| [0] | $\overline{\text{Quality}}$ Indicator | RO | 1: Poor quality link.<br>0: Good quality link. | 1 |

### Write Enable

During a write to this register, setting bit 15 to 1 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

### Shadow Register Selector

Bits [14:10] of this register must be set to 01000 to enable read and write to the LED Status register.

### $\overline{\text{Slave}}$ Indicator

When bit 8 returns 0, the device is in the slave mode. When this bit returns 1, the device is not in the slave mode.

### $\overline{\text{FDX}}$ Indicator

When bit 7 returns 0, the device is in the full-duplex mode. When this bit returns 1, the device is not in the full-duplex mode.

### $\overline{\text{INTR}}$ Indicator

When bit 6 returns 0, the device is in the interrupted mode. When this bit returns 1, the device is not in the interrupted mode.

### $\overline{\text{LINKSPD}}$ Indicator

When bits 4:3 return 00, the device is in the BroadR-ReachX Link mode. When these bits return 01, the device is in the 100 Mb/s link mode. When these bits return 10, the device is in the 10 Mb/s link mode. When these bits return 11, the device is not linked.

### $\overline{\text{Transmit}}$ Indicator

When bit 2 returns 0, the device is transmitting data. When this bit returns 1, the device is not transmitting data.

### $\overline{\text{Receive}}$ Indicator

When bit 1 returns 0, the device is receiving data. When this bit returns 1, the device is not receiving data.

### $\overline{\text{Quality}}$ Indicator

When bit 0 returns 0, the quality of the link is deemed to be good. When this bit returns 1, the quality of the link is deemed to be poor.

# Register 1Ch (Shadow 01001): LED Control

The following register is enabled by accessing register 1Ch with shadow value 01001 in bits [14:10].

***Table 34: LED Control Register (Address 1Ch, Shadow 01001)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 01001: LED Control register. | 01001 |
| [9:6] | Reserved | R/W | Write as 0h, ignore on read. | 0h |
| [5] | Reserved | R/W | Write as 0, ignore on read. | 0 |
| [4] | Activity/Link LED Enable | R/W | 1: Drive activity/link data on $\overline{\text{ACTIVITY}}$ LED.<br>0: Drive activity data on $\overline{\text{ACTIVITY}}$ LED. | 0 |
| [3] | $\overline{\text{ACTIVITY}}$ LED Enable | R/W | 1: Drive activity data on $\overline{\text{ACTIVITY}}$ LED.<br>0: Drive receive data on $\overline{\text{ACTIVITY}}$ LED. | 1 |
| [2] | Remote Fault LED Enable | R/W | 1: Remote fault on quality LED.<br>0: Normal operation. | 0 |
| [1:0] | Link Utilization LED Selector | R/W | 00: Normal activity (fixed blink rate).<br>01: Transmit activity with variable blink rate.<br>10: Receive activity with variable blink rate.<br>11: Transmit/receive activity with variable blink rate.<br>***Note:*** This mode has higher priority than the activity LED Enable mode in bit 3. | 00 |

## Write Enable

During a write to this register, setting bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] of this register must be set to 01001 to enable read and write to the register address 1Ch.

## Activity/Link LED Enable

Setting bit 4 configures the $\overline{\text{ACTIVITY}}$ LED as an activity/link indicator.

## $\overline{\text{ACTIVITY}}$ LED Enable

Setting bit 3 configures the $\overline{\text{ACTIVITY}}$ LED as an activity/link indicator. Otherwise, it configures the $\overline{\text{ACTIVITY}}$ LED as a receive-data indicator only.

### Remote Fault LED Enable

Setting bit 2 configures the quality LED as a remote fault indicator.

### Link Utilization LED Selector

Bits [1:0] are only applicable when the ACTIVITY LED is programmed as an activity indicator. In the activity LED mode, the LED expresses an estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by increments of 10%. For activity duty cycles of 0.001% to10%, the LED blinks at 3 Hz; for duty cycles of 10% to 20%, the LED blinks at 6 Hz; and for duty cycles of 90% to 96%, the LED blinks at 30 Hz. Even though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. The ACTIVITY LED can be programmed to display the following:

- 00: Normal activity (fixed blink rate).
- 01: Transmit activity with variable blink rate.
- 10: Receive activity with variable blink rate.
- 11: Transmit/receive activity with variable blink rate.

## Register 1Ch (Shadow 01011): External Control

The following register is enabled by accessing register 1Ch with shadow value 01011 in bits [14:10].

***Table 35: External Control Register (Address 1Ch, Shadow 01011)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 01011: External Control register. | 01011 |
| [9:8] | Reserved | R/W | Write as 00, ignore on read. | 00 |
| [7] | Freeze AGC at Link | R/W | 1: Freeze AGC shortly after link is achieved.<br>0: Normal AGC operation. | 1 |
| [6:5] | Reserved | R/W | Write as 00, ignore on read. | 00 |
| [4:3] | RGMII Pad Configuration | R/W | RGMII pad voltage selector settings:<br>00: 3.3V MII.<br>01: 2.5V RGMII.<br>10: Reserved.<br>11: 3.3V RGMII. | Default set by LED3/ LED2 pins |
| [2] | LOM-LED Mode | R/W | 1: Enable LOM LED mode.<br>0: Normal LED mode. | Default set by LED4 pin |
| [1:0] | Reserved | R/W | Write as 01, ignore on read. | 01 |

### Write Enable

During a write to this register, setting bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Register bits [14:10] must be set to 01011 to enable read and write to the External Control register address 1Ch.

## Freeze AGC at Link

Setting this bit freezes the Automated Gain Control value of the receive data path shortly after link is achieved. This function is useful to mitigate emissions caused by steps of the gain control value. This function is on by default.

## RGMII Pad Configuration

These two bits determine the operating voltage of the RGMII pads. The default values for these register bits are determined by the LED3 and LED2 pins during reset, as shown in Table 14.

## LOM-LED Mode

Setting this bit enables the LOM-LED mode of operation, where the LEDs report link and speed in a slightly different fashion, as described in Table 15. The default value for this register bit is determined by the LED4 pin during reset, as shown in Table 14.

## Register 1Ch (Shadow 01101): LED Selector 1

The following register is enabled by accessing register 1Ch with shadow value 01101 in bits [14:10].

***Table 36: LED Selector 1 Register (Address 1Ch, Shadow 01101)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0]<br>0: Read bits [9:0] | 0 |
| [14:10] | Shadow Register Selector | R/W | 01101: LED Selector 1 register | 01101 |
| [9:8] | Reserved | R/W | Write as 00, ignore on read | 00 |
| [7:4] | LED2 Selector | R/W | 0000: $\overline{\text{LINKSPD[1]}}$<br>0001: $\overline{\text{LINKSPD[2]}}$<br>0010: $\overline{\text{XMITLED}}$<br>0011: $\overline{\text{ACTIVITYLED}}$<br>0100: $\overline{\text{LED2/FDX}}$<br>0101: $\overline{\text{SLAVE}}$<br>0110: $\overline{\text{INTR}}$<br>0111: $\overline{\text{QUALITY/REMOTE FAULT}}$<br>1000: $\overline{\text{RCVLED}}$<br>1001: Reserved<br>1010: $\overline{\text{MULTICOLOR[2]}}$<br>1011: Reserved<br>1100: Reserved<br>1101: Reserved<br>1110: Off (high)<br>1111: On (low) | 0001<br>— |
| [3:0] | LED1 Selector | R/W | 0000: $\overline{\text{LINKSPD[1]}}$<br>0001: $\overline{\text{LINKSPD[2]}}$<br>0010: $\overline{\text{XMITLED}}$<br>0011: $\overline{\text{ACTIVITYLED}}$<br>0100: $\overline{\text{LED2/FDX}}$<br>0101: $\overline{\text{SLAVE}}$<br>0110: $\overline{\text{INTR}}$<br>0111: $\overline{\text{QUALITY/REMOTE FAULT}}$<br>1000: $\overline{\text{RCVLED}}$<br>1001: Reserved<br>1010: $\overline{\text{MULTICOLOR[1]}}$<br>1011: Reserved<br>1100: Reserved<br>1101: Reserved<br>1110: Off (high)<br>1111: On (low) | 0000 |

## Write Enable

During a write to this register, setting 1 bit 15 to 1 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] of this register must be set to 01101 to enable read and write to the LED Selector register 1 address 1Ch.

## LED2 Selector

Bits [7:4] select the LED2 mode.

## LED1 Selector

Bits [3:0] select the LED1 mode.

## Register 1Ch (Shadow 01110): LED Selector 2

The following register is enabled by accessing register 1Ch with shadow value 01110 in bits [14:10].

***Table 37: LED Selector 2 Register (Address 1Ch, Shadow 01110)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0]<br>0: Read bits [9:0] | 0 |
| [14:10] | Shadow Register Selector | R/W | 01110: LED Selector 2 register | 01110 |
| [9:8] | Reserved | R/W | Write as 00, ignore on read | 00 |
| [7:4] | LED4 Selector | R/W | 0000: $\overline{\text{LINKSPD[1]}}$<br>0001: $\overline{\text{LINKSPD[2]}}$<br>0010: $\overline{\text{XMITLED}}$<br>0011: $\overline{\text{ACTIVITYLED}}$<br>0100: $\overline{\text{LED2/FDX}}$<br>0101: $\overline{\text{SLAVE}}$<br>0110: $\overline{\text{INTR}}$<br>0111: $\overline{\text{QUALITY/REMOTE FAULT}}$<br>1000: $\overline{\text{RCVLED}}$<br>1001: Reserved<br>1010: $\overline{\text{MULTICOLOR[2]}}$<br>1011: Reserved<br>1100: Reserved<br>1101: Reserved<br>1110: Off (high)<br>1111: On (low) | 0110 |
| [3:0] | LED3 Selector | R/W | 0000: $\overline{\text{LINKSPD[1]}}$<br>0001: $\overline{\text{LINKSPD[2]}}$<br>0010: $\overline{\text{XMITLED}}$<br>0011: $\overline{\text{ACTIVITYLED}}$<br>0100: $\overline{\text{LED2/FDX}}$<br>0101: $\overline{\text{SLAVE}}$<br>0110: $\overline{\text{INTR}}$<br>0111: $\overline{\text{QUALITY/REMOTE FAULT}}$<br>1000: $\overline{\text{RCVLED}}$<br>1001: Reserved<br>1010: $\overline{\text{MULTICOLOR[1]}}$<br>1011: Reserved<br>1100: Reserved<br>1101: Reserved<br>1110: Off (high)<br>1111: On (low) | 0011 |

### Write Enable

During a write to this register, setting bit 15 to 1 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

### Shadow Register Selector

Bits [14:10] of this register must be set to 01110 to enable read and write to the LED Selector 2 register address 1Ch.

### LED4 Selector

Bits [7:4] select the LED4 mode.

### LED3 Selector

Bits [3:0] select the LED3 mode.

## Register 1Ch (Shadow 01111): LED GPIO Control/Status

The following register is enabled by accessing register 1Ch with shadow value 01111 in bits [14:10].

***Table 38: LED GPIO Control/Status Register (Address 1Ch, Shadow 01111)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| [14:10] | Shadow Register Selector | R/W | 01111: LED GPIO Control/Status register. | 01111 |
| [9:8] | Reserved | R/W | Write as 00, ignore on read. | 00 |
| [7:4] | LED I/O Status | RO | Bit 7: LED4 pin status.<br>Bit 6: LED3 pin status.<br>Bit 5: LED2 pin status.<br>Bit 4: LED1 pin status.<br>1: LED pin is an input.<br>0: LED pin is an output. | 0h |
| [3:0] | Programmable LED I/O Control | R/W | Bit 3: LED4 pin control.<br>Bit 2: LED3 pin control.<br>Bit 1: LED2 pin control.<br>Bit 0: LED1 pin control.<br>1: Disable LED output.<br>0: Enable LED output. | 0h |

## Write Enable

During a write to this register, setting bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] must be set to 01111 to enable read and write to the register address 1Ch.

## LED I/O Status

Bits [7:4] read back the status of the LED pin.

## Programmable LED I/O Control

Setting bits [3:0] sets the LED pin to disable LED output. Clearing LED GPIO Control/Status register bits [3:0] sets the LED pin to enable LED output.

## Register 1Ch (Shadow 10101): SGMII Slave Register

The following is enabled by the SGMII Slave Register 1Ch with shadow value 10101 in bits [14:10].

***Table 39: SGMII Slave (Address 1Ch, Shadow 10101)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| 15 | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| 14:10 | Shadow Register Selector | R/W | Shadow Register Selector. | 10101 |
| 9 | SerDes Link | RO | 1: SGMII Linkup<br>0: SGMII Link-down. | 0 |
| 8 | SerDes Duplex | RO | 1: Link full-duplex.<br>0: Link half-duplex. | 1 |
| 7:6 | SerDes Speed | RO | 10: Reserved<br>01: SerDes speed 100 (SGMII 100).<br>00: Reserved.<br>11: Reserved. | 10 |
| 5 | SerDes Link Status Change | RO<br>LH | 1: Link status change detected since last read.<br>0: Link status change is not detected since last read. | 0 |
| 4:3 | Interface Select | RO | 00: Reserved<br>01: Reserved<br>10: SGMII—BroadR-Reach.<br>11: Reserved | 00 |
| 2 | Reserved | R/W | Reserved—write as 0 | 0 |
| 1 | Reserved | R/W | Reserved—write as 0 | 0 |

*Table 39: SGMII Slave (Address 1Ch, Shadow 10101) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 0 | Reserved | R/W | Reserved—write as 0 | 0 |

### Write Enable

During a write to this register, setting SGMII Slave Register Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

### SerDes Link

Bit 9 of the SGMII Slave register indicates if the link is up or down. When the link is up, this register returns a 1. When the link is down, this register returns 0.

### SerDes Duplex

Bit 8 of the SGMII Slave register indicates if the link is full-duplex or half-duplex. When the link is full-duplex, this register returns a 1. When the link is half-duplex, this register returns 0.

### SerDes Speed

Bits 7:6 of the SGMII Slave register indicate the traffic rate on the SerDes interface.

### SerDes Link Status Change

Bit 5 of the SGMII Slave register reports that the link status has changed since the last time this register was read.

### Interface Select

Bits 4:3 of the SGMII Slave register indicate the interface selection that is currently set for the SerDes interface.

## Register 1Ch (Shadow 11000): 1000BASE-X Autodetect SGMII

The following register is enabled by accessing register 1Ch with shadow value 11000 in bits [14:10].

*Table 40: 1000BASE-X Autodetect SGMII Register (Address 1Ch, Shadow 11000)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| 14:10 | Shadow Register Selector | R/W | 11000: Autodetect SGMII register. | 11000 |
| 9 | SerDes Resolution Fault | RO | 1: Selected field mismatch.<br>0: No mismatch or SGMII autodetect mode is disabled. | 0 |
| 8:3 | Reserved | RO | Write as 00h, ignore on read. | 00h |
| 2 | Reserved | R/W | Reserved | 1 |
| 1 | SGMII 100M RX FIFO Frequency Lock mode | R/W | 1: Enable FIFO Frequency Lock mode.<br>0: No operation. | 0 |
| 0 | Reserved | R/W | Write as 0, ignore on read. | 0 |

## Write Enable

During a write to this register, setting bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Register bits [14:10] must be set to 11000 to enable a read/write to the 1000BASE-X Autodetect SGMII address 1Ch.

## SerDes Resolution Fault

Bit 9 indicates there is a selected field mismatch on bit 0 of the auto-negotiation base page code-word. Otherwise, it reads 0.

## SGMII 100M RX FIFO Frequency Lock Mode

- 0: Normal operation
- 1: Uses phase-delay receive FIFO instead of the frequency offset FIFO to reduce latency (Switch/MAC and PHY must use same clock source

# Register 1Ch (Shadow 11110): Autodetect Medium Register

The following is enabled by Autodetect Medium Register 1Ch with shadow value 11110 in bits [14:10].

*Table 41: Autodetect Medium (Address 1Ch, Shadow 11110)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |

*Table 41: Autodetect Medium (Address 1Ch, Shadow 11110) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 14:10 | Shadow Register Selector | R/W | Shadow Register Selector. | 11110 |
| 9 | Reserved | R/W | Write as 0, ignore on read. | 0 |
| 8 | Invert Fiber SD From Pin | R/W | 1: Fiber signal detect is active low from pin.<br>0: Fiber signal detect is active high from pin. | 0 |
| 7 | Reserved | R/W | Write as 0 | 0 |
| 6 | Reserved | R/W | Write as 0 | 0 |
| 5 | Reserved | R/W | Write as 1, ignore on read. | 1 |
| 4 | Reserved | R/W | Write as 0 | 0 |
| 3 | Reserved | R/W | Write as 0, ignore on read. | 0 |
| 2 | Reserved | R/W | Write as 0 | 0 |
| 1 | Reserved | R/W | Write as 0 | 1 |
| 0 | Reserved | R/W | Write as 0 | 0 |

## Write Enable

During a write to this register, setting Autodetect Medium Register Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] of this register must be set to 11110 to enable read/write to the register address 1Ch.

## Invert Fiber SD From Pin

Bit 8 of this register inverts the polarity of SD pin.

# Register 1Ch (Shadow 11111): Mode Control Register

The following is enabled by Mode Control Register 1Ch with shadow value 11111 in bits [14:10].

***Table 42: Mode Control (Address 1Ch, Shadow 11111)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Write Enable | R/W | 1: Write bits [9:0].<br>0: Read bits [9:0]. | 0 |
| 14:10 | Shadow Register Selector | R/W | Shadow Register Selector. | 11111 |
| 9 | Reserved | RO | Write as 0, ignore on read. | 0 |
| 8 | Interface Mode Select Change | RO LH | 1: Interface Mode Select status changed since last read.<br>0: Interface Mode Select status did not change since last read. | 0 |
| 7 | Copper Link | RO | 1: Link is good on the copper interface.<br>0: Copper link is down. | 0 |
| 6 | Reserved | RO | Ignore on read | 0 |
| 5 | Copper Energy Detect | RO | 1: Energy detected on the copper interface.<br>0: Energy is not detected on the copper interface. | 0 |
| 4 | Reserved | RO | Ignore on read | 0 |
| 3 | Reserved | RO | Write as 1, ignore on read. | 1 |
| 2:1 | Interface Select | R/W | 00: Reserved.<br>01: Reserved.<br>10: SGMII to copper.<br>11: Reserved. | INTERF_SEL[1:0] |
| 0 | Enable 1000-X Registers | R/W | 1: Select SerDes registers 00–0Fh.<br>0: Select copper registers 00–0Fh. | 0 |

## Write Enable

During a write to this register, setting Mode Control Register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

## Shadow Register Selector

Bits [14:10] of this register must be set to 11111 to enable read/write to the register address 1Ch.

## Interface Mode Select Change

Bit 8 of the Mode Control register indicates that there is change in the interface mode selection (bits 2:1). Otherwise, it reads a 0.

### Copper Link

Bit 7 of the Mode Control register indicates that the link status of the copper interface is up. Otherwise, it reads a 0.

### Copper Energy Detect

Bit 5 of the Mode Control register indicates that energy is detected in the copper interface. Otherwise, it reads a 0.

### Interface Select

Bits [2:1] of the Mode Control register selects the interface type, overwriting the INTERF_SEL[1:0] pins.

### Enable 1000-X Registers

Bit 0 of the Mode Control register selects which Register Set is accessible. Writing a 1 to bit 0 activates the SerDes Register Set (registers 00h to 0Fh). Writing a 0 to bit 0 activates the copper Register Set.

## Register 1Eh: Test Register 1

***Table 43: Test Register 1 (Address 1Eh)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| [15] | CRC Error Counter Selector | R/W | 1: Receiver NOT_OK Counters (register 14h) becomes 16-bit CRC error counter (CRC errors are counted only after this bit is set).<br>0: Normal operation. | 0 |
| [14:13] | Reserved | R/W | Write as 00, ignore on read. | 00 |
| [12] | Force Link BroadR-Reach | R/W | 1: Force link pass.<br>0: Normal operation. | 0 |
| [11:0] | Reserved | R/W | Write as 0000, ignore on read. | 000h |

### CRC Error Counter Selector

Setting bit 15 of Test Register 1 enables the “Register 14h: BroadR-Reach Receiver NOT_OK Counter” to start counting CRC errors in receive packets.

### Force Link

Setting bit 12 forces the Link State Machine into the link pass state.

# SerDes Register Descriptions

## Register 00h: SerDes MII Control

The following SerDes registers are enabled by writing to "Register 1Ch (Shadow 11111): Mode Control Register" bit 0 = 1 or when the device is powered up in SerDes mode.

***Table 44: SerDes MII Control Register (Address 00h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reset | R/W SC | 1: PHY reset.<br>0: Normal operation. | 0 |
| 14 | Internal Loopback | R/W | 1: Loopback mode.<br>0: Normal operation. | 0 |
| 13 | Reserved | RO | Write as 0, ignore on read. | 0 |
| 12 | Auto-Negotiation Enable | R/W | 1: Auto-negotiation enabled.<br>0: Auto-negotiation disabled. | 1 |
| 11 | Power-Down | R/W | 1: Power-down.<br>0: Normal operation. | 0 |
| 10 | Isolate | R/W | 1: Electrically isolate PHY from SGMII/SerDes.<br>0: Normal operation. | 0 |
| 9 | Restart Auto-Negotiation | R/W SC | 1: Restarting auto-negotiation.<br>0: Auto-negotiation restart complete. | 0 |
| 8 | Duplex Mode | R/W | 1: Full-duplex.<br>0: Reserved. | 1 |
| 7:0 | Reserved | R/W | Write as 40h, ignore on read. | 40h |

### Reset

To reset the BCM89820 transceiver by software control, 1 must be written to bit 15 of the SerDes MII Control register. This bit clears itself after the reset process is complete, and does not need to be cleared using a second MII write. Writes to other SerDes MII Control register bits have no effect until the reset process is completed, which requires approximately 2.0 microseconds. Writing 0 to this bit has no effect. When this bit is read during the reset process, a 1 is returned; otherwise, a 0 is returned.

### Internal Loopback

The BCM89820 can be placed into internal loopback mode by setting bit 14 of the SerDes MII Control register. Loopback mode can be cleared by writing 0 to bit 14 of the SerDes MII Control register or by resetting the chip. When this bit is read and the chip is in loopback mode, a 1 is returned; otherwise, a 0 is returned.

## Auto-Negotiation Enable

When bit 12 of the SerDes MII Control register is set, the BCM89820 mode of operation is controlled by auto-negotiation. When this bit is cleared, the BCM89820 mode of operation is determined by the duplex mode. When this bit is read with auto-negotiation enabled, a 1 is returned; otherwise, a 0 is returned.

## Power-Down

When bit 11 of the SerDes MII Control register is set, the BCM89820 is placed into I/O power standby mode. The SerDes interface is powered down when the device is in copper mode.

**Note:** When auto-medium mode detection is enabled, bit 11 of the SerDes MII Control register is controlled by the internal state machine to power down the interface when it is selected. A 1 must not be written to this bit.

## Isolate

The BCM89820 can be isolated from the SGMII bus by setting bit 10 of the SerDes MII Control register. All SGMII/SerDes outputs are tristated, and all SGMII/SerDes inputs are ignored. Because the management interface is still active, isolate mode can be cleared by writing 0 to bit 10 of the SerDes MII Control register or resetting the chip. When this bit is read and the chip is in isolate mode, a 1 is returned; otherwise, a 0 is returned. The default of this bit is 0.

## Restart Auto-Negotiation

Setting bit 9 of the SerDes MII Control register forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns 0.

## Duplex Mode

When auto-negotiation is disabled, duplex mode can be controlled by writing to bit 8 of the SerDes MII Control register. The BCM89820 only supports full-duplex operation. The default value of this bit is determined by the FDX pin at reset.

# Register 01h: SerDes MII Status

The following SerDes registers are enabled by writing to “Register 1Ch (Shadow 11111): Mode Control Register” bit 0 = 1.

***Table 45: SerDes MII Status Register (Address 01h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | RO L | Ignore on read | 0 |

*Table 45: SerDes MII Status Register (Address 01h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 14 | 100BASE-X Full-duplex Capable | RO L | 1: 100BASE-X full-duplex capable.<br>0: Not 100BASE-X full-duplex capable. | 0 |
| 13 | Reserved | RO L | Ignore on read | 0 |
| 12 | Reserved | RO L | Ignore on read | 0 |
| 11 | Reserved | RO L | Ignore on read | 0 |
| 10 | Reserved | RO L | Ignore on read | 0 |
| 9 | Reserved | RO L | Ignore on read | 0 |
| 8 | Extended Status | RO H | 1: Extended status information in reg 0Fh.<br>0: No extended status information in reg 0Fh. | 1 |
| 7 | Reserved | RO | Write as 0, ignore on read. | 1 |
| 6 | Management Frames Preamble Suppression | RO H | 1: Preamble can be suppressed<br>0: Preamble always required | 1 |
| 5 | Auto-Negotiation Complete | RO | 1: Auto-negotiation complete<br>0: Auto-negotiation in progress | 0 |
| 4 | Remote Fault | RO LH | 1: Remote fault detected.<br>0: No remote fault detected. | 0 |
| 3 | Auto-Negotiation Ability | RO H | 1: Auto-negotiation capable.<br>0: Not auto-negotiation capable. | 1 |
| 2 | Link Status | RO LL | 1: Link is up (link pass state).<br>0: Link is down (link fail state). | 0 |
| 1 | Jabber Detect | RO L | 1: Jabber condition detected.<br>0: No jabber condition detected. | 0 |
| 0 | Extended Capability | RO H | 1: Extended register capabilities.<br>0: No extended register capabilities. | 1 |

## 100BASE-X Full-Duplex Capable

The BCM89820 is not capable of 100BASE-X full-duplex operation and returns 0 when bit 14 of the SerDes MII Status register is read.

## Extended Status

The BCM89820 contains an IEEE Extended Status register at address 0Fh and returns 1 when bit 8 of the SerDes MII Status register is read.

## Management Frames Preamble Suppression

The BCM89820 accepts MII management frames whether or not they are preceded by the preamble pattern and returns 1 when bit 6 of the SerDes MII Status register is read.

**Note:** Preamble is still required on the first read or write.

## Auto-Negotiation Complete

The BCM89820 returns 1 in bit 5 of the SerDes MII Status register when auto-negotiation has completed, and the contents of registers 4, 5, and 6 are valid. This bit returns 0 while auto-negotiation is in progress.

## Remote Fault

The BCM89820 returns 1 in bit 4 of the SerDes MII Status register when its link partner has signaled a remote fault condition. When a remote fault occurs, the bit is set and remains so until the remote fault condition has been cleared and the register is read.

## Auto-Negotiation Ability

Even if the auto-negotiation function has been disabled, the BCM89820 is capable of performing IEEE auto-negotiation and returns 1 when bit 3 of the SerDes MII Status register is read.

## Link Status

The BCM89820 returns 1 in bit 2 of the SerDes MII Status register when the link monitor is in the link pass state (indicating that a valid link has been established); otherwise it returns 0. When a link failure occurs, the Link Status bit is latched at 0 and remains so until the bit is read and the BCM89820 is in the link pass state.

## Jabber Detect

The jabber detect function is not supported for the SerDes. This bit always returns 0.

## Extended Capability

The BCM89820 supports extended capability registers and returns 1 when bit 0 of the 1000BASE-X MII Status register is read.

# Register 04h: SerDes Auto-Negotiation Advertisement

The following SerDes registers are enabled by writing to “Register 1Ch (Shadow 11111): Mode Control Register” bit 0 = 1.

*Table 46: SerDes Auto-Negotiation Advertisement Register (Address 04h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| ***SGMII Mode*** | | | | |
| 15 | Copper Link | RO | 1: Link established at copper interface.<br>0: Link is not established at copper interface. | 0 |
| 14 | Acknowledge | RO | 1: Link partner has received link code word.<br>0: Link partner has not received link code word. | 0 |
| 13 | Reserved | RO | Write as 0, ignore on read. | 0 |
| 12 | Copper Duplex | RO | 1: Copper link partner is full-duplex.<br>0: Copper link partner is not full-duplex. | 0 |
| 11:10 | Copper Speed | RO | 00: Reserved<br>01: 100 Mb/s.<br>10: Reserved.<br>11: Reserved. | 00 |
| 9:1 | Reserved | RO | Write as 000h, ignore on read. | 000h |
| 0 | SGMII Selector | RO | SGMII selector. | 1 |

***Note:*** When SGMII mode is enabled, reading register 04h reflects the ability sent to the link partner. The values written to the register are stored, but not used.

## SGMII Mode

### Copper Link

This bit indicates the link is established on the copper interface.

### Acknowledge

This bit indicates the SGMII link partner has received the link code word.

### Copper Duplex

This bit indicates the copper link partner is linked up at full-duplex mode.

### Copper Speed

Bits [11:10] indicate the copper linkup speed.

# Register 05h: SerDes Auto-Negotiation Link Partner Ability

The following SerDes registers are enabled by writing to "Register 1Ch (Shadow 11111): Mode Control Register" bit 0 = 1.

***Table 47: SerDes Auto-Negotiation Link Partner Ability Register—Base Page (Address 05h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| ***SGMII Mode*** | | | | |
| 15 | Copper Link | R/O | 1: Link established at copper interface.<br>0: Link is not established at copper interface. | 0 |
| 14 | Acknowledge | R/O | 1: Link partner has received link code word.<br>0: Link partner has not received link code word. | 0 |
| 13 | Reserved | R/O | Write as 0, ignore on read. | 0 |
| 12 | Copper Duplex | R/O | 1: Copper link partner is full-duplex.<br>0: Copper link partner is not full-duplex. | 0 |
| 11:10 | Copper Speed | R/O | 00: Reserved<br>01: 100 Mb/s.<br>10: Reserved.<br>11: Reserved. | 00 |
| 9:1 | Reserved | R/O | Write as 00h, ignore on read. | 00h |
| 0 | SGMII Selector | R/O | 1: SGMII mode.<br>0: 1000BASE-X mode. | 1 |
| ***Note:*** As indicated by bit 5 of the SerDes MII Status register, the values contained in the Auto-Negotiation Link Partner Ability register are guaranteed to be valid only after auto-negotiation has successfully completed. | | | | |

## SGMII Mode

### Copper Link

This bit indicates the link is established on the copper interface. The MAC sends 0 only.

### Acknowledge

This bit indicates the SGMII link partner has received the link code word.

### Copper Duplex

This bit indicates the copper link partner is linked up at full-duplex mode. The MAC sends 0 only.

### Copper Speed

Bits [11:10] indicate the copper linkup speed. The MAC sends 0 only.

# Expansion Registers

## Expansion Register 00h: Receive/Transmit Packet Counter

Expansion register 00h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits [11:0] = F00h, and read and write access is through register 15h.

***Table 48: Expansion Register 00h: Receive/Transmit Packet Counter***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:0] | Packet Counter | R/W CR | Returns the transmitted and received packet count. | 0000h |

### Packet Counter

The mode of this counter is set by bit 11 of "Miscellaneous Control Register (Address 18h, Shadow 111)". Either receive or transmit packets are counted. This counter is cleared on read and freezes at FFFFh.

## Expansion Register 04h: Multicolor LED Selector

Expansion register 04h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits 11:0 = F04h, and read and write access is through register 15h.

***Table 49: Expansion Register 04h: Multicolor LED Selector***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:10] | Reserved | R/W | Write as 00h, ignore on read. | 00h |
| [9] | Flash Now | R/W SC | 1: Initiate a multicolor LED flash. This works only when the multicolor selector is set to 0111. | 0 |
| [8] | In Phase | R/W | 1: $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in phase.<br>0: $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in opposite phase.<br>***Note:*** This is only valid when Multicolor LED Selector bits are set to 0000, 0010, 0011, 0110, 0111, 1000, 1001, 1010. | 0 |

*Table 49: Expansion Register 04h: Multicolor LED Selector (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [7:4] | MULTICOLOR[2] LED Selector | R/W | Selects the Multicolor mode for MULTICOLOR[2] LED<br>0000: Encoded link/activity LED<br>0001: Encoded speed LED<br>0010: Activity flash LED<br>0011: Full-duplex LED<br>0100: Forced off<br>0101: Forced on<br>0110: Alternating LED (toggling between two of the states at 50% duty cycle with a 320 ms period)<br>0111: Flashing LED (toggling between 2 of the states with an 80 ms period)<br>1000: Link LED<br>1001: Activity LED<br>1010: Programmable blink LED | 0h |
| [3:0] | MULTICOLOR[1] LED Selector | R/W | Selects the Multicolor mode for MULTICOLOR[1] LED.<br>0000: Encoded link/activity LED<br>0001: Encoded speed LED<br>0010: Activity flash LED<br>0011: Full-duplex LED<br>0100: Forced off<br>0101: Forced on<br>0110: Alternating LED (toggling between 2 of the states at 50% duty cycle with a 320 ms period)<br>0111: Flashing LED (toggling between 2 of the states with an 80 ms period)<br>1000: Link LED<br>1001: Activity LED<br>1010: Programmable blink LED | 0h |

## Flash Now

Asserting this bit causes a single flash to occur on either MULTICOLOR[2:1] LED, as long as its multicolor selector is set to 0111.

## In Phase

When both LEDs are selected to the same mode, the MULTICOLOR[2:1] output pins toggle at the same time. This bit determines whether the pins are identical to each other or are inverses of each other. When the two LED pins are attached to a special multicolored LED, the resulting LED colors alternate either between off/amber (in phase) or red/green (out of phase).

## MULTICOLOR[2] LED Selector

The bits [7:4] select the multicolor LED mode for MULTICOLOR[2]. The user must determine what functions should appear on the two LED pins.

***Example:*** To enable color combinations other than the two mentioned above (off/amber and red/green), the user can put one of the selectors to the preferred toggle mode and the other selector to a forced one.

## MULTICOLOR[1] LED Selector

Bits [3:0] select the multicolor LED mode for MULTICOLOR[1].

# Expansion Register 05h: Multicolor LED Flash Rate Controls

Expansion register 05h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits 11:0 = F05h, and read and write access is through register 15h.

***Table 50: Expansion Register 05h: Multicolor LED Flash Rate Controls***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:12] | Reserved | R/W | Write as 0h, ignore on read. | 0h |
| [11:6] | Alternating Rate | R/W | Determines the width and gap for multicolor LED selector 0110 (alternating LED mode).<br>00h: 21 ms width, 21 ms gap<br>01h: 42 ms width, 42 ms gap<br>02h: 63 ms width, 63 ms gap<br>...<br>07h: 168 ms width, 168 ms gap<br>...<br>3Fh: 1.344s | 07h |
| [5:0] | Flash Rate | R/W | Determines the width and minimum gap of every flash pulse for multicolor LED selector 0000 (encoded link/Activity mode), 0010 (Activity Flash mode) and 0111 (Flashing LED mode).<br>00h: 21 ms width, 21 ms gap<br>01h: 42 ms width, 42 ms gap<br>02h: 63 ms width, 63 ms gap<br>...<br>3Fh: 1.344s | 01h |

## Alternating Rate

Setting Bits [11:6] changes the width and gap of the alternating LED modes. These bits are only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0110. The duty cycle of the LEDs is exactly 50%.

### Flash Rate

Setting Bits [5:0] determines the width and minimum gap of the flashing pulse. These bits are only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111. The duty cycle of the flash rate is not exactly 50%.

## Expansion Register 06h: Multicolor LED Programmable Blink Controls

Expansion register 06h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits [11:0] = F06h, and read and write access is through register 15h.

***Table 51: Expansion Register 06h: Multicolor LED Programmable Blink Controls***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:6] | Reserved | R/W | Write as 000h, ignore on read. | 000h |
| [5] | Blink Update Now | R/W | 1: Change to the new blink rate now.<br>0: Wait 1s before changing the blink rate.<br>Controls when a change in the blink rate is actually displayed on the programmable blink LED. | 0 |
| [4:0] | Blink Rate | R/W | Programs the number of blinks per second of the programmable blink LED.<br>00000: No blink<br>00001: 1 blink per second<br>00010: 2 blinks per second<br>00011: 3 blinks per second<br>...<br>11111: 31 blinks per second | 00000 |

### Blink Update Now

Setting bit 5 updates the blink rate immediately. Clearing this bit causes the blink rate to be updated after the 1s interval timer expires. This bit is only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111.

### Blink Rate

Setting bits [4:0] determines the blink rate of the programmable blink LED. These bits are only valid when the MULTICOLOR[1] LED Selector and/or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111.

# Expansion Register 0Eh: Synchronous Ethernet Controls

Expansion register 0Eh is enabled by writing to "Expansion Register Access Register (Address 17h)" bits [11:0] = F0Eh, and read and write access is through register 15h.

***Table 52: Expansion Register 0Eh: Synchronous Ethernet Controls***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:12] | Reserved | R/W | Write as 0000, ignore on read. | 0000 |
| [11] | MII-Lite Enable | R/W | MII-Lite enable (no TXER, RXER, CRS, COL). | 0 |
| [10] | TX SOP Enable | R/W | 1: Enable TX SOP output. | 0 |
| [9:8] | TX SOP Select | R/W | Mapping of TX SOP to output pins:<br>00: LED1<br>01: LED2<br>10: LED3<br>11: LED4 | 00 |
| [7] | RX SOP Enable | R/W | 1: Enable RX SOP output. | 0 |
| [6:5] | RX SOP Select | R/W | Mapping of RX SOP to output pins:<br>00: LED1<br>01: LED2<br>10: LED3<br>11: LED4 | 00 |
| [4] | Reserved | R/W | Write as 0, ignore on read. | 0 |
| [3] | RX_ER Mux Control | R/W | RX_ER mux control. | 0 |
| [2:0] | Reserved | R/W | – | 0h |

## MII-Lite Enable

Setting bit 11 allows the device to operate in a fashion similar to MII mode, except without the functions of the TXER, RXER, CRS, and COL pins. This mode is only available for 10 Mb/s and 100 Mb/s speeds.

## TX SOP Enable

Writing 1 to bit 10 enables a special transmit start-of-packet (SOP) indicator to be output from the device.

## TX SOP Select

Bits [9:8] determine which LED output is mapped to the TX SOP indicator.

## RX SOP Enable

Writing 1 to bit 7 enables a special receive start-of-packet (SOP) indicator to be output from the device.

## RX SOP Select

Bits [6:5] determine which LED output is mapped to the RX SOP indicator.

## RXCLK Select

Bit 4 determines which output pin contains the recovered clock. When bit 4 is 1, the recovered clock appears on the RXC output, and when bit 4 is 0, it appears on the CLK125 output pin.

## RX_ER Mux Control

Bit 3 allows the RX_ER function, which does not have its own pin in RGMII mode, to be mapped to the LED4 output pin.

# Expansion Register 70h: Soft Reset Register

Expansion register 70h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits[11:0] = F70h, and read and write access is through register 15h.

***Table 53: Expansion Register 70h: Soft Reset Register***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| [15:3] | Reserved | R/W | Write as 0, ignore on read. | 0001h |
| [2:1] | Reserved | R/W | Write as 0, ignore on read. | 00 |
| [0] | Soft Reset | R/W SC | 1: Issue soft-reset for 640 ns that clears all registers in the BCM89820 except for MDIO control registers. All MDIO status registers are cleared.<br>0: Normal operation. | 0 |

### Soft Reset

Setting bit 0: 1 issues a soft reset for 640 ns that clears all registers in the BCM89820 except for the MDIO control registers. All MDIO status registers are cleared.

# Expansion Register 90h: BroadR-Reach LRE Misc Control

Expansion register 90h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits [11:0] = F90h, and read and write access is through register 15h.

***Table 54: Expansion Register 90h: BroadR-Reach LRE Misc Control***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Digital High Pass Filter | R/W | 1: Enable digital HPF and bypass analog HPF.<br>0: Enable analog HPF and bypass digital HPF. | 0 |
| [14:2] | Reserved | R/W | Reserved. Write as 0 ignore on read. | 0000h |
| [1] | BroadR-Reach Force Link Control | R/W | 1: Force BroadR-Reach transceiver link up.<br>0: Normal operation. | 0 |
| [0] | BroadR-Reach Enable | R/W | 1: Enable BroadR-Reach function.<br>0: Disable BroadR-Reach function. | 1 |

## Digital High Pass Filter

Setting bit 15 to 1 enables the digital high-pass filter. Setting bit 15 to 0 enables the analog high-pass filter and disables the digital HPF.

## BroadR-Reach Force Link Control

This bit forces the BroadR-Reach transceiver to link up.

## BroadR-Reach Enable

This bit enables BroadR-Reach operation.

# Expansion Register 91h: BroadR-Reach LRE Misc Control

Expansion register 91h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits[11:0] = F91h, and read and write access is through register 15h.

***Table 55: Expansion Register 91h: BroadR-Reach LRE Misc Control***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15] | Digital HPF Overwrite | R/W | Overwrite the decision for the enabling of digital HPF.<br>1: Digital HPF enable is controlled by Exp_Reg90[15].<br>0: Digital HPF enable is not controlled by Exp_Reg90[15]. | 0 |
| [14:12] | Reserved | RO | — | 0 |

*Table 55: Expansion Register 91h: BroadR-Reach LRE Misc Control (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [11:9] | BR-PGA | R/W | BroadR-Reach PGA gain control:<br>100: 0.7X gain (~0.689X)<br>010: 1X gain<br>001: 3X gain (~2.92X)<br>000: 6X gain (~5.31X) | 010 |
| [8:4] | Reserved | R/W | Must write value 01010. | 00010 |
| [3:0] | Reserved | RO | — | 8h |

### Digital HPF Overwrite

Setting bit 15 to 1 overwrites the decision for the enabling of digital HPF.

### BR-PGA

Bits [11:9] provide various PGA gain control values.

## Expansion Register 92h: BroadR-Reach LRE Misc Control

Expansion register 92h is enabled by writing to "Expansion Register Access Register (Address 17h)" bits [11:0] = F92h, and read and write access is through register 15h.

*Table 56: Expansion Register 92h: BroadR-Reach LRE Misc Control*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| [15:13] | Reserved | RO | — | — |
| [12:11] | BroadR-Reach Edge Rate Selection | R/W | Shapes the BroadR-Reach transmitter's waveform. | 10 |
| [10:6] | Reserved | RO | — | — |
| [5] | Reserved | R/W | Must write value of 1. | 1 |
| [4:0] | Reserved | RO | — | — |

#### BroadR-Reach Edge Rate Selection

This bit shapes the BroadR-Reach transmitter's waveform.

# Section 6: Timing and AC Characteristics

The following table and Figure 6 show the timing and AC characteristics of the BCM89820.

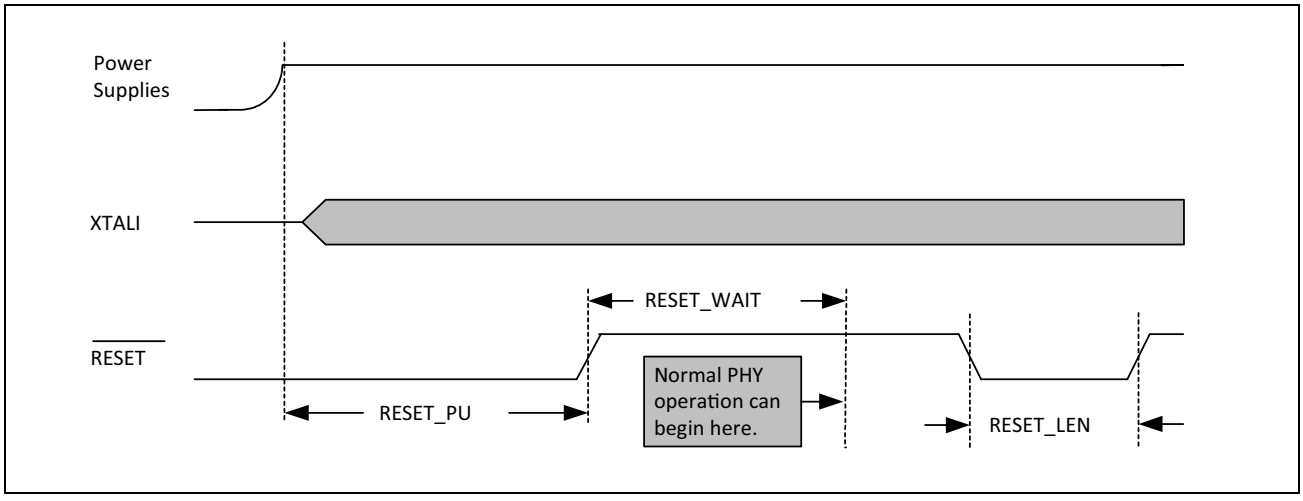
***Table 57: Reset Timing***

| *Parameter* | *Symbol* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| Power up to $\overline{\text{RESET}}$ deassertion | RESET_PU | 10 | — | — | ms |
| $\overline{\text{RESET}}$ deassertion to normal PHY operation | RESET_WAIT | 20 | — | — | µs |
| $\overline{\text{RESET}}$ pulse length | RESET_LEN | 2 | — | — | µs |
| $\overline{\text{RESET}}$ rise/fall time | — | — | — | 25 | ns |

***Note:***

- When $\overline{\text{RESET}}$ is low, there must be a valid clock signal at the XTALI input.
- All external power supplies must be stable.
- Internal regulator output REGOUT requires approximately 1 ms to stabilize after the voltage to the regulator input pin REGSUPPLY is stable.
- MII register read and write access and normal PHY operation can start at the end of the RESET_WAIT time.
- RESET_PU must be performed when the device is first powered up. Software reset or RESET_LEN are not required after RESET_PU.
- Software reset or RESET_LEN should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a software reset or a RESET_LEN, normal PHY operation can begin after waiting RESET_WAIT time of 20 µs.

**Figure 6: Reset Timing**



# Clock Input Timing

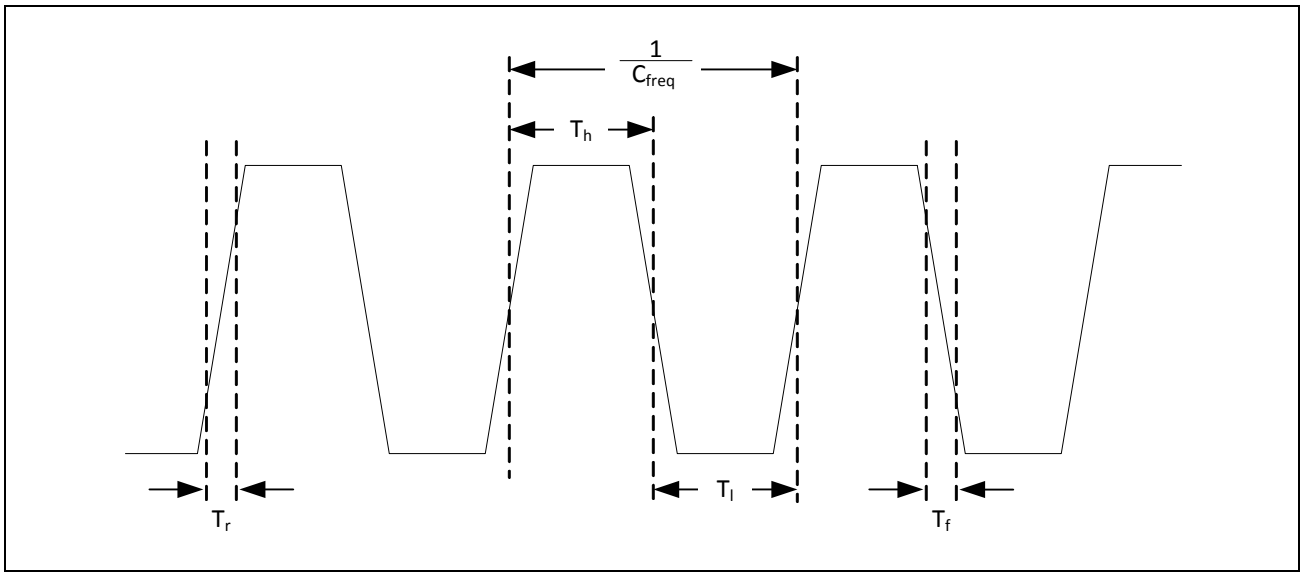
***Table 58: Clock Input Timing***

| *Parameter* | *Symbol* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| Frequency | $C_{freq}$ | — | 25 | — | MHz |
| Accuracy[a] | — | –100 | — | +100 | ppm |
| Duty Cycle Distortion[b] | — | 40 | — | 60 | % |
| Rise/Fall time[c] | $T_r/T_f$ | — | — | 4 | ns |
| RMS Phase Jitter[d] | – | — | — | 1.5 | ps-rms |

***Note:*** Do not use PLL-based oscillators or zero-delay buffers as a source for REFCLK because this introduces excessive jitter that may result in unacceptable bit error rate performance.

a. The clock accuracy specification includes the total variance due to crystal/oscillator frequency tolerance, temperature, aging, and circuit variations.
b. Measured at 50% point.
c. Measured at the 20% to 80% points.
d. Fj = 12 kHz to 20 MHz offset frequency.

**Figure 7: Clock Input Timing**

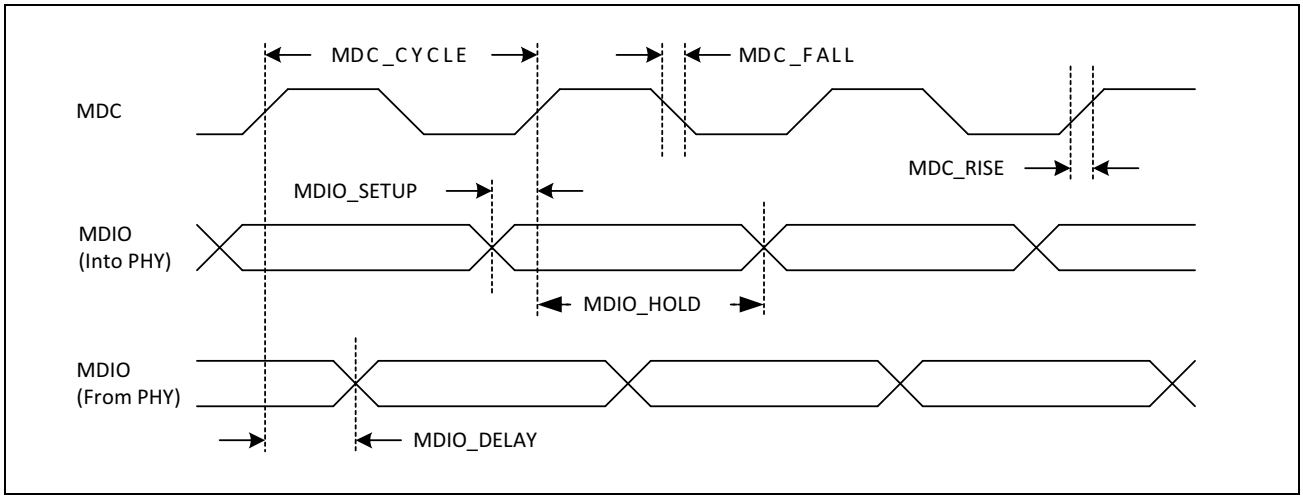


# Management Interface Timing

***Table 59: Management Interface Timing***

| *Parameter* | *Symbol* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| MDC cycle time | MDC_CYCLE | 80 | — | — | ns |
| MDC high/low | — | 30 | — | — | ns |
| MDIO input setup time to MDC rising | MDIO_SETUP | 10 | — | — | ns |
| MDIO input hold time from MDC rising | MDIO_HOLD | 10 | — | — | ns |
| MDIO output delay from MDC rising | MDIO_DELAY | 0 | — | 50 | ns |

**Figure 8: Management Interface Timing**



# SGMII Timing

***Table 60: SGMII Timing***

| *Parameter* | *Symbol* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| Clock signal duty cycle | Duty_C | 48 | — | 52 | % |
| Maximum Pk-PK output jitter | $T_{JIT}$ | — | — | 192 | ps pk-pk |
| Fall time (20% to 80%) SGOUT± | $T_F$ | 100 | — | 200 | ps |
| Rise time (20% to 80%) SGOUT± | $T_R$ | 100 | — | 200 | ps |
| Skew between two members of a differential pair SGOUT± | $T_{SKEW}$[a] | — | — | 20 | ps |
| Clock to data relationship from either edge of the clock to valid data | $T_{CLOCK2Q}$[b] | 250 | — | 550 | ps |

a. Measured at 50% transition.
b. Measured at 0V differential.

# Section 7: Electrical Characteristics

The following tables show the electrical characteristics of the BCM89820.

***Table 61: Absolute Maximum Ratings***

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Supply voltage (OVDD) | — | GND – 0.3 | 3.8 | V |
| Supply voltage (AVDD, BIASVDD, XTALVDD) | — | GND – 0.3 | 3.8 | V |
| Supply voltage (AVDDL, DVDD) | — | GND – 0.3 | 1.4 | V |
| Storage temperature | $T_{STG}$ | –55 | +150 | °C |
| ESD Protection (Human Body Model) | $V_{ESD}$ | –2500 | +2500 | V |
| ***Note:*** These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device. | | | | |

***Table 62: DC Characteristics***

| Parameter | Symbol | Minimum | Maximum | Unit | Condition |
|---|---|---|---|---|---|
| ***Power Supply*** | | | | | |
| Supply voltage 3.3V | $V_{OVDD}$ | 3.14 | 3.46 | V | — |
| Supply voltage 2.5V | $V_{OVDD}$ | 2.38 | 2.62 | V | — |
| Supply voltage 3.3V | $V_{AVDD, BIASVDD, XTALVDD}$ | 3.14 | 3.46 | V | — |
| Supply voltage 1.2V | $V_{AVDDL, DVDD, PLLVDD}$ | 1.14 | 1.26 | V | — |
| ***XTALI Pin*** | | | | | |
| Input high voltage (XTALI) | $V_{IH}$ | 2.40 | XTALVDD + 0.5 | V | XTALI pin |
| Input low voltage (XTALI) | $V_{IL}$ | –0.30 | +1.20 | V | XTALI pin |
| ***Digital Pin Operating @ 3.3V OVDD or 2.5V OVDD*** | | | | | |
| Input high voltage, digital pin | $V_{IH}$ | 2.0 | OVDD + 0.30 | V | — |
| Input low voltage, digital pin | $V_{IL}$ | –0.30 | +0.80 | V | — |
| Output high voltage, digital pin | $V_{OH}$ | OVDD – 0.40 | — | V | $I_{OH}$ = –8 mA |
| Output low voltage, digital pin | $V_{OL}$ | — | 0.40 | V | $I_{OL}$ = 8 mA |
| ***Note:*** When OVDD = 2.5V, LED pins have a maximum $I_{OH}$ of –6 mA and maximum $I_{OL}$ of 6 mA. | | | | | |
| ***RESET, MDIO, MDC Pins*** | | | | | |
| Input high voltage (RESET, MDIO, MDC) | $V_{IH}$ | 2.0 | OVDD + 0.30 | V | $\overline{\text{RESET}}$, MDIO, MDC pins |
| Input low voltage (RESET, MDIO, MDC) | $V_{IL}$ | –0.30 | +0.80 | V | $\overline{\text{RESET}}$, MDIO, MDC pins |

***Table 62: DC Characteristics (Cont.)***

| *Parameter* | *Symbol* | *Minimum* | *Maximum* | *Unit* | *Condition* |
|---|---|---|---|---|---|
| Hysteresis @ 3.3V OVDD | $V_{HYST}$ | 150 | 400 | mV | $\overline{\text{RESET}}$, MDIO, MDC pins |
| Hysteresis @ 2.5V OVDD | $V_{HYST}$ | 90 | 400 | mV | $\overline{\text{RESET}}$, MDIO, MDC pins |

# Section 8: Power Requirements

*Table 63: BroadR-Reach One-Pair Operating Mode*

| *Supply* | *Max Voltage (V)* | *Supply (mA)* | *Power (mW)* |
|---|---|---|---|
| DVDD | 1.26 | TBD | TBD |
| AVDDL | 1.26 | TBD | TBD |
| AVDDH | 3.47 | TBD | TBD |
| OVDD | 3.47 | TBD | TBD |
| Total Power | | | TBD |
| ***Note:*** Maximum power is less than 340 mW. Power measured with all LEDs disabled. | | | |

*Table 64: Standby Mode*

| *Supply* | *Voltage (V)* | *Supply (mA)* | *Power (mW)* |
|---|---|---|---|
| DVDD | 1.2 | 3.1 | 3.7 |
| AVDDL | 1.2 | 0.5 | 0.6 |
| AVDDH | 3.3 | 6.6 | 21.8 |
| OVDD | 3.3 | 1.0 | 3.3 |
| Total Power | | | 29.4 |

*Table 65: IDDQ Mode*

| *Supply* | *Voltage (V)* | *Supply (mA)* | *Power (mW)* |
|---|---|---|---|
| DVDD | 1.2 | 1.4 | 1.7 |
| AVDDL | 1.2 | 0.2 | 0.2 |
| AVDDH | 3.3 | 2.8 | 9.2 |
| OVDD | 3.3 | 0.9 | 3.0 |
| Total Power | | | 14.2 |

# Section 9: Mechanical and Thermal

## RoHS-Compliant Packaging

Broadcom offers an RoHS package that is compliant with RoHS and WEEE directives. The table below shows the RoHS-compliant parts.

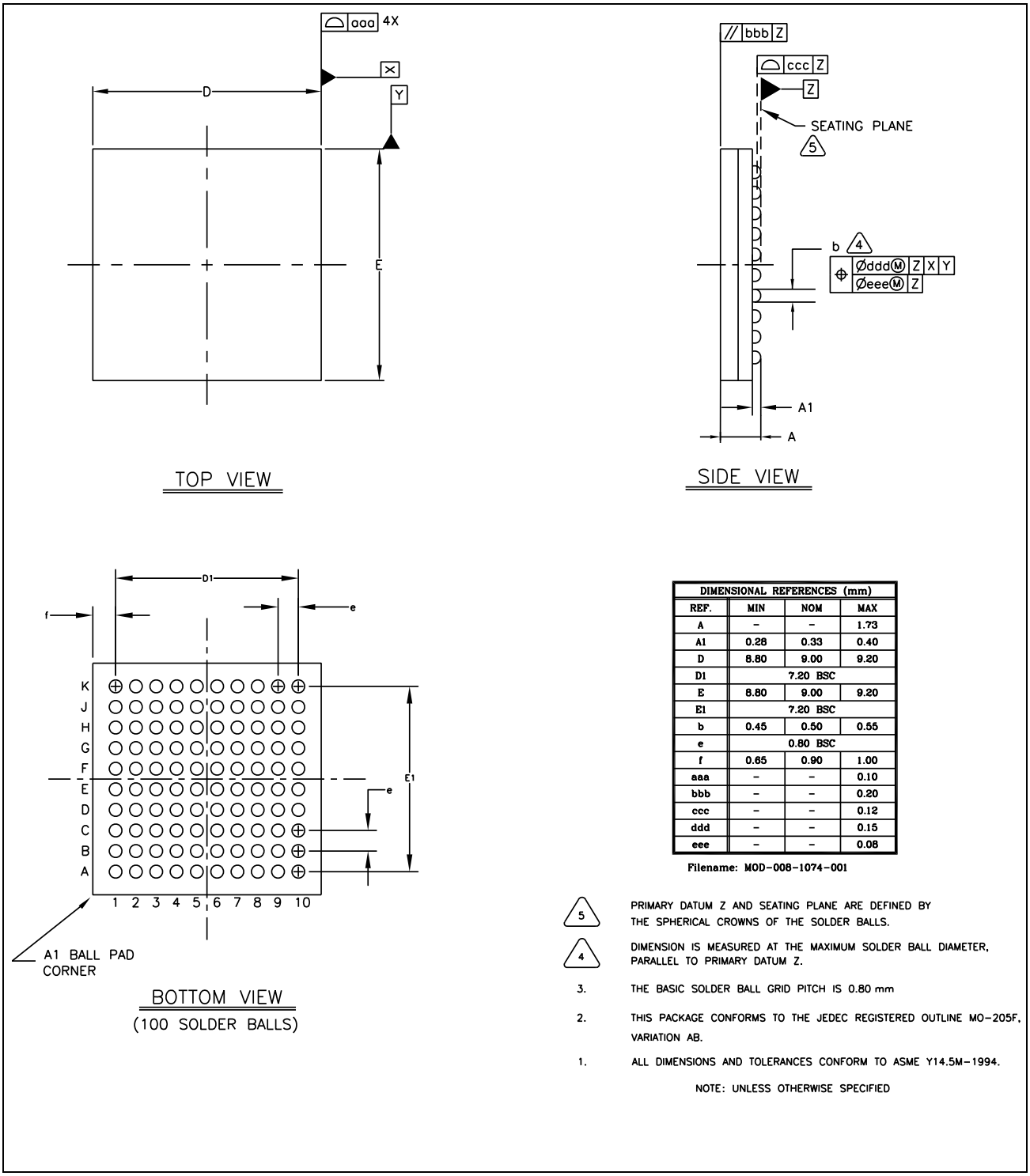
RoHS-compliant parts have the letter G added to the top line of the part marking. Refer to the *Pkg Reflow Process Guidelines for Surface Mount Assemblies* (document number PACKAGING-AN1xx-R) for additional details.

***Table 66: RoHS-Compliant Packages***

| *Part Number* | *Package* | *Solder Composition* | *Maximum Reflow Temperature* |
|---|---|---|---|
| BCM89820A2AMLG | 100-ball FBGA (RoHS-compliant package) | 100% Sn (Tin-Matte) | 260°C |

# Mechanical Information

**Figure 9: 100-ball FBGA Package**




| DIMENSIONAL REFERENCES (mm) | | | |
|---|---|---|---|
| REF. | MIN | NOM | MAX |
| A | – | – | 1.73 |
| A1 | 0.28 | 0.33 | 0.40 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | | 7.20 BSC | |
| E | 8.80 | 9.00 | 9.20 |
| E1 | | 7.20 BSC | |
| b | 0.45 | 0.50 | 0.55 |
| e | | 0.80 BSC | |
| f | 0.65 | 0.90 | 1.00 |
| aaa | – | – | 0.10 |
| bbb | – | – | 0.20 |
| ccc | – | – | 0.12 |
| ddd | – | – | 0.15 |
| eee | – | – | 0.08 |

Filename: MOD-008-1074-001

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.80 mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-205F, VARIATION AB.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTE: UNLESS OTHERWISE SPECIFIED

# Thermal Information

This section includes basic thermal information pertaining to the BCM89820 100-ball FBGA packages.

The following table provides a comparison of Theta-$J_A$ versus airflow for the 100-ball FBGA package. $Theta_{JC}$ for this package is TBD°C/W. The BCM89820 is designed and rated for a maximum ambient temperature of 105°C and a maximum junction temperature of 125°C.

***Table 67: Theta-$J_A$ vs. Airflow for the BCM89820 100-Pin FBGA Package***

| | ***Airflow (feet per minute)*** | | | | |
|---|---|---|---|---|---|
| ***100-ball FBGA Package*** | ***0*** | ***100*** | ***200*** | ***400*** | ***600*** |
| Theta-$J_A$ (°C/W) | TBD | — | — | — | — |
| PSI_$J_T$ (°C/W) | — | — | — | — | — |

# Section 10: Ordering Information

***Table 68: Ordering Information***

| *Part Number* | *Package* | *Ambient Temperature* |
|---|---|---|
| BCM89820A2BFBG | 100-ball FBGA (RoHS-compliant package) | –40°C to +105°C |

# Appendix A: Acronyms and Abbreviations

For a more complete list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

***Table 69: Acronyms and Abbreviations***

| *Term* | *Description* |
|---|---|
| ADC | Analog to Digital Converter |
| BER | Bit Error Rate |
| CESD | Cable Electro Static Discharge |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DAC | Digital to Analog Converter |
| DCC | Data Communication Channel |
| DFE | Decision Feedback Equalization |
| EMI | Electro Magnetic Interference |
| ESD | Electrostatic Discharge |
| FFE | Feed Forward Equalization |
| GM | Grandmaster |
| HPF | High Pass Filter |
| INTR | Interrupt |
| LDS | Long Distance Signalling/Link Discovery Signalling |
| LRE | Long-Range Ethernet |
| MDC | Management Data Clock |
| MDI | Medium Dependent Interface |
| MDIO | Management Data Input/Output |
| MII | Media Independent Interface |
| MLP | Micro Leadframe Package |
| MSB | Most Significant Bit |
| NSE | Network Synchronization Engine |
| NCO | Numerically Controlled Oscillator |
| OP | Operation Code |
| OUI | Organizationally Unique Identifier |
| PHY | Physical Layer Interface |
| PRE | Preamble |
| PTP | Precision Time Protocol |
| RO | Read Only |
| RX | Receive |
| RXD | Receive Data |
| SC | Self-Clearing |
| SOR | Sample on Reset |

***Table 69: Acronyms and Abbreviations (Cont.)***

| *Term* | *Description* |
|---|---|
| ST | Start of Frame |
| TA | Turn Around |
| TC | Transparent Clock |
| TX | Transmit |
| TXD | Transmit Data |
| UTP | Unshielded Twisted Pair |
| VDD | Voltage supply: Drain (typically used as the positive voltage supply for CMOS circuits) |
| XTALI | Crystal Input pin |
| XTALO | Crystal Output pin |

# Revision History

| *Revision* | *Date* | *Change Description* |
|---|---|---|
| BCM89820-DS100-R | 09/14/16 | Initial release. |

Web: www.broadcom.com
Corporate Headquarters: San Jose, CA


89820-DS100-R September 14, 2016