Mingyi Huang

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https://huangmy233.github.io/

Education

Ph.D(Research Assistant) in Purdue University, IN, United States **Aug.2025-Present**
Advisor: Irith Pomeranz
Courses: ECE 60800 - Computational Models and Methods (A), ECE 57000 – Artificial intelligence (B)

Extension in University of California-Santa Barbara (UCSB), CA, United State **Sep.2024-Jun.2025**
Graduate Courses:
Tensor Computation for Machine Learning and Big Data (A), VLSI Project Design (A), Advanced Computer Atchitecture (A), VLSI Architecture and Design (B+)

B.Eng in Huazhong University of Science and Technology (HUST), Wuhan, China **Sep.2021-Jul.2024**
Major GPA: 4.42/5.0(89.2/100)
GPA (overall): 4.19/5.0(87/100)
Core courses: Calculus(I)(A) (96/100), Probability Theory and Mathematical Statistics (96/100), Fundamental of Software Programming (89/100), Semiconductor Physics (II) (94/100), Principles of Computer Organization (96/100), Hardware Description Language and Design of Digital System (94/100), Embedded System Principles and Design (94/100).

Research Experience

Fast Test Generation for Structurally Similar Circuit Sep.2025 – Jan.2026
Researcher,* Advisor: Irith Pomeranz, *Department of ECE, Purdue University

- Implemented a C++-based Static Compaction engine and validated it using Siemens Tessent ATPG and fault simulation flows.
- Proposed a cone-aware test cube splitting strategy to partition patterns by structural and sequential cones for scalable test generation.
- Designed a fault-class–aware pattern filtering algorithm to eliminate redundant tests while maintaining fault coverage on structurally similar circuits.

Design of a 32-bit Pipeline RISC-V Processor Sep.2024 – Dec.2024
Research Leader,* Advisor: Bongjin Kim, *Department of ECE, UCSB

- Design the 32-bit Pipeline RISC-V Processor Architecture using Verilog RTL and Simulate it on Vivado
- Full-Custom Design and Simulate the Memory Circuit (including SRAM for Instruction/Data Memory and D flip-flop for Register File) by Cadence virtuoso
- Full-Custom 32-bit Pipeline RISC-V Processor design including Arithmetic Logic Unit (ALU), Control Unit (CU), memory and so on

FPGA Acceleration for Tensorized Transformer Training Sep.2024 – Jun.2024
Research Leader,* Advisor: Zheng Zhang, *Department of ECE, UCSB

- Investigated the implementation and design of low-precision training system on FPGA
- Design and simulate of a 16-bit floating point (fp16) tensorized tucker linear layer kernel on Vitis_HLS and dynamic rank selection
- Select low-precision data format (minifloat), quantization and embed it in Transformer training

Design and test of Operational Amplifier Chips Feb.2024 - Jul.2024

Team Leader,* Advisor: Xiaofei Chen, D*epartment of Integrated Circuit(IC), HUST

- Designed and simulated an amplifier with extremely high performance, including Open loop gain over 80dB, GBW over 80MHz, SR over 30V/us, CMRR over 60dB, NSRR over 80dB and low power, under all extreme PVT simulation condition and Monte-Carlo simulation
- Drew the layout and post-simulate under all extreme PVT simulation

Design of RTF-based Signal Detection Circuit for MEMS Gas Sensor Feb.2023 - Apr.2024

Research Leader,* Advisor: Zhige Zou, D*epartment of Integrated Circuit(IC), HUST

- Developed and improved traditional RTF scheme by comparing different circuit structures, like designing high-precision current mirror, cross-coupled pairs of OTA
- Optimized the circuit to fit with lower voltage supply in order to reduce power consumption
- Simulated bandgap reference source, voltage follower, current mirror section, OTA comparator by Cadence virtuoso

Design of a Switched-Capacitor Sound Classification System based on SAR ADCs Feb.2023 - Apr.2024

Research Member,* Advisor: Guoyi Yu, *Center for Very Large-Scale IC and Systems, HUST

- Investigated the structure and design of switched-capacitor filters and the optimization for reliability and performance of sound classification system
- Designed switched-capacitor filter by comparing different structures, like the Precise Opamp Gain (POG) approach, switched-current assisting (SCA) and recharging (PC) methods
- Simulated first-order and second-order switched-capacitor filters by Cadence virtuoso

Professional Experience

Intern, Wuhan Integrated Circuit Design & Engineering Co, Hubei, China Jul.2023 - Aug.2023

- Learned about approaches of testing and measuring chips or circuits, including using test equipment and writing testbench by using Verilog HDL
- Assisted engineers to document test results, organizing and analyzing experimental data by using MATLAB

Honors & Awards

- Silver Prize of National College Students IC Innovation Competition in Central China Region Jul.2024
- Silver Prize of National College Students Mathematics Competition in Hubei Province Nov.2022
- Scholarships for academic excellence in HUST (2/26) Sep.2022
- Outstanding Student Leader Scholarship in HUST (1/26) Sep.2022
- U.S. Collegiate Mathematical Modeling Competition S Award May.2022
- Freshman Academic Excellence Scholarship in HUST (2/27) Mar.2022
- Freshmen Cultural and Sports Scholarships in HUST (2/27) Mar.2022

Skills & Interests

Language skills: Chinese (Native); English (**IELTS: 7.5**)

Programming skills: C, C++, MATLAB, Verilog, Keil, Python, LaTeX

Tools: Cadence virtuoso, Vivado, Quartus, Modelsim, Vitis, Tessent