Mingyi Huang

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https://huangmy233.github.io/

Education

University of California-Santa Barbara (UCSB), California, United States Sep.2024 - Present
Graduate Courses: *Tensor Computation for Machine Learning and Big Data, VLSI Project Design*

Huazhong University of Science and Technology (HUST), Wuhan, China Sep.2021 - Jul.2024
Bachelor of Engineering in Integrated Circuit Design and Integrated System (expected in July 2025)
Major GPA: 4.42/5.0(89.2/100) | **GPA (Overall):** 4.19/5.0(87.0/100)
Core Courses: *Calculus(I)(A) (96/100), Probability Theory and Mathematical Statistics (96/100), Fundamental of Software Programming (89/100), Semiconductor Physics (II) (94/100), Principles of Computer Organization (96/100), Hardware Description Language and Design of Digital System (94/100), Course Project for Digital IC Design (91/100), Course Project for Analog IC Design (93/100), Embedded System Principles and Design (94/100)*

Research Experience

Design of a 32-bit Pipeline RISC-V Processor Sep.2024 - Present
Research Leader,* Advisor: Bongjin Kim, *Department of ECE, UCSB

- Design the 32-bit Pipeline RISC-V Processor Architecture using Verilog RTL and Simulate it on Vivado
- Full-Custom Design and Simulate the Memory Circuit (including SRAM for Instruction/Data Memory and D flip-flop for Register File) by Cadence virtuoso
- Full-Custom 32-bit Pipeline RISC-V Processor design including Arithmetic Logic Unit (ALU), Control Unit (CU), memory and so on

FPGA Acceleration for Tensorized Transformer Training Sep.2024 - Present
Research Leader,* Advisor: Zheng Zhang, *Department of ECE, UCSB

- Investigated the implementation and design of low-precision training system on FPGA
- Design and simulate of a 16-bit floating point (fp16) tensorized tucker linear layer kernel on Vitis_HLS and test it with a Transformer end-to-end training module on FPGA
- Optimize the processing unit to an 8-bit floating point (fp8) for training efficiency

Design of Operational Amplifier Chips Feb.2024 - Jul.2024
Team Leader,* Advisor: Xiaofei Chen, D*epartment of Integrated Circuit(IC), HUST

- Designed and simulated an amplifier with extremely high performance, including Open loop gain over 80dB, GBW over 80MHz, SR over 30V/us, CMRR over 60dB, NSRR over 80dB and low power, under all extreme PVT simulation condition and Monte-Carlo simulation
- Drew the layout and post-simulate under all extreme PVT simulation

Design of RTF-based Signal Detection Circuit for MEMS Gas Sensor Feb.2023 - Apr.2024
Research Leader,* Advisor: Zhige Zou, D*epartment of Integrated Circuit(IC), HUST

- Developed and improved traditional RTF scheme by comparing different circuit structures, like designing high-precision current mirror, cross-coupled pairs of OTA
- Optimized the circuit to fit with lower voltage supply in order to reduce power consumption
- Simulated bandgap reference source, voltage follower, current mirror section, OTA comparator by Cadence virtuoso

Design of a Switched-Capacitor Sound Classification System based on SAR ADCs Feb.2023 - Apr.2024
Research Member,* Advisor: Guoyi Yu*, Center for Very Large-Scale IC and Systems, HUST

- Investigated the structure and design of switched-capacitor filters and the optimization for reliability and performance of sound classification system
- Designed switched-capacitor filter by comparing different structures, like the Precise Opamp Gain (POG) approach, switched-current assisting (SCA) and recharging (PC) methods
- Simulated first-order and second-order switched-capacitor filters by Cadence virtuoso

Professional Experience

Intern, Wuhan Integrated Circuit Design & Engineering Co, Hubei, China Jul.2023 - Aug.2023

- Learned about approaches of testing and measuring chips or circuits, including using test equipment and writing testbench by using Verilog HDL
- Assisted engineers to document test results, organizing and analyzing experimental data by using MATLAB

Honors & Awards

- Silver Prize of National College Students IC Innovation Competition in Central China Region Jul.2024
- Silver Prize of National College Students Mathematics Competition in Hubei Province Nov.2022
- Scholarships for academic excellence in HUST (2/26) Sep.2022
- Outstanding Student Leader Scholarship in HUST (1/26) Sep.2022
- U.S. Collegiate Mathematical Modeling Competition S Award May.2022
- Freshman Academic Excellence Scholarship in HUST (2/27) Mar.2022
- Freshmen Cultural and Sports Scholarships in HUST (2/27) Mar.2022

Leadership & Activities

Student Union of the Entrepreneurship Department Feb.2023 - Jul.2023

Minister, Center for Learning and Creativity, School of Integrated Circuits, HUST

- Spearheaded an activity unique to IC Academy called "Research Group Open Day" in the college, which provides undergraduate students with a full understanding of the research directions of the faculty professor's subject area

Student Union of the Outreach Department Sep.2022 - Feb.2023

Minister, Innovation and Entrepreneurship Division, School of OEI, HUST

- Organized various professional seminars and an Electronic Intelligence Competition

Skills & Interests

Language skills: Chinese (Native); English (**IELTS: 7.5**)
Programming skills: C, MATLAB, Verilog, Keil, Python, LaTeX
Tools: Cadence virtuoso, Vivado, Quartus, Modelsim