Review

III-V-on-Silicon Photonic Devices for Optical Communication and Sensing

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Abstract: In the paper, we review our work on heterogeneous III-V-on-silicon photonic components and circuits for applications in optical communication and sensing. We elaborate on the integration strategy and describe a broad range of devices realized on this platform covering a wavelength range from 850 nm to 3.85 μm.

Keywords: heterogeneous integration; optical communication; optical sensing

1. Introduction

Silicon photonics is emerging as a powerful technology for the integration of optical functions on a chip. The main advantages of the technology are the compactness of the resulting circuits (due to the high refractive index contrast), the availability of high-speed opto-electronic components on the platform and the use of the well-developed silicon electronics fabrication tools for the realization of these photonic integrated circuits. However, silicon as well as germanium, the two main materials used in silicon photonic integrated circuits (PICs), have an indirect bandgap, making monolithic laser integration onto silicon photonic integrated circuits difficult. High performance semiconductor lasers (as well as other opto-electronic components) are realized in III-V semiconductors. Therefore, there is a need for the integration of III-V semiconductors on silicon photonic integrated circuits, in order to complete the toolkit for the realization of complex and advanced heterogeneous silicon photonic integrated circuits. The integration of III-V semiconductor opto-electronic components onto silicon photonic integrated circuits can be realized in various ways, ranging from flip-chip integration [1] over bonding approaches [2–4] to hetero-epitaxial growth [5]. Flip-chip integration has the advantage that the devices can be grown and fabricated on their native substrate, while it does require accurate alignment in the assembly process. Hetero-epitaxial growth allows for front-end, wafer-scale integration of the III-V materials, but it is challenging to grow high quality III-V materials on silicon, realize electrical injection and integrate such devices in a typical silicon photonics process flow. Bonding approaches, on the other hand, combine some of the advantages of flip-chip integration (*i.e.*, epitaxial layer structures grown on their native substrate) with the scalability of hetero-epitaxial integration and is therefore considered as a very attractive approach for III-V integration onto silicon photonic integrated circuits. Several bonding techniques are being used: molecular bonding [2], metal bonding [3] and adhesive bonding [4]. In this paper, we elaborate on the adhesive bonding heterogeneous integration technology developed in our group, as well as the devices that have been demonstrated on this platform. Devices for both communication applications as well as sensing applications are described.

2. III-V-on-Silicon Integration Technology

2.1. Adhesive Die-to-Wafer Bonding and Wafer-to-Wafer Bonding Technology

While there are various methods of transferring compound semiconductors onto a silicon-based waveguide platform (molecular bonding, adhesive bonding, anodic bonding, metallic bonding), adhesive bonding offers some significant advantages. Since the adhesive planarizes the surface, the cleanliness requirements are more relaxed, resulting in a significant reduction in bonding preparation. In addition, surface roughness requirements are relaxed.

The adhesive of choice in our work is DVS-BCB (divinylsiloxane-bis-benzocyclobutene), because of its low curing temperature, high degree of planarization, high optical clarity, good thermal stability, excellent chemical stability, low moisture absorption, and wide applicability, as will be shown in the examples below. Diluting the DVS-BCB with mesitylene, thin bonding layers can be achieved (<50 nm). The largest disadvantage of DVS-BCB is probably the low thermal conductivity, especially in the context of power consuming devices such as semiconductor lasers or optical amplifiers. However, with sub 100 nm thick bonding layers, the several micron thick buried oxide of the silicon-on-insulator photonic integrated circuit (PIC) is dominant in the thermal resistance of the device.
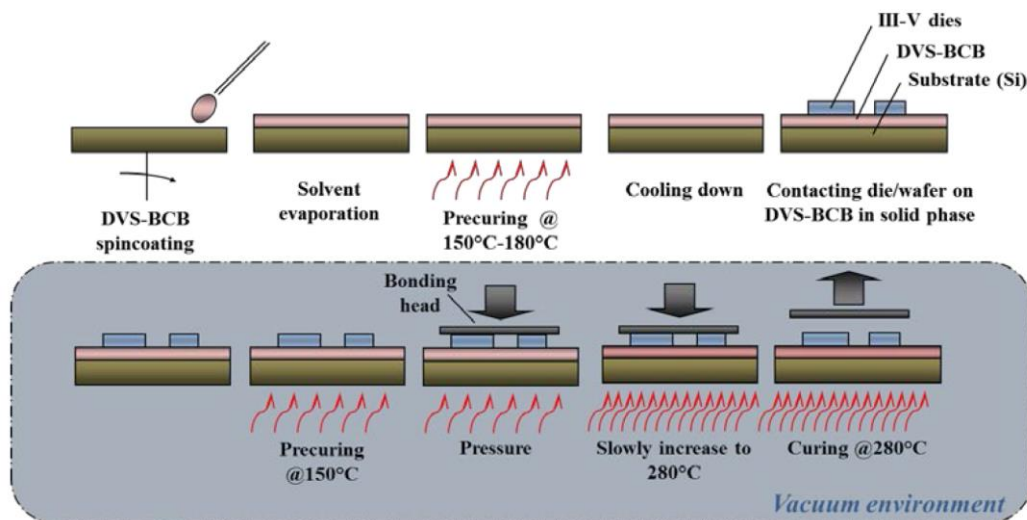

Figure 1. III-V on silicon heterogeneous integration process flow (reproduced from [1]).

The bonding process is schematically depicted in Figure 1. It starts with cleaning both III-V and silicon-on-insulator (SOI). The SOI cleaning is performed by immersing the sample for 15 min into a Standard Clean (SC-1) solution, *i.e.*, $NH_4OH:H_2O_2:H_2O$ 1:1:5, heated to 70 °C. Alternatively, one can also use a microwave O_2 plasma. To achieve thin bonding layers, mesitylene is added to the DVS-BCB (Cyclotene 3022-35). The dilution depends on the required bonding layer thickness and the topography of the silicon PIC. Prior to bonding, the spun DVS-BCB is pre-cured to evaporate all the solvents. In this step, the DVS-BCB is already partially polymerized, making it more solid-like, thereby improving the bonding layer thickness uniformity. For the III-V preparation one or more sacrificial layers are etched. The etch chemistry depends on the material system. Afterwards, a thin (<10 nm) silicon oxide layer is deposited to improve the adhesion to BCB. Alternatively one can use the native oxide of the III-V surface. The III-V dies are then brought into contact with the DVS-BCB coated silicon

photonics substrate and loaded in a Suss MicroTec ELAN CB6L wafer bonder. After pumping to vacuum and heating the sample to 150 °C, 300 kPa pressure is applied. After 10 min, the temperature is further increased to 280 °C and the DVS-BCB is fully cured for one hour. The III-V substrate is removed by grinding and wet etching. The III-V membrane is now transferred to a Si sample. Because of the simplicity of the bonding process, it is very versatile. Virtually any compound semiconductor can be transferred, as will be discussed later on in the paper. In addition, multiple die bonding and full wafer bonding has been demonstrated [4].

2.2. III-V on Si Device Processing Technology

The processing of the 200 mm silicon-on-insulator wafers is carried out in imec's CMOS pilot line. Several etching depths are available, depending on the device requirements. Fiber-to-chip grating couplers are typically used to interface with the photonic integrated circuit, allowing for wafer-scale measurements. After waveguide processing, the wafer is covered by a thick SiO_2 layer, and the subsequent chemical mechanical polishing process planarizes the wafer, leaving about 20 nm SiO_2 above the silicon waveguide.

After bonding of the III-V substrate onto the silicon PIC as described in Section 2.1, the III-V substrate is removed. Since most device demonstrations in this paper are based on InP-based III-V layer stacks, in this section we will elaborate on the process flow for InP-based heterogeneously integrated devices. The process flow is schematically described in Figure 2. The InP substrate is removed using $HCl:H_2O$ (3:1, 40 °C) (Figure 2c) until the InGaAs etch stop layer is reached. After etching the InGaAs sacrificial layer using $H_2SO_4:H_2O_2:H_2O$ (1:1:18), a SiN layer of 200 nm is deposited on top of the p+ contact layer by PECVD. The III-V waveguide pattern is transferred into this SiN hard mask by optical lithography and reactive ion etching (RIE) (Figure 2d). Then, the pattern is further etched into the p+ contact layer by ICP-RIE (Figure 2e). Since the designed coupler (see Section 3.1) between III-V and silicon waveguides requires narrow III-V tips (500 nm), wet etching with $HCl:H_2O$ (1:1) is used to etch the thick p-InP layer, forming an inverted-trapezoid-shaped waveguide that has a much smaller waveguide width at the bottom (Figure 2f). Once again, a thin layer of SiN (~200 nm) is deposited and patterned (by optical lithography and RIE) to protect the III-V waveguide while exposing the active III-V layers from two sides (Figure 2g). Etching of the active layers is carried out using $H_2SO_4:H_2O_2:H_2O$ (1:1:10) (Figure 2h). Ni/Ge/Au contacts are evaporated onto the InP n+ contact layer by a lift-off process (Figure 2i). In order to electrically isolate the devices, the n+ contact layer between neighboring devices is etched using $HCl:H_2O$ (1:1) (Figure 2j). A photoresist mask is used to protect the III-V waveguide during this etching process. Afterwards, DVS-BCB is spin-coated on top of the wafer to planarize the top surface (Figure 2k). Etch-back using RIE thins down the DVS-BCB layer thickness to expose the SiN hard mask on top of the p+ contact layer (Figure 2l). After removing the SiN layer by RIE (Figure 2m), the metal p-contact layer (Ti/Au) is formed on top of the p+ contact layer by lift-off (Figure 2n). Optical lithography and RIE etching are used to etch deep vias into the DVS-BCB layer down to the n-metal contact (Figure 2o). As the final step, Au is deposited on top of the p and n metal contacts by lift-off or plating for probing (Figure 2p).
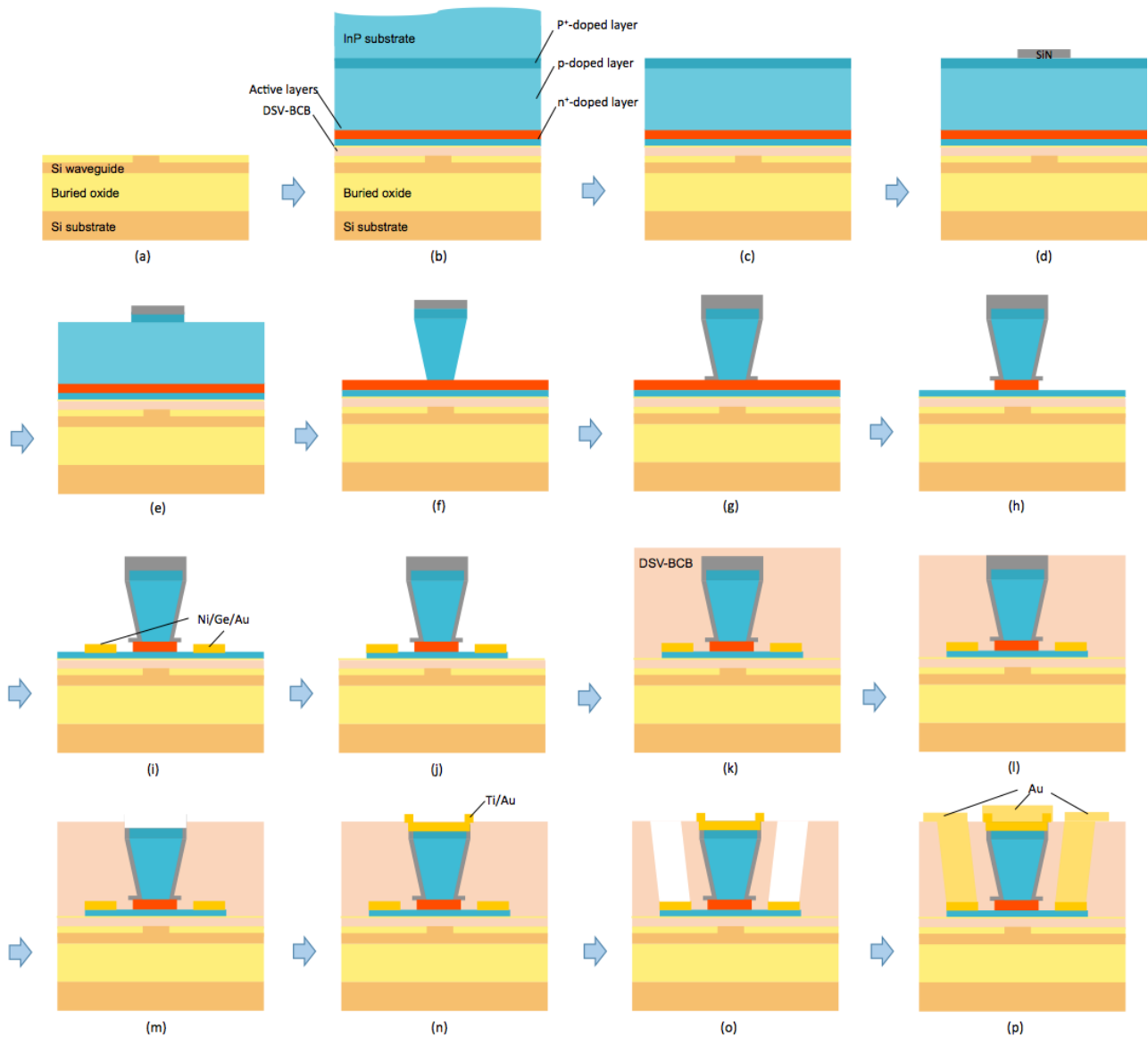
Figure 2. Step-by-step typical process flow for heterogeneously integrated III-V on Si devices.

3. Optical Coupling between the III-V Device Layer and the Silicon Waveguide Layer

Efficient optical coupling between the III-V device layer and the silicon waveguide layer is critical for the integration of III-V opto-electronic components on silicon PICs. The optical coupling scheme should not only be efficient, it should also work over a broad wavelength range and be fabrication (alignment) tolerant. In order to satisfy these requirements for waveguided III-V opto-electronic devices, an adiabatic taper scheme was developed. For bonded surface illuminated photodetector structures, a diffractive grating structure is used.

3.1. Adiabatic Taper Interface

Optical coupling between a waveguided III-V opto-electronic component and the underlying silicon waveguide layer is realized through a taper-based spot-size converter structure. In our heterogeneous III-V/Si devices the optical mode is strongly confined to the III-V waveguide (for efficiency) and a strong wave vector mismatch exists between the III-V and silicon photonic wire waveguide layer. By tapering the

III-V and/or silicon waveguide, wave vector matching can occur and the optical mode can be gradually transformed to eventually reside in the silicon waveguide. If the waveguide dimensions vary slowly along the propagation direction, the tapering is adiabatic [6]. This means that no power exchange occurs between the fundamental waveguide mode and the higher order waveguide modes. In many of our recently developed laser devices, a double adiabatic tapered coupler has been successfully implemented [7–9]. For use in electro-absorption modulator (EAM) devices, a very compact tri-sectional tapered coupler has recently been proposed [10]. Both structures will be briefly discussed below.

The device geometry of the double adiabatic tapered coupler is shown in Figure 3a [9]. The coupler is piecewise linear and consists of two parts: the first part (Taper I) has a length of 35 μm and decreases the III-V waveguide width from 3 μm to 1 μm. In the second taper part (Taper II) the actual III-V-to-silicon coupling takes place through gradual tapering of both the III-V and silicon waveguide. Taper II has a length of 150 μm with the III-V waveguide being tapered from 1 μm to a narrow taper tip (<500 nm), whereas the silicon waveguide width is tapered from 180 nm to 1 μm. A 400 nm thick silicon waveguide is used in this coupling scheme, as this simplifies the III-V-to-silicon coupling compared to the case of direct coupling to a 220 nm thick device layer (considered as a standard layer thickness for the realization of high index contrast silicon photonic waveguide structures). The thick silicon waveguide layer also relaxes the requirements on the III-V taper tip width: a width of 500 nm is sufficient to achieve a highly-efficient, low-reflection power transfer from the III-V mesa to the silicon waveguide. This is illustrated in Figure 3b. A second spot-size converter structure is used to eventually couple the light from the 400 nm thick waveguide to the standard 220 nm single mode silicon strip waveguide. Finally, we note that along with the taper tip width and the III-V/silicon spacing, taper misalignment also has a direct impact on the taper coupling efficiency. A longer taper leads to a more tolerant structure, at the expense of a larger device footprint. Typically, the used adiabatic taper structures allow for a 300 nm misalignment between III-V and silicon waveguide layer.
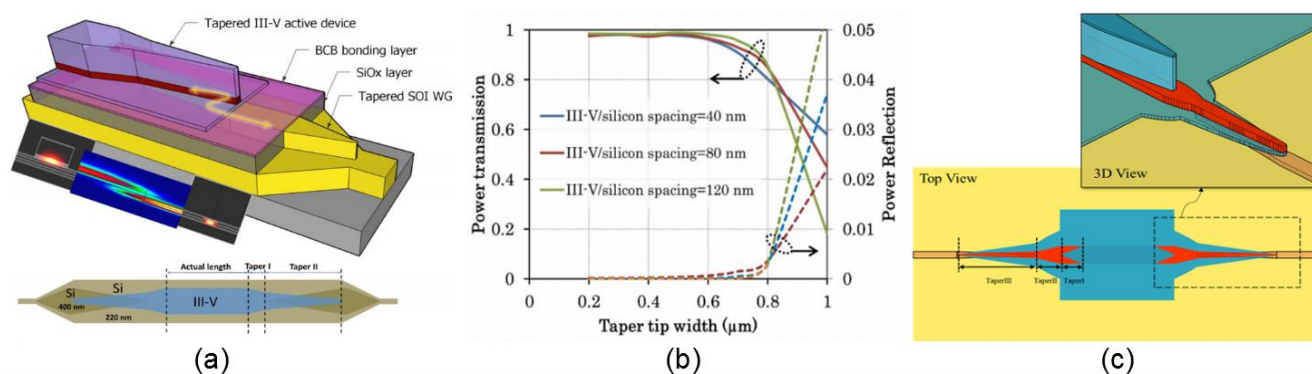

Figure 3. (**a**) Double adiabatic tapered coupler; (**b**) Simulated power transmission and reflection at the taper tip as a function of III-V taper tip width; (**c**) Tri-sectional tapered coupler. Reproduced from [9] and [10].

Figure 3c shows the geometry of tri-sectional tapered coupler for EAM devices [10]. Because the taper mimics a semi-3D taper to prevent the excitation of higher order modes in the thick p-InP cladding layer, the taper length of this device can be substantially reduced down to 10 μm. The removal of the p-type

indium phosphide (p-InP) layer in part of the taper structure prevents the electrical driving of part of the taper structure, limiting the types of devices for which this approach can be used.

3.2. Grating Coupler Interfaces

For the integration of surface illuminated III-V photodetectors on silicon PICs, a vertical grating coupler interface can be used [11–15]. Figure 4a schematically shows this coupling scheme where the light confined in a silicon waveguide is diffracted vertically to the III-V photodetector bonded on the grating coupler. The required photodetector length depends on the grating coupler strength. An important design consideration in this coupling structure is to maximize the directionality of the grating (the ratio of optical power diffracted upwards to the total diffracted power). A vertical cavity is formed by the reflection at the DVS-BCB/III-V interface at the top and the SiO_2/Si substrate interface at the bottom. This means that the directionality depends on the exact location of the SOI grating in this cavity. By optimizing the DVS-BCB bonding thickness and buried oxide thickness, the directionality can be optimized. Figure 4b shows a two-dimensional full vectorial simulation of the absorbed power in a bonded III-V photodetector as a function of the DVS-BCB thickness (design A). Adding an anti-reflection coating between III-V material and DVS-BCB avoids the formation of such a vertical cavity, resulting in a much more robust optical coupling (design B).
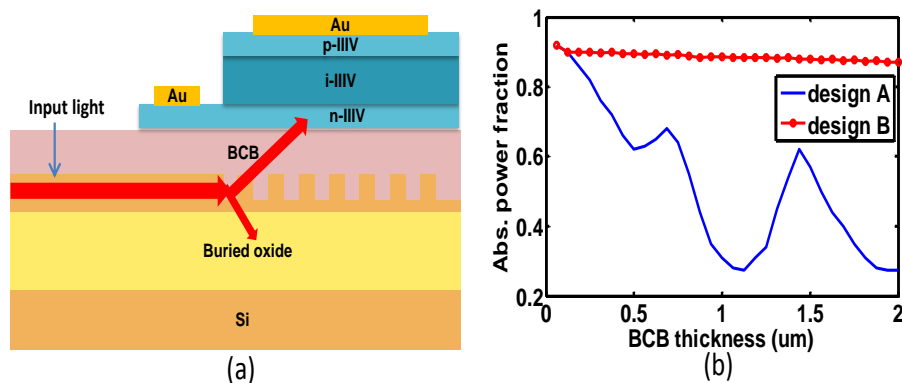

Figure 4. (**a**) Schematic view of grating coupler interface between Si waveguide circuit and III-V photodetector (**b**) Simulation example of grating based coupling to a III-V photodetector. Design B has antireflection coating while Design A does not (reproduced from [13]).

4. III-V-on-Silicon Devices for Optical Communication Applications

Silicon photonic integrated circuits are currently finding applications mostly in the realm of optical communication. Both transceivers for optical interconnects in datacenters as well as transceivers for long-haul coherent communication are being commercialized. These transceivers use external III-V laser sources that are interfaced with the PIC. The scaling of the required aggregate bandwidth of these transceivers, especially in the context of optical interconnect applications, will require wavelength division multiplexed transceivers, therefore requiring the integration of multiple lasers on a single transceiver chip. This requires a scalable approach to laser integration, for which we use adhesive die-to-wafer bonding. Besides lasers, other opto-electronic devices such as EAMs can also be integrated

this way. In the subsequent sections, we will elaborate on the realization of III-V-on-silicon laser sources and EAMs for optical communication applications.

4.1. III-V-on-Silicon Laser Sources for Optical Communication Applications

4.1.1. 1550 nm Semiconductor Optical Amplifiers Integrated on Silicon Photonic Integrated Circuits

Optical amplifiers form an essential part of most photonic circuits in order to compensate for losses [16]. Amplifiers can be used in receivers, boosting the signal before being detected which increases sensitivity [17], but are also used in more complex photonic circuits [18]. The III-V-on-silicon platform offers a large design space for semiconductor optical amplifiers (SOAs), as the optical mode distribution over the III-V and silicon device layer can be tailored by design. This allows optimization of the gain and saturation power of the amplifier. Amplifiers are generally optimized either for high output power or for low power consumption and small footprint [19]. A compact and low injection current III-V-on-silicon optical amplifier has been realized in which the optical mode is predominantly confined to the III-V waveguide [20]. 18 dB small signal gain with low power consumption was demonstrated. The output power in the silicon waveguide as a function of the waveguide-coupled input power at several wavelengths is shown in Figure 5a for an injection current of 100 mA. We see that the output power saturates at 10 dBm. The gain saturation is shown in Figure 5b. The noise figure at 1550 nm reaches 7 dB for low optical input power levels at the highest amplifier drive current of 100 mA, as shown in Figure 5c. Gain-clamped optical amplifiers were also demonstrated. In this case a distributed feedback grating is implemented underneath the optical amplifier (see Section 4.1.2) for the device to lase away from the gain peak of the III-V active region. The gain as a function of optical output power is shown in Figure 5d. The gain is substantially lower than for the classical configuration, however it remains flat over a wider range of optical output power compared to the classical SOA.

4.1.2. 1550 nm Distributed Feedback Lasers Integrated on Silicon Photonic Integrated Circuits

Distributed feedback lasers are important optical sources for integrated transceivers because they provide single mode emission, have a small footprint, high optical output power and relatively narrow linewidth. Their small footprint also makes direct modulation of these laser sources attractive. Direct modulation of laser diodes for high-speed transceivers has significant advantages over the use of external modulators in terms of power consumption, fabrication complexity and compactness [21–25], especially for short distance optical interconnects. High-speed directly modulated lasers on the InP platform and bonded to a silicon substrate have been demonstrated recently [21–23]. Given the mentioned advantages of silicon photonics, it would be desirable to have directly modulated lasers with a high modulation bandwidth, heterogeneously integrated on and coupled to silicon PICs. This was recently demonstrated [26]. The device layout and a device SEM cross-section are shown in Figure 6. The laser structure consists of the amplifier structure elaborated in Section 4.1.1, with a silicon distributed feedback grating implemented underneath the III-V mesa. The grating coupling strength is determined by the spacing between the III-V and silicon layer. The distributed feedback (DFB) grating period in the experiment is 245 nm and has a 50% duty cycle. The length of the DFB laser is 340 μm and two 220 μm long tapers are used to realize a high efficiency and low reflection coupling from the laser

to the silicon waveguide. The grating coupling strength is 135 cm^{-1}. The laser operates single mode and has 6 mW single facet waveguide coupled output power at 100 mA bias. The device has a 3 dB electro-optic bandwidth of 15 GHz at 100 mA bias current as shown in Figure 7a. 28-Gbps non-return-to-zero (NRZ) direct modulation with 2.1 dB extinction ratio is demonstrated as shown in the inset of Figure 7a. After transmission of over 2 km of dispersion shifted single mode fiber, only 1 dB power penalty is incurred (see Figure 7b).
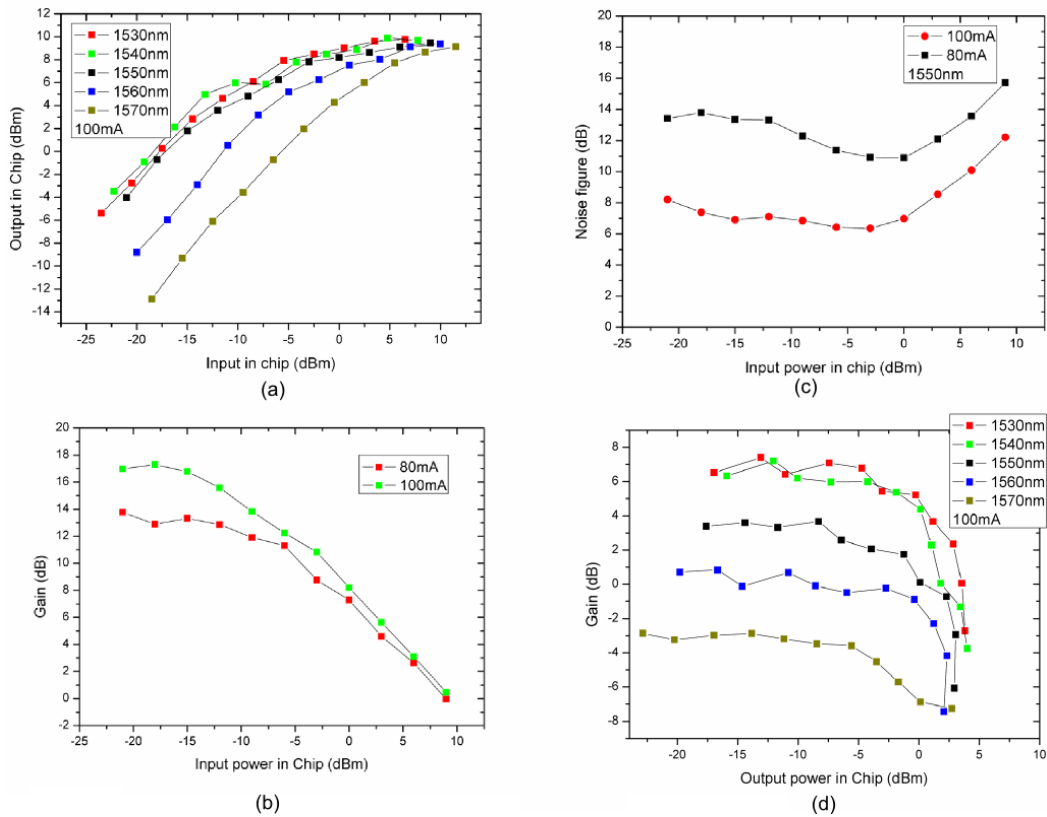

Figure 5. (**a**) Output on chip as function of the input power on chip. (**b**) Gain as function of input power for different injection current. (**c**) Noise figure of the amplifier as function of on-chip input power for different injection currents. (**d**) Gain as function of output power on-chip in gain-clamped operation.
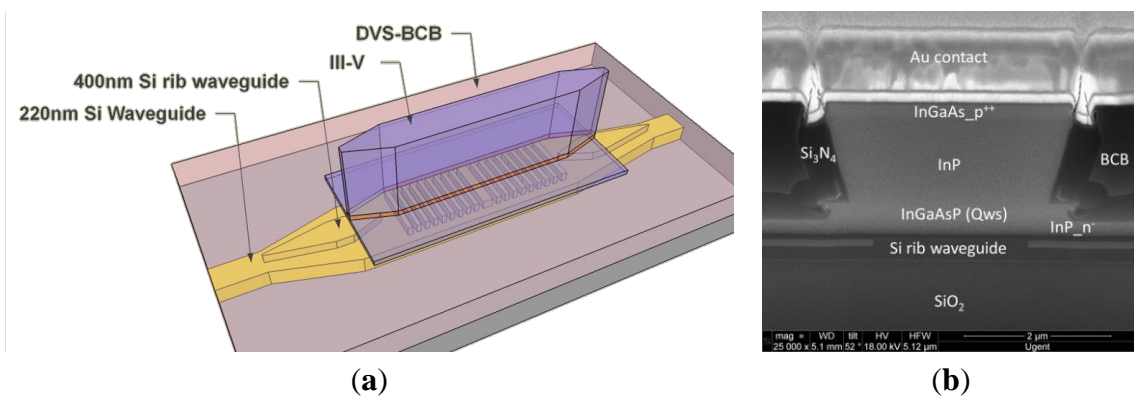

Figure 6. (**a**) Layout of the distributed feedback laser structure. (**b**) SEM device cross-section of the fabricated devices.
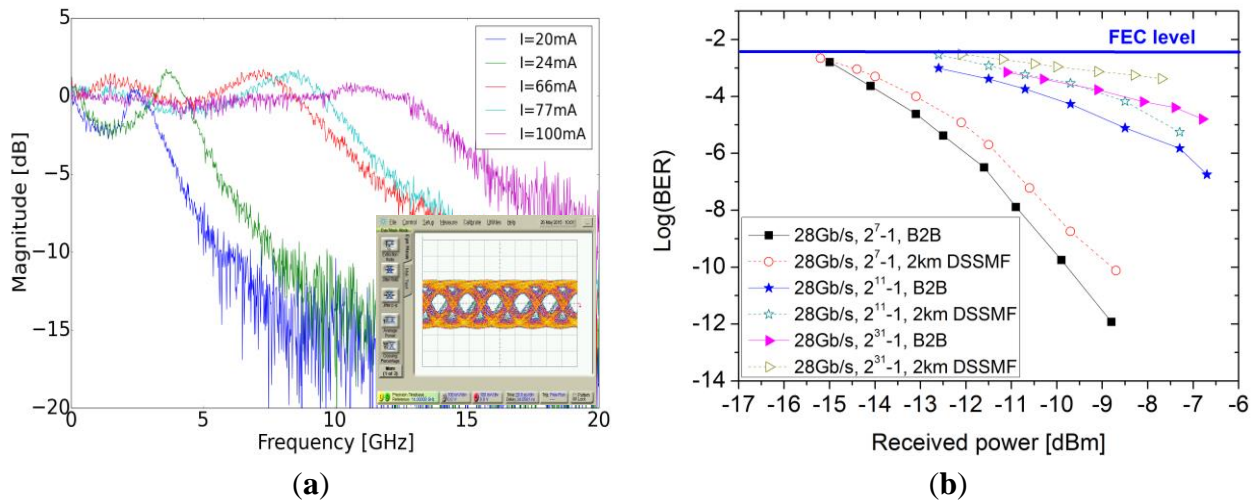
(**a**) (**b**)

Figure 7. (**a**) Small signal response at different bias currents and large signal eye diagram at 28 Gbps with 2.1 dB extinction ratio using 2^{11}-1 pattern length (inset). (**b**) bit error ratio (BER) measurements for back-to-back and 2 km DSSMF configuration. Reproduced from [26].

4.1.3. 1550 nm Tunable and Multi-Wavelength Lasers Integrated on Silicon PICs

Once having a high performance III-V silicon hybrid optical amplifier available, it is possible to combine it with the rich variety of building blocks offered by the silicon photonics platform to construct more complex laser devices as illustrated in Figure 8. Figure 8a shows some of the typical building blocks being used: the hybrid amplifier itself, DBR-mirrors used as on-chip reflectors and tunable ring resonators and wavelength multiplexers for providing wavelength selectivity. The DBR-mirrors used as on-chip reflectors define the laser cavity and replace traditional cleaved facets. It is important that they are well designed to have controllable reflection and low transmission loss, especially at the output side of the device. They could e.g., be implemented using a shallow etch step in a locally widened 220 nm high waveguide as described in [27].
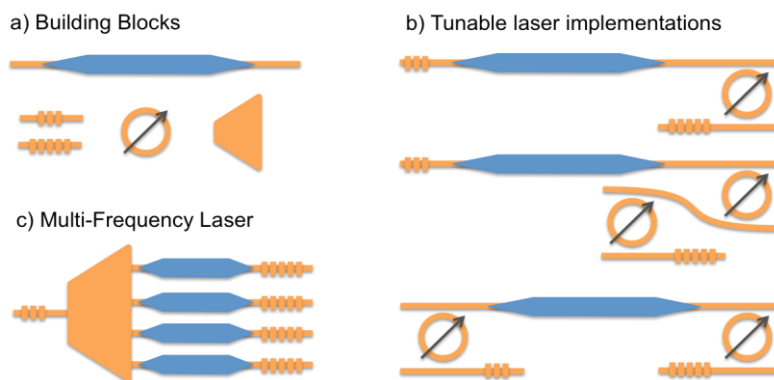

Figure 8. Schematic layout of complex hybrid III-V silicon tunable and multi-frequency lasers. (**a**) Some basic building blocks in our tool box, including a III-V on silicon hybrid amplifier, a standard and high reflection DBR-mirror, a tunable ring resonator and an integrated wavelength multiplexer. (**b**) Different implementations for tunable lasers. (**c**) A multi-frequency laser.

Integrating the optical amplifier with a tunable ring resonator allows building a tunable laser as shown in Figure 8. To ensure wide tunability, narrow linewidth and a relatively straightforward implementation thermal tuning is generally preferred. Using a single ring resonator, tuning of around 10 nm typically can be reached. E.g., in [8] we demonstrated up to 8 nm tuning by applying 25 mW of electrical power to the ring resonator (Figure 9a). This device had a threshold current of 45 mA and output power of up to 10 mW at room temperature. The linewidth was measured to be around 1.7 MHz (at 80 mA). In addition, more complex ring resonator based reflectors have been demonstrated [28]. To increase the tuning range, multiple ring resonators with slightly different free spectral range (FSR) could be integrated, exploiting the so-called Vernier effect. Several different configurations have been proposed in literature (e.g., a 35 nm tuning range was demonstrated in [29]). The exact placement of the ring resonators can influence the maximal attainable output power and care has to be taken in optimizing the overall design.
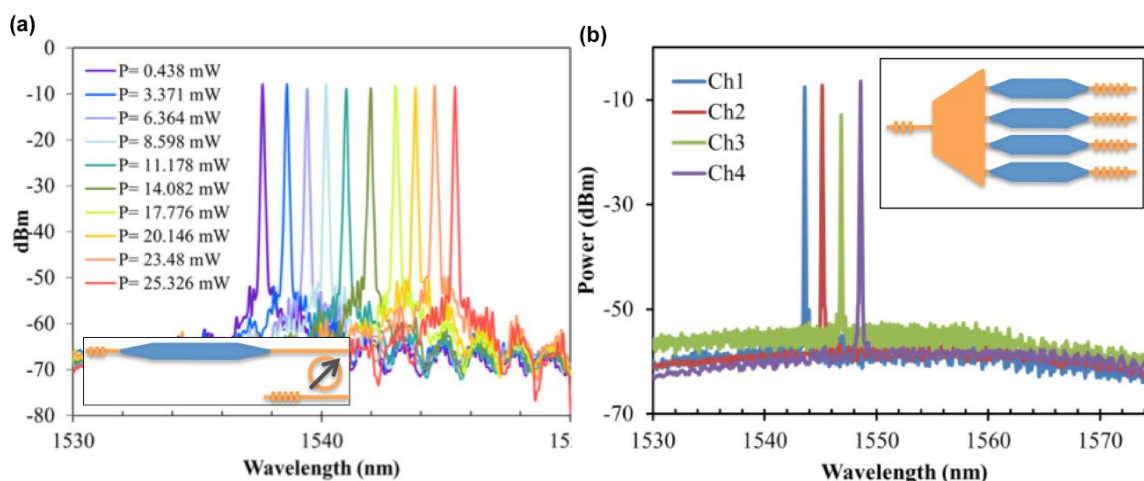

Figure 9. Spectral response of hybrid III-V silicon lasers. (**a**) tunable laser (from [8]) (**b**) AWG-based multi-frequency laser (from [27]).

The ring resonator based tunable lasers described above typically require a rather complex tuning scheme and are designed to generate only a single wavelength channel at a time. To alleviate this problem, so-called digitally tunable lasers or multi-frequency lasers were demonstrated [27]. They consist of an amplifier array, in this case a hybrid III-V on silicon amplifier array, integrated with a wavelength multiplexing device such as an arrayed waveguide grating (AWG), a series of ring resonators or a planar concave grating (PCG). Turning on a single amplifier generates a single well-defined wavelength channel without further control. Turning on multiple amplifiers allows generating a comb of wavelengths with well-defined channel spacing in a single output waveguide. Figure 9b shows the output spectrum for a 4-channel device realized by integrating 4 amplifiers with a silicon AWG. Very good suppression of the side modes is obtained. A similar device was realized integrating the amplifier array with a demultiplexer consisting of four ring resonators with slightly increasing radii coupled to a common bus waveguide [27]. Similar threshold currents, output powers and linewidths were obtained as for the single ring tunable laser described above.

These examples show the strength of the hybrid III-V on silicon platform in building complex laser devices fully integrated on chip. The use of on-chip DBR-reflectors to form the laser cavities allow

straightforward integration with further functionality offered by the silicon photonics platform such as silicon modulators and Ge-detectors, as demonstrated in [30].

4.1.4. 1550 nm Distributed Feedback Dual Wavelength Laser Sources for THz Signal Generation

The ever-increasing demand for bandwidth and mobile data transfer has driven the need for higher frequency carriers for wireless communications up to the THz range [31]. A promising technology to generate such carriers is optical heterodyning [32,33]. In this approach a dual-wavelength laser source is combined with a high-speed photodiode, typically a uni-travelling-carrier photodiode (UTC-PD). The beat between the two laser wavelengths generates the THz carrier. The integration of UTC-PDs on silicon photonic integrated circuits was recently demonstrated [34]. For the dual-wavelength laser implementation, several solutions have been proposed: a tailored spectrum Fabry-Perot laser [35], a multi-section distributed feedback (DFB) lasers [36] and a chip with two independent laser diodes [37]. In our work, an array of asymmetric DFB lasers was designed and fabricated using III-V-on-silicon technology [38]. In an asymmetric DFB laser, the quarter wave phase shift is placed away from the center, as illustrated in Figure 10a. The asymmetrical grating allows two longitudinal modes to lase at the same time (see Figure 10b), while a central phase shift typically results in single mode operation. To ensure stable dual-mode lasing, both modes must be spectrally positioned symmetrically around the gain peak. Instead of a single device, an array of asymmetric DFBs with slightly varying parameters was fabricated. As a result, independent of temperature or manufacturing variations a dual-wavelength device can be found in the array. A major advantage of an asymmetric DFB laser compared to a multi-section DFB laser [36] is that only one current source needs to be controlled. An advantage when compared to two independent laser diodes is that the two laser lines are emitted by the same cavity, therefore a more stable THz signal can be expected. The performance of the realized devices was assessed by connecting the output of the dual-wavelength DFB laser to a UTC-PD with integrated antenna [38]. The signal emitted by the antenna was collected by a WR 2.8 horn antenna and down-converted using an electronic mixer. This down-converted signal is then analyzed by an electrical spectrum analyzer. The linewidth of the carrier and its frequency drift are shown in Figure 10c,d. The instantaneous 3 dB-linewidth of the signal at 357 GHz is 4.2 MHz. A longer sweep of 30 s shows that the signal drifts 28 MHz. This performance allows for on-off keying wireless data transfer using envelope detection.

4.1.5. 1550 nm Mode-Locked Lasers

Mode-locked laser diodes are gaining interest as compact wavelength division multiplexing (WDM) sources since one single laser can generate a large number of coherent wavelength channels. Also, they are the laser source of choice for optical time division multiplexing applications [39]. A mode-locked laser (MLL) produces a train of short pulses, which corresponds with a wide comb of optical modes in the frequency domain.

Low noise, high output power and a broad output spectrum are of great importance for optical communication applications. In order to achieve low-noise performance, it is important to limit the length of the optical amplifier (to reduce spontaneous emission) and realize a low-loss optical cavity.

The III-V-on-silicon platform allows using low-loss silicon waveguide structures (both in terms of nonlinear two-photon absorption as well as linear scattering losses) to form the laser cavity.
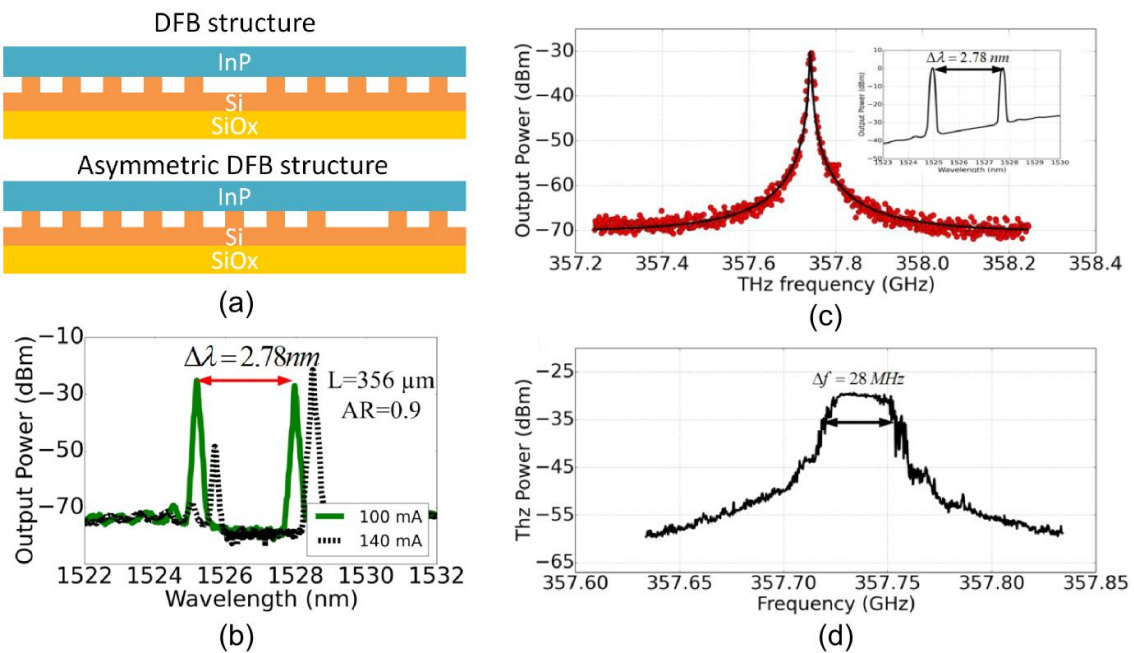

Figure 10. (**a**) Cross section of a III-V-on-silicon DFB laser and asymmetric dual-mode DFB laser. (**b**) Optical output spectrum of asymmetric DFB laser at different injection currents. (**c**) Electrical output spectrum of UTC-photodiode illuminated by the dual wavelength laser showing an instantaneous linewidth of 4.2 MHz. (**d**) Integrated trace of electrical signal over thirty seconds. Reproduced from [38].

This fact was also recognized by others, demonstrating low phase noise hybrid silicon MLLs. A 15 kHz 3 dB RF line width (at 9.95 GHz) was demonstrated in a linear cavity design with on-chip feedback in [40]. In this section we will discuss three different MLL geometries studied in our work. The first demonstrations were based on classical colliding ring cavity and linear cavity arrangements [41] as shown in Figure 11a,b. Further improvement of the output power and RF spectral purity was achieved with a novel anti-colliding pulse MLL design [42] as shown in Figure 11c.

Mode-locking can be realized by placing a saturable absorber (SA) in a standard multimode laser cavity. In our case, the SA is made by electrically isolating a small part of the III-V gain material and reverse biasing that section. In the first two designs, the SA is placed in the center of the laser cavity. In the anti-colliding geometry, the SA is implemented on the low-reflectivity out-coupling mirror of the laser cavity. The optical mode is then coupled to the silicon waveguide using an adiabatic taper structure. The main part of the laser cavity length is realized in the silicon waveguide layer using a spiral waveguide structure. In each case, the length of the cavity is designed to reach a repetition rate of 5 GHz. Details about the device processing can be found in [41,42]. To induce passive mode-locking, the gain section was biased at 160 mA and the SA was reverse biased at −1.2 V for the colliding linear cavity design, 179 mA and −1.3 V for the ring design and 61 mA and −0.7 V for the anti-colliding pulse geometry. The output of the mode-locked laser was coupled to an optical fiber

through a fiber-to-chip grating coupler. Device characterization is carried out on a thermo-electric cooler at 20 °C. Table 1 compares the output characteristics of the three laser geometries.
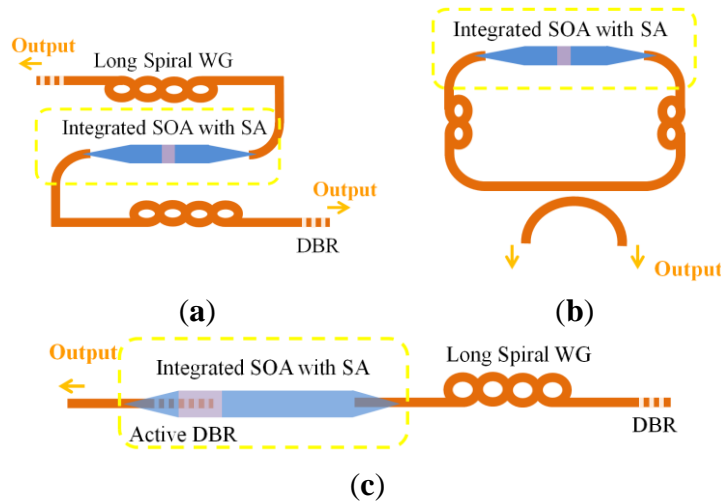

Figure 11. Layout of the different III-V-on-silicon mode-locked laser cavity designs: (**a**) A linear cavity colliding pulse geometry; (**b**) A ring cavity geometry; (**c**) The linear cavity anti-colliding pulse geometry.

Table 1. Comparison of the performance of the different mode-locked laser (MLL) designs.

Method	Self-Colliding [41]	Ring [41]	Anti-Colliding [42]
10 dB optical bandwidth (nm)	>10	7	3.5
Pulse width (ps)	1.5	-	3
3 dB electrical line width (kHz)	12	16	1.7
Integrated timing jitter (50 kHz–10 MHz) (ps)	2.65	1.65	2.8
Threshold current (mA)	40	50	30
Output power at thermal roll-over (mW)	0.2–0.3	0.04–0.08	8–10

We note that the optical bandwidth of the self-colliding MLL, plotted in Figure 12a, is the widest of the three designs. The cavity of this laser is formed by two broadband DBR gratings etched in the silicon, whereas in the anti-colliding laser design, the bandwidth of the grating underneath the SA limits the bandwidth of the optical comb.
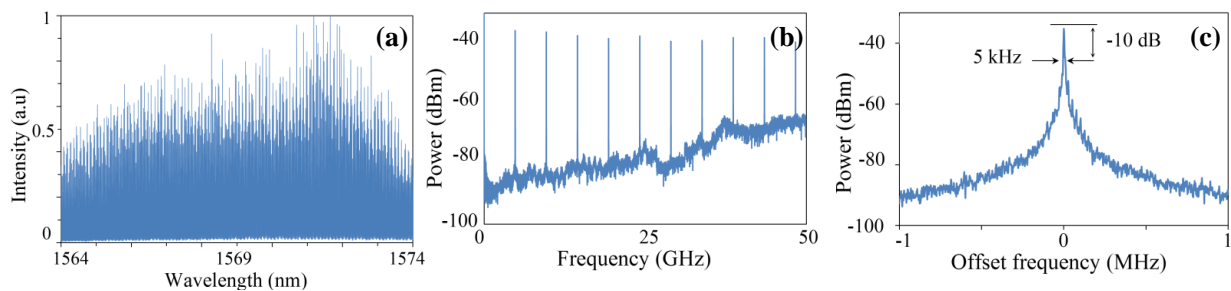

Figure 12. (**a**) High resolution optical spectrum (bandwidth: 20 MHz) of the linear cavity colliding pulse mode-locked laser. (**b**) Wide span electrical spectrum of the generated pulse train of the anti-colliding pulse MLL. (**c**) Linewidth of the fundamental RF tone of the anti-colliding pulse MLL. Reproduced from [41,42].

Furthermore, the anti-colliding pulse MLL clearly outperforms the other two geometries in terms of output power and RF line width. This is in accordance with the theoretical analysis of such a cavity under passive mode-locking [43]. Figure 12b shows a wide span electrical spectrum of the anti-colliding pulse MLL, showing both the fundamental RF tone and its harmonics. The electrical line width of the fundamental RF tone of this laser (1.7 kHz 3 dB linewidth and 5 kHz 10 dB linewidth) is plotted in Figure 12c.

4.1.6. III-V-on-Silicon Microlasers

For applications such as on-chip optical interconnects, requiring low output power laser sources (10–100 µW), a small footprint and low power consumption, microsources are of great interest. Reducing the laser cavity dimensions however puts more stringent requirements on the cavity Q-factor in order to obtain continuous wave lasing with low threshold current. Below we elaborate on 3 types of heterogeneously integrated microlaser sources: InP-based microdisk and resonant cavity laser structures coupled to silicon waveguide circuits, as well as GaAs-based hybrid III-V/silicon vertical cavity surface emitting laser (VCSEL) structures.

1550 nm Microdisk Lasers

Heterogeneously integrated microdisk lasers have been studied for about a decade. A schematic of such a microdisk laser is shown in Figure 13, together with a SEM picture of a typical device cross section. Single mode, CW operating lasers with a typical diameter of 7 µm can be realized with low threshold currents of 0.5 mA and output powers of a few tens of µW coupled to a silicon waveguide circuit. The low threshold currents are possible thanks to the small volume of the InP membrane and the low losses of the whispering gallery mode. These losses can be minimized by using a tunnel junction and limiting the overlap of the mode with the top contact using careful alignment of the top contact, limiting the scattering loss due to sidewall surface roughness by optimizing the etching process and by designing a small evanescent coupling of the whispering gallery mode to the underlying silicon waveguide [44–46].
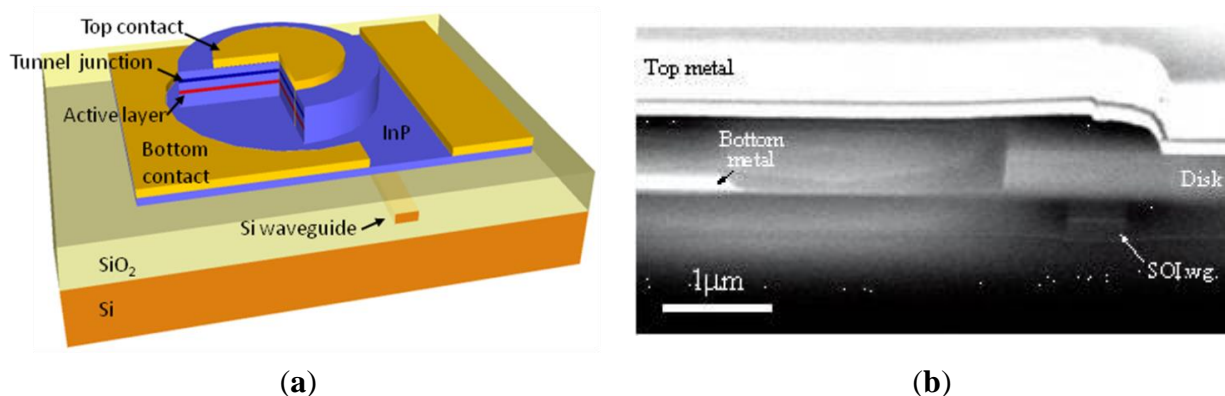

(**a**)   (**b**)

Figure 13. (**a**) Schematic view of an InP microdisk laser heterogeneously integrated onto SOI. (**b**) SEM picture of the device cross section. Reproduced from [44].

A special feature of microdisk lasers and ring lasers in general is the possibility of unidirectional lasing. This feature has potential applications in all-optical flip-flops and in low-power optical signal regeneration. In a symmetrical microdisk laser, without coupling between clockwise and counter clockwise modes, a bistable unidirectional behaviour is generally found just above the threshold current, with the lasing direction being determined by initial conditions or by externally injected optical pulses. This bistable unidirectional behaviour is possible because the cross gain suppression is twice as large as the self-gain suppression [47]. Due to sidewall surface roughness and reflections inside the silicon bus waveguide, there is usually coupling between clockwise and counter clockwise modes. In this case, bistable unidirectional operation is still observed in a symmetrical microdisk configuration, but only for sufficiently high bias currents (determined by the amount of coupling). Asymmetric microdisk configurations (with different coupling from clockwise to counter clockwise than from counter clockwise to clockwise) behave unidirectional in a direction determined by the strongest of the two coupling coefficients. In particular, if coupling from the clockwise to the counter clockwise mode is the largest, then lasing will be predominantly in the counterclockwise mode. The unidirectionality becomes progressively better with increasing bias current, again owing to the larger cross gain saturation [48]. The bistable unidirectional behavior found in symmetric microring or microdisk device configurations can be exploited to implement all-optical flip-flops. The lasing direction can be changed by injecting short optical pulses (with a wavelength sufficiently close to the lasing wavelength in order to obtain injection locking). Switching has been demonstrated with 100 ps pulses with energy as low as 1.8 fJ and switching times are less than 60 ps [49]. The unidirectional asymmetric microring lasers have been demonstrated to be suitable for low power all-optical 2R regeneration [50]. The regeneration relies on the fact that the injection of light with a wavelength within the injection locking bandwidth is physically equivalent to an extra reflection of the laser light. Hence, by externally injecting light into the direction opposite to the lasing direction, one can modify the equivalent coupling coefficients such that the lasing direction switches to the direction of the injected light signal. Figure 14 shows measured bit error rate curves at 10 Gbps without and with regeneration in a microdisk laser as a function of the received power, demonstrating this regenerative capacity.
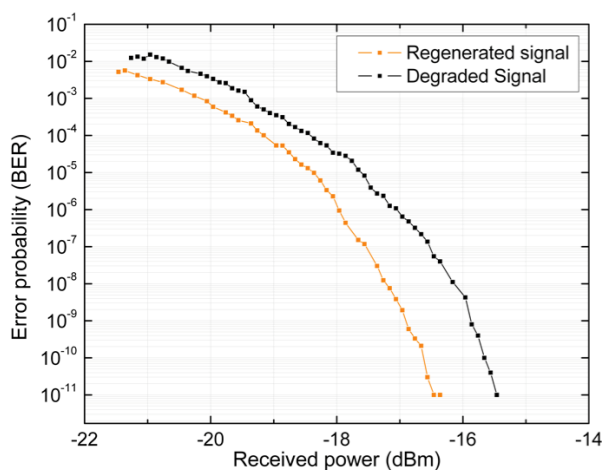
Figure 14. Measured BER curves at 10 Gbps, before and after regeneration with a microdisk laser. Reproduced from [50]. © 2013 IEEE

Finally, by using an epitaxial layer stack with detector layers stacked on top of the laser epitaxial structure, it is possible to densely co-integrate detectors with microdisk lasers enabling the realization of compact bidirectional optical links on silicon [51,52]. Photodetectors fabricated using such epitaxial structure, bonded onto an SOI waveguide, had dark currents of 22 and 67 nA and responsivities of 0.69 and 0.73 A/W for lengths of 40 and 60 μm respectively. A bandwidth of 12 and 18 GHz was obtained for 0 and −1 V bias. The direct modulation bandwidth of the microdisk lasers was 7.8 GHz, but could be increased using injection locking methods. The bandwidth of photodetectors and microdisk lasers permitted the demonstration of a 10 Gbps SOI-based optical interconnect link [51,52]. Figure 15 shows the large signal modulation response for a complete link consisting of a heterogeneously integrated microdisk laser and photodetector on an SOI waveguide.
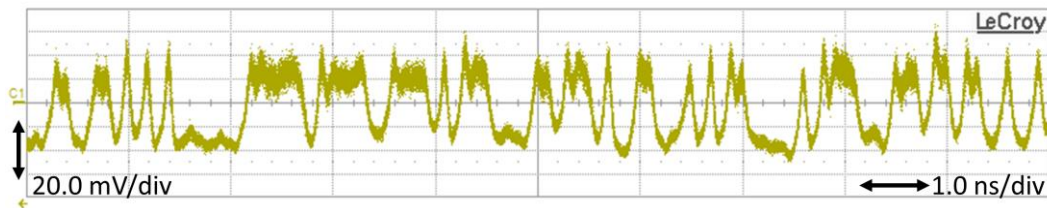

Figure 15. Large signal modulation response of a full optical link based on a microdisk laser, an SOI waveguide and a heterogeneously integrated photodetector for a 10 Gbps 2^7-1 PRBS pattern. Reproduced from [52]. © 2013 IEEE

1550 nm Resonant Cavity Mirror Lasers

While microdisk lasers can obtain small footprint, single mode operation and low threshold current, the laser wavelength of the device is determined by the diameter of the III-V microdisk, which is therefore prone to variation on the wafer. Therefore, ideally one would like to use structures defined in the silicon device layer to determine the laser wavelength, while keep the optical confinement in the III-V waveguide layer high, in order to reduce device footprint and power consumption. This can be realized by the resonant cavity mirror design shown in Figure 16a. Two identical passive silicon grating cavities are coupled to the III-V waveguide above to form a linear device. Each silicon cavity is evanescently coupled to the InP waveguide. If the optical mode in the InP waveguide is of the silicon cavity's resonance wavelength, the silicon cavity will be excited. The energy built-up inside the silicon cavity couples back into the InP waveguide both co- and counter-directionally to the incoming light. The co-directional light will interfere destructively with the InP waveguide mode while the counter-directionally coupled light propagates back into the III-V waveguide. Because CMOS manufacturing techniques allow for compact, high-Q silicon cavities, this approach enables high and narrow band reflectivity over a short distance. An optically pumped proof-of-concept device [53] confirmed the potential advantages of using resonant mirrors as resonators in III-V-on-Si lasers. The threshold pump power of the experimentally demonstrated device was mW-level and the laser operated in single mode with a side-mode suppression ratio of up to 39 dB. However, the practical usability of optically pumped lasers is rather limited, as most applications require an electrical pumping mechanism. To achieve electrical pumping, metallic contacts have to be placed on the III-V waveguide structure to allow injection of electrical carriers. These metallic structures should be placed sufficiently far away

from the optical mode to prevent excessive loss due to absorption in the metal. This leads to relatively thick III-V waveguides (1–2 μm) and therefore a high modal effective index (~3.3), which prevents phase matching with the underlying silicon cavity. Moreover, such a large waveguide supports multiple transversal modes. Therefore, a novel mesa geometry was adopted, that allows for electrical injection in high vertical index contrast III-V membranes, as shown in Figure 16b. Lasing of resonant cavity mirror structures in pulsed operation was demonstrated, as discussed in [54]. Single mode operation was obtained with a threshold current of 4 mA in a 160 μm long device.
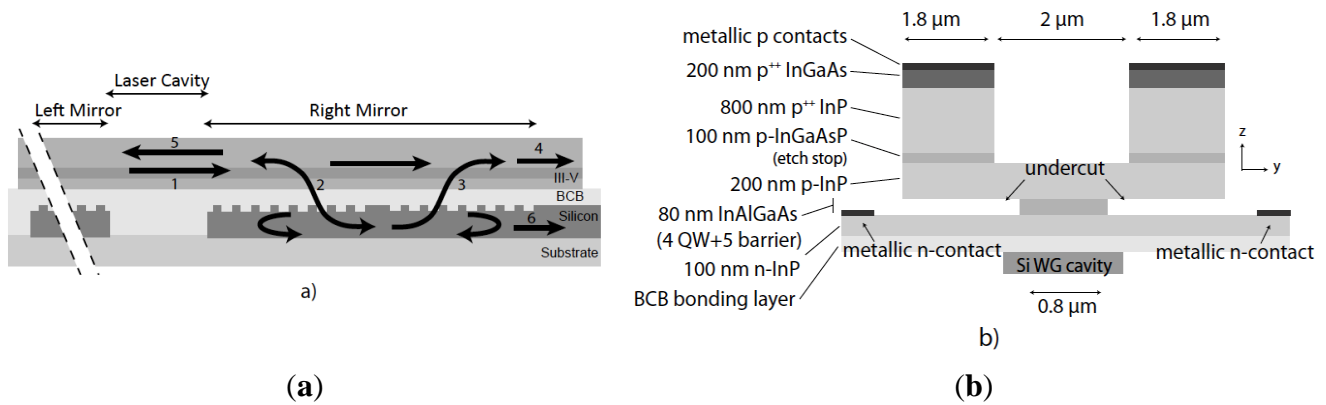

Figure 16. (**a**) Longitudinal cross-section of the resonant cavity mirror laser. (**b**) Transversal cross section of the electrically pumped device. Reproduced from [53,54].

850 nm VCSEL Integration

For various applications in the visible-NIR wavelength range, such as short reach optical data communication and spectroscopy, an integrated short-wavelength III-V-on-Si laser is of great interest. GaAs-based VCSELs are very energy-efficient light sources. While silicon photonic integrated circuits are opaque in the visible-NIR, Silicon nitride (SiN) based waveguide circuits can be used. Those circuits can also be fabricated in a CMOS fab, thereby inheriting the same advantages as the silicon-on-insulator waveguide platform. As a first step towards GaAs VCSEL integration on SiN waveguide circuits, we demonstrate a heterogeneously integrated short-wavelength hybrid-cavity VCSEL on Si, by bonding a GaAs-based "half-VCSEL" to a dielectric DBR (Ta_2O_5/SiO_2) on Si using ultra-thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive bonding. After bonding, oxide-confined GaAs VCSEL structures were fabricated in Chalmers University of Technology [55].

The device cross-section is illustrated in Figure 17a whereas the light-current-voltage characteristics under continuous operation, measured at 25 ℃ can be seen in Figure 17b. VCSELs with different oxide aperture diameters of three, five, seven, and nine μm were characterized. Threshold currents of 0.3 mA and 1.2 mA, respectively were measured with smallest and largest oxide aperture. A nine μm oxide aperture diameter VCSEL produces a maximum output of 1.6 mW at 845 nm wavelength, limited by thermal rollover at 6.0 mA bias current. These hybrid VCSEL structures show ~3 times higher thermal impedance than ordinary oxide-confined VCSELs, because of the low thermal conductivity of the dielectric DBR. At present the performance of VCSEL is mainly limited by high thermal impedance, which can be further improved by integrating a metallic heat spreader.
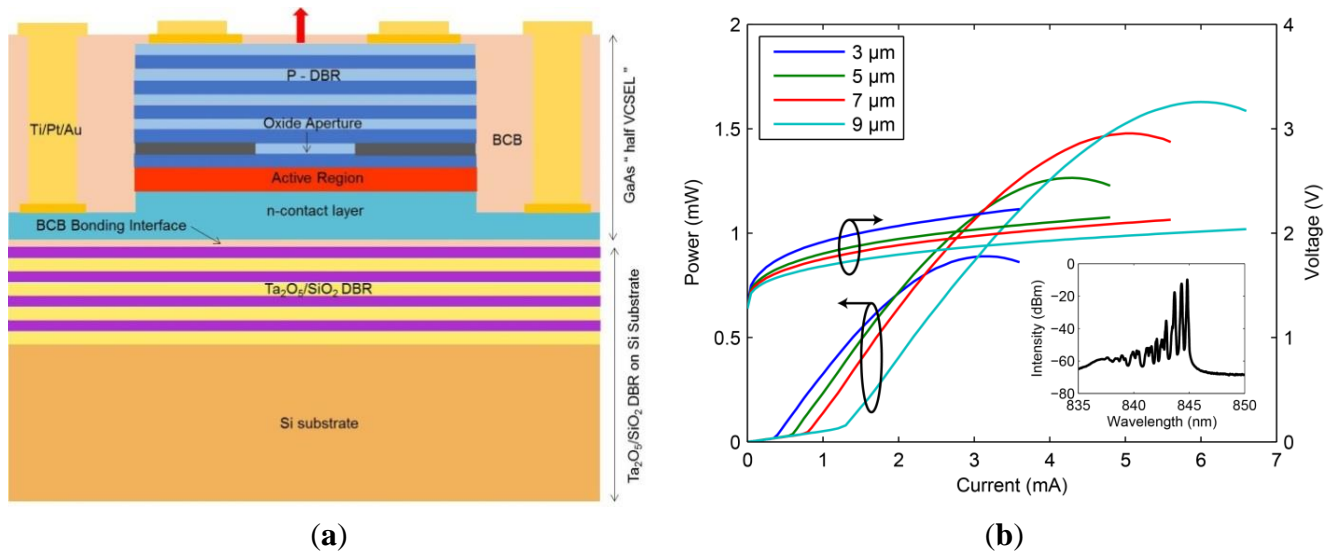
(**a**)   (**b**)

Figure 17. (**a**) Schematic cross-section of the oxide-confined hybrid-cavity VCSEL. (**b**) Measured light-current-voltage characteristics for hybrid-cavity VCSELs with oxide aperture diameters of 3–9 μm. Inset: laser spectrum for a 7 μm aperture VCSEL operated at 3.0 mA. Reproduced from [55].

4.2. III-V-on-Silicon Electro-Absorption Modulators for Optical Communication Applications

Wavelength division multiplexing (WDM) modules are of key importance for realizing high aggregate bitrate optical interconnects. To imprint data on the individual optical carriers, both direct modulation and external modulation can be used. In the case of external modulation, for shorter distance links III-V EAMs are often used. We developed a 5×20 Gbps WDM transmitter consisting of an array of 5 EAMs heterogeneously integrated on a silicon PIC used for wavelength multiplexing (using an AWG) and fiber-chip interfacing, operating around 1.55 μm [56]. The lumped III-V EAMs show a 3-dB E/O bandwidth of 17 GHz and can operate up to 28 Gbps. A module with a compact footprint (1.5×0.5 mm^2), a low driving voltage (~2.5 V$_{pp}$), and a large extinction ratio (4.9–6.9 dB) is obtained with 100 Gbps capacity. Figure 18a shows the schematic of the chip layout. On each channel of the AWG, a separate EAM is integrated. The AWG is formed using 220 nm height silicon rib waveguides and it has five channels with 200 GHz channel spacing. The top view of the EAMs is shown in Figure 18b. The passive silicon waveguide underneath is a rib waveguide with 1.5 μm width and is 160 nm etched into the 380 nm silicon layer. The optical coupling between the silicon device layer and the III-V epitaxial stack is realized using a multi-level taper consisting of two linearly tapered sections in the III-V structure, as discussed in Section 3.1. The coupling efficiency from the passive silicon waveguide to the III-V waveguide using this 45 μm long taper can be more than 95%.

The minimum insertion loss of the EAM at 0 V bias is measured to be 1.2 dB. The spread in insertion loss is attributed to device-to-device fabrication variations. Figure 19a illustrates the measured static extinction ratio of the 100 μm long EAMs under different reverse biases. More than 12 dB extinction ratio can be achieved when the bias is changed from 0 V to −2.5 V. Figure 19b–f shows the eye diagrams after the AWG multiplexer at 20 Gbps for the five different channels. All EAMs exhibit clean and open eyes. The dynamic extinction ratios vary between 4.9 dB and 6.9 dB.
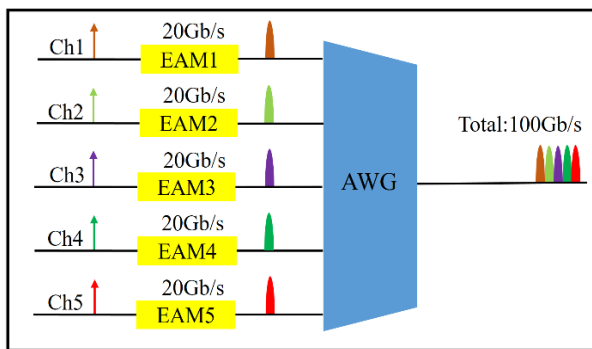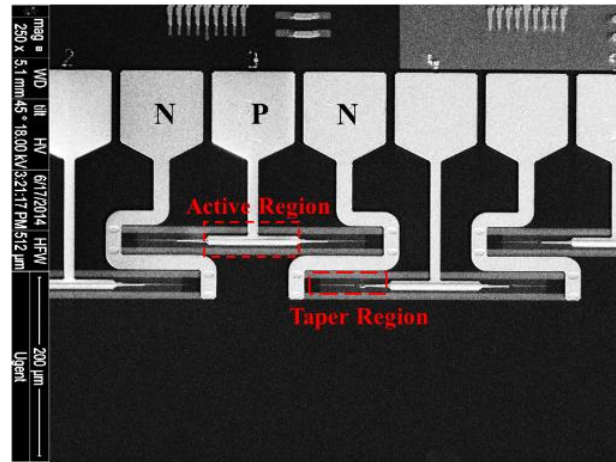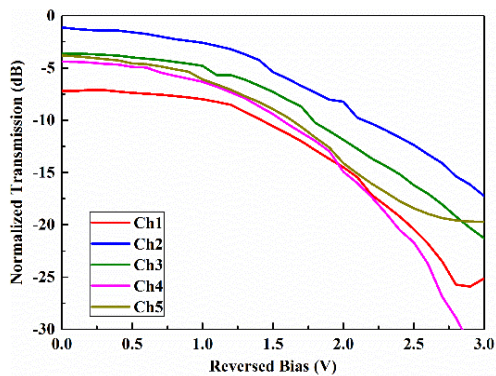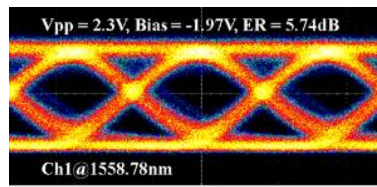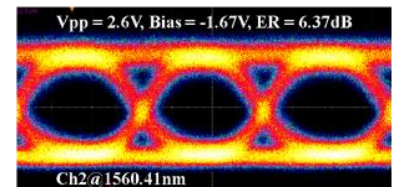
(**a**) (**b**)

Figure 18. (**a**) Schematic diagram of the chip layout. (**b**) top-view of the III-V on silicon EAMs. Reproduced from [56].
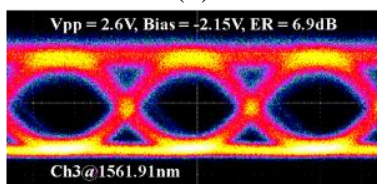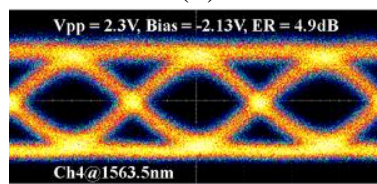

(**a**) (**b**) (©)
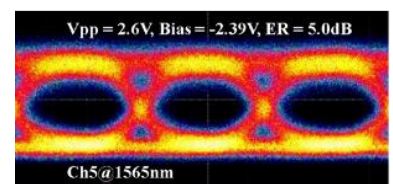
(**d**) (**e**) (**f**)

Figure 19. (**a**) Bias dependent normalized transmission of each channel. (**b**–**f**) Optical eye diagrams at 20 Gbps for each channel. Reproduced from [56].

5. III-V-on-Silicon Devices for Optical Sensing Applications

While PICs are mainly targeting optical communication applications, the use of the integration platform is currently also being considered for optical sensing applications. Most efforts so far have been focused on bio-sensors, using chemically functionalized integrated optical resonators as the transducer for the binding of bio-molecules to the silicon surface. Large arrays of chemically functionalized resonators can this way be integrated on a low-cost, disposable chip. In this application, the selectivity of the sensor is completely determined by the functionalization chemistry. Therefore, it is interesting to study whether other integrated sensor systems could be realized on the silicon photonic platform, and

could get their selectivity not from chemical functionalization, but rather from the specific absorption spectrum that each molecule possesses. This absorption spectrum serves as a fingerprint for the molecule and allows for the analysis of the composition of a liquid, gas or solid sample. Opposite to small gas molecules, which have very sharp absorption lines, the absorption spectrum of many molecules of interest in the context of bio-applications show rather broad absorption spectra. This makes the use of integrated laser sources less suitable for this purpose. Rather, there is a need for broadband light sources and integrated spectrometers integrated on a single chip. Depending on the molecules of interest, the operational wavelength range of the spectroscopic sensor will also be different. In this section, we will elaborate on our work towards the integration of broadband optical sources on a silicon PIC, as well as the realization of integrated spectrometers. For the broadband sources, we will focus on the 1.2 μm to 2 μm wavelength range, while for the integrated spectrometers operation up to 3.8 μm wavelength will be described.

5.1. III-V-on-Silicon Broadband Light Sources for Optical Sensing Applications

5.1.1. Superluminescent LEDs

An important building block for the realization of a full on-a-chip spectroscopic system is an efficient broadband light source that can be integrated onto PICs. In many of such sensor applications high power and wide bandwidth sources are of critical importance, making superluminescent LEDs the preferred option. To achieve the wide bandwidth, we opted, in a collaboration with the University of California—Santa-Barbara, for a combination of quantum well intermixing and multiple die bonding. Other techniques use a dual QW design [57], multistate QWs [58], quantum dots [59] or use supercontinuum generation. The latter is discussed in paragraph 5.2.3, the others are difficult to design and optimize given their complex structure and only work well at specific drive currents. Quantum well intermixing is a technique where the composition of the quantum well and barrier is changed by atom disordering. Before bonding, the InP epitaxial layer stack is implanted with phosphorous atoms, which are annealed into the active region. Depending on the mask applied before the implant and the annealing duration and temperature, the band gap is locally blue shifted. A typical maximum shift is 100 nm at telecom wavelengths [60]. To shift the band gap further, a second die was bonded. Since each die was intermixed, four band gaps were transferred to SOI. The emission from these different active regions was combined in series, as depicted in Figure 20. This implies that the longest wavelengths propagate through all the other sections.

After combining multiple die bonding and quantum well intermixing, a broadband superluminescent LED was fabricated with the process described in [60]. Each band gap section can be pumped separately, as shown in Figure 21a. In order to maximize the 3 dB bandwidth, the pumping currents are individually tuned, resulting in the spectrum shown in Figure 21b. The on-chip power is −8 dBm and the 3 dB bandwidth is 292 nm, ranging from 1258 nm to 1550 nm.

These devices were heterogeneously integrated using molecular bonding. A COMSOL heat simulation of the superluminescent LED shows a thermal resistance (normalized to surface area) of $12.8 \frac{Kcm^2}{kW}$ for a 50 nm thick BCB bonding layer and $10.5 \frac{Kcm^2}{kW}$ for molecular bonding, indicating that

the largest source of thermal impedance is the buried oxide layer underneath the silicon waveguides, and not the thin DVS-BCB bonding layer.
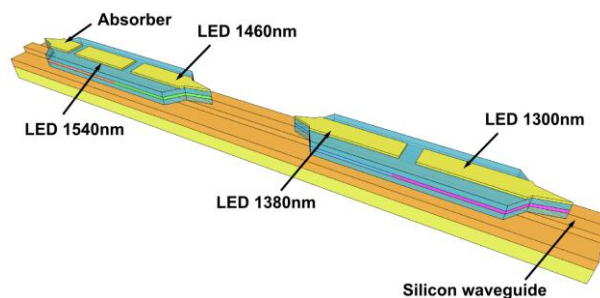

Figure 20. Illustration of superluminescent LED comprised of four band gaps connected to a silicon waveguide circuit. Reproduced from [60].
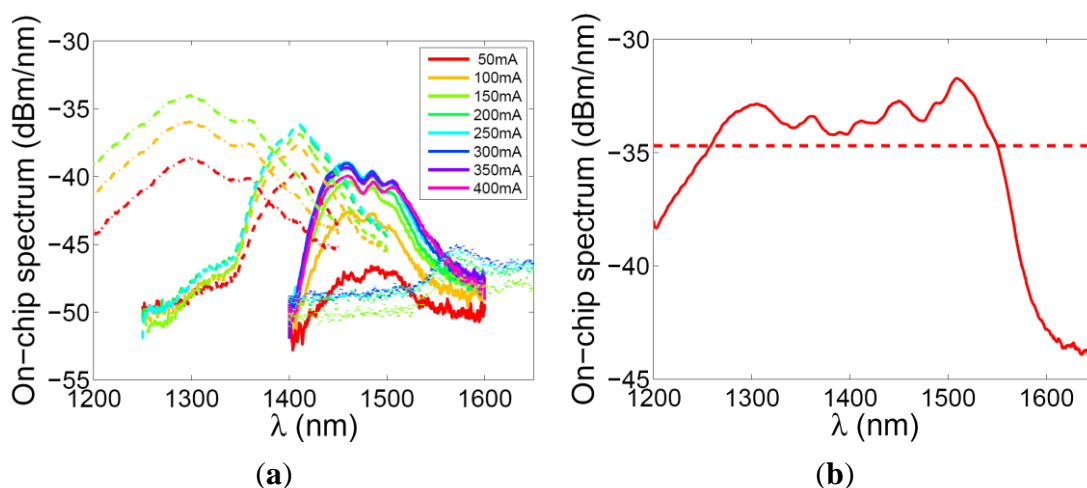

(**a**)   (**b**)

Figure 21. (**a**) On-chip spectra when pumping the different sections of the superluminescent LED. The dashed, dash-dotted, solid and dotted lines indicate the section at 1300 nm, 1380 nm, 1460 nm and 1540 nm respectively. (**b**) On-chip spectrum when pumping the different sections of the superluminescent LED differently to maximize optical bandwidth. The pumping currents were 70 mA, 50 mA, 300 mA and 140 mA for the sections at 1300 nm, 1380 nm, 1460 nm and 1540 nm respectively. Reproduced from [60].

5.1.2. Power-Efficient Single Spatial Mode LEDs

Similar to superluminescent LEDs, power efficient LEDs would be of great use in sensing applications. Especially if this integrated LED can combine efficiency and fabrication simplicity, one can think of high-volume low-cost spectroscopic sensors based on these devices. Using heterogeneous integration, very high refractive index contrast III-V membranes can be realized. In a high refractive index contrast waveguide, the efficiency of capturing the spontaneous emission into a single spatial mode is boosted compared to classical low index contrast structures. While electrical injection of such thin membranes is difficult, an optically pumped membrane LED can be envisioned, pumped by an efficient waveguide coupled laser sources, such as a VCSEL. Avoiding the electrical pumping also makes the device fabrication more straightforward.

We have been investigating the integration of thin InP membranes on top of an SOI waveguide to create an efficient optically pumped waveguide coupled LED [61]. The thin membranes are obtained by bonding an ultra-thin III-V stack onto the SOI chips via DVS-BCB bonding, as shown in Figure 22. In combination with an appropriate waveguide design, the membrane (LED) can be optically pumped via the single mode SOI waveguide underneath. A significant power fraction of the entire spontaneously emitted light couples back into the single mode of the SOI waveguide.

The device in Figure 22a consists of an SOI photonic wire waveguide that tapers down, squeezing the pumping mode into the III-V membrane. The III-V is shaped as a ridge waveguide and has a taper connection to the silicon as well. The membrane material is chosen to strongly absorb the optical pump. The absorbed light will generate electron-hole pairs that lead to spontaneous emission, which is collected efficiently into a single spatial mode in the III-V membrane waveguide because of the high refractive index contrast.
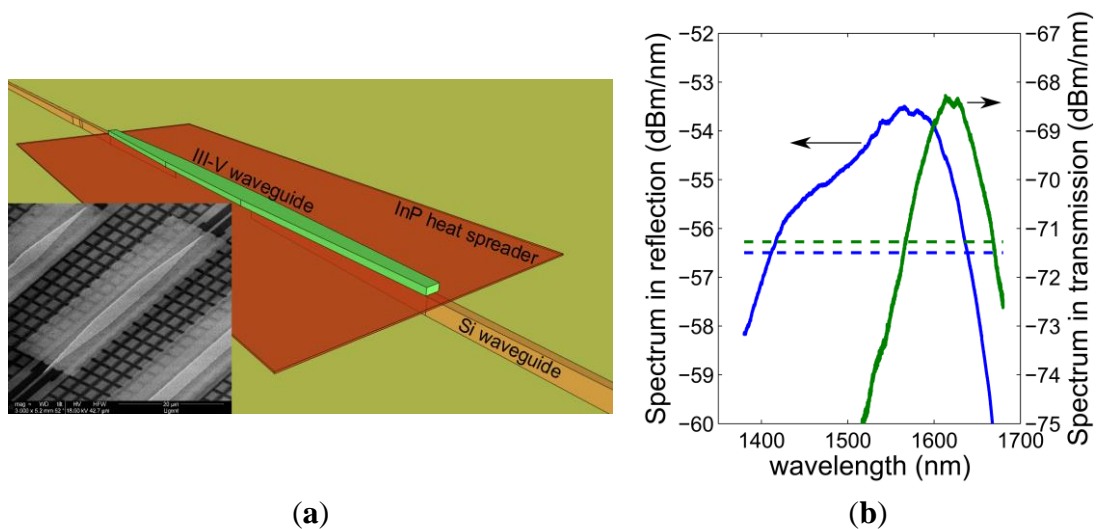

<div align="center">(a)   (b)</div>

Figure 22. (**a**) Illustration of an optically pumped membrane LED. (inset) SEM image of the fabricated device. (**b**) Measured spectra of an optically pumped LED (50 μm device length; green: in transmission; blue: in reflection). Reproduced from [61].

By optimizing the confinement of the pump light in the III-V material and the spontaneous emission collection efficiency in the SOI waveguide, an optimum membrane thickness of 115 nm is obtained. For the layer stack reported in [61], the confinement factor in the four quantum well structure is 18.4%. The spontaneous emission collection efficiency into the fundamental guided mode in the SOI, is around 10%. The spontaneous emission couples to both forward and backward propagating modes in the SOI, meaning it is possible to collect light both in transmission and in reflection. Given the strong pump absorption, the carrier concentration will be highest at the first taper and lower towards the end of the III-V waveguide due to pump depletion. For the signal in transmission, there will be an optimum device length: a very long device may not be pumped completely to transparency and hence reabsorb the spontaneous emission. The spontaneous emission in reflection does not suffer from this problem, but then a photonic integrated circuit to (de)multiplex signal and pump has to be designed. Figure 22b shows the LED spectra collected both in transmission and reflection for a 50 μm long LED. Optical pumping was done at a wavelength of 1310 nm using 0.5 mW waveguide coupled power. The collected spectrum

in reflection is broad (3 dB bandwidth of 230 nm) peaking at 1565 nm, while in transmission the collected spectrum is both weaker (15 dB difference) and narrower (3 dB bandwidth of 100 nm). It is also red-shifted to 1613 nm. The difference between the transmission and reflection spectrum is attributed to incomplete pumping of the LED. Towards the end of the device, the shorter wavelengths are absorbed again.

5.1.3 Supercontinuum Generation in a III-V on Silicon Waveguide Structure

On-chip supercontinuum generation (SCG) has attracted a lot of attention from researchers because of a number of exciting potential applications such as sensing [62,63], spectroscopy [64], telecommunications [65], optical clocks and frequency metrology [66]. On the SOI platform, by taking advantage of the large Kerr index of silicon ($n_2 \approx 6 \times 10^{-18}$ m^2/W) and the tight confinement of light due to its large index contrast, SCG has been successfully demonstrated in different pump pulse width regimes and wavelength ranges [67–71]. However, silicon as a nonlinear material for SCG has certain drawbacks: its small bandgap of 1.1 eV means that it suffers from large nonlinear losses due to two-photon absorption (TPA) and the associated free-carrier absorption (FCA) when pumping at wavelengths below 2.2 µm. While this effect is somewhat reduced by the use of hydrogenated amorphous silicon [68,70], certain III-V materials like InGaP offer not only a similarly large Kerr index and linear refractive index as silicon but also have a large bandgap (E_g = 1.9 eV) thereby eliminating TPA-based nonlinear losses for pumping in the telecom wavelength range. Unlike silicon, III-V materials also possess a strong second-order nonlinearity, which can be further exploited alongside the third-order nonlinearity.

In order to generate a supercontinuum in the 1–2 µm wavelength range we consider the use of InGaP membrane waveguides integrated on top of a SOI or SiN waveguide circuit. As a first step, the generation of a supercontinuum on an InGaP membrane waveguide not interfaced with a silicon-based PIC is demonstrated. In this case, the InGaP membrane—which is grown lattice matched on a GaAs substrate—is adhesively bonded to a silicon substrate with 3 µm thick thermal oxide on top. The GaAs substrate is then removed by wet etching. Using e-beam lithography and ICP etching in a two-step process—in collaboration with the Laboratoire de Photonique et Nanostructure, Paris and Thales Research and Technology—photonic wire waveguides coupled to shallow etched fiber-to-chip grating couplers are fabricated. Details about the fabrication and the linear and nonlinear properties of the fabricated waveguides can be found in [72]. The large index contrast between the III-V membrane and the oxide or DVS-BCB layer beneath allows for strong nonlinear interactions through the tight confinement of light. For SCG, we pump dispersion engineered InGaP membrane waveguides with 170 fs pump pulses centered at 1550 nm [73]. In this pulse duration regime, SCG is known to occur via soliton fission and dispersive wave generation both of which depend critically on the dispersion properties of the waveguide [74,75]. As such, the waveguide is designed to exhibit anomalous dispersion at the pump wavelength and have two zero-dispersion wavelengths (ZDWs) on either side of the pump. Figure 23a shows the supercontinuum spectrum at the output of InGaP membrane waveguides of different widths. Dispersive waves can be observed flanking the spectra on both ends of the spectrum and their positions vary for the different waveguides. The locations of the ZDWs relative to the pump wavelength (see Figure 23b) are critical in determining the position of these dispersive waves and thus the overall bandwidth of the supercontinuum. For the case of the 700 nm wide waveguide, the dispersive waves are located at 1005 nm

and 2097 nm as shown in Figure 23c. The supercontinuum is thus octave-spanning which is important for certain frequency metrology applications. This clearly demonstrates the importance of dispersion engineering for achieving the widest possible supercontinuum. The octave-spanning spectrum was achieved with a pulse energy of only 2 pJ which constitutes an order of magnitude improvement over the state-of-the-art SCG achieved in SOI at these wavelengths [71]. Figure 23d shows the simulated evolution of the spectrum along the length of the 700 nm wide waveguide and is seen to match well with the experimentally observed spectrum shown in Figure 23c. Spectral broadening occurring due to self-phase modulation, soliton fission and dispersive wave emission can be seen. One can also see that the octave spanning SCG is achieved in a waveguide of only 1.5 mm long.
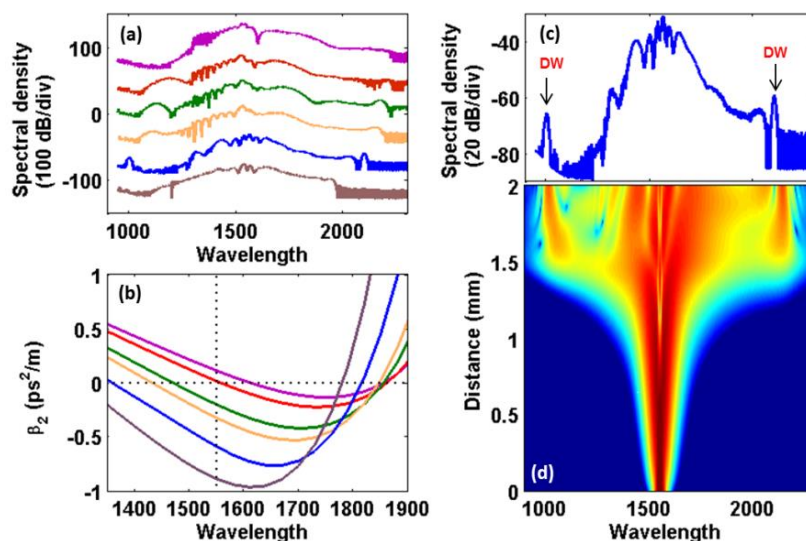

Figure 23. (**a**) The supercontinuum spectra at the output of 2 mm long waveguides of widths 800 nm, 790 nm, 770 nm, 760 nm, 700 nm and 650 nm respectively from top to bottom. Individual spectra have been displaced by 40 dB for clarity. Dispersive waves can be observed at the ends of the spectra for all the waveguides. (**b**) The simulated dispersion profiles of the waveguides showing the ZDWs on either side of the pump wavelength at 1550 nm. (**c**) The experimental octave-spanning supercontinuum for the 700 nm wide waveguide with arrows showing the position dispersive waves. (**d**) The simulated evolution of the supercontinuum spectrum along the waveguide propagation length, which matches well with the experimental spectrum shown in (**c**). Reproduced from [73].

5.2. III-V-on-Silicon Spectrometers for Optical Sensing Applications

As discussed above, there is an interest in spectroscopic sensors in which the absorption spectrum of a sample is measured. When a broadband light source is used, a spectrometer is required to spectrally decompose the transmitted light and compare it to the light that went through a reference path that did not go through the sample under study. Single mode optical spectrometers provide the best possible resolution for a given device footprint and are therefore of great interest for these applications. Besides passive spectrometers, also integrated photodetector arrays are required. For the telecommunication wavelength range, Ge-based photodetectors are typically used. Recently, low dark current, high

responsivity devices have been demonstrated with a cut off wavelength of about 1600 nm [76]. In many spectroscopic sensing applications one wants to work beyond a wavelength of 1600 nm, because of the more pronounced absorption features at longer wavelengths. This again requires the heterogeneous integration of III-V semiconductor devices onto the silicon photonic spectrometers. In next sections, we will elaborate on such III-V-on-silicon spectrometers for operation beyond the telecom wavelength window.

5.2.1. Passive Integrated Spectrometers

Integrated spectrometers are essential components for on-chip spectroscopic systems. Arrayed Waveguide Grating (AWG) and Planar Concave Grating (PCG) are the two most commonly used dispersive integrated spectrometers. Both types of devices work on the principle of interference of multiple light paths. An AWG consists of two free propagation regions (also known as star couplers), which are connected by delay lines having constant path length increment between them. Light is split up in the input star coupler and the different contributions after passing through delay lines interfere in the output star coupler. As a result, different wavelengths are focused at different places and can therefore be guided to separate output waveguides. In a PCG, the same slab is used for de-focusing as well as focusing while the constant length increment is achieved by a curved grating. More information about theory and design of AWGs can be found in [77] and details about PCG design are available in [78]. We have demonstrated different integrated spectrometers in different silicon and silicon nitride based platforms. The performance summary is given in Table 2 with references to the original publications. Figure 24 shows measured transmission spectra—in collaboration with the University of Southampton—of an AWG and PCG in the mid-infrared wavelength range.

Table 2. Representative integrated spectrometers across different platforms.

| Device/Technology	Central Wavelength (μm)	Footprint (mm²)	No of Channels/Channel Spacing (nm)	FSR (nm)	Insertion Loss (dB)	Crosstalk (dB)
AWG/SOI [79]	1.55	0.231	16/3.2	57.6	<3.0	>25.0
AWG/Si₃N₄ [80]	0.89	0.337	12/2	30	<1.5	>20.0
S-AWG/SOI [81]	1.55	0.079	4/30	144	<2.0	>19.0
AWG/SOI [14]	2.20	1.000	6/1.6	13	<3.0	>17.0
AWG/SOI [82]	2.37	0.439	7/5	50	<3.0	>25.0
AWG/SOI [83]	3.80	0.858	6/10	80	<2.0	>20.0
PCG/SOI [14]	1.55	0.269	8/6.5	100	<1.5	>20.0
PCG/SOI [14]	2.32	1.040	8/5	60	<6.0	>15.0
PCG/SOI [83,84]	3.80	3.060	8/10	105	<2.0	>20.0
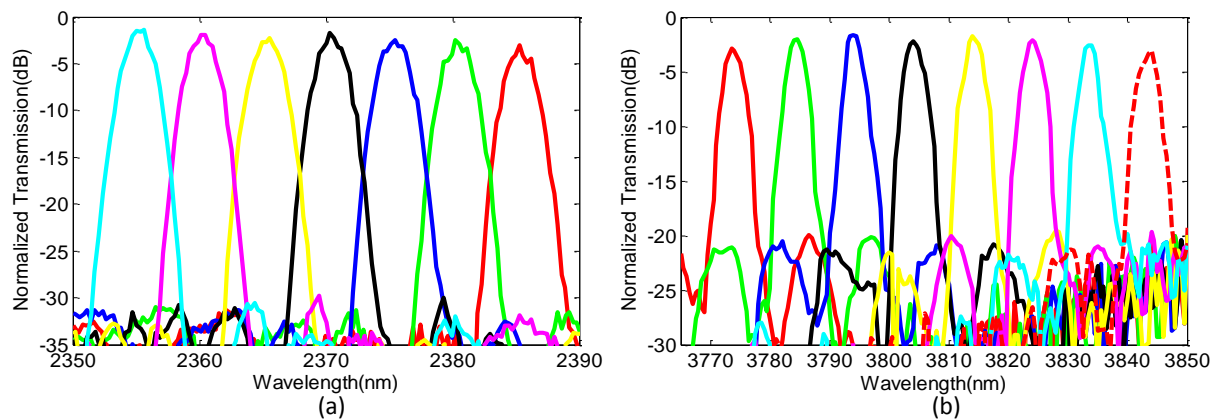
Figure 24. (**a**) Measured transmission spectra of short-wave infrared AWG [82]. (**b**) Measured transmission spectra from a mid-infrared PCG [83].

5.2.2. GaSb-Based Photodetector Integration

The antimony-based material system can be used for photodetection beyond the telecommunication wavelength window. This material system can make use of three group III elements (Al, Ga, In) and two group V elements (As, Sb) to cover a wide wavelength range. Epitaxial layers of this material system can be grown lattice matched to GaSb or InAs substrates. Solid-source Molecular Beam Epitaxy (MBE) is used by the University of Montpellier to grow GaInAsSb and InAsSb based epitaxial layer stacks on on-axis (100) oriented n-type GaSb substrates. The MBE reactor is equipped with both As- and Sb-valved cracker cells and conventional element-III cells. Be and Te are used as p- and n-type dopants. $Ga_{0.79}In_{0.21}As_{0.19}Sb_{0.81}$ based PIN diode structures have been grown to reach a cut-off wavelength of 2.65 µm whereas $InAs_{0.91}Sb_{0.09}$ based PIN diode structures are used to cover the 3 µm wavelength range. Details about epitaxial layer stacks and their growth can be found in [13,15,85,86]. The integration process starts with the fabrication of the SOI spectrometers in imec's CMOS pilot line. Then DVS-BCB based adhesive bonding is used to bond the III-V die to the SOI chip. After bonding, the GaSb substrate is removed using mechanical grinding and wet etching with a HF/CrO_3 solution, until the etch stop layer is reached. After removing the etch stop layers by wet etching, the photodetector mesa is fabricated lithographically aligned to the underlying output grating couplers of the SOI spectrometer. Ti (2 nm)/Pt (35 nm)/Au (100 nm) contacts are then deposited using e-beam evaporation. To passivate the device, DVS-BCB is then spin coated on the sample and cured at 250 °C for 1 h. Finally, deposition of Ti/Au contact pads is carried out after etching the DVS-BCB to access the top and bottom contacts. Figure 25a shows a microscope image of a fabricated silicon photonic AWG with integrated photodetectors.

We have demonstrated evanescently coupled GaInAsSb based photodetectors in [85] and [13] with a responsivity as high as 1.4 A/W at room temperature. Grating-coupled GaInAsSb based photodetectors are demonstrated in [13–15] with an on-chip responsivity as high as 0.6 A/W. In [14] an array of 46 detectors was integrated onto a spectrometer chip, showing the scalability of the integration process. Recently, we have also successfully integrated grating-assisted InAsSb-based photodetectors on an AWG operating at wavelength of 3.8 µm. A responsivity of 0.3 A/W at room temperature was obtained [86].
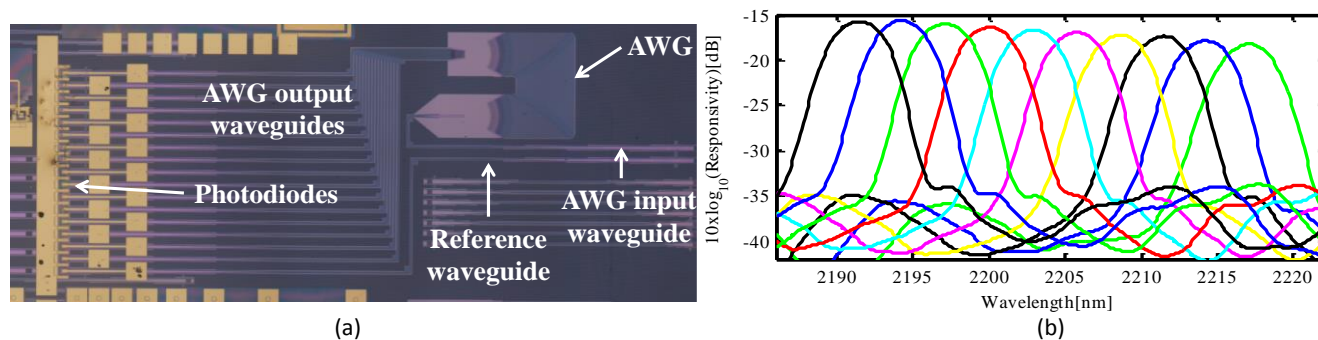
Figure 25. (**a**) Microscope image of a silicon AWG after integration of GaInAsSb photodetectors. (**b**) Measured photoresponse of this III-V-on-silicon spectrometer. Reproduced from [15].

5.2.3. InP-Based Photodetector Integration

Compared with GaSb, the InP-based material system uses a cheaper substrate for epitaxial growth and the related heterogeneous integration technology is more mature. The cut-off wavelength of active device based on type-I lattice matched active regions is limited to about 1.75 μm. By straining the active region, operation up to 2.3 μm can be obtained [87]. In recent years, high performance electrically pumped lasers using type-II InP-based heterostructures were reported, lasing in a wavelength range from 2.2 μm to 2.7 μm [88]. Therefore, the heterogeneous integration of type-II active devices on SOI is attractive for spectroscopic sensors operating in the 2 μm wavelength range. Type-II InP-based photodiodes were integrated on a silicon waveguide circuit using adhesive bonding technology [89]. The absorbing active region of the photodiodes consists of six periods of a "W"-shaped quantum well as shown in the inset of Figure 26a. Light is coupled from the silicon waveguide to the III-V waveguide using a taper structure. The dark current under reverse bias of 0.5 V is 12 nA as shown Figure 26a, which is much lower than the hybrid GaSb-based photodiodes (1.13 μA at −0.1 V). Figure 26b shows the fiber-referred optical spectral responsivity of the photodiodes, together with the fiber-to-chip grating coupler efficiency. The waveguide-referred responsivity is higher than 0.5 A/W over the wavelength range of 2.2–2.42 μm (the wavelength range limitation of our laser source). The peak fiber-referred responsivity is 0.12 A/W at 2.32 μm, corresponding to a waveguide-referred responsivity of 1.2 A/W. The epitaxial layer stack used for the photodiode integration can also be used to realize edge emitting lasers or superluminescent LEDs, thereby enabling fully integrated spectroscopic sensor systems in the 2 μm wavelength range.
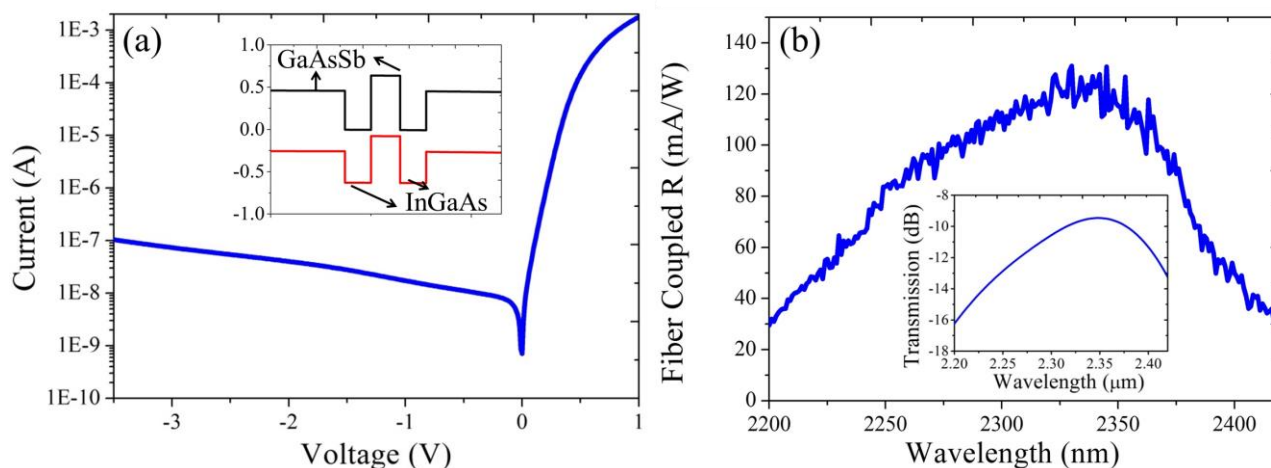
Figure 26. (**a**) I-V curve of the photodiodes without light input, the inset picture shows the band structure of one period of the "W"-shaped quantum well. (**b**) Wavelength dependence of the fiber-referred responsivity of type-II photodiodes (inset: fiber-to-chip grating coupler efficiency). Reproduced from [89].

6. Conclusions

Heterogeneous integration is a powerful approach to integrate high performance III-V opto-electronic components onto silicon-based photonic integrated circuits. In this paper, the integration of different types of opto-electronic components including semiconductor lasers, optical amplifiers, electro-absorption modulators, light emitting diodes and photodetectors onto silicon photonic integrated circuits is demonstrated. In most of these examples, the opto-electronic components are integrated on planarized and passive silicon waveguide circuits. While already quite complex, photonic integrated circuits can be realized this way, by co-integrating different III-V opto-electronic components, much added value could be created if these III-V opto-electronic components were heterogeneously integrated on the full silicon photonics platform, including high speed silicon optical modulators, germanium (avalanche) photodetectors, heaters, efficient fiber-to-chip couplers, *etc.* This requires the local removal of the back-end stack in order to bring the III-V epitaxial material in close proximity to the silicon device layer. It can be expected that the etching of the back-end dielectric stack down to the silicon device layer will result in a non-flat surface. In addition, in this context, the use of adhesive die-to-wafer bonding is very appealing, as it is quite forgiving in terms of surface topography and roughness, giving the planarizing action of the DVS-BCB bonding agent. This integration is the subject of future research.

Acknowledgments

Conflicts of Interest

The authors declare no conflict of interest.

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