Ultra-low-voltage Micro-ring Modulator Integrated with a CMOS Feed-forward Equalization Driver

J. C. Rosenberg, W. M. J. Green, A. V. Rylyakov, C. L. Schow, S. Assefa, B. G. Lee, C. Jahnes, Y. A. Vlasov
IBM T. J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY 10598
jcrosenb@us.ibm.com

Abstract: We present an all-CMOS micro-ring modulator packaged with a feed-forward equalization driver circuit, operating in charge-injection mode at 8 Gbps with a drive voltage of only 50 mVp-p and a power consumption of 1.8 pJ/bit.

OCIS codes: (250.7360) Waveguide modulators; (250.5300) Photonic integrated circuits

1. Introduction

Short-reach VCSEL-based optical interconnects provide high bandwidth, low power communication between modules and racks in large high-performance computing systems [1]. In a typical configuration, signals are passed through backplane circuit board channels to an optical transceiver, where electrical signals are transferred into the optical domain. However, traveling over tens of inches on the backplane, the electrical signals are strongly attenuated [2]. Thus, the transmitter needs to not only be low-power and high bandwidth, but should also provide a high sensitivity to be able to re-transmit these highly attenuated signals.

Silicon photonics potentially can provide even higher performance and lower power. Silicon micro-ring modulators are good candidates for building CMOS-compatible ultra-low-power transmitters. A recent demonstration has shown 5 Gbps operation utilizing a micro-ring carrier-depletion modulator integrated with a CMOS driver equipped with a circuit to increase the voltage swing to 2 V, achieving a power consumption of 400 fJ/bit [3]. However, this device was driven directly from a digital signal, so would not be suited for receiving highly attenuated signals transmitted from distant chips on the same PCB.

Carrier-injection devices can, in contrast, achieve large modulation for very small voltage swings because of the comparatively large current flowing across the diode at turn-on [4]. This sensitivity allows them to be more easily driven by CMOS drivers, and increases the overall sensitivity of the transmitter. However, the operating speed of carrier-injection-based devices is traditionally limited to below 1 Gbps by the slow diffusion of minority carriers [5]. This effect can be mitigated by applying a pre-emphasized drive signal [6,7], but thus far the pre-emphasis signal processing has always been performed off-chip as the drive voltages required have been far outside the realm of standard CMOS circuitry, as high as 7 [6] or 16 Vp-p [7]. Not only are such large drive voltages impractical to produce on chip, but they also draw a considerable amount of power.

Here we combine a custom-designed CMOS pre-emphasis driver with a silicon micro-ring modulator that operates with an ultra-low voltage swing, resulting in a packaged transmitter that achieves 8 Gbps operation at a drive voltage on the modulator of only 50 mVp-p with single-ended operation.

2. Micro-ring modulator

The micro-ring modulator device shown in Fig. 1(a) was fabricated on an SOI substrate with a 2 μm buried oxide layer, using a subset of IBM standard front-end CMOS processes and following the requirements of 90 nm CMOS mask design rules, as described in Ref. 8. The ring was designed with a p^+-i-n^+ doping profile for charge injection-based operation, with a 156.8 μm circumference in a racetrack configuration with 6.5 μm bends, coupled to one rib waveguide. The ring and bus waveguides were measured to be 500 nm in width and 170 nm in height, with a 50 nm silicon slab providing carrier transport from the electrical contacts. To provide an optimally low RC time constant, the highly doped contact regions extended to 200 nm from the edges of the micro-ring resonator, and the use of mature CMOS processing technologies allowed for a low diode resistance of approximately 10 Ω. The proximity of the contacts results in a moderate optical quality factor of approximately 9000, trading a larger extinction ratio for superior stability and speed of the device. This quality factor could easily be increased, if desired, by using a lower doping concentration in the regions near the ring.

As can be seen in Fig. 1(b), an applied current of 630 μA is enough to shift the resonance wavelength by 80 pm, resulting in optical modulation of the input signal. Without any form of pre-emphasis, the modulation response is necessarily slow due to carrier dynamics, limited to 1 Gbps for this device. An eyeline diagram resulting from a standard voltage drive is shown in Fig. 1(c).

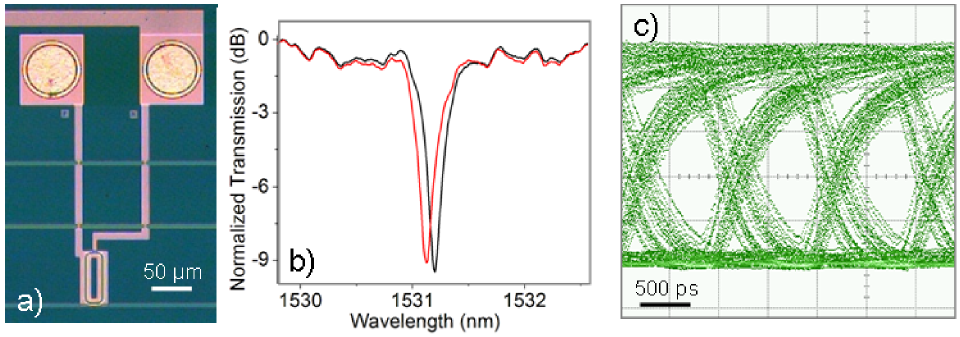

Fig. 1. a) Image of the micro-ring modulator device prior to packaging. b) Normalized transmission spectra of the micro-ring modulator, showing the resonance at zero bias (black) and at an applied current of 630 µA (red). c) 1 Gbps eyeline diagram without pre-emphasis, at an applied bias current of 80 µA.

3. CMOS feed-forward equalization circuit

The feed-forward equalization (FFE) circuit was fabricated using a standard digital 90-nm IBM bulk CMOS process, and is depicted schematically in Figure 2(a). The driver input stage consists of a 5-stage high-gain Cherry Hooper limiting amplifier (LA), specifically designed to operate with extremely low input drive signals as small as 10-20 mVp-p. The LA is equipped with an offset cancellation circuit designed to correct for transistor threshold variations in the differential gain stages. After amplification through the LA, the input signal is divided into two branches, referred to as the "main" and the "tap." The main signal passes through a current-mode logic buffer (main buffer), as illustrated by the red waveform. The tap signal is delayed in time relative to the main signal by passing through a series of buffers, and is subsequently amplified by an inverting output buffer (tap buffer), as shown by the blue waveform. The main and tap signals are summed at the FFE output, with the resultant waveform depicted in black. As the schematic illustrates, the variable delay and tap gain/weight (controlled by bias voltages VB_{DELAY} and VB_{TAP} respectively) can be adjusted to provide an electronically controllable pre-emphasis drive waveform to equalize the performance of the forward-biased p-i-n diode micro-ring modulator.

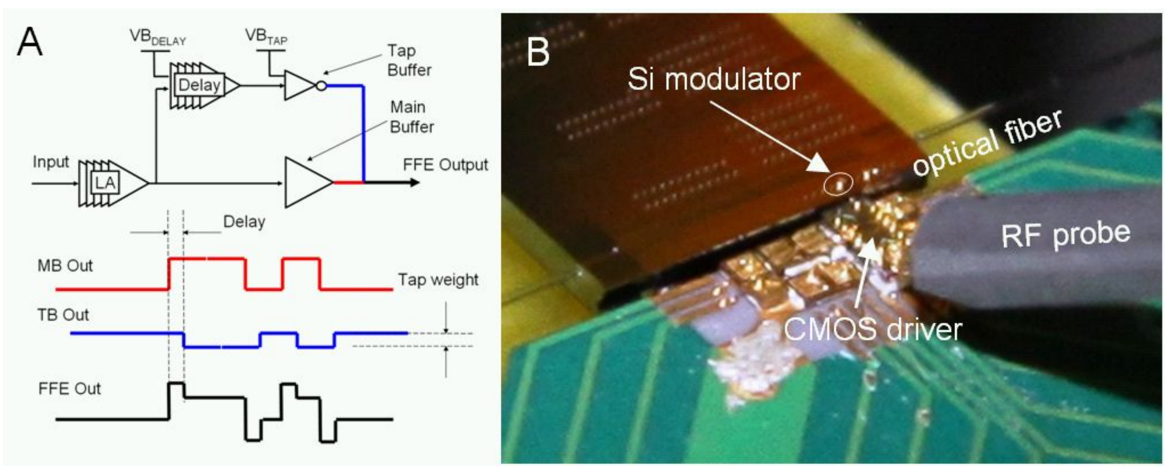

Fig. 2. a) Diagram of the CMOS feed-forward equalization circuit, showing the generation of the pre-emphasized output waveform. b) Image of the packaged transmitter.

4. Packaged Device

The photonics chip and CMOS driver circuit were packaged together on a modified printed circuit board, cut away to expose the edges of the photonics chip for coupling to tapered and lensed fibers on either side. Electrical contact between the chips was made via wirebonding. The packaged device is shown in Fig. 2(b).

To demonstrate the feasibility of high bit-rate operation of a charge injection-based transmitter under CMOS-compatible drive conditions, we drive the feed-forward equalized micro-ring modulator at 8 Gbps, much faster than would be possible without equalization. The pre-emphasis waveform from the driver is shown in Fig. 3(a), and the resulting eyeline diagram in Fig. 3(b). By measuring the supply voltages and currents on the CMOS driver circuit and subtracting the excess current drawn to provide a 50 Ω input termination, we calculate a total power consumption for the packaged device of 14.2 mW, resulting in an energy of approximately 1.8 pJ/bit at 8 Gbps. As the power consumption of the analog driver circuit is roughly constant as the bit rate increases, significant improvements in energy efficiency can be achieved by moving to higher bit rates. In addition, by sacrificing some of the small-signal input sensitivity, the number of high-power limiting amplifier stages in the circuit could be reduced, resulting in a projected power consumption of 1.5 pJ/bit when driven directly from a digital signal for on-chip applications.

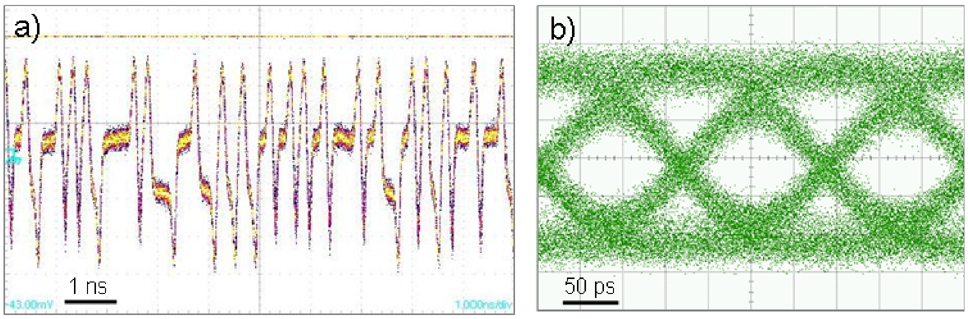

Fig. 3. a) A pre-emphasis drive waveform from the CMOS driver, with a peak-to-peak amplitude of 50 mV. b) Eyeline diagram of the modulated optical output at 8 Gbps with PRBS $2^7 - 1$.

5. Conclusion

We have demonstrated a charge injection-based silicon modulator that, when bonded to a CMOS feed-forward-equalization circuit, performs at 8 Gbps with a modulator drive voltage of only 50 mVp-p and with a low total power consumption of 1.8 pJ/bit. In addition, this transmitter is designed to operate with extremely low input drive signals, down to 20 mVp-p, making it well-suited to amplify and repeat heavily attenuated signals passed over long distances between chips. By bringing down the previously very large drive voltages and high powers required for pre-emphasis operation of forward-bias modulators, this packaged device takes advantage of the large variations of free-carrier density accessible in a charge injection-based device while maintaining the capability for on-chip integration using present-day CMOS technology.

6. References

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