5 x 20 Gb/s heterogeneously integrated III-V on silicon electro-absorption modulator array with arrayed waveguide grating multiplexer

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Abstract: We present a five-channel wavelength division multiplexed modulator module that heterogeneously integrates a 200 GHz channel-spacing silicon arrayed-waveguide grating multiplexer and a 20 Gbps electro-absorption modulator array, showing the potential for 100 Gbps transmission capacity on a 1.5x0.5 mm^2 footprint.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (250.7360) Waveguide modulators.

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1. Introduction

Wavelength division multiplexing (WDM) modules are of key importance for realizing high aggregate bitrate optical networks and optical interconnects. WDM transmitters and receivers require low cost and high performance devices for maximal bandwidth usage and high energy-efficiency. For the key opto-electronic components in a WDM system, both silicon and III-V based devices are available. Potentially CMOS compatible, low-cost, monolithic silicon WDM modulator chips have been reported [1, 2]. However, an optically broadband silicon-based modulator usually has a large footprint and requires a relatively high driving voltage and hence high power consumption for sufficient extinction ratio [3]. Alternatively, purely III-V WDM modulator chips have been demonstrated [4, 5]. Although they are more efficient than silicon modulators, the monolithic integration with passive wavelength division multiplexing devices, e.g. arrayed waveguide gratings (AWG) and etched diffractive gratings (EDG) requires involved techniques such as selected area growth (SAG), butt joint regrowth (BJR) or quantum well intermixing (QWI). In order to overcome these issues, a hybrid silicon platform that combines the advantages of III-V based materials and silicon is being studied. III-V/Si hybrid active devices with excellent performance, such as hybrid silicon narrow linewidth lasers [6], high-speed modulators [7], and high-speed detectors [8] have already been demonstrated. The highest speed modulators on silicon were achieved by transferring a III-V epitaxy stack onto a SOI wafer to realize a 67GHz bandwidth traveling-wave hybrid silicon electro-absorption modulator (EAM) [7]. These hybrid devices can be integrated together to build up more complex on-chip photonic modules [9, 10] on silicon-based substrates, which shows its potential for high density, high performance WDM transmitters and receivers for optical communication networks and multi-CPU optical interconnects in the future.

In this paper, a silicon AWG and an array of five III-V EAMs are heterogeneously integrated using adhesive bonding technology [11]. The (lumped) III-V EAMs show 17 GHz E/O bandwidth and can operate up to 28 Gb/s. A five-channel wavelength division multiplexed modulator module with an ultracompact size (1.5x0.5 mm^2), a low driving voltage (~2.5 Vpp), and a large extinction ratio (4.9-6.9 dB) is obtained with 100Gbps capacity.

2. Design

Figure 1 shows the schematic of the chip layout. On each channel of the AWG, a separate EAM is integrated. The AWG is formed by 220 nm height silicon waveguides and it has five channels with 200 GHz channel spacing. The III-V layer stack used for the EAM is shown in Table 1. The InAlGaAs multiple-quantum-well (MQW) stack is sandwiched between two separate confinement heterostructure layers (SCHs). It's composed of 10 compressively strained wells and 11 tensile strained barriers and has its photoluminescence (PL) peak at 1480 nm. Compared with InGaAsP quantum wells, the InAlGaAs quantum wells give a stronger quantum confined stark effect (QCSE) and hence a better modulation efficiency, due to its larger conduction band offset [12]. The layer stack is designed for transverse electric (TE) polarization [13] in the C-band, compatible with conventional semiconductor diode lasers. In our design, the confinement factors in the MQW region and in Si are 0.41 and 0.03,

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respectively. The superlattice layer structure is incorporated to prevent the propagation of dislocations into the active region due to the bonding.

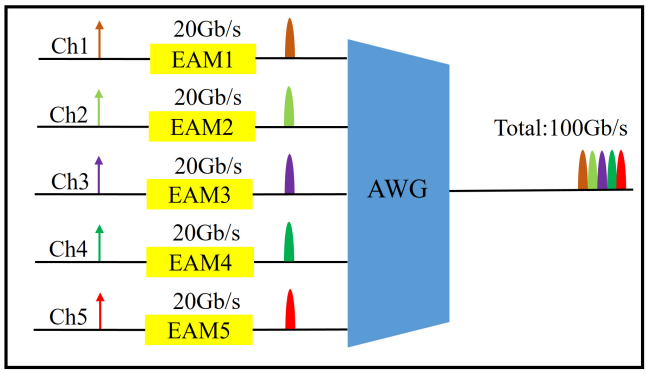

Fig. 1. The schematic diagram of the chip layout.

Table 1. Detailed III-V epitaxy stack.

Layer	Composition	Thickness(nm)
P contact	$In_{0.53}Ga_{0.47}As$	100
Cladding	InP	1500
SCH	$In_{0.52}Al_{0.16}Ga_{0.32}As$	150
MQW (λ_{PL}~1.48μm)	$In_{0.47}Al_{0.2}Ga_{0.33}As$ (11X)	7
	$In_{0.59}Al_{0.08}Ga_{0.33}As$ (10X)	11
SCH	$In_{0.52}Al_{0.16}Ga_{0.32}As$	100
N contact	InP	110
Super lattice	$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$ (2X)	7.5
	InP (2X)	7.5
Bonding layer	InP	10

Figures 2(a) and 2(b) are the cross-sectional view and top view of the EAM, respectively. The length of the active modulator section is 100 μm and it is 2 μm wide. Benzocyclobutene (DVS-BCB) is adopted for adhesive bonding and is also used for passivation to decrease the parasitic capacitance. A lumped electrode structure is adopted, which means the RC time constant limits the high speed performance of the EAM. The passive silicon waveguide underneath is a rib waveguide with 1.5 μm width and is 160 nm shallowly etched into the 380 nm silicon layer. The optical coupling between the silicon device layer and the III-V epitaxial stack is realized using a bi-level taper consisting of two linearly tapered sections in the III-V structure. In the first taper section, the optical mode is converted from the silicon waveguide to the MQW (including SCH layers) waveguide without the thick p-cladding layer. Then, the second taper section adiabatically transforms the waveguide mode to that of the full III-V structure. The thickness of the Si at the hybrid modulator section is set to be 380 nm to achieve a better coupling between the Si and III-V waveguides. This is realized by depositing poly-silicon on the 220nm thick crystalline silicon SOI wafer. We analyze the performance of the tapers for different values of Lt1, L_{t2} and the BCB bonding layer thickness hBCB, using a commercial software FIMMWAVE [14]. L_{t1} and L_{t2} are the lengths of MQW taper and p-InP taper, respectively. W_{tip1} and W_{tip2} are the widths of the tips of the MQW taper and p-InP taper, respectively. The BCB thickness is labeled as h_{BCB}. Figures 3(a) and 3(b) show the coupling efficiency as a function of the lengths L_{t1}, L_{t2}, when h_{BCB} varies. Here we assume W_{tip1} = W_{tip2} = 0.2 μm, and while one taper is investigated, the other taper is set to be long enough for adiabatic conversion. From the figures we can find that the smaller h_{BCB}, the better

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the coupling efficiency and the shorter the taper length. However, thinner BCB bonding layers reduce the yield of the bonding process and hence a trade-off needs to be made is selecting the bonding layer thickness.

In our design, we assume L_{t1} = 30 μm, L_{t2} = 15 μm and h_{BCB} = 0.03 μm. The mode transformation under this condition is presented in Fig. 3(c). The coupling efficiency from the passive silicon waveguide to the III-V waveguide using this 45 μm long taper can be more than 95%.

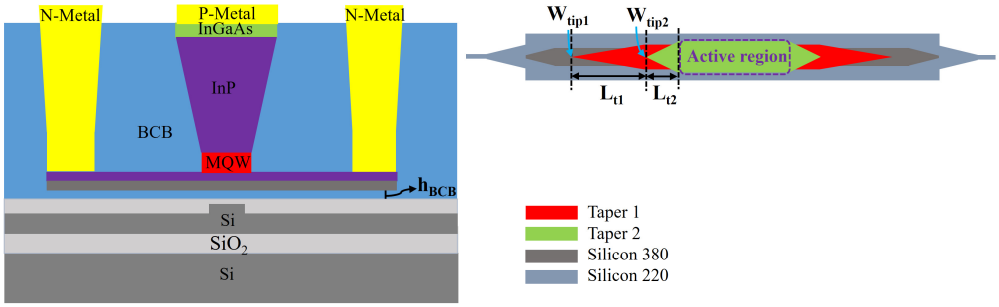

Fig. 2. (a) Schematic cross-sectional view; (b) Top-view of the structure.

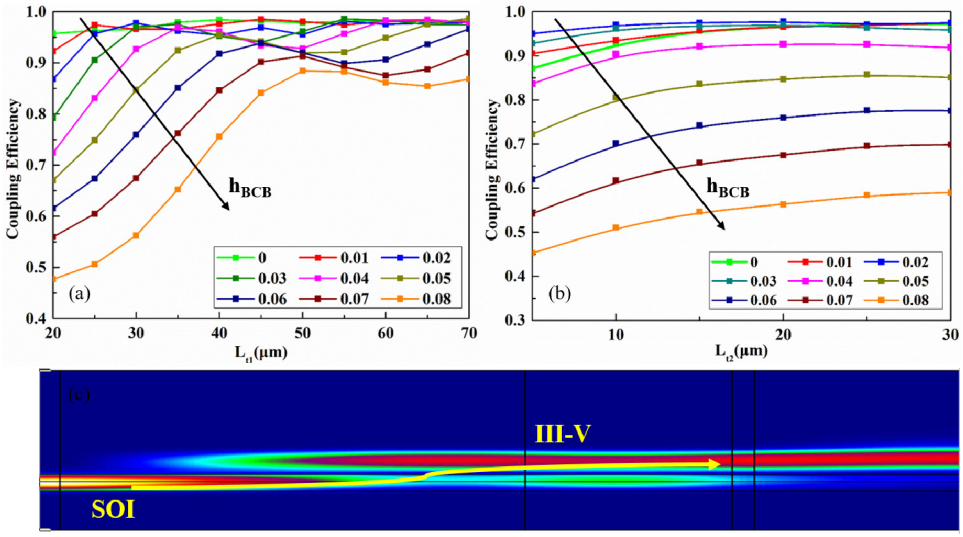

Fig. 3. (a) The coupling efficiency as Lt1 varies for different thicknesses of the BCB layer (from 0 to 0.08 μm) when L_{t2} = 20 μm; (b) The coupling efficiency as Lt2 varies for different thicknesses of the BCB layer (from 0 to 0.08 μm) when L_{t1} = 30 μm; (c) Mode transformation in the bi-sectional tapered coupler with L_{t1} = 30 μm, L_{t2} = 15 μm, h_{BCB} = 0.03 μm.

3. Fabrication

Figure 4 shows a schematic diagram of the fabrication process. The silicon photonic components are defined on 200 mm silicon-on-insulator (SOI) wafers with a 380 nm thick poly-silicon / crystalline silicon layer using 193 nm deep UV lithography. The rib silicon waveguides are etched 160 nm deep using inductively-coupled-plasma (ICP) dry etching. The silicon waveguide circuits are then planarized through SiO_2 PECVD deposition followed by chemical mechanical polishing down to the silicon device layer. The III-V layer stack is adhesively bonded to this silicon waveguide using a 30 nm thick DVS-BCB layer. The

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thickness of BCB at different bonding locations may vary by 10% (so 3nm). HCl is then used to remove the InP substrate.

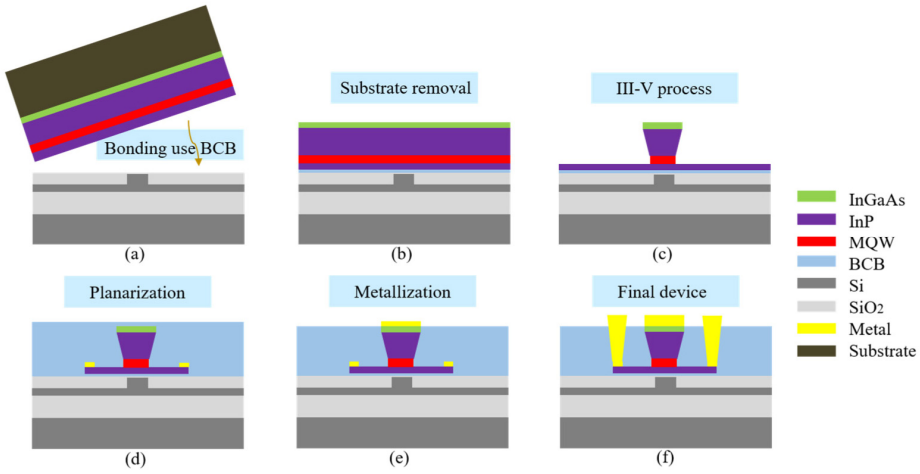

Fig. 4. Schematic diagram of the fabrication process (a) BCB bonding; (b) Substrate removal; (c) III-V process; (d) Planarization; (e) Metallization; (f) Final device.

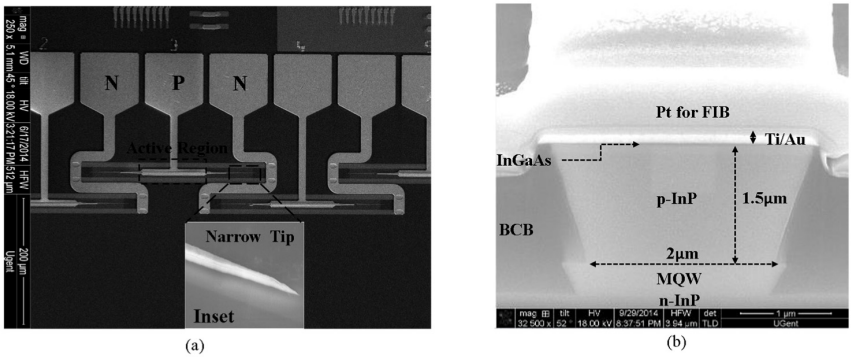

Fig. 5. (a) SEM picture of the top-view of a III-V on silicon EAM, the inset shows the narrow taper tips; (b) SEM picture of the cross section.

The p-InP mesa with a width of 3.5 µm is defined by using the top p-metal (Ti/Au) as a hard mask. The 100 nm InGaAs layer and 1.5 µm InP p-doped layer are etched using selective wet chemical etching with $1H_3PO_4$: $1H_2O_2$: $20H_2O$ and 1HCl:$1H_2O$, respectively. The waveguide is oriented along the [0 1-1] direction of the III-V. The width of the p-InP at the bottom is reduced to 2 µm as the orientation of the EAM mesa with respect to the InP crystal planes introduces an inverted trapezoidal mesa. Afterwards, a 5 µm wide SiN mask is defined using UV lithography. 20CitricAcid: $1H_2O_2$ is used for wet etching of the MQW layer and the MQW is underetched by 3 µm in order to reach 2 µm in width. The etching is selective to the n-InP beneath. The widths of the tips (W_{tip1} = W_{tip2} = 0.2 µm) are quite critical for a good coupling. In this work, such narrow taper tips are defined using UV lithography and carefully controlled by wet chemical etching, which demonstrates the manufacturability of these components in standard III-V processing lines. When the III-V mesa is defined, the n-type layer is etched using HCl. Then Ni/Ge/Au is deposited for the n-contacts. In the next step, the III-V structure is encapsulated with DVS-BCB for passivation to decrease parasitic capacitance. Reactive ion etching (RIE) is used to etch through the DVS-BCB layer to open the n-contacts and the p-contacts. Finally, ground-signal-ground (GSG) metal contact pads with 100 µm pitch are formed for the RF ports. The SEM pictures of the top view and cross

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section of the EAM are shown in Figs. 5(a) and 5(b), respectively. The inset of Fig. 5(a) shows the narrow taper tip.

4. Experimental results

The normalized transmission spectra of the 5-channel multiplexer before and after the heterogeneous integration of EAMs are shown in Fig. 6. The curves are normalized to a reference waveguide with grating couplers showing 12dB fiber-to-fiber insertion loss. By comparing the spectra shown in Fig. 6(a) and 6(b), one finds that the central wavelength of each AWG channel shifts a little after the hybrid integration, and the side lobes of the AWG are slightly broadened. This is attributed to the different top cladding of the AWG after the III-V processing. Therefore, the phase relation will be affected and finally the spectrum will change. The channel spacing of the AWG is 1.6 nm and the device has an insertion loss less than 3 dB. However, after EAM integration the insertion loss varies from between –9.3 dB to –3.4 dB (measured after passing through the EAMs). However, after EAM integration the insertion loss varies from between –9.3 dB to –3.4 dB (measured after passing through the EAMs and AWG), which is mainly attributed to non-uniform insertion losses of the fabricated EAMs, although each EAM is designed to be identical. The III-V processing is expected to have no influence on the passive silicon waveguide circuit, as the etching is selective and the silicon layer is well protected beneath the oxide layer. The minimum insertion loss of the EAM at 0V bias is measured to be 1.2 dB. Figure 7 illustrates the measured static extinction ratio of the 100μm-long EAMs under different reverse biases. More than 12 dB extinction ratio can be achieved when the bias is changed from 0 V to –2.5 V.

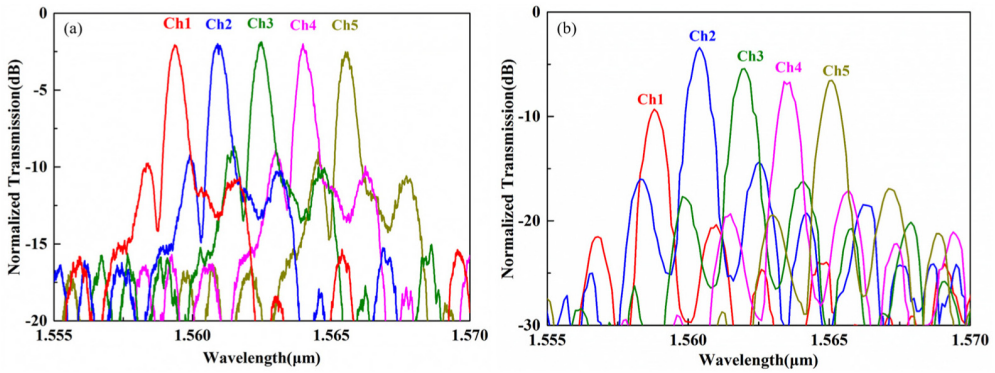

Fig. 6. Optical spectra of the AWG before (a) and after (b) the heterogeneous integration (including the EAMs).

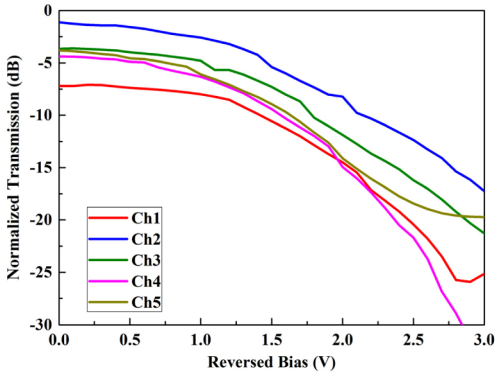

Fig. 7. Bias dependent normalized transmission of each channel.

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The small-signal modulation of the hybrid EAMs was measured using a vector network analyzer. Figure 8 shows the typical electro/optical (E/O) modulation response and the microwave reflection (S11) to the RF source for an EAM under a reverse bias of −2 V. The measurement indicates the E/O 3 dB bandwidth is 17 GHz. The red lines in the figures are the fitting results of the measured data according to an equivalent electrical circuit model [15] of the modulator [see the inset of Fig. 8(b)]. In the circuit diagram, Z_s is the 50 Ω source impedance, L_m is the inductance, R_a is the device resistance, C_a is the junction capacitance, R_j is the device junction leakage resistance and C_e is the parasitic capacitance between the electrodes. Besides, we also consider the resistance and capacitance between the electrodes and the Si substrate R_{sub} and C_{sub}. The junction capacitance C_a is fitted to be 0.145 pF. As the electrodes of the modulators are lumped electrodes, it suffers from strong microwave reflection.

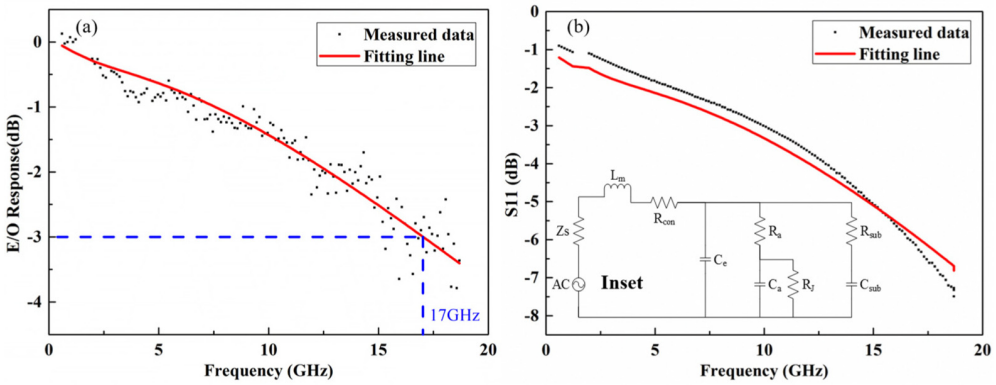
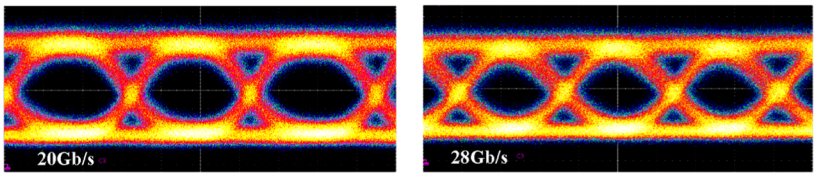


Fig. 8. (a) Small signal E/O response and (b) the microwave reflection to the RF source (S11) for the hybrid EAM of channel 2; the inset of (b) shows the equivalent circuit.



(a) (b)

Fig. 9. Eye diagram of channel 2 at (a) 20 Gb/s; (b) 28 Gb/s.

For the large signal modulation measurements, a tunable continuous wave (CW) laser was aligned to each channel of the AWG. A SHF pattern generator followed by a driving amplifier and a bias tee produced a PRBS signal with 2.3 to 2.6 Vpp with a DC offset of −1.5 V to −2 V to drive the EAMs. The modulated light was boosted by an erbium-doped fiber amplifier (EDFA). A narrow optical filter was inserted to remove the amplified spontaneous emission (ASE) noise generated by the EDFA. Finally, eye diagrams were obtained with a Tektronix 8300A digital series analyzer. The 20 Gb/s and 28 Gb/s eye diagram of the EAM on channel 2 are displayed in Figs. 9(a) and 9(b), respectively. Figures 10(a)-10(e) shows the eye diagrams after the AWG multiplexer at 20 Gbps for the five different channels. All EAMs exhibit clean and open eyes. The dynamic extinction ratios vary between 4.9 dB and 6.9 dB, limited by the large insertion loss of the chip in the experiment.

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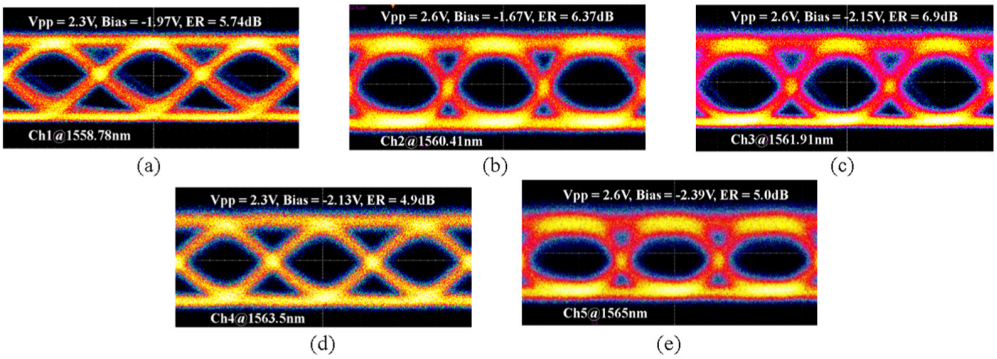

Fig. 10. Optical eye diagrams at 20 Gb/s for each channel.

5. Conclusion

We report a five-channel WDM modulator module that heterogeneously integrates a 200 GHz channel-spacing arrayed waveguide grating multiplexer and a 20 Gbps electro-absorption modulator array reaching 100 Gbps capacity. The total size of the device is 1.5x0.5 mm^2. The bandwidth of each modulator is around 17 GHz enabling 20 Gbps and 28Gbps modulation. The device modulation bandwidth can be further enhanced by reducing the device length (thereby decreasing the RC) or introducing a travelling wave design. The realization of the module on a hybrid silicon photonic platform allows in a next step to co-integrate the laser sources as well.

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