Ultra-Low Energy 1D Silicon Photonic Crystal Electro-Optic Modulator with Sub-100- mV Switching Voltage

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1. Abstract: We demonstrate a 1D silicon photonic crystal electro-optic modulator with the lowest reported switching and holding energies at GHz speeds. The device operates with only 50 mV_{pp}, and provides the first demonstration of sub-100-mV_{PP} operation.

2. Introduction: The interest in silicon photonics as a future technology for achieving higher data processing speeds and bandwidths is growing rapidly as evident by the significant improvements made in the performance of individual components such as electrically pumped silicon light sources [1], detectors [2] and modulators [3-7]. However, the use of silicon optical interconnects can only be justified if the power consumption is also lower than that of its electrical counterpart. For this purpose, it is necessary to reduce the power consumption of all the components of an optical interconnect including the modulator.

The total energy consumed by electro-optic (EO) modulators has two components; the switching energy and the holding energy. The switching energy relates to the applied voltage swing and depends on the capacitance of the device. On the other hand, the state holding energy or DC energy consumption is dependent on the resistance. For carrier injection modulators, the energy consumption of the device is usually dominated by the holding energy. However, after photonic-electronic integration, low voltage swing operation can substantially reduce the external energy consumption by using simpler drive electronics, eliminating the need for amplifiers and reducing the transient energy requirements. With this in mind, efforts have been made to reduce the switching voltage of a silicon modulator [6]. For practical applications, it is beneficial to reduce both the switching and holding energies, and this can be accomplished by reducing the capacitance and resistance of the device, respectively. The capacitance and resistance can be reduced by minimizing the device footprint. One way of reducing the device size is to use high Q-factor and low mode volume cavities to enhance the light-matter interaction, e.g., ring resonators [5, 6] and photonic crystal (PhC) cavities [4, 7]. Although the cavity approach has reduced the device energy consumption of carrier injection silicon EO modulators compared with those based on Mach-Zehnder interferometers, the total energy is still high (of the order of 100 fJ/bit). Thus, there is a need to develop modulators with a much smaller footprint to reduce the capacitance, resistance and hence the total energy consumption. Although 2D PhC cavities are well developed and their Q/V values can be controlled, unfortunately their 2D nature imposes a limit on the minimum device size and on the lowest achievable capacitance and resistance. This size limitation can be removed by using a 1D PhC cavity leading to low resistance and capacitance values and hence a low energy EO modulator.

In this report, we demonstrate a low energy carrier injection silicon EO modulator, realized by reducing both the switching and holding energies to record levels at GHz modulation speeds. To minimize the energy consumption, we lowered the capacitance, resistance and EO modal volume of the device by reducing its footprint using our previously reported novel 1D PhC cavity [8] and incorporating a small and optimized *p-i-n* junction across it. By virtue of its improved electrical properties, our device operates with a switching voltage of only 50 mV leading to an ultra-low 0.1 fJ/bit switching energy for a 3 dB extinction ratio (ER) and a 42 fJ/bit holding energy. The holding energy can be reduced by slightly increasing the voltage swing and hence the switching energy. For example, the device can operate with a total energy of as low as 13.9 fJ/bit (0.9 fJ/bit switching energy and 13 fJ/bit holding energy) with an ER exceeding 8 dB if we increase the voltage swing to just 0.4 V. This demonstration of a very small, low energy and high ER silicon EO modulator constitutes a very important advance in terms of the development of future low energy and densely integrated silicon optical interconnects.

3. Device design: We used a mode-gap 1D PhC cavity with a width (w) of only 600 nm. To create the cavity the hole radius *r(i)* was changed according to a parabolic function $r(i)=r_0\ (1-i^2/m^2)$, where $m=17$, $r_o=0.3a$, and a (hole periodicity)$=350\ nm$, until the radius remained larger than $0.22a$, as shown in Fig. 1b. Trenches were etched on both sides of the PhC, leaving side slabs with a thickness (h) of 50 nm and a width (sw) of 1.2 µm. Complete details of the cavity design can be found in [8]. With these parameters, the resonance wavelength of the cavity was 1598 nm with a loaded Q-factor of 20K and a mode volume of 0.078 μm^3. A moderate Q-factor was used to create a balance between the energy consumption and modulation speed. The mode profile of the PhC cavity calculated by 3D FDTD is shown in Fig.1b. For the current injection, a *p-i-n* junction was created across the cavity with doped fingers separated by a distance (d) of only 1.4 µm.

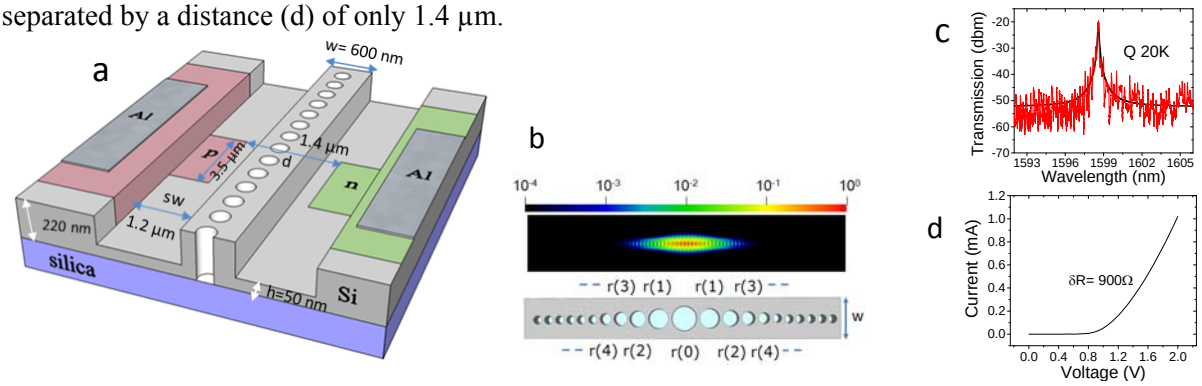

Figure 1 (a) Schematic of device. (b) Mode profile of 1D PhC cavity calculated by 3D FDTD. (c) T- spectrum showing Q- factor of 20K (d) IV curve of device showing differential resistance (inverse of slope of IV curve) of only 900 Ω.

The sample was fabricated with multiple photo- and e-beam lithography steps and dry etching. The *p* and *n* regions having $10^{18}/cm^3$ doping level were created by ion implantation. The fabrication process is detailed in [4, 8]. The schematic and physical dimensions of the device are shown in Fig. 1a.

The junction capacitance of the device including the fringe capacitance is only 0.08 fF as numerically calculated using Comsol Multiphysics. In fact, with such small physical dimensions, the capacitance is dominated by the fringe capacitance, with 0.06 fF contribution to the total value of 0.08 fF originating from the fringing fields. Similarly, because of the very small physical dimensions and the doped regions being only in the silicon area, the experimentally measured differential resistance (the inverse of the slope of the IV curve) of the device is only 900 Ω, which is considerably lower than that reported in [4, 7], where the device resistances are 1 MΩ and 100 KΩ, respectively.

4. Results: A CW tunable laser with TE polarization was used for the measurements. For EO modulation, a rectangular 2^7-1 bit long PRBS signal from a pulse pattern generator was applied to metal pads via a bias-T through electrical probes terminating with a 50 Ω resistance. The AC peak-to-peak voltage (V_{pp}) was tuned from 50 to 400 mV while keeping V_{top} fixed at 1.0 V by using an attenuator and adjusting the DC bias level. Please refer to Fig. 2a for the definitions of the different voltage terms.

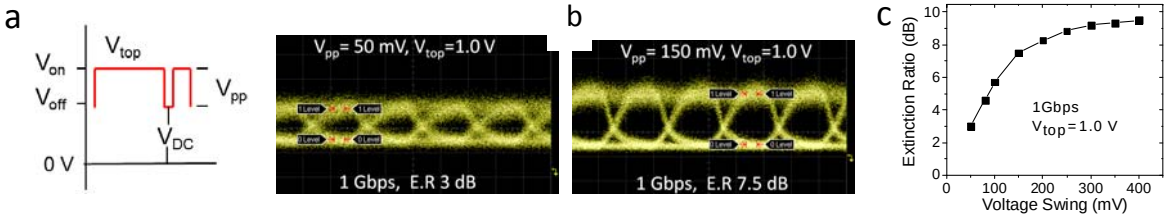

Figure 2 (a) Schematic of input electrical signal showing definitions of different voltage terms used. (b) Eye diagrams for 1 Gbps modulation speed using 50 mV voltage swing (left) and 150 mV (right). (c) Extinction ratio vs voltage swing for 1Gbps.

As shown in Fig. 2b (left), we observed an open eye diagram with a 3 dB ER by using only a 50 mV V_{pp} at around a 0.975V DC bias (V_{top}=1.0 V) at 1 Gbps. The ER is improved by increasing V_{pp} and approaches 10 dB at only 0.4 V_{pp} while keeping V_{top} fixed at 1.0 V, as shown in Fig. 2c. This is the first

ever demonstration of GHz silicon EO modulators with a sub-100- mV voltage swing. Operation with an ultra-low voltage swing became possible thanks to the significant improvement in the electrical properties achieved by minimizing the device footprint.

Our device can operate at up to 2 Gbps with $V_{pp} \leq 400$ mV and V_{top}=1.0 V but with a slightly lower ER than with the 1 Gbps case as shown in Fig. 3a. Furthermore, by slightly increasing V_{top} to 1.1 V, and V_{pp} to 0.5 V, the device speed and ER ratio improve further with an 11 dB ER achieved for 1 Gbps and 8 dB for 3 Gbps as shown in Fig. 3b, c.

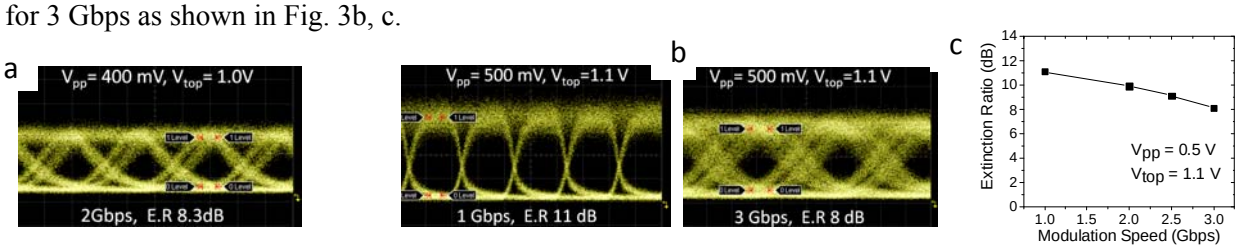

Figure 3 (a) Eye diagram for 2 Gbps using V_{top}=1.0 V and V_{pp}=0.4 V leading to 13.9 fJ/bit total energy consumption. (b) Eye-diagrams for 1 Gbps (left) and 3 Gbps (right) for V_{pp}=0.5 V and V_{top}= 1.1 V showing ERs of 11 and 8 dB, respectively (c) Extinction ratios for different modulation speeds for V_{pp}=0.5 V and V_{top}=1.1 V

To calculate the switching energy requirement for on-off state transition, we used the method reported in [5]. Although we experimentally observed a 30 pm blue shift of the resonance wavelength for 1.0 V, which led to an extremely small switching energy (< 0.1 fJ/bit), but in fact 30 pm is the net shift including the thermal response. Hence, we estimated the switching energy corresponding to the wavelength shift by complete FWHM. A FWHM (80 pm in our device) wavelength shift corresponds to a refractive index change of $8.76e^{-4}$ for a 20% confinement factor, which in turn corresponds to an injected charge density of $2.35e^{17}/cm^3$ and a 9.4 fC total injected charge for 0.25 μm^3 physical intrinsic region volume. For a 50 mV V_{pp}, our device thus operates at only 0.1 fJ/bit, the lowest switching energy yet reported, with a state holding energy of 42 fJ/bit for 1 Gbps. The holding energy is calculated by taking the average of DC power consumption (the product of voltage and current) in the on (1.0 V) and off (0.950 V) states. The holding energy can be reduced substantially by slightly increasing the voltage swing. For example, by using a V_{pp} of 0.4 V while keeping V_{top} fixed at 1.0 V (Fig. 3a), the holding energy is only 13 fJ/bit at 2 Gbps and the switching energy still remains very low at 0.9 fJ/bit for 8.3 dB ER. Thus, the device operates with a total energy of only 13.9 fJ/bit, which is considerably lower than reported in the literature [5-7] with the additional advantage of a much higher ER. Thus, our device not only exhibits the lowest ever switching energy but also reduces the DC energy requirement considerably due to low resistance.

5. Conclusions: By using a 1D PhC cavity with a small footprint, we have demonstrated a carrier injection silicon EO modulator with the lowest reported switching and holding energies by reducing the capacitance and resistance, respectively. The device exhibits a 3 dB ER for an ultra-low voltage swing of 50 mV leading to a switching energy of only 0.1 fJ/bit. Increasing V_{pp} to 0.4 V still keeps the switching energy low at only 0.9 fJ/bit, with a 13 fJ/bit holding energy, resulting in a total energy consumption of only 13.9 fJ/bit at a 2 Gbps modulation speed and 8.3 dB ER. Overall, the device demonstrated a maximum speed of 3 Gbps with an 8 dB ER, while an ER as high as 11 dB was measured at 1 Gbps. This demonstration of low energy with a high ER and a small footprint silicon EO modulator operating at GHz speeds marks a step towards low energy and miniaturized silicon based optical interconnects.

References

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