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Homework 4

Due 14:20, Tuesday @ Week 8

"Digital Fundamentals", **11th Edition**

Chapter 6, Problems

8，14，18(a,b)，20，26(a,b), 28, 30, 32, 46

T8

8. The input waveforms in Figure 6–72 are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.
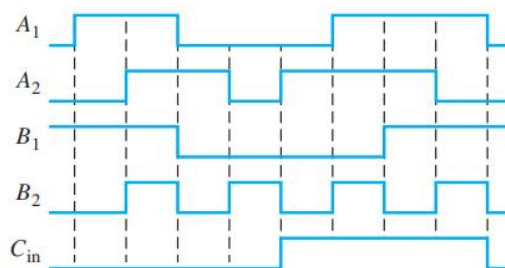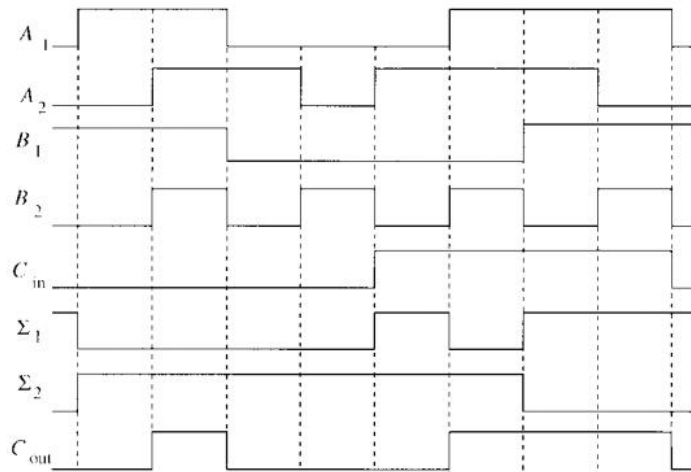

FIGURE 6–72

T14

14. For the 4-bit comparator in Figure 6–74, plot each output waveform for the inputs shown. The outputs are active-HIGH.
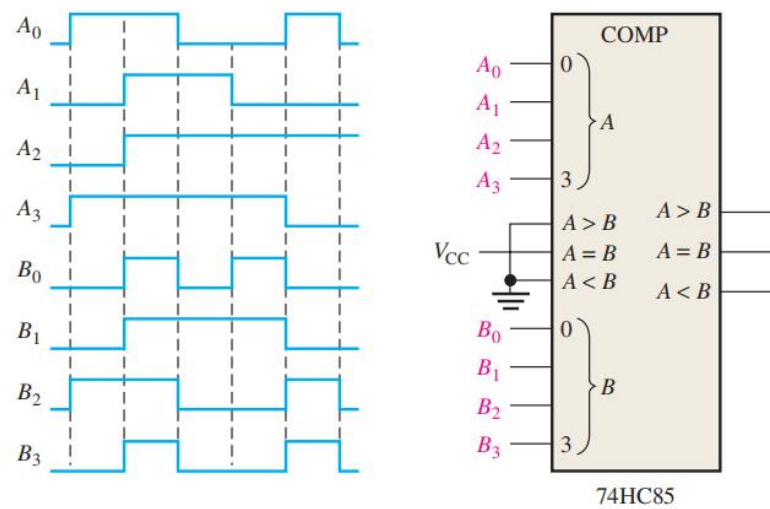

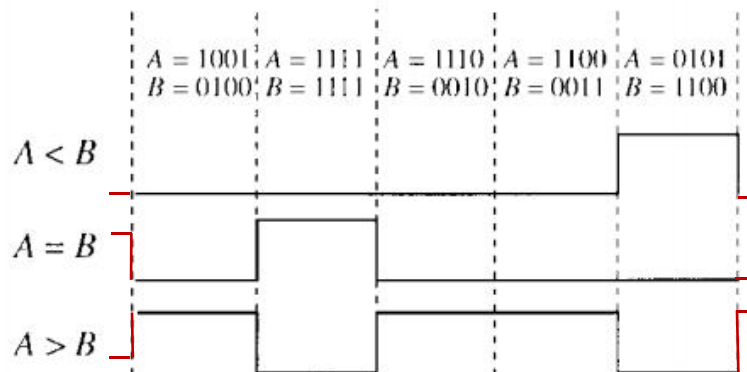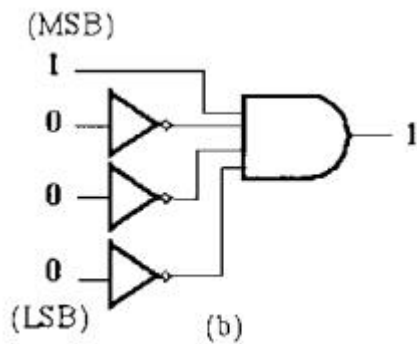74HC85

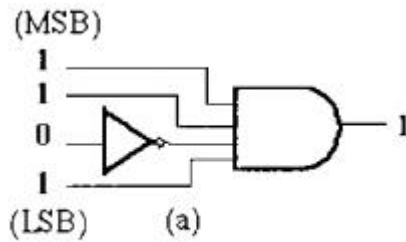**FIGURE 6–74**

$A = 1001$	$A = 1111$	$A = 1110$	$A = 1100$	$A = 0101$
$B = 0100$	$B = 1111$	$B = 0010$	$B = 0011$	$B = 1100$

$A < B$

$A = B$

$A > B$

FIGURE 6-7

T18(a,b)

17. Show the decoding logic for each of the following codes if an active-HIGH (1) output is required:

    (a) 1101   (b) 1000   (c) 11011   (d) 11100
    (e) 101010   (f) 111110   (g) 000101   (h) 1110110

18. Solve Problem 17, given that an active-LOW (0) output is required.

(MSB) ... (LSB) (a)

(MSB) ... (LSB) (b)

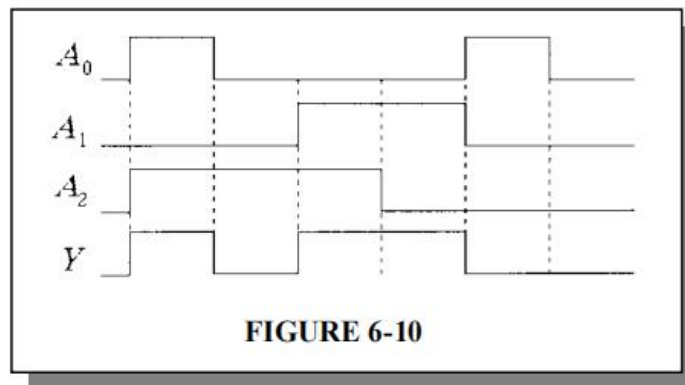Change the AND gates to NAND gates in Figure

T20

20. If the input waveforms are applied to the decoding logic as indicated in Figure 6–76, sketch the output waveform in proper relation to the inputs.
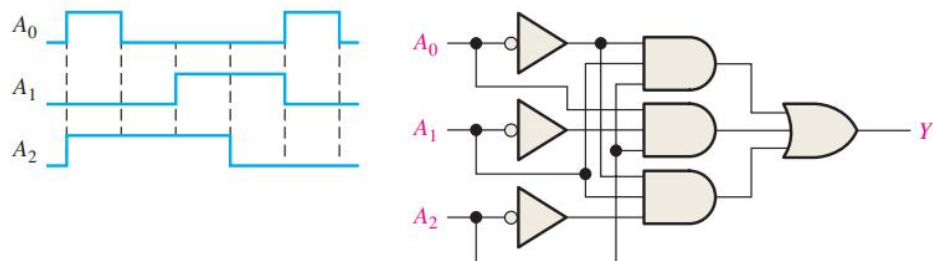
20. $Y = A_2 A_1 \overline{A_0} + A_2 \overline{A_1} A_0 + \overline{A_2} A_1 \overline{A_0}$
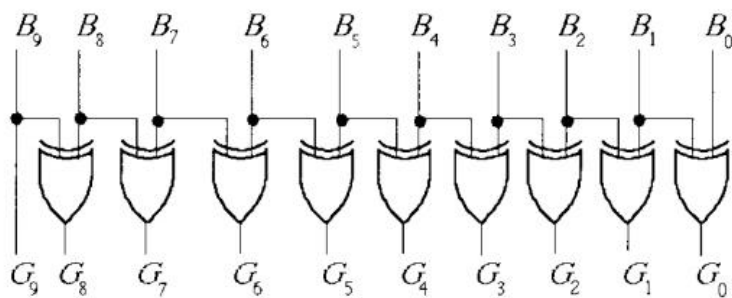
See Figure 6-10.

FIGURE 6-10

T26(a,b)

26. Show the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:

(a) 1010111100   **(b)** 1111000011   **(c)** 1011110011   **(d)** 1000000001
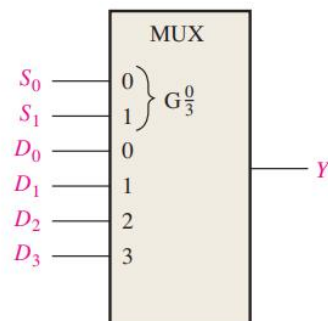

(a) 1010111100——>1111100010
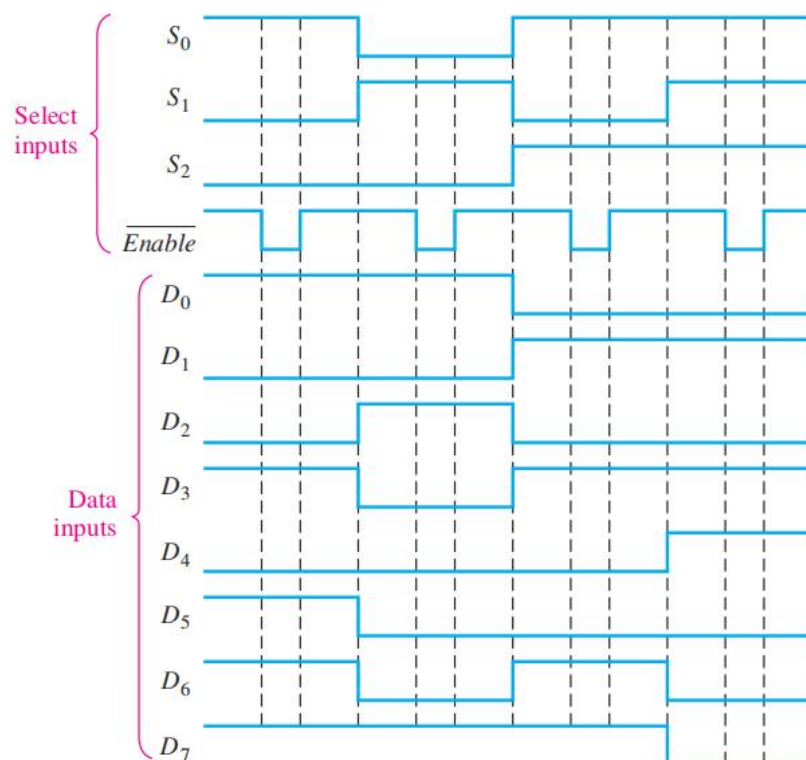(b) 1111000011——>1000100010

T28

28. For the multiplexer in Figure 6–79, determine the output for the following input states: $D_0 = 1$, $D_1 = 0$, $D_2 = 0$, $D_3 = 1$, $S_0 = 0$, $S_1 = 1$.
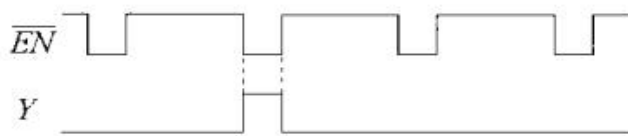

S1S0 = 10, select D2, Y=0

T30

30. The waveforms in Figure 6–81 are observed on the inputs of a 74HC151 8-input multiple: Sketch the Y output waveform.

T32

32. The waveforms in Figure 6–82 are applied to the 4-bit parity logic. Determine the output waveform in proper relation to the inputs. For how many bit times does even parity occur, and how is it indicated? The timing diagram includes eight bit times.
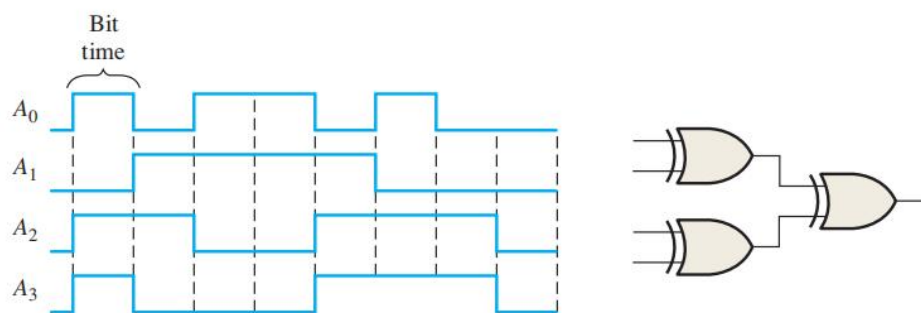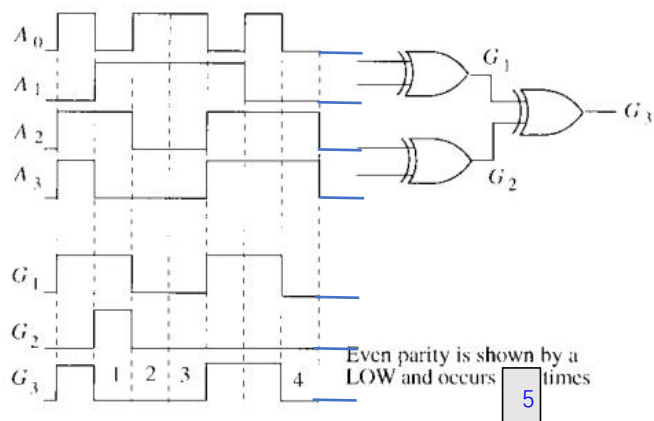

FIGURE 6–82

Even parity is shown by a LOW and occurs ⬚5 times

46. Implement the logic function specified in Table 6–14 by using a 74HC151 data selector.

TABLE 6–14

Inputs				Output
A_3	A_2	A_1	A_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

46. $Y = \overline{A_3}\,\overline{A_2}A_1\overline{A_0} + \overline{A_3}\,\overline{A_2}A_1A_0 + \overline{A_3}A_2A_1\overline{A_0} + \overline{A_3}A_2A_1A_0 + A_3\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$
$+ A_3\,\overline{A_2}A_1\overline{A_0} + A_3\,\overline{A_2}A_1A_0 + A_3A_2\,\overline{A_1}A_0 + A_3A_2A_1A_0$

See Figure 6-25.

FIGURE 6-25