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Shiyou(Alan) Huang

Research

My areas of interest are model checking, system security, and bug reproduction. The goal of my research is to help develop automated systems combining program analysis, hardware advances, and systematic testing to improve the reliability and security of the software.

Education

9/2015– **Ph.D., Computer Science, Texas A&M University, USA.**

12/2019 *Thesis: Fast and Effective Approaches for Verifying and Debugging Concurrent Programs*
Advisor: Jeff Huang

9/2011– **B.E. in Computer Science, Huazhong University of Science and Technology**
6/2015 *(HUST), Wuhan, China.*

Work Experience

5/2018 - **Research Intern, Alibaba Group US.**, 525 Almanor Ave., Sunnyvale, California.

8/2018 Study the crashes caused by the improper use of Java Unsafe API, and present a bytecode-level transformation to enhance the safety of Java Unsafe API.

Publication

TOPLAS 2020 *Maximal Causality Reduction with Switch Equivalence (in submission)*

Shiyou Huang and Jeff Huang

ACM Transactions on Programming Languages and Systems (TOPLAS)

ICSE 2019 *SafeCheck: Safety Enhancement of Java Unsafe API*

Shiyou Huang, Jianmei Guo, Sanhong Li, Xiang Li, Yumin Qi, Kingsum Chow and Jeff Huang

Proceedings of International Conference on Software Engineering Companion, 2019

USENIX ATC 2017 *Towards Production-Run Heisenbugs Reproduction on Commercial Hardware*

Shiyou Huang, Bowen Cai and Jeff Huang

Proceedings of USENIX Annual Technical Conference, 2017

ECOOP 2017 *Speeding Up Maximal Causality Reduction with Static Dependency Analysis*

Shiyou Huang and Jeff Huang

31st European Conference on Object-Oriented Programming, 2017

OOPSLA 2016 *Maximal Causality Reduction for TSO and PSO*

Shiyou Huang and Jeff Huang

Proceedings of ACM SIGPLAN conference on Object-Oriented Programming, Systems, Languages, and Applications, 2016

Skills

Research Model Checking, Bug Reproduction, Testing, Static Analysis
Languages JAVA, C/C++, PYTHON, RUBY
Misc. ASM, Z3, LLVM, INTEL PT, JAVA UNSAFE, JVM

Research Projects

2015-2019 **Stateless Model Checking with Maximal Causality Reduction (MCR)**

- **Extend MCR to TSO/PSO** In this project, I develop novel extensions to MCR by solving two key problems under TSO and PSO: 1) encoding TSO and PSO semantics using SMT constraints and 2) implementing a scheduler to support the out-of-order execution.
- **Use static dependency analysis to improve performance** In this work, I use static dependency analysis to reduce the size of the constraints, thus speeding up the efficiency of the state space exploration.

2016-2017 **Concurrency Bug Reproduction Using Intel PT**

In this work, I develop H3, a new *record* and *replay* system to reproduce Heisenbugs with Intel Processor Tracing to reduce the runtime overhead of the state-of-the-art.

5/2018-9/2018 **Memory Bound Check for Java Unsafe APIs**

The Unsafe API is powerful but can lead to data corruption, resource leaks and JVM crashed if used improperly. In this work, I study the Unsafe crash patterns and propose a memory checker to enforce memory safety at the bytecode level to avoid the JVM crash caused by the misuse of the Unsafe API.

Honor & Awards

Fall 2018 **Graduate Teaching Fellow**, Department of Engineering, Texas A&M.
June 2017 **Student Scholar for 50th Turing Award Celebration**.
March 2017 **Graduate Research Excellence Award**, Department of CSE, Texas A&M.
OOPSLA **SIGPLAN PAC Award**, OOPSLA, 2016.
ICSE **SIGSOFT CAPS Award**, ICSE, 2016.
ICSE **Third Place, Student Research Competition**, ICSE, 2016.

Teaching Experience

Fall 2018 **CSCE111: Introduction to Computer Science Concepts and Programming**, Texas A&M University.
Instructor
Spring 2018 **CSCE314: Programming Languages, Haskell & Java**, Texas A&M University.
Teaching Assistant
Spring 2017 **CSCE431: Software Engineering**, Texas A&M University.
Teaching Assistant
Fall 2016 **CSCE606: Software Engineering**, Texas A&M University.
Teaching Assistant