成都海光集成电路设计有限公司

系统软件部

PCIe 错误注入工具操作手册

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系统软件部 SV *项目组*

修订历史

修订前版本	修订内容	完成日期	修订人	修订后版本
	创建文档	2020/01/21	林佳森	V1.0
	删除使用限制中 ASPM 部分	2020/04/23	林佳森	V1.1
	增加 PCIe RAS 部分	2020/04/27	林佳森	V1.2

注：“草稿”状态的文档版本为 0.Y.Z，Y≥0，Z>0，Y、Z 的数值不断累加；
“正式发布”状态的文档版本为 X.Y，X≥1，Y≥0，且 X、Y 值不断累加；

“正在修改”状态的文档指对“正式发布”后的文档进行修改，文档版本为X.Y.Z，其中X.Y同修改之前的文档版本号，Z>0，Z的数值不断累加。

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1. 术语

缩略词	定义
ACS	Access Control Services.
AER	Advanced Error Reporting. A component of the PCIe specification.
DF	Data Fabric. On-chip coherent interconnect.
DPC	Downstream Port Containment. A component of the PCIe specification.
ECRC	Transaction Layer end-to-end 32-bit CRC.
eDPC	Enhanced Downstream Port Containment. A component of the PCIe specification.
EP	EndPoint
HP	HotPlug
IOHUB	Input Output Hub.
LCRC	Data Link Layer 32-bit CRC
NBIF	New PCIe Bus Interface.
NBIO	Northbridge Input Output
PCIe	PCI Express.
RAS	Reliability, availability and serviceability
RP	Root Port

2. OS 支持

Linux : Debian and RHEL

3. 支持特性

PCIe LCRC	LCRC_RX	需要 BIOS 和 OS 支持 AER 功能
	LCRC_TX	需要 BIOS 和 OS 支持 AER 功能
PCIe ECRC	ECRC_RX	需要 RP 到 EP 的整个 PCIe 链路支持 ecrc 功能，并且 BIOS/OS 使能 ECRC
	ECRC_TX	需要 RP 到 EP 的整个 PCIe 链路支持 ecrc 功能，并且 BIOS/OS 使能 ECRC
ACS	ACS Fatal	需要 BIOS 和 OS 支持 ACS 功能
	ACS Non_Fatal	需要 BIOS 和 OS 支持 ACS 功能

注意：注入错误时需要 RP 和 EP 之间的 PCIe 链路是 linkup 的，且 EP 没有从 PCIe 系统中 remove 掉（DPC、AER 进行修复、HP 进行热插拔或者手动 remove，都会把 EP 从 PCIe 系

统中 remove 掉）。
EP 推荐使用下面两种：
Intel Corporation I210 Gigabit Network Connection
Intel Corporation I350 Gigabit Network Connection

4. 命令帮助

4.1. 版本号查询

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject
set default log level to 3.

HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.
Version:v00.26 Build Apr 27 2020 - 14:04:40
```

命令：./pcieinject

4.2. Usage 帮助

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject -help
set default log level to 3.

HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.
Version:v00.26 Build Apr 27 2020 - 14:04:40

Usage: ./pcieinject options
./pcieinject support 6 functions, need to select [One] function by first parameter.

function 0 argument: alldev, funname: show all dev, usage: ./pcieinject alldev.
function 1 argument: hygondev, funname: show hygon all dev, usage: ./pcieinject hygondev.
function 2 argument: gpp, funname: show hygon gpp bridge, usage: ./pcieinject gpp.
function 3 argument: pcie_err, funname: inject pcie err on gpp bridge, usage: ./pcieinject pcie_err -t [pcie errty
function 4 argument: nbio_sram_info, funname: show nbio internal sram info, usage: ./pcieinject nbio_sram_info.
function 5 argument: nbio_sram_inject, funname: inject err to nbio internal sram, usage: ./pcieinject nbio_sram_ir
pcie_err type0: lcrc_tx, smn bitmask 0x10.
pcie_err type1: lcrc_rx, smn bitmask 0x20.
pcie_err type2: ecrc_tx, smn bitmask 0x40.
pcie_err type3: ecrc_rx, smn bitmask 0x80.
pcie_err type4: acs_fatal, smn bitmask 0x0.
pcie_err type5: acs_nonfatal, smn bitmask 0x0.
pcie_err type6: completion_timeout, smn bitmask 0xc0000.
pcie_err type7: unexpected_cmplt, smn bitmask 0xc000.
pcie_err type8: malformed_tlp, smn bitmask 0x3000.
pcie_err type9: ecrc, smn bitmask 0xc00.
pcie_err type10: unsupported_req, smn bitmask 0x300.
pcie_err type11: bad_tlp, smn bitmask 0xc0.
pcie_err type12: bad_dllp, smn bitmask 0x30.
pcie_err type13: advisory_nonfatal, smn bitmask 0xc0000.
pcie_err report ctrl0: unmask_err_report.
pcie_err report ctrl1: mask_err_report.
```

命令：./pcieinject -help

4.3. 显示系统中所有的设备

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject alldev
set default log level to 3.

HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.
Version:v00.26 Build Apr 27 2020 - 14:04:40

=====================================================================================================
=========================System have 2 socket, per sokect support 2 die==========================
Idx     bus     dev     func    Vid     Did     irq   name
  0     00      00      0       1d94    1450      0   Device 1d94:1450
  1     00      00      2       1d94    1451     28   Device 1d94:1451
  2     00      01      0       1d94    1452      0   Device 1d94:1452
  3     00      01      2       1d94    1453     32   Device 1d94:1453
  4     00      01      4       1d94    1453     33   Device 1d94:1453
  5     00      02      0       1d94    1452      0   Device 1d94:1452
  6     00      03      0       1d94    1452      0   Device 1d94:1452
  7     00      04      0       1d94    1452      0   Device 1d94:1452
  8     00      07      0       1d94    1452      0   Device 1d94:1452
  9     00      07      1       1d94    1454     34   Device 1d94:1454
 10     00      08      0       1d94    1452      0   Device 1d94:1452
 11     00      08      1       1d94    1454     36   Device 1d94:1454
 12     00      14      0       1d94    790b      0   Device 1d94:790b
```

```
   94     60     04     0     1d94    1452      0    Device 1d94:1452
   95     60     07     0     1d94    1452      0    Device 1d94:1452
   96     60     07     1     1d94    1454     45    Device 1d94:1454
   97     60     08     0     1d94    1452      0    Device 1d94:1452
   98     60     08     1     1d94    1454     47    Device 1d94:1454
   99     61     00     0     8086    1521    192    Device 8086:1521
  100     61     00     1     8086    1521    202    Device 8086:1521
  101     62     00     0     1d94    145a      0    Device 1d94:145a
  102     62     00     2     1d94    1456     11    Device 1d94:1456
  103     62     00     3     1d94    145f     75    Device 1d94:145f
  104     63     00     0     1d94    1455      0    Device 1d94:1455
  105     63     00     2     1d94    7901    136    Device 1d94:7901
==========================================================================================
```

命令：./pcieinject alldev

4.4. 显示系统中所有的 HYGON 设备

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject hygondev
set default log level to 3.

              HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

                   Version:v00.26 Build Apr 27 2020 - 14:04:40

==========================================================================================
========================System have 2 socket, per sokect support 2 die=========================
Idx       bus     dev     func    Vid      Did      irq    name
   0      00      00      0      1d94     1450      0    Device 1d94:1450
   1      00      00      2      1d94     1451     28    Device 1d94:1451
   2      00      01      0      1d94     1452      0    Device 1d94:1452
   3      00      01      2      1d94     1453     32    Device 1d94:1453
   4      00      01      4      1d94     1453     33    Device 1d94:1453
   5      00      02      0      1d94     1452      0    Device 1d94:1452
   6      00      03      0      1d94     1452      0    Device 1d94:1452
   7      00      04      0      1d94     1452      0    Device 1d94:1452
   8      00      07      0      1d94     1452      0    Device 1d94:1452

  87      60      03      1      1d94     1453     44    Device 1d94:1453
  88      60      04      0      1d94     1452      0    Device 1d94:1452
  89      60      07      0      1d94     1452      0    Device 1d94:1452
  90      60      07      1      1d94     1454     45    Device 1d94:1454
  91      60      08      0      1d94     1452      0    Device 1d94:1452
  92      60      08      1      1d94     1454     47    Device 1d94:1454
  93      62      00      0      1d94     145a      0    Device 1d94:145a
  94      62      00      2      1d94     1456     11    Device 1d94:1456
  95      62      00      3      1d94     145f     75    Device 1d94:145f
  96      63      00      0      1d94     1455      0    Device 1d94:1455
  97      63      00      2      1d94     7901    136    Device 1d94:7901
==========================================================================================
```

命令：./pcieinject hygondev

4.5. 显示系统中所有的 GPP 桥及 GPP 桥下接设备

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject gpp
set default log level to 3.

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==========================================================================================
========================System have 2 socket, per sokect support 2 die=======================
----------------System info start addr 0x240b5d0, increment by 0x20 bytes 1 time----------------
Idx    addr         socketid    dieid   logical_dieid   iohc_bus    RC            DF0           DF1
0      0x240b5d0     0           0       0               0x00        (00:00.0)     (00:18.0)     (00:18.1).
1      0x240b5f0     0           1       1               0x20        (20:00.0)     (00:19.0)     (00:19.1).
2      0x240b610     1           0       2               0x40        (40:00.0)     (00:1c.0)     (00:1c.1).
3      0x240b630     1           1       3               0x60        (60:00.0)     (00:1d.0)     (00:1d.1).
==========================================================================================
==========================================================================================
Idx    GPP bridge   [Vid:Did]    DLActive irq   socket  die   core   phyport logicport    RC           DF0          DF1
 0     (00:01.2)    [1d94:1453]     +      32     0      0     0       6       1         (00:00.0)    (00:18.0)    (00:18.1)
 1     (00:01.4)    [1d94:1453]     +      33     0      0     0       4       3         (00:00.0)    (00:18.0)    (00:18.1)
 2     (40:01.2)    [1d94:1453]     +      40     1      0     0       1       1         (40:00.0)    (00:1c.0)    (00:1c.1)
 3     (60:03.1)    [1d94:1453]     +      44     1      1     1       8       8         (60:00.0)    (00:1d.0)    (00:1d.1)
==========================================================================================
Idx    GPP subdev   [Vid:Did]      irq     name
+++++++++++++++++++++++++GPP (00:01.2) subdev+++++++++++++++++++++++++
 0     (01:00.0)    [1a03:1150]    162     Device 1a03:1150
 1     (02:00.0)    [1a03:2000]    162     Device 1a03:2000
+++++++++++++++++++++++++GPP (00:01.4) subdev+++++++++++++++++++++++++
 0     (03:00.0)    [8086:1521]    152     Device 8086:1521
 1     (03:00.1)    [8086:1521]     48     Device 8086:1521
+++++++++++++++++++++++++GPP (40:01.2) subdev+++++++++++++++++++++++++
 0     (41:00.0)    [8086:1521]    172     Device 8086:1521
 1     (41:00.1)    [8086:1521]    182     Device 8086:1521
+++++++++++++++++++++++++GPP (60:03.1) subdev+++++++++++++++++++++++++
 0     (61:00.0)    [8086:1521]    192     Device 8086:1521
 1     (61:00.1)    [8086:1521]    202     Device 8086:1521
```

命令：./pcieinject gpp

4.6. 注入 lcrc_tx

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t lcrc_tx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

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=================================================================================================
========================System have 2 socket, per sokect support 2 die========================
================System info start addr 0x19d75d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x19d75d0       0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x19d75f0       0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x19d7610       1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x19d7630       1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
=================================================================================================
=================================================================================================
Idx     GPP bridge      [vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]        +     32     0       0       0       6       1               (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]        +     33     0       0       0       4       3               (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]        +     40     1       0       0       1       1               (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]        +     44     1       1       1       8       8               (60:00.0)       (00:1d.0)       (00:1d.1)
=================================================================================================
Idx     GPP subdev      [vid:Did]       irq     name
+++++++++++++++++++++++++GPP (00:01.2) subdev+++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
+++++++++++++++++++++++++GPP (00:01.4) subdev+++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
+++++++++++++++++++++++++GPP (40:01.2) subdev+++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
+++++++++++++++++++++++++GPP (60:03.1) subdev+++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:203]: Success to disable dpc, write 0x0 to dpc ctrl reg for dev 0:1.4.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 0, expect err 0x40, write 0x2040 to AER CAP reg offset 0x14 for dev 03:00.0 to mask lcrc_tx error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x2040 reach expect, success to mask lcrc_tx error report for dev dev 03:00.0.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 03:00.0.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 03:00.0.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 03:00.0.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 03:00.0 success.
[pcieinject [INFO] pcietest_set_severity_reg, line:3259]: Idx 0 severity 2 is correct, do not need modify aer severity reg.
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2616]: The val 0x500 of smn addr 0x111441a8 for dev 0:1.4, inject lcrc_tx, corresponding bitmask is 0x10.
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2626]: Write 0x10 to smn addr 0x111441a8 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject lcrc_tx.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0x8086 deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0x8086 deviceid 0x1521.
=============================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Corrected, type=Data Link Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [8086:1521] 03:00.0 error status/mask=00000040/00002040
[pcieinject [INFO] __aer_print_error, line:180]:     [ 6] BadTLP
=============================================================================
[pcieinject [INFO] pcietest_inject_tl_err_gpp, line:2720]: After 1 retry, success to inject lcrc_tx to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔

命令：./pcieinject pcie_err -t lcrc_tx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

4.7. 注入 lcrc_rx

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t lcrc_rx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

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=================================================================================================
========================System have 2 socket, per sokect support 2 die========================
================System info start addr 0x212b5d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x212b5d0       0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x212b5f0       0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x212b610       1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x212b630       1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
=================================================================================================
=================================================================================================
Idx     GPP bridge      [vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]        +     32     0       0       0       6       1               (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]        +     33     0       0       0       4       3               (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]        +     40     1       0       0       1       1               (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]        +     44     1       1       1       8       8               (60:00.0)       (00:1d.0)       (00:1d.1)
=================================================================================================
Idx     GPP subdev      [vid:Did]       irq     name
+++++++++++++++++++++++++GPP (00:01.2) subdev+++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
+++++++++++++++++++++++++GPP (00:01.4) subdev+++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
+++++++++++++++++++++++++GPP (40:01.2) subdev+++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
+++++++++++++++++++++++++GPP (60:03.1) subdev+++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 1, expect err 0x40, write 0x6040 to AER CAP reg offset 0x14 for dev 00:01.4 to mask lcrc_rx error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x6040 reach expect, success to mask lcrc_rx error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 success.
[pcieinject [INFO] pcietest_set_severity_reg, line:3259]: Idx 1 severity 2 is correct, do not need modify aer severity reg.
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2616]: The val 0x0 of smn addr 0x111441a8 for dev 0:1.4, inject lcrc_rx, corresponding bitmask is 0x20.
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2626]: Write 0x120 to smn addr 0x111441a8 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject lcrc_rx.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0x8086 deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0x8086 deviceid 0x1521.
=============================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Corrected, type=Data Link Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00000040/00006040
[pcieinject [INFO] __aer_print_error, line:180]:     [ 6] BadTLP
=============================================================================
[pcieinject [INFO] pcietest_inject_tl_err_gpp, line:2720]: After 1 retry, success to inject lcrc_rx to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔

命令：./pcieinject pcie_err -t lcrc_rx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

4.8. 注入 ecrc_rx

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t ecrc_rx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.
 _____ _____ _____ _____ _____ _____ _____
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|_____|_____|_____|_____|_____|_____|_____|


HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.
Version:v00.26 Build Apr 27 2020 - 14:04:40

================================================================================
=========================System have 2 socket, per sokect support 2 die=========================
=================System info start addr 0x73d5d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x73d5d0        0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x73d5f0        0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x73d610        1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x73d630        1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
================================================================================
================================================================================================================
Idx     GPP bridge      [vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]     +       32      0       0       0       6       1               (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]     +       33      0       0       0       4       3               (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]     +       40      1       0       0       1       1               (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]     +       44      1       1       1       8       8               (60:00.0)       (00:1d.0)       (00:1d.1)
================================================================================================================
Idx     GPP subdev      [vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521
[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 3, expect err 0x80000, Write 0x4580000 to AER CAP reg offset 0x8 for dev 00:01.4 to mask ecrc_rx error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x4580000 reach expect, success to mask ecrc_rx error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 success.
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 3 (ecrc_rx) severity is 1, success to change severity reg from 0x4e2030 to 0x4e2030(set bitmask 0x80000).
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2616]: The val 0x0 of smn addr 0x111441a8 for dev 0:1.4, inject ecrc_rx, corresponding bitmask is 0x80.
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2626]: Write 0x180 to smn addr 0x111441a8 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject ecrc_rx.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0x8086 deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0x8086 deviceid 0x1521.
================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00080000/04580000
[pcieinject [INFO] __aer_print_error, line:180]:    [19] ECRC
================================================================================
[pcieinject [INFO] pcietest_inject_tl_err_gpp, line:2720]: After 1 retry, success to inject ecrc_rx to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔

命令：./pcieinject pcie_err -t ecrc_rx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：ecrc 错误是整个 pcie 链路上端到端的 crc 校验，注入错误前请检查 RP-Switch-EP 是否支持 ecrc。

4.9. 注入 ecrc_tx

```
root@ubuntu:/home/hygon/pcieinjectnew# ./pcieinject pcie_err -t ecrc_tx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.
 _   _  __   __  ____   ___   _   _
| | | | \ \ / / / ___| / _ \ | \ | |
| |_| |  \ V /  | |  _ | | | ||  \| |
|  _  |   | |   | |_| || |_| || |\  |
|_| |_|   |_|    \____| \___/ |_| \_|

HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.
        Version:v00.26 Build Apr 27 2020 - 14:04:40

================================================================================
=========================System have 2 socket, per sokect support 2 die=========================
=================System info start addr 0x160b5d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x160b5d0       0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x160b5f0       0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x160b610       1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x160b630       1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
================================================================================
================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport        RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]     +       32      0       0       0       6       1               (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]     +       33      0       0       0       4       3               (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]     +       40      1       0       0       1       1               (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]     +       44      1       1       1       8       8               (60:00.0)       (00:1d.0)       (00:1d.1)
================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]     48      Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 2, expect err 0x80000, Write 0x80000 to AER CAP reg offset 0x8 for dev 03:00.0 to mask ecrc_tx error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x80000 reach expect, success to mask ecrc_tx error report for dev dev 03:00.0.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 03:00.0.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 03:00.0.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 03:00.0.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 03:00.0 success.
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 2 (ecrc_tx) severity is 1, success to change severity reg from 0x4e2031 to 0x4e2031(set bitmask 0x80000).
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2616]: The val 0x100 of smn addr 0x111441a8 for dev 0:1.4, inject ecrc_tx, corresponding bitmask is 0x40.
[pcieinject [INFO] pcietest_write_errctrl_injecterr, line:2626]: Write 0x40 to smn addr 0x111441a8 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject ecrc_tx.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0xffff deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0x8086 deviceid 0x1521.
================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [8086:1521] 03:00.0 error status/mask=00080000/00080000
[pcieinject [INFO] __aer_print_error, line:180]:        [19] ECRC
================================================================================
[pcieinject [INFO] pcietest_inject_tl_err_gpp, line:2720]: After 1 retry, success to inject ecrc_tx to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t ecrc_tx -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

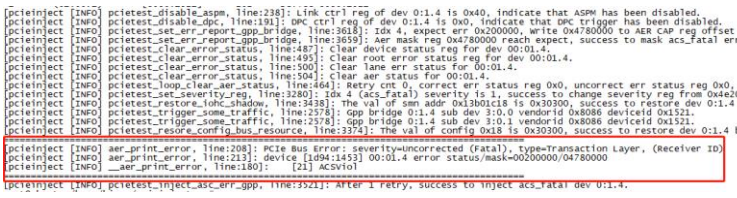
备注：ecrc 错误是整个 pcie 链路上端到端的 crc 校验，注入错误前请检查 RP-Switch-EP 是否支持 ecrc。

4.10. 注入 acs_fatal

```
root@ubuntu:/home/hygon/pcieinjectnew# ./pcieinject pcie_err -t acs_fatal -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.
 _   _  __   __  ____   ___   _   _
| | | | \ \ / / / ___| / _ \ | \ | |
| |_| |  \ V /  | |  _ | | | ||  \| |
|  _  |   | |   | |_| || |_| || |\  |
|_| |_|   |_|    \____| \___/ |_| \_|

HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.
        Version:v00.26 Build Apr 27 2020 - 14:04:40

================================================================================
=========================System have 2 socket, per sokect support 2 die=========================
=================System info start addr 0x1cd65d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x1cd65d0       0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x1cd65f0       0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x1cd6610       1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x1cd6630       1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
================================================================================
================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport        RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]     +       32      0       0       0       6       1               (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]     +       33      0       0       0       4       3               (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]     +       40      1       0       0       1       1               (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]     +       44      1       1       1       8       8               (60:00.0)       (00:1d.0)       (00:1d.1)
================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]     48      Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521
```



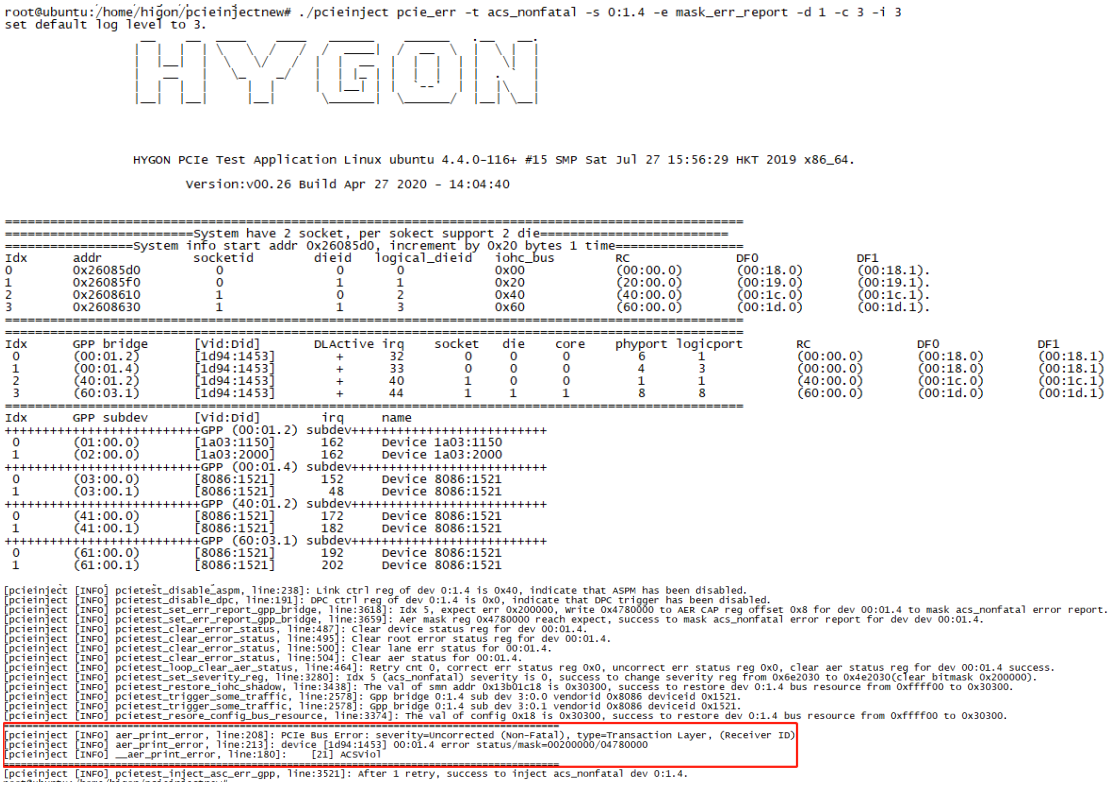
1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t acs_fatal -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：ACS violation 依赖于下面网卡发送 memory 请求，一次注入有可能网卡没有发包。

4.11. 注入 acs_nonfatal



1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t acs_nonfatal -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：ACS violation 依赖于下面网卡发送 memory 请求，一次注入有可能网卡没有发包。

4.12. 注入 completion timeout

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t completion_timeout -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.
```

```
HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

        Version:v00.26 Build Apr 27 2020 - 14:04:40

================================================================================
=========================System have 2 socket, per sokect support 2 die=========================
================System info start addr 0xb1d5d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0xb1d5d0          0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0xb1d5f0          0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0xb1d610          1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0xb1d630          1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
================================================================================================
================================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]       +       32      0       0       0       6       1             (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]       +       33      0       0       0       4       3             (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]       +       40      1       0       0       1       1             (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]       +       44      1       1       1       8       8             (60:00.0)       (00:1d.0)       (00:1d.1)
================================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 6, expect err 0x4000, write 0x4784000 to AER CAP reg offset 0x8 for dev 00:01.4 to mask completion_timeout error repor
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x4784000 reach expect, success to mask completion_timeout error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 success.
[pcieinject [INFO] pcietest_dbg_porta_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_porta_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 6 (completion_timeout) severity is 1, success to change severity reg from 0x4e2030 to 0x4e6030(set bitmask 0x4000).
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11144210 for dev 0:1.4, inject completion_timeout, corresponding bitmask is 0xc0000.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: write 0xc0000 to smn addr 0x11144210 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject completion_timeout.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0xffff deviceid 0xffff.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0xffff deviceid 0xffff.
================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Requester ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00004000/04784000
[pcieinject [INFO]   __aer_print_error, line:180]:        [14] CmpltTO
================================================================================
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject completion_timeout to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t completion_timeout -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入

4.13. 注入 unexpected completion

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t unexpected_cmplt -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.
```

```
HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

        Version:v00.26 Build Apr 27 2020 - 14:04:40

================================================================================
=========================System have 2 socket, per sokect support 2 die=========================
================System info start addr 0x9ec5d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x9ec5d0          0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x9ec5f0          0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x9ec610          1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x9ec630          1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
================================================================================================
================================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]       +       32      0       0       0       6       1             (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]       +       33      0       0       0       4       3             (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]       +       40      1       0       0       1       1             (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]       +       44      1       1       1       8       8             (60:00.0)       (00:1d.0)       (00:1d.1)
================================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521
```

```
[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 7, expect err 0x10000, write 0x4794000 to AER CAP reg offset 0x8 for dev 00:01.4 to mask unexpected_cmplt error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x4794000 reach expect, success to mask unexpected_cmplt error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 success.
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 7 (unexpected_cmplt) severity is 1, success to change severity reg from 0x4e6030 to 0x4f6030(set bitmask 0x10000).
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11144210 for dev 0:1.4, inject unexpected_cmplt, corresponding bitmask is 0xc000.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0xc000 to smn addr 0x11144210 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject unexpected_cmplt.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0xffff deviceid 0xffff.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0xffff deviceid 0xffff.
==========================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Requester ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00014000/04794000
[pcieinject [INFO] __aer_print_error, line:180]:    [14] CmpltTO
[pcieinject [INFO] __aer_print_error, line:180]:    [16] UnxCmplt
==========================================================================================
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject unexpected_cmplt to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t completion_timeout -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入

4.14. 注入 malformed tlp

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t malformed_tlp -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

        HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

              Version:v00.26 Build Apr 27 2020 - 14:04:40

==========================================================================================
========================System have 2 socket, per sokect support 2 die====================
================System info start addr 0x1b765d0, increment by 0x20 bytes 1 time==========
Idx     addr        socketid    dieid  logical_dieid  iohc_bus   RC           DF0          DF1
0       0x1b765d0   0           0      0              0x00       (00:00.0)    (00:18.0)    (00:18.1).
1       0x1b765f0   0           1      1              0x20       (20:00.0)    (00:19.0)    (00:19.1).
2       0x1b76610   1           0      2              0x40       (40:00.0)    (00:1c.0)    (00:1c.1).
3       0x1b76630   1           1      3              0x60       (60:00.0)    (00:1d.0)    (00:1d.1).
==========================================================================================
==========================================================================================
Idx     GPP bridge  [Vid:Did]    DLActive irq  socket  die  core  phyport logicport   RC          DF0         DF1
 0      (00:01.2)   [1d94:1453]     +     32     0      0    0      6       1         (00:00.0)   (00:18.0)   (00:18.1)
 1      (00:01.4)   [1d94:1453]     +     33     0      0    0      4       3         (00:00.0)   (00:18.0)   (00:18.1)
 2      (40:01.2)   [1d94:1453]     +     40     1      0    0      1       1         (40:00.0)   (00:1c.0)   (00:1c.1)
 3      (60:03.1)   [1d94:1453]     +     44     1      1    1      8       8         (60:00.0)   (00:1d.0)   (00:1d.1)
==========================================================================================
Idx     GPP subdev  [Vid:Did]    irq    name
++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++
 0      (01:00.0)   [1a03:1150]  162    Device 1a03:1150
 1      (02:00.0)   [1a03:2000]  162    Device 1a03:2000
++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++
 0      (03:00.0)   [8086:1521]  152    Device 8086:1521
 1      (03:00.1)   [8086:1521]  48     Device 8086:1521
++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++
 0      (41:00.0)   [8086:1521]  172    Device 8086:1521
 1      (41:00.1)   [8086:1521]  182    Device 8086:1521
++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++
 0      (61:00.0)   [8086:1521]  192    Device 8086:1521
 1      (61:00.1)   [8086:1521]  202    Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 8, expect err 0x40000, write 0x47d4000 to AER CAP reg offset 0x8 for dev 00:01.4 to mask malformed_tlp error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x47d4000 reach expect, success to mask malformed_tlp error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 success.
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 8 (malformed_tlp) severity is 1, success to change severity reg from 0x4f6030 to 0x4f6030(set bitmask 0x40000).
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11144210 for dev 0:1.4, inject malformed_tlp, corresponding bitmask is 0x3000.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0x3000 to smn addr 0x11144210 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject malformed_tlp.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0xffff deviceid 0xffff.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0xffff deviceid 0xffff.
==========================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Requester ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00044000/047d4000
[pcieinject [INFO] __aer_print_error, line:180]:    [14] CmpltTO
[pcieinject [INFO] __aer_print_error, line:180]:    [18] MalfTLP
==========================================================================================
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject malformed_tlp to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t malformed_tlp -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入

4.15. 注入 ecrc

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t ecrc -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

            HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

                 Version:v00.26 Build Apr 27 2020 - 14:04:40

==============================================================================================
========================System have 2 socket, per sokect support 2 die========================
=================System info start addr 0x1fb55d0, increment by 0x20 bytes 1 time=================
Idx     addr        socketid      dieid   logical_dieid   iohc_bus      RC            DF0           DF1
0       0x1fb55d0      0            0         0             0x00        (00:00.0)     (00:18.0)     (00:18.1).
1       0x1fb55f0      0            1         1             0x20        (20:00.0)     (00:19.0)     (00:19.1).
2       0x1fb5610      1            0         2             0x40        (40:00.0)     (00:1c.0)     (00:1c.1).
3       0x1fb5630      1            1         3             0x60        (60:00.0)     (00:1d.0)     (00:1d.1).
==============================================================================================
==============================================================================================
Idx     GPP bridge    [Vid:Did]     DLActive irq    socket   die    core    phyport logicport      RC            DF0           DF1
 0      (00:01.2)     [1d94:1453]      +      32       0      0      0        6       1        (00:00.0)     (00:18.0)     (00:18.1)
 1      (00:01.4)     [1d94:1453]      +      33       0      0      0        4       3        (00:00.0)     (00:18.0)     (00:18.1)
 2      (40:01.2)     [1d94:1453]      +      40       1      0      0        1       1        (40:00.0)     (00:1c.0)     (00:1c.1)
 3      (60:03.1)     [1d94:1453]      +      44       1      1      1        8       8        (60:00.0)     (00:1d.0)     (00:1d.1)
==============================================================================================
Idx     GPP subdev    [Vid:Did]      irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++
 0      (01:00.0)     [1a03:1150]    162     Device 1a03:1150
 1      (02:00.0)     [1a03:2000]    162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++
 0      (03:00.0)     [8086:1521]    152     Device 8086:1521
 1      (03:00.1)     [8086:1521]     48     Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++
 0      (41:00.0)     [8086:1521]    172     Device 8086:1521
 1      (41:00.1)     [8086:1521]    182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++
 0      (61:00.0)     [8086:1521]    192     Device 8086:1521
 1      (61:00.1)     [8086:1521]    202     Device 8086:1521


[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 9, expect err 0x80000, Write 0x47d4000 to AER CAP reg offset 0x8 for dev 00:01.4 to mask ecrc error report
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x47d4000 reach expect, success to mask ecrc error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 succes
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 9 (ecrc) severity is 1, success to change severity reg from 0x4f6030 to 0x4f6030(set bitmask 0x80000).
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11144210 for dev 0:1.4, inject ecrc, corresponding bitmask is 0xc00.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0xc00 to smn addr 0x11144210 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject ecrc.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0x8086 deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0x8086 deviceid 0x1521.
==============================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00080000/047d4000
[pcieinject [INFO] __aer_print_error, line:180]:    [19] ECRC
------------------------------------------------------------------------------
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject ecrc to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t ecrc -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入，需要从 RP 到 EP 整个链路上都支持 ECRC。

4.16. 注入 unsupported request

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t unsupported_req -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.
 _____ _____ _____ _____ _____ _____
|  _  |  |  |  _  |   __|     |   | |
|     |  |  |     |  |  |  |  | | | |
|__|__|\___/|__|__|_____|_____|_|___|

HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

        Version:v00.26 Build Apr 27 2020 - 14:04:40

================================================================================
=========================System have 2 socket, per sokect support 2 die=========================
=================System info start addr 0x89d5d0, increment by 0x20 bytes 1 time=================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x89d5d0          0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x89d5f0          0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x89d610          1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x89d630          1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
================================================================================================
================================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]       +      32       0       0       0       6       1       (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]       +      33       0       0       0       4       3       (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]       +      40       1       0       0       1       1       (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]       +      44       1       1       1       8       8       (60:00.0)       (00:1d.0)       (00:1d.1)
================================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
++++++++++++++++++++++++++GPP (40:01.2) subdev++++++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521
```

```
[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 60:3.1 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:203]: Success to disable dpc, write 0x0 to dpc ctrl reg for dev 60:3.1.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 10, expect err 0x100000, write 0x4500000 to AER CAP reg offset 0x8 for dev 60:03.1 to mask unsupported_req error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x4500000 reach expect, success to mask unsupported_req error report for dev dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 60:03.1.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 60:03.1 success.
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3280]: Idx 10 (unsupported_req) severity is 1, success to change severity reg from 0x4e2030 to 0x5e2030(set bitmask 0x100000).
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11240210 for dev 60:3.1, inject unsupported_req, corresponding bitmask is 0x300.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0x300 to smn addr 0x11240210 of dev 60:3.1 (socket 1, die 1 core 1, phyport 8) to inject unsupported_req.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 60:3.1 sub dev 61:0.0 vendorid 0x8086 deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 60:3.1 sub dev 61:0.1 vendorid 0x8086 deviceid 0x1521.
================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Uncorrected (Fatal), type=Transaction Layer, (Requester ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 60:03.1 error status/mask=00100000/04500000
[pcieinject [INFO] __aer_print_error, line:180]:        [20] UnsupReq
================================================================================
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject unsupported_req to dev 60:3.1.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t unsupported_req -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入，需要 EP 发送一笔 memory 请求才能产生 UR 的错误，建议在管理网卡对应的 GPP 桥注入。

4.17. 注入 bad tlp

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t bad_tlp -s 0:1.4 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

            HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

                   Version:v00.26 Build Apr 27 2020 - 14:04:40

==============================================================================================
=========================System have 2 socket, per sokect support 2 die========================
================System info start addr 0xbd45d0, increment by 0x20 bytes 1 time================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0xbd45d0          0               0         0           0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0xbd45f0          0               1         1           0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0xbd4610          1               0         2           0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0xbd4630          1               1         3           0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
==============================================================================================
==============================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]         +     32        0     0       0        6        1           (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]         +     33        0     0       0        4        3           (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]         +     40        1     0       0        1        1           (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]         +     44        1     1       1        8        8           (60:00.0)       (00:1d.0)       (00:1d.1)
==============================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
+++++++++++++++++++++++++GPP (00:01.2) subdev+++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
+++++++++++++++++++++++++GPP (00:01.4) subdev+++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
+++++++++++++++++++++++++GPP (40:01.2) subdev+++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
+++++++++++++++++++++++++GPP (60:03.1) subdev+++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 0:1.4 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 0:1.4 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 11, expect err 0x40, Write 0x6040 to AER CAP reg offset 0x14 for dev 00:01.4 to mask bad_tlp error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x6040 reach expect, success to mask bad_tlp error report for dev dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 00:01.4.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 00:01.4.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 00:01.4 success.
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3259]: Idx 11 severity 2 is correct, do not need modify aer severity reg.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11144210 for dev 0:1.4, inject bad_tlp, corresponding bitmask is 0xc0.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0xc0 to smn addr 0x11144210 of dev 0:1.4 (socket 0, die 0 core 0, phyport 4) to inject bad_tlp.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.0 vendorid 0xffff deviceid 0xffff.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 0:1.4 sub dev 3:0.1 vendorid 0xffff deviceid 0xffff.
==============================================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Corrected, type=Data Link Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 00:01.4 error status/mask=00000040/00006040
[pcieinject [INFO] __aer_print_error, line:180]:    [ 6] BadTLP
==============================================================================================
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject bad_tlp to dev 0:1.4.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t bad_tlp -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入。

4.18. 注入 bad dllp

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t bad_dllp -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

            HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

                   Version:v00.26 Build Apr 27 2020 - 14:04:40

==============================================================================================
=========================System have 2 socket, per sokect support 2 die========================
================System info start addr 0x223d5d0, increment by 0x20 bytes 1 time================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x223d5d0         0               0         0           0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x223d5f0         0               1         1           0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x223d610         1               0         2           0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x223d630         1               1         3           0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
==============================================================================================
==============================================================================================
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]         +     32        0     0       0        6        1           (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]         +     33        0     0       0        4        3           (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]         +     40        1     0       0        1        1           (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]         +     44        1     1       1        8        8           (60:00.0)       (00:1d.0)       (00:1d.1)
==============================================================================================
Idx     GPP subdev      [Vid:Did]       irq     name
+++++++++++++++++++++++++GPP (00:01.2) subdev+++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
+++++++++++++++++++++++++GPP (00:01.4) subdev+++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
+++++++++++++++++++++++++GPP (40:01.2) subdev+++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
+++++++++++++++++++++++++GPP (60:03.1) subdev+++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521
```

```
[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 60:3.1 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 60:3.1 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 12, expect err 0x80, write 0x6080 to AER CAP reg offset 0x14 for dev 60:03.1 to mask bad_dllp error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x6080 reach expect, success to mask bad_dllp error report for dev dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 60:03.1.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 60:03.1 success.
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3259]: Idx 12 severity 2 is correct, do not need modify aer severity reg.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11240210 for dev 60:3.1, inject bad_dllp, corresponding bitmask is 0x30.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0x30 to smn addr 0x11240210 of dev 60:3.1 (socket 1, die 1 core 1, phyport 8) to inject bad_dllp.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 60:3.1 sub dev 61:0.0 vendorid 0x8086 deviceid 0x1521.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 60:3.1 sub dev 61:0.1 vendorid 0x8086 deviceid 0x1521.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t bad_dllp -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入。DLLP 包可能是 ACK、NACK 包，也可能是 updata flow ctrl 等，DLLP 丢失，导致不可预知的错误

4.19. 注入 advisy non fatal

```
root@ubuntu:/home/higon/pcieinjectnew# ./pcieinject pcie_err -t advisory_nonfatal -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3
set default log level to 3.

          HYGON PCIe Test Application Linux ubuntu 4.4.0-116+ #15 SMP Sat Jul 27 15:56:29 HKT 2019 x86_64.

                Version:v00.26 Build Apr 27 2020 - 14:04:40

==============================================================================
========================System have 2 socket, per sokect support 2 die========================
================System info start addr 0x25e85d0, increment by 0x20 bytes 1 time================
Idx     addr            socketid        dieid   logical_dieid   iohc_bus        RC              DF0             DF1
0       0x25e85d0       0               0       0               0x00            (00:00.0)       (00:18.0)       (00:18.1).
1       0x25e85f0       0               1       1               0x20            (20:00.0)       (00:19.0)       (00:19.1).
2       0x25e8610       1               0       2               0x40            (40:00.0)       (00:1c.0)       (00:1c.1).
3       0x25e8630       1               1       3               0x60            (60:00.0)       (00:1d.0)       (00:1d.1).
==============================================================================
==============================================================================
Idx     GPP bridge      [vid:Did]       DLActive irq    socket  die     core    phyport logicport       RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]     +       32      0       0       0       6       1               (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]     +       33      0       0       0       4       3               (00:00.0)       (00:18.0)       (00:18.1)
 2      (40:01.2)       [1d94:1453]     +       40      1       0       0       1       1               (40:00.0)       (00:1c.0)       (00:1c.1)
 3      (60:03.1)       [1d94:1453]     +       44      1       1       1       8       8               (60:00.0)       (00:1d.0)       (00:1d.1)
==============================================================================
Idx     GPP subdev      [vid:Did]       irq     name
+++++++++++++++++++++++++GPP (00:01.2) subdev+++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     162     Device 1a03:1150
 1      (02:00.0)       [1a03:2000]     162     Device 1a03:2000
+++++++++++++++++++++++++GPP (00:01.4) subdev+++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     152     Device 8086:1521
 1      (03:00.1)       [8086:1521]      48     Device 8086:1521
+++++++++++++++++++++++++GPP (40:01.2) subdev+++++++++++++++++++++++++
 0      (41:00.0)       [8086:1521]     172     Device 8086:1521
 1      (41:00.1)       [8086:1521]     182     Device 8086:1521
+++++++++++++++++++++++++GPP (60:03.1) subdev+++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Device 8086:1521
 1      (61:00.1)       [8086:1521]     202     Device 8086:1521

[pcieinject [INFO] pcietest_disable_aspm, line:238]: Link ctrl reg of dev 60:3.1 is 0x40, indicate that ASPM has been disabled.
[pcieinject [INFO] pcietest_disable_dpc, line:191]: DPC ctrl reg of dev 60:3.1 is 0x0, indicate that DPC trigger has been disabled.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3618]: Idx 13, expect err 0x2000, write 0x6000 to AER CAP reg offset 0x14 for dev 60:03.1 to mask advisory_nonfatal error report.
[pcieinject [INFO] pcietest_set_err_report_gpp_bridge, line:3659]: Aer mask reg 0x6000 reach expect, success to mask advisory_nonfatal error report for dev dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:487]: Clear device status reg for dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:495]: Clear root error status reg for dev 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:500]: Clear lane err status for 60:03.1.
[pcieinject [INFO] pcietest_clear_error_status, line:504]: Clear aer status for 60:03.1.
[pcieinject [INFO] pcietest_loop_clear_aer_status, line:464]: Retry cnt 0, correct err status reg 0x0, uncorrect err status reg 0x0, clear aer status reg for dev 60:03.1 success.
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80000000 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xe to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001026 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0xf to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2762]: Sucess to write 0x80001010 to debug port A index reg (smn addr 0x700).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2772]: Sucess to write 0x5ff10001 to debug port A data low reg (smn addr 0x704).
[pcieinject [INFO] pcietest_dbg_portA_write, line:2782]: Sucess to write 0x0 to debug port A data high reg (smn addr 0x708).
[pcieinject [INFO] pcietest_set_severity_reg, line:3259]: Idx 13 severity 2 is correct, do not need modify aer severity reg.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2952]: The val 0x0 of smn addr 0x11240210 for dev 60:3.1, inject advisory_nonfatal, corresponding bitmask is 0xc0000.
[pcieinject [INFO] pcietest_write_inject_transaction, line:2963]: Write 0xc0000 to smn addr 0x11240210 of dev 60:3.1 (socket 1, die 1 core 1, phyport 8) to inject advisory_nonfatal.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 60:3.1 sub dev 61:0.0 vendorid 0xffff deviceid 0xffff.
[pcieinject [INFO] pcietest_trigger_some_traffic, line:2578]: Gpp bridge 60:3.1 sub dev 61:0.1 vendorid 0xffff deviceid 0xffff.
==============================================================================
[pcieinject [INFO] aer_print_error, line:208]: PCIe Bus Error: severity=Corrected, type=Transaction Layer, (Receiver ID)
[pcieinject [INFO] aer_print_error, line:213]: device [1d94:1453] 60:03.1 error status/mask=00002000/00006000
[pcieinject [INFO] __aer_print_error, line:180]:    [13] NonFatalErr
==============================================================================
[pcieinject [INFO] pcietest_inject_pcie_ras_err_gpp, line:3182]: After 1 retry, success to inject advisory_nonfatal to dev 60:3.1.
```

1、通过命令：./pcieinject gpp 显示出系统中所有 linkup 的 GPP 桥。

2、往对对应 GPP 桥注入对应错误，-s 后面参数就是 GPP bridge 对应的 bus:device.function。-c 注错重试次数，-i 注错重试时间间隔。

命令：./pcieinject pcie_err -t advisory_nonfatal -s 60:3.1 -e mask_err_report -d 1 -c 3 -i 3

备注：unlock 的 MP 设备或者 ES 的设备才可以注入。

5. 使用限制

下面几个功能和工具提供的错误注入功能没有直接关系，但是设计的系统配置会影响错

误上报，从而影响错误注入后的观察，需要手动配置。

1、DPC 功能

新版本的 OS 会支持 DPC 的 service，当不可修复错误触发 DPC 时，DPC service 会把 GPP 下接设备 remove，从而导致错误只能注入 1 次。如果想多次注入，需要输入-d 1，如果想触发 DPC，则输入-d 0。

```
root@cd-100:/home/higon/pcieinject# cat /proc/interrupts | grep dpc
  32:          0          0          0          0          0          0          0          0
          0          0          0          0          0          0          0          0
     0          0          0          0          0          0          0          0
0  IR-PCI-MSI 20480-edge      aerdrv, PCIe PME, pcie-dpc
  33:          0          0          0          0          0          0          0          0
          0          0          0          0          0          0          0          0
     0          0          0          0          0          0          0          0
0  IR-PCI-MSI 24576-edge      aerdrv, PCIe PME, pcie-dpc
  37:          0          0          0          0          0          0          0          0
          0          0          0          0          0          0          0          0
     0          0          0          0          0          0          0          0
0  IR-PCI-MSI 16830464-edge      aerdrv, PCIe PME, pcie-dpc
  44:          0          0          0          0          0          0          0          0
          0          0          0          0          0          0          0          0
     0          0          0          0          0          0          0          0
0  IR-PCI-MSI 50382848-edge      aerdrv, PCIe PME, pcie-dpc
```

7.31.3. DPC Control Register (Offset 06h)

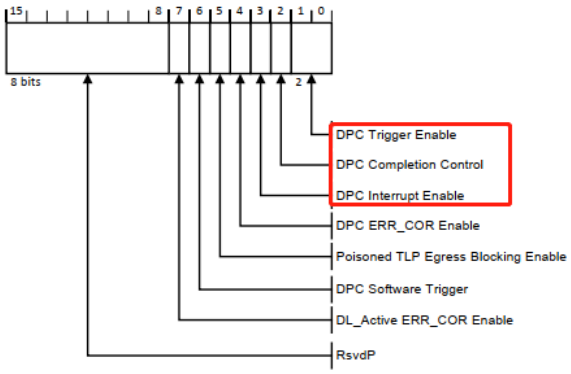


Figure 7-153: DPC Control Register

lspci -s bus:device.function -vvv 对应 GPP 桥的 DPC ctrl 已经被 disable。

```
Capabilities: [380 v1] Downstream Port Containment
        DpcCap: INT Msg #0, RPExt+ PoisonedTLP+ SwTrigger+ RP PIO Log 6, DL_ActiveErr+
        DpcCtl: Trigger:0 Cmpl- INT- ErrCor- PoisonedTLP- SwTrigger- DL_ActiveErr-
        DpcSta: Trigger- Reason:00 INT- RPBusy- TriggerExt:00 RP PIO ErrPtr:1f
        Source: 0000
```

2、Firmware first model

对应某些错误，如果错误上报是走到的 firmware first model 这条路，BIOS 会配置产生对应错误会 syncflood，从而导致系统重启，不方便观察结果。如果想多次注入错误，可以使用 script 目录下的 iohc_ras.sh 关闭对应的 GPP 的 firmware first model 功能。

```
root@cd-100:/home/higon/pcieinject# ./pcieinject gpp
set default log level to 3.
```

```
HYGON PCIe Test Application Linux cd-100 4.15.13-hygon #93 SMP Tue Mar 27 11:42:55 CST 2018 x86_64.
        Version:v00.15 Build Jan 15 2020 - 17:10:13

==========================System have 2 socket, per sokect support 2 die=====
Idx     GPP bridge      [Vid:Did]       DLActive irq    socket  die     core    phyport logicport        RC              DF0             DF1
 0      (00:01.2)       [1d94:1453]       +       32      0       0       0       6       1       (00:00.0)       (00:18.0)       (00:18.1)
 1      (00:01.4)       [1d94:1453]       +       33      0       0       0       4       3       (00:00.0)       (00:18.0)       (00:18.1)
 2      (20:03.2)       [1d94:1453]       +       37      0       1       1       9       9       (20:00.0)       (00:19.0)       (00:19.1)
 3      (60:03.1)       [1d94:1453]       +       44      1       1       1       8       8       (60:00.0)       (00:1d.0)       (00:1d.1)
Idx     GPP subdev      [Vid:Did]       irq     name
++++++++++++++++++++++++++GPP (00:01.2) subdev++++++++++++++++++++++++++
 0      (01:00.0)       [1a03:1150]     152     ASPEED Technology, Inc. AST1150 PCI-to-PCI Bridge
 1      (02:00.0)       [1a03:2000]     152     ASPEED Technology, Inc. ASPEED Graphics Family
++++++++++++++++++++++++++GPP (00:01.4) subdev++++++++++++++++++++++++++
 0      (03:00.0)       [8086:1521]     153     Intel Corporation I350 Gigabit Network Connection
 1      (03:00.1)       [8086:1521]     48      Intel Corporation I350 Gigabit Network Connection
++++++++++++++++++++++++++GPP (20:03.2) subdev++++++++++++++++++++++++++
 0      (21:00.0)       [8086:1521]     172     Intel Corporation I350 Gigabit Network Connection
 1      (21:00.1)       [8086:1521]     182     Intel Corporation I350 Gigabit Network Connection
++++++++++++++++++++++++++GPP (60:03.1) subdev++++++++++++++++++++++++++
 0      (61:00.0)       [8086:1521]     192     Intel Corporation I350 Gigabit Network Connection
 1      (61:00.1)       [8086:1521]     202     Intel Corporation I350 Gigabit Network Connection
root@cd-100:/home/higon/pcieinject# cd ./script/
root@cd-100:/home/higon/pcieinject/script# ./iohc_ras.sh 0 read
```

第一个参数是 logical dieid，算法为：socketid*每个 socket 支持多少 die+socket 内部 dieid

./iohc_ras.sh 0 read 是对应 die 的 ras action reg。

./iohc_ras.sh 0 write 是把 ras action reg 清零。

3、ecrc 支持

ecrc 是整个 pcie 链路上的 crc 校验，注入前请检查整个 pcie 链路上是否支持 ecrc 错误校验。

```
root@cd-100:/home/higon/pcieinject# lspci -s 0:1.4 -vvvvv
00:01.4 PCI bridge: Chengdu Haiguang IC Design Co., Ltd. PCIE GPP Bridge (prog-if 00 [Normal decode])
        Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx+
        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-
        Latency: 0, Cache Line Size: 64 bytes
        Interrupt: pin ? routed to IRQ 33
        NUMA node: 0
        Bus: primary=00, secondary=03, subordinate=03, sec-latency=0
        I/O behind bridge: 00001000-00001fff [size=4K]
        Memory behind bridge: ef600000-ef6fffff [size=1M]
        Prefetchable memory behind bridge: 00000323a0000000-00000323a00fffff [size=1M]
        Secondary status: 66MHz- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort+ <SERR- <PERR-
        BridgeCtl: Parity- SERR- NoISA- VGA- VGA16+ MAbort- >Reset- FastB2B-
                PriDiscTmr- SecDiscTmr- DiscTmrStat- DiscTmrSERREn-
        Capabilities: [50] Power Management version 3

Capabilities: [150 v2] Advanced Error Reporting
        UESta:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC+ UnsupReq- ACSViol-
        UEMsk:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC+ UnsupReq+ ACSViol-
        UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC+ UnsupReq- ACSViol-
        CESta:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr-
        CEMsk:  RxErr- BadTLP+ BadDLLP- Rollover- Timeout- AdvNonFatalErr+
        AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn+ ECRCChkCap+ ECRCChkEn+
                MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
        HeaderLog: 00000000 00000000 00000000 00000000
        RootCmd: CERptEn+ NFERptEn+ FERptEn+
        RootSta: CERcvd- MultCERcvd- UERcvd- MultUERcvd-
                 FirstFatal- NonFatalMsg- FatalMsg- IntMsg 0
        ErrorSrc: ERR_COR: 0000 ERR_FATAL/NONFATAL: 0000

root@cd-100:/home/higon/pcieinject# lspci -s 3:0.0 -vvvvv
03:00.0 Ethernet controller: Intel Corporation I350 Gigabit Network Connection (rev 01)
        DeviceName:  LOM 1
        Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx+
        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-
        Latency: 0, Cache Line Size: 64 bytes
        Interrupt: pin A routed to IRQ 153
        NUMA node: 0
        Region 0: Memory at ef620000 (32-bit, non-prefetchable) [size=128K]
        Region 2: I/O ports at 1020 [size=32]
        Region 3: Memory at ef644000 (32-bit, non-prefetchable) [size=16K]
        Capabilities: [40] Power Management version 3
                Flags: PMEClk- DSI+ D1- D2- AuxCurrent=0mA PME(D0+,D1-,D2-,D3hot+,D3cold-)
                Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=1 PME-

Capabilities: [100 v2] Advanced Error Reporting
        UESta:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
        UEMsk:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
        UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC+ UnsupReq- ACSViol-
        CESta:  RxErr- BadTLP+ BadDLLP- Rollover- Timeout- AdvNonFatalErr-
        CEMsk:  RxErr- BadTLP+ BadDLLP- Rollover- Timeout- AdvNonFatalErr+
        AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn+ ECRCChkCap+ ECRCChkEn+
                MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
        HeaderLog: 00000000 00000000 00000000 00000000
```

如果不支持，请检查 OS 配置是否把 ecrc 编入 OS 和 cmdline 是否打开了 ecrc 检查：ecrc=on。

4、测试完毕后环境恢复

错误注入测试可能修改了系统的默认配置，测试完毕请重启系统恢复环境。