AMD EPYC™ PROCESSOR
FAMILY 17H MODELS 30H-3FH SP3 "ROME"

REV 2020.10.02

“ROME” IO CERTIFICATION UPDATE

- PCIe
  - Gen3 officially certified and listed on PCI-SIG Integrators List
  - Gen4 officially certified and listed on PCI-SIG Integrators List
    - Passed all interoperability testing across 35 cards from 21 vendors
    - Passed all electrical compliance testing
- SATA
  - Officially certified and listed on the SATA-IO Integrators List
- USB
  - Officially certified and listed on the USB Integrators List

SECURITY UPDATE

- Fallout, Rogue In-Flight Data Load (RIDL), and ZombieLoad Attack (CVE-2018-12126, CVE-2018-12130, CVE-2018-12127, CVE-2019-11091)
- At AMD we develop our products and services with security in mind. Based on our analysis and discussions with the researchers, we believe our products are not susceptible to 'Fallout', 'RIDL' or 'ZombieLoad Attack' because of the hardware protection checks in our architecture. We have not been able to demonstrate these exploits on AMD products and are unaware of others having done so.
- For more information, see our new whitepaper, titled "Speculation Behavior in AMD Micro-Architectures."
- AMD security updates available at https://www.amd.com/en/corporate/product-security

“CLKREQ#” L1 PM SUBSTATES/PCIE LINK ACTIVATION ECN SUPPORT

- ECNs for PCIe “CLKREQ#” define an optional CLKREQ# signal for PCIe cards using a formerly “Reserved” pin on the PCIe connector (Pin B12)
  - If CLKREQ# is not implemented, this pin should be unconnected
  - If CLKREQ# is implemented, this pin should be pulled up by default and connected to control logic to define when to ASSERT
- Some add-in cards use B12 for “PROCHOT” functionality
  - These add-in cards are now considered legacy and are unsupported
- AMD Ethanol-X and Daytona-XT CRBs do not support CLKREQ#, and designs should not directly copy either CRB’s circuits for this signal

BOARD DESIGN GUIDANCE UPDATES FOR PCIE CARDS: PWRBRK#

- ECN for the PCIe spec defines an optional PWRBRK# signal for PCIe cards using a formerly “Reserved” pin on the PCIe connector (pin B30)
  - If PWRBRK# *is not* implemented, this pin should be unconnected (float)
  - If PWRBRK# *is* implemented, this pin should be pulled up by default and connected to control logic to define when to ASSERT (pull down to assert)
- AMD’s Ethanol-X CRB does not support PWRBRK#, designs should not directly copy Ethanol-X’s circuit for this signal
  - On Ethanol-X, B30 has a pull-down resistor, but is actively pulled high by a GPIO expander

“ROME” KEY PROCESSOR SAMPLES MILESTONES

Milestone	Release<ed>	Availability	Customer Usage
ES1: Proto Samples	Starts shipping <09/27/2018>	225W 64C 180W 32C fused non-secure	BIOS development, Platform Bring-up, Platform functional and electrical checks, OS Boot, Early system validation
Ethanol X Reference Platforms	Starts shipping <10/05/2018>		
A0 PC: Production Candidate Samples	Starts shipping <11/30/2018>: 225W 64C Starts shipping <12/19/2018>: 180W 32C fused non-secure		System validation, Power cycling, Thermal test, Early performance estimates, Pre-certification tests
B0 PR: Production Ready Samples	Starts shipping <06/2019 Wave1> <09/2019 Wave 2>	See next page for Wave OPNs fused secure	Final regressions, Certification tests, Production solutions, Thermal test, Benchmark testing, Pilot support
AMD Production Ramp	Starts shipping <06/2019 Wave1> <09/2019 Wave 2>		Production
AMD Launch	<08/07/2019>		

- Dates reflect start in sampling ship date
- Updates from previous revisions are marked in blue font
- <date> Reflects completed milestone
- Please contact your AMD sales representative for details on sample shipment quantities and dates

“ROME” PROCESSOR PRODUCT STACK (PAGE 1 OF 2)

2P/1P	Model	Production OPN*	Default TDP (W)	cTDP Min (W)	cTDP Max (W)	Cores	Threads	Base Freq (GHz)	Max. Boost Freq (GHz)**	L3 Cache (MB)	DDR Channels	Max DDR Freq (1 DPC)	PCIe
2P/1P	7H12	100-000000055	280	225	280	64	128	2.6	3.3	256	8	3200	x128
2P/1P	7742	100-000000053	225	225	240	64	128	2.25	3.4	256	8	3200	x128
2P/1P	7702	100-000000038	200	165	200	64	128	2.0	3.35	256	8	3200	x128
2P/1P	7662	100-000000137	225	225	240	64	128	2.0	3.3	256	8	3200	x128
2P/1P	7642	100-000000074	225	225	240	48	96	2.3	3.3	256	8	3200	x128
2P/1P	7552	100-000000076	200	165	200	48	96	2.2	3.3	192	8	3200	x128
2P/1P	7542	100-000000075	225	225	240	32	64	2.9	3.4	128	8	3200	x128
2P/1P	7532	100-000000136	200	180	200	32	64	2.4	3.3	256	8	3200	x128
2P/1P	7502	100-000000054	180	165	200	32	64	2.5	3.35	128	8	3200	x128
2P/1P	7452	100-000000057	155	155	180	32	64	2.35	3.35	128	8	3200	x128
2P/1P	7F72	100-000000141	240	225	240	24	48	3.2	3.7	192	8	3200	x128
2P/1P	7402	100-000000046	180	165	200	24	48	2.8	3.35	128	8	3200	x128
2P/1P	7352	100-000000077	155	155	180	24	48	2.3	3.2	128	8	3200	x128
2P/1P	7F52	100-000000140	240	225	240	16	32	3.5	3.9	256	8	3200	X128
2P/1P	7302	100-000000043	155	155	180	16	32	3.0	3.3	128	8	3200	X128
2P/1P	7282	100-000000078	120	120	150	16	32	2.8	3.2	64	8	3200***	x128
2P/1P	7272	100-000000079	120	120	150	12	24	2.9	3.2	64	8	3200***	x128
2P/1P	7F32	100-000000139	180	165	200	8	16	3.7	3.9	128	8	3200	X128
2P/1P	7262	100-000000041	155	155	180	8	16	3.2	3.4	128	8	3200	X128
2P/1P	7252	100-000000080	120	120	150	8	16	3.1	3.2	64	8	3200***	X128

PR OPNs will contain -00 suffix ** Maximum single core frequency ***8 channel and 3200 capable, performance optimized for 4 channels @ 2666

NOTE: 7F32, 7F52, and 7F72 require AGESA RomePI-SP3_1.0.0.5 based BIOS or greater to achieve performance

“ROME” PROCESSOR PRODUCT STACK (PAGE 2 OF 2)

2P/1P	Model	Production OPN*	Default TDP (W)	cTDP Min (W)	cTDP Max (W)	Cores	Threads	Base Freq (GHz)	Max. Boost Freq (GHz)**	L3 Cache (MB)	DDR Channels	Max DDR Freq (1 DPC)	PCIe
1P	7702P	100-000000047	200	165	200	64	128	2.0	3.35	256	8	3200	x128
1P	7502P	100-000000045	180	165	200	32	64	2.5	3.35	128	8	3200	x128
1P	7402P	100-000000048	180	165	200	24	48	2.8	3.35	128	8	3200	x128
1P	7302P	100-000000049	155	155	180	16	32	3.0	3.3	128	8	3200	X128
1P	7232P	100-000000081	120	120	150	8	16	3.1	3.2	32	8	3200***	x128

* PR OPNs will contain -00 suffix ** Maximum single core frequency ***8 channel and 3200 capable, performance optimized for 4 channels @ 2666

ROME B0 PR SAMPLE WAVES

- Wave 1:
  - 64 core 225W (2P/1P)
  - 64 core 200W (2P/1P and 1P)
  - 48 core 200W (2P/1P)
  - 32 core 225W (2P/1P)
  - 32 core 180W (2P/1P and 1P)
  - 32 core 155W (2P/1P)
  - 24 core 180W (2P/1P and 1P)
  - 24 core 155W (2P/1P)
  - 16 core 155W (2P/1P and 1P)
  - 8 core 155W (2P/1P)
- Wave 2:
  - 48 core 225W (2P/1P)
  - 16 core 120W (2P/1P)
  - 12 core 120W (2P/1P)
  - 8 core 120W (2P/1P and 1P)
  - 64 core 225W (2P/1P)
  - 32 core 200W (2P/1P)
  - 64 core 280W (2P/1P)
- Wave 3:
  - 8 core 180W (2P/1P)
  - 16 core 240W (2P/1P)
  - 24 core 240W (2P/1P)

"ROME" AGESA SCHEDULE

- AGESA will release at an approximate monthly cadence from first samples
- AGESA dates are dependent upon sample availability
- BIOS Partners: AMI, Insyde, BMC Partners: AMI, Insyde
- AMD enables IBVs to provide core BIOS. Please contact your IBV for platform BIOS release schedules. In general, IBV code is available 1-2 weeks after AGESA release.

AGESA release	Release Date	Comments
RomePI-SP3_1.0.0.1	<07/05/2019>	
RomePI-SP3_1.0.0.2	<08/02/2019>	
RomePI-SP3_1.0.0.3	<09/13/2019>	
RomePI-SP3_1.0.0.4	<10/04/2019>	
RomePI-SP3_1.0.0.5	<12/04/2019>	This release adds support for AMD ROM Armor, an NDA security feature that improves protection of the SPI ROM. AMD recommends enabling this feature in platform BIOS. Please contact your IBV or AMD support team for details.
RomePI-SP3_1.0.0.6	<01/28/2020>	This release provides the capability to select the ROM3 address range with a new APCB token, APCB_TOKEN_UID_FCH_ROM3_BASE_HIGH. AMD recommends setting this to 0x000007FC if ROM3 access is desired.
RomePI-SP3_1.0.0.7	<04/02/2020>	As this release contains an update to improve LRDIMM 2D training, AMD recommends requalifying all LRDIMMs. This change does not impact RDIMMs, 3DS RDIMMs or NVDIMMs
RomePI-SP3_1.0.0.8	<07/03/2020>	
RomePI-SP3_1.0.0.9	<10/02/2020>	LOWER_SKP_OS_RCV_SUPPORT capability is disabled in SRIS mode to assure RP receiver can handle the extra clock dilation. Please contact your AMD support team for details.
RomePI-SP3_1.0.0.A	TBD	Schedule and availability of AGESA 1.0.0.A will depend upon reported high-priority issues, please contact your AMD support team for details.

DUAL NAPLES/ROME BIOS SUPPORT WITH ROMEPI-SP3_0.0.8.0

AMD

- Provides the ability to combine Naples and Rome BIOS images in a singular BIOS flash image
- Naples and Rome binaries are generated separately
  - Naples from NaplesPI
  - Rome from RomePI
- Re-validation and QA efforts on Naples are minimized given leverage of previous Naples validation/BIOS
  - Customers will still need to confirm Naples production support with new dual image
- AMD has completed Dual Boot proof of concept on AMD CRBs with 32MB and 64MB ROMs
- First AGESA support will be provided with RomePI-SP3_0.0.8.0
- Rome A0 samples will support SPI Dual Boot, B0 is required for LPC boot

"ROME" TOOLS CAPABILITIES

Tool	Current Version	Comments
AMD SST (ASST)	• Version 7.4.9 for Windows • Version 7.4.9 for Linux	
MemEye	• Version 1.26.11	• MemEye Training Guide v 1.2
AMD XpressIO	• Version 3.0.2.1 for Windows • Version 3.0.2.1 for Linux	• Adds SystemDeck functionality • AMD XpressIO (AMDXIO) Training Guide v 1.2, AMD XpressIO User's Guide PID 56463 v0.60
AMD XpressIO Margin Visualization (AMV)	• Version 1.50	
AMD Compliance Pattern Recipe Tool	• Version 1.2	
Machine Error Decode Tool	• Version 2.8.11 for Windows • Version 2.8.11 for Linux RPM • Version 2.8.11 for Linux Debian	
RAS Error Injection Test	• Version 1.7.13 for Windows • Version 1.7.13 for Linux RPM • Version 1.7.13 for Linux Debian	• RAS Error Injection Tool Platform Guidance v 2.10
AMD Validation Toolkit (AVT)	• Version 2.7.6 for Windows • Version 2.7.6 for Linux	
HDT	• Version 20.2.50.4926	• HDT20 version 20.2.21.4778 or greater is required for Milan B0
SDLE-2	• Version 2.9.13	• Analysis spreadsheets and batch files v2.07 • DDR4 SDLE-2 Load Pod Installation Guide v1.0
Net Tool Database for SPE Server	• Version 1.0.2.20200803	
AMD Server Schematic Checker	• Version 1.01	

“ROME” NVDIMM-N SUPPORT

AMD

- Rome Processors offer improved NVDIMM-N support
  - The Rome processor supports the open software ecosystem
    - Support for the ‘ADR’ style programming model (data is durable after it leaves the CPU caches)
    - Supports ACPI and UEFI standards for persistent memory
    - Support for Windows, Linux, PMDK (formerly called NVML)
    - Retains data across Warm Resets, Cold Resets, S5 entry, and power failure
  - Rome includes the new CLWB and WBNOINVD x86 instructions for improved performance
- NVDIMM-N requires a platform designed for NVDIMM-N
  - These platforms support power loss detection and hold-up power
  - The platform warns the processor about an imminent power loss to allow in-flight data to be committed
  - Not all platforms will be designed to support NVDIMM-N
- Reference PID 56333 NVDIMM-N Support for Socket SP3 Family 17h Models 30h-3Fh Processors Application Note

"ROME" MAXIMUM MEMORY FREQUENCY AND CAPACITY – 1 DIMM PER CHANNEL[1]

	DIMM Population[2]	DDR4 Frequency MT/s		Capacity (8 Gbit x4 devices)	Capacity (16 Gbit x4 devices)
DIMM Type[3]	DIMM 0	Rome in legacy platforms[4]	Rome in optimized platforms[4]	1 channel / 8 channels	1 channel / 8 channels
RDIMM[5]	1R (1 rank)	2666	3200	16GB / 128GB	32GB / 256GB
	2R or 2DR (2 ranks)	2666	3200	32GB / 256GB	64GB / 512GB
LRDIMM (dual die package devices)	4DR (4 ranks)	2666	3200	64GB / 512GB	128GB / 1TB
LRDIMM (3DS devices)	2S2R (4 ranks)	2666[6]	3200	64GB / 512GB	128GB / 1TB
	2S4R (8 ranks)	2666	3200	128GB / 1TB	256GB / 2TB
3DS RDIMM	2S2R (4 ranks)	2666	3200	64GB / 512GB	128GB / 1TB
	2S4R (8 ranks)	2666	3200	128GB / 1TB	256GB / 2TB

Notes:

1. Refer to PID 55803, Processor Programming Reference (PPR) as the official source for the memory support matrix
2. JEDEC nomenclature used to describe DDR4 DIMM types. For 2 DIMMs populated on a channel, DIMM 1 is the furthest distance from the processor.
3. NVDIMM-N is supported, speed is TBD
4. Refer to PID 55414, Socket SP3 Processor Motherboard Design Guide for the official descriptions and requirements for Naples legacy and Rome optimized platforms. Rome optimized platforms may require 14 layer thin stack up, low loss or ultra low loss PCB dielectric with HVLP foil, lowered margin targets, and limited AVL.
5. RDIMMs built from x4 and x8 devices are supported and the frequencies shown apply to both. However, the capacities represent those of x4 DIMMs only. RDIMMs built with x8 devices have half the capacity of the x4 RDIMMs with an equal number of ranks.
6. 2S2R LRDIMMs are not supported in Naples.

"ROME" MAXIMUM MEMORY FREQUENCY AND CAPACITY – 2 DIMMS PER CHANNEL[1]

	DIMM Population / Chan[2]		DDR4 Frequency MT/s		Capacity (8Gbit x4 devices)	Capacity (16Gbit x4 devices)
DIMM Type[3]	DIMM 0	DIMM 1	Rome in legacy platforms[4]	Rome in optimized platforms[4]	1 channel / 8 channels	1 channel / 8 channels
RDIMM[5]	-	1R	2666	3200	16GB / 128GB	32GB / 256GB
	1R	1R	2133	2933	32GB / 256GB	64GB / 512GB
	-	2R or 2DR	2400	3200	32GB / 256GB	64GB / 512GB
	1R	2R or 2DR	2133	2933	48GB / 384GB	96GB / 768GB
	2R or 2DR	2R or 2DR	2133	2933	64GB / 512GB	128GB / 1TB
LRDIMM (dual die package devices)	-	4DR	2666	3200	64GB / 512GB	128GB / 1TB
	4DR	4DR	2133	2933	128GB / 1TB	256GB / 2TB
LRDIMM (3DS devices)	-	2S2R (4 ranks)	2666[6]	3200	64GB / 512GB	128GB / 1TB
	-	2S4R (8 ranks)	2666	3200	128GB / 1TB	256GB / 2TB
	2S2R (4 ranks)	2S2R (4 ranks)	2133[6]	2933	128GB / 1TB	256GB / 2TB
	2S2R (4 ranks)	2S4R (8 ranks)	2133[6]	2933	192GB / 1.5TB	384GB / 3TB
	2S4R (8 ranks)	2S4R (8 ranks)	2133	2933	256GB / 2TB	512GB / 4TB
3DS RDIMM	-	2S2R (4 ranks)	2400	2933	64GB / 512GB	128GB / 1TB
	2S2R (4 ranks)	2S2R (4 ranks)	1866	2666	128GB / 1TB	256GB / 2TB
	-	2S4R (8 ranks)	2400	2933	128GB / 1TB	256GB / 2TB
	2S2R (4 ranks)	2S4R (8 ranks)	1866	2666	192GB / 1.5TB	384GB / 3TB
	2S4R (8 ranks)	2S4R (8 ranks)	1866	2666	256GB / 2TB	512GB / 4TB

1, 2, 3, 4, 5, 6 See notes on prior page

“ROME” DIMM VALIDATED MEMORY MATRIX

- See PID 56573 Socket SP3 Validated Memory for Family 17h Models 30h-3Fh posted on DevHub

SP3 “ROME” TECHNICAL DOCUMENTATION

PLEASE REFER TO THE DEVHUB FOR LATEST DOCUMENTATION

“Rome” shares documentation with “Naples” as both are Socket SP3, “Naples” is Family 17h models 00h-0Fh, “Rome” is Family 17h models 30h-3Fh

PID	TITLE	Release<ed>
55421	Socket SP3 Processor Motherboard Schematic Checklist (NDA)	<Rev: 3.02 May 2020>
55422	Socket SP3 Processor Motherboard Layout Checklist (NDA)	<Rev: 3.01 May 2020>
55414	Socket SP3 Processor Motherboard Design Guide	<Rev: 1.09 Feb 2020>
55996	AMD Socket SP3 Processor NVMe Drive Implementation App Note	<Rev: 0.72 Aug 2017>
56211	Socket SP3 Thermal Test User’s Guide	<Rev: 0.16 Feb 2020>
56333	NVDIMM-N Support for Socket SP3 Family 17h Models 30h-3Fh Processors Application Note	<Rev: 0.50 Jun 2018>
56361	Secure Debug Specification and Implementation Guide for AMD Family 17h Models 00h-0Fh and Models 30h-3Fh	<Rev: 0.70 Aug 2018>
56412	AMD Socket SP3 Processor IO Configuration Guide	<Rev: 0.78 June 2020>
56421	SEV-ES / Guest-Hypervisor Communication Block Standardization	<Rev: 0.70 Oct 2018>
56419	Hadoop Tuning Guide for AMD EPYC Processor Based Servers	<Rev: 1.10 Sept 2020>
56338	Socket SP3 Platform NUMA Topology for AMD Family 17h Models 30h-3Fh	<Rev: 1.10 May 2020>
56502	Memory Population Guidelines for AMD EPYC™ 7002 Generation “Rome”	<Rev: 1.00 Sept 2020>
56573	Socket SP3 Validated Memory for Family 17h Models 30h-3Fh	<Rev: 0.87 Sept 2020>
56743	Socket SP3 NVME Hotplug Specification for Family 17h 30h-3Fh	<Rev: 1.31 Mar 2020>
56763	VMware® Network Tuning Guide for AMD EPYC™ 7002 Series	<Rev: 0.90 Nov 2019>
56746	Windows® Network Tuning Guide for AMD EPYC™ 7002 Series	<Rev: 0.90 Nov 2019>
56739	Linux® Network Tuning Guide for AMD EPYC™ 7002 Series	<Rev: 0.20 Oct 2019>
56745	Workload Tuning Guide for AMD EPYC™ 7002 Series	<Rev: 0.80 Nov 2019>
56826	NVMe Performance Tuning for EPYC 7002 Generation Processors	<Rev: 0.70 June 2020>
56901	EU 2019/424 Eco Design Lot 9 Guidance for AMD EPYC Processors	<Rev: 1.00 May 2020>

PID	TITLE	Release<ed>
EthanolX	Ethanol-X design files	<Rev A Dec 2018>
EthanolX_DBG	Ethanol-X debug design files	<Rev A Dec 2018>
EthX_setupguide	Ethanol-X Setup Guide	<Rev 1.04 Oct 2018>
56283	Functionality Guide for Socket SP3 Platform Code-Named Ethanol-X	<Rev: 0.71 Sept 2018>
EthX_FPGA	Ethanol-X FPGA	<Rev 2.1 Aug 2018>
2U_RC	2U Rackmount Rome-based Reference with SMT DIMMs paper study	<Rev A Oct 2018>
Daytona XT	Daytona XT design files	<Rev A Jan 2019>
DXT_Readme	Daytona XT Platform Readme	<Rev 1.0 Mar 2019>
Daytona FPGA	Dayton XT FPGA System Update	<Rev 2.2 Aug 2019>
56284	Socket SP3 Processor Platform Code-Named "Daytona XT" System Manual (NDA)	<Rev 1.03 Apr 2019>
56480	Functionality Guide for Socket SP3 Processor Platform Code-Named “Daytona XT” (NDA)	<Rev 1.0 Mar 2019>
Diesel for Rome	Diesel Power reference for Rome	<Rev A Jan 2019>
56415	Socket SP3 Processors Models 30h-3Fh Server System Validation Manual	<Rev: 0.76 Jun 2019>

SP3 “ROME” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
55423	Thermal Design Guide for Socket SP3 Processors (NDA)	<Rev: 1.05 Feb 2020>
55423	Thermal Design Guide for Socket SP3 Processors (PUB)	<Rev: 3.00 Nov 2017>
55424	Flotherm Thermal Model for Socket SP3 Processors User's Guide (NDA)	<Rev: 1.06 Mar 2020>
55949	Socket SP3 Thermal Test Slug User’s Guide	<Rev: 0.84 Aug 2020>
55426	Functional Data Sheet (FDS) for Socket SP3 Processors	<Rev: 1.03 Feb 2020>
55441	Electrical Data Sheet (EDS) for AMD Family 17h Socket SP3 Processors	<Rev: 0.65 July 2020>
56366	AMD Family 17h Models 30h-3Fh Processor Engineering Sample Information	<Rev: 1.03 Apr 2018>
56585	Power and Thermal Data Sheet for AMD Family 17h Models 30h-3Fh Socket SP3 Processors	<Rev: 0.88 July 2020>
56323	Revision Guide for AMD Family 17h Models 30h-3Fh Processors (NDA)	<Rev: 0.77 Sept 2020>
BSDL	BSDL for Socket SP3 Processors for AMD Family 17h Models 30h-3Fh, Revision B0	<Rev: 2.00 July 2019>
48022	AMD Serial VID Interface 2.0 (SVI2) Specification (NDA)	<Rev: 1.10 Feb 2020>
55260	Socket SP3 Design Specification (NDA)	<Rev: 1.16 Aug 2020>
55261	Socket SP3 Qualification Plan (NDA)	<Rev: 1.04 June 2017>
56104	Socket SP3 Electrical Qualification Test and Measurement Methodology	<Rev: 0.7 June 2017>
55418	Infrastructure Roadmap (IRM) for Socket SP3 Processors (NDA)	<Rev: 1.17 Feb 2020>
55701	Socket SP3 Mechanical CAD Package	<Rev: 1.01 June 2017>
55821	SP3 Carrier Frame Installation Procedure	<Rev: 1.00 June 2016>
55823	Socket SP3 Post Reflow Assembly & Package Insertion Procedure	<Rev: 1.10 June 2016>
SeaSim_SP3_Rome	SEASIM Tools and Models for SP3 Rome (PCIe/XGMI)	<Rev: 0077 Nov 2018>
SP3_Rome_IBIS_DDR4	SP3 Rome DDR4 IBIS Models	<Rev: 001 Feb 2018>
SP3_Rome_IBIS_GPIO	SP3 Rome GPIO IBIS Models	<Rev: 1.0 Oct 2019>
SP3_Rome_Pkg_Trace	SP3 Rome Package Trace	<Rev: 001 Feb 2018>

SP3 “ROME” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
55483	AMD Generic Encapsulated Software Architecture (AGESA) V9 Interface Specification	<Rev: 1.52 Sept 2020>
55730	Common Platform Module Implementation Guide	<Rev: 1.21 Apr 2019>
56305	Software Optimization Guide for AMD Family 17h Models 30h and Greater Processors (NDA)	<Rev: 1.01 Aug 2018>
56305	Software Optimization Guide for AMD Family 17h Models 30h and Greater Processors (PUB)	<Rev: 3.02 Mar 2020>
56278	Socket SP3 RAS Platform Specification and Implementation Guide for AMD Family 17h Models 30h-3Fh	<Rev: 1.04 May 2019>
56375	AMD64 Technology Platform Quality of Service Extensions (PUB)	<Rev: 1.01 Sept 2018>
55758	AMD Platform Security Processor BIOS Architecture Design Guide for AMD Family 17h Processors	<Rev: 1.11 Aug 2020>
48882	AMD I/O Virtualization Technology (IOMMU) Specification	<Rev: 3.05 Jan 2020>
56329	AMD Family 17h Models 30h-3Fh ACPI v6.2 Porting Guide	<Rev: 1.00 Feb 2019>
56534	Enabling Platform Secure Boot for AMD Family 17h Processor Based Server Platforms	<Rev: 0.90 June 2020>
56334	AMD Family 17h Models 30h-3Fh SP3 Platform Performance and Power Optimization Guide	<Rev: 1.08 Mar 2020>
AOCLv2.1	AMD Optimized CPU Libraries and User Guide	<Rev: 2.2.1 July 2020>
56653	AMD Collaborative Processor Performance Control (CPPC)	<Rev: 0.7 July 2019>
55766	Secure Encrypted Virtualization API Specification (PUB)	<Rev: 0.22 Aug 2019>
56570	Preferred IO Usage Guide	<Rev: 0.92 Mar 2020>
55803	Processor Programming Reference (PPR) for AMD Family 17h Models 30h-3Fh Processors, Revision B0	<Rev: 0.91 Sept 2020>
RomePI-SP3	RomePI-SP3 Platform Initialization Package	<Rev: 1.0.0.9 Sept 2020>
RomePI_Rel_Notes	RomePI-SP3 Release Notes	<Rev: 1.0.0.9 Sept 2020>
EthanolX_RM_BIOS	Ethanol-X Rome BIOS	<Rev: REX1009A Sept 2020>
DaytonaX_RM_BIOS	Daytona-X Rome BIOS	<Rev: RDY1009A Sept 2020>
Insyde_BMC	Insyde Universal BMC Binary for AMD CRBs	<Rev: 3.53 Oct 2020>
Windows IO drivers	SP3 Windows Peripheral-IO Drivers	<Rev: 2.10.09.156 Sept 2020>
	SP3 Windows PSHED Plug-in Driver	<Rev: 2.09.21.544 Sept 2020>
AMD uProf	AMD uProf for Linux (Deb), Linux (RPM), Linux (Tar), Windows, FreeBSD	<Rev: 3.3 Aug 2020>

"ROME" VOLTAGE REGULATORS

Supplier	Supplier Part Number	Part Description
INFINEON	IR3584MTRPBF	RH DIGITAL MULTI-PHASE BUCK CONTROLLER, DUAL OUTPUT 3.3V, 5x5mm, QFN-40 SMT
INFINEON	IR35201MTRPBF	IC: IR35201, Dual Output Digital 8-Phase PWM Controller for CPU Voltage Regulation, 3.3V
INFINEON	IR35204MTRPBF	RH IR35204, DIGITAL MULTI-PHASE BUCK CONTROLLER, DUAL OUTPUT, 3.3V, 5x5mm, QFN-40, SMT
INFINEON	TDA21472	RH TDA21472 High Freq. DC-DC Converter, 70A PowerStage w/Integrated MOSFET, 4.25V - 16V, 5x6x1mm, PQFN-39, SMT

Supplier	Supplier Part Number	Part Description
RENESAS (INTERSIL)	ISL68127IRAZ-T	RH Digital Dual-Output 7-Phase Configurable PWM Controller w/PMBus, QFN-48
RENESAS (INTERSIL)	ISL69144IRAZ-T	RH DIGITAL DUAL O/P, 4 PHASE AMD PWM CONTROLLER, PMBus AND SVI2 INTERFACE, 5X5mm, TQFN-40
RENESAS (INTERSIL)	ISL69147IRAZ-T	RH DIGITAL DUAL O/P, 7 PHASE AMD PWM CONTROLLER, PMBus AND SVI2 INTERFACE, 6X6mm, QFN-48
RENESAS (INTERSIL)	ISL99227IRZ-T	RH Smart Power Stage Module w/Integrated Hi Accuracy Current & Temp Monitors,3.3Vin PWM, 60A, QFN-32
RENESAS (INTERSIL)	ISL99227FRZ-T	RH Smart Power Stage Module w/Integrated Hi Accuracy Current & Temp Monitors,3.3Vin PWM, 60A, QFN-32

Contact your AMD representative for other VRM partner options

SP3 "ROME" TARGETED OPERATING SYSTEMS & HYPERVISORS

	N - 1	Launch (N)
Microsoft	**Server 2016** x2APIC/256T not supported	**Server 2019** See next pages for Windows updates
vmware	**vSphere 6.5 EP15**	**vSphere 6.7u3**
redhat	**RHEL 7.6.6**	**RHEL 8.0.2**
SUSE	**SLES 12 SP4**	**SLES 15 SP1**
CANONICAL	**Ubuntu 16.04.6**	**Ubuntu 18.04.3**
CITRIX		**Hypervisor 8.1**

Linux notes:

- Essential Rome Support (including X2APIC/IOMMU patches to utilize 256T) available with Linux Kernel 4.19
- Rome 256 CPU thread support requires X2APIC in cooperation with IOMMU interrupt remapping
- Disabling the IOMMU (or X2APIC) will result in a system only capable of supporting up to 255 CPU threads
- Ubuntu 18.04.3 has released. For support, users must upgrade from 18.04.2
- Now that Rome has launched, please contact the OS partners for officially supported versions.

	AMD EPYC 7xx2 "Rome" Engineering Support	OS Version	Linux Kernel	Xen	Release	End of Maintenance Mainstream	End of Maintenance Extended	
Microsoft	✓	Server 2019			11/2018	1/2024	1/2029	https://support.microsoft.com/en-us/lifecycle
	✓	Server 2016			10/2016	1/2022	1/2027	MSFT Rome Support Link
		Server 2012 R2			11/2013	10/2018	10/2023	
vmware	✓	vSphere 6.7 u3			3Q/2019	11/2021	11/2023	https://www.vmware.com/content/dam/digitalmarketing/vmware/en/pdf/support/product-lifecycle-matrix.pdf
	✓	vSphere 6.5 EP15			3Q/2019	11/2021	11/2023	
CITRIX	✓	Hypervisor 8.1	4.19	4.13	12/2019			https://www.citrix.com/support/product-lifecycle/product-matrix.html http://hcl.xenserver.org/cpus/
redhat	✓	RHEL 8.0.2	4.18		5/2019	5/2024	2/2029	https://access.redhat.com/support/policy/amd https://wiki.centos.org https://fedoraproject.org/wiki/Fedora_Release_Life_Cycle
	✓	RHEL 7.6.6	3.10		10/2018	4Q/2019	11/2020	
		CentOS 8.0	4.18		5/2019			
		CentOS 7.6	3.10		12/2018	4Q/2020	6/2024	
		Fedora 29+	4.18		10/2018	10/2019		
SUSE	✓	SLES 15 SP1	4.12	4.12.1	6/2019	15SP2+6m	TBD	https://www.suse.com/lifecycle/ https://en.opensuse.org/Lifetime * Continuously updated
	✓	SLES 12 SP4	4.12	4.4.1	10/2018	12SP5+6m	TBD	
		OpenSUSE Leap 15.1	4.12		5/2019	11/2020	N/A	
		Tumbleweed	*		*	*		
CANONICAL	✓	Ubuntu 18.04.3 LTS	5.0		08/2019	4/2023	4/2028	http://www.ubuntu.com/info/release-end-of-life
	✓	Ubuntu 16.04.6 LTS	4.15		2/2019	4/2021	4/2024	
Other		Debian 9.9	4.9		4/2019	~2020	~2022	https://wiki.debian.org/DebianReleases
		Debian 8.11	3.16		6/2018	6/2018	6/2020	https://blogs.oracle.com/scoter/oracle-linux-and-unbreakable-enterprise-kernel-uek-releases
		Oracle Linux UEK 5.1	4.14		Mid/2019	7/2024	N/A	

X2APIC FOR WINDOWS SERVER 2019 (WS2019)

AMD

- Microsoft Windows Server 2019 now supports x2APIC Mode on AMD EPYC 7*xx*2 / Rome Processors.
  - The specific patch (which could be used on existing installs) is:
    - https://support.microsoft.com/en-us/help/4512534/windows-10-update-kb4512534
  - Current Windows Cumulative Updates will automatically include this patch.
  - Unless update\patch is applied, Windows Server 2019 will not boot a 256 thread AMD EPYC system (i.e. this only affects 2P systems with 64-core Rome OPNs).
  - To install original WS2019 ISO, and this patch (on AMD EPYC 2P 64-core system): disable SMT in BIOS, install original WS2019, run Windows Update until fully patched and\or ensure KB4512534 is installed, re-enable SMT in BIOS.
- Microsoft has also refreshed media to include corresponding x2APIC patch, so disabling of SMT is no longer necessary.
  - Please use the latest updated Windows Server 2019 ISO (Oct.2019 or beyond) provided by Microsoft.
    - Users can obtain an evaluation copy from the Evaluation Center here.
    - For customers with a Visual Studio Subscription (formerly MSDN or Microsoft Developer Network) October 2019 or beyond here.
    - It is also be available on the Microsoft Partner Network (MPN) here.
    - For customers with a valid Software Assurance, this new version of Windows Server 2019 can be downloaded from the Volume Licensing Service Center (VLSC) here.
- Please reference Microsoft AMD EPYC 7xx2 KB article for additional details:
  - https://support.microsoft.com/en-us/help/4514607/windows-server-support-and-installation-instructions-for-amd-rome-proc

ROME WINDOWS SERVER 2019 POWER PROFILE RECOMMENDED SETTINGS

AMD

- AMD is discussing with Microsoft incorporating recommended power profiling settings into Windows Server. Until changes are implemented it is AMD's recommendation to use "PerfAutonomousMode" on AMD Rome platforms
- Additional information on Static Performance options is documented by Microsoft here: https://docs.microsoft.com/en-us/windows-hardware/customize/power-settings/static-configuration-options-for-the-performance-state-engine
- Autonomous mode is supported by CPPC 2, which is the version implemented on Windows Server 2019
- March 2020 Windows Cumulative Update (or later) contains a fix simplifying the below Powercfg settings below.

- For Windows Balanced Mode:
  - Step 1: Configure Windows power plan to Balanced
  - Step 2: Run the following commands on Windows prompt terminal
    - Powercfg /setacvalueindex scheme_current sub_processor perfautonomous 1
    - Powercfg /setacvalueindex scheme_current sub_processor PERFEPP 100
    - Powercfg /setactive scheme_current
- For Windows Performance Mode:
  - Step 1: Configure Windows power plan to High Performance
  - Step 2: Run the following commands on Windows prompt terminal
    - Powercfg /setacvalueindex scheme_current sub_processor perfautonomous 1
    - Powercfg /setacvalueindex scheme_current sub_processor PERFEPP 0
    - Powercfg /setactive scheme_current
- For Windows HLK Mode:
  - Step 1: Configure Windows power plan to Balanced
  - Step 2: Run the following commands on Windows prompt terminal
    - Powercfg /setacvalueindex scheme_current sub_processor PROCTHROTTLEMIN 0
    - Powercfg /setacvalueindex scheme_current sub_processor PROCTHROTTLEMAX 100
    - Powercfg /setacvalueindex scheme_current sub_processor perfautonomous 1
    - Powercfg /setacvalueindex scheme_current sub_processor PERFEPP 0
    - Powercfg /setacvalueindex scheme_current sub_processor PERFBOOSTMODE 4
    - Powercfg /setactive scheme_current

DEVICES TESTED BY PARTNERS WITH ROME

PLEASE CONTACT THE RESPECTIVE PARTNER FOR MORE INFORMATION

Category	Partner	Devices
Connectivity (NIC, FC)	Mellanox (NIC)	25G: MCX4421A-ACAN 25G: MCX512A-ACAT 100G: MCX556A-EDAT, MCX516A-CDAT 200G: MCX654106A-HCAT
	Broadcom (NIC)	1G: BCM5719, BCM5720 10G: BCM57454, BCM57416, BCM57416, BCM57412 (PCIe NIC and OCP 3.0) 25G: BCM57414 (2 x 25G PCIe NIC and OCP 3.0) 100G: Stratus – BCM57454(P1100P) 100G: THOR – BCM57504 (P425G – 4 x 25G PCIe NIC, N425G – 4 x 25G OCP 3.0) 200G: THOR – BCM57508 (P2100G – 2 x 100G PCIe NIC, N2100G – 2 x 100G OCP 3.0, P2200G – 2 x 200G High-Availability PCIe NIC, N2200G – 2 x 200G High-Availability OCP 3.0)
	Broadcom (FC)	Lancer-G6: LPe31000, LPe31002, LPe31004, LPe32000, LPe32002 Lancer-G7: LPe35000, LPe35002, LPe35004
	Marvell (NIC & FC)	NIC: QL45xxx, QL41xxx FC: QLE269x, QLE27xx, QLE277x

DEVICES TESTED BY PARTNERS WITH ROME

PLEASE CONTACT THE RESPECTIVE PARTNER FOR MORE INFORMATION

Category	Partner	Devices
Storage	SK Hynix	• PE6011/PE6031 • PE4011
	Kioxia (Toshiba)	• CM6 (Gen4) • XD5 • HK6-R
	Micron	• 2300 M.2 • 9300 • 7300 PRO and MAX
	Western Digital	• Ultrastar DC SN200 (Omaha), Ultrastar DC SN630 (Aspen) • Ultrastar DC HC (Leo-B), Ultrastar DC SN640 (Aspen+)
	Samsung	• PM1733 (Gen4) • PM1723b
Accelerator (dGPU, FPGA)	NVIDIA	• Tesla - V100, P40, P4, M10 • Quadro – P4000
	AMD Radeon GPU's	• MI25, MI50, MI60 • WX7100, WX5100
	Xilinx	• Alveo: U50, U200, U250, U280

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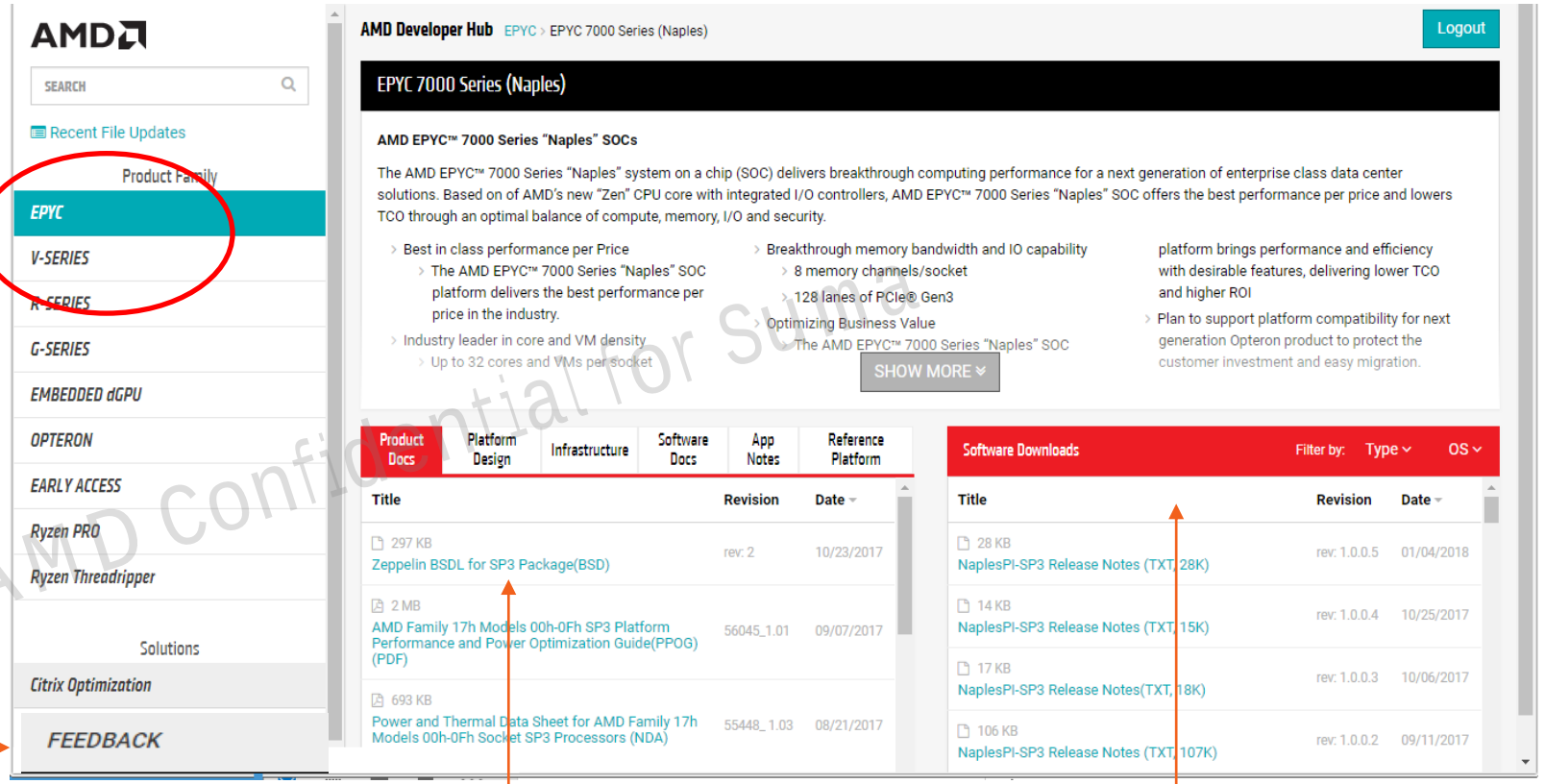

Technical Documents organized in tabs.

- Software Downloads includes Drivers, Tools, AGESA PI00
- Filter by Title, Revision, Type, and OS

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