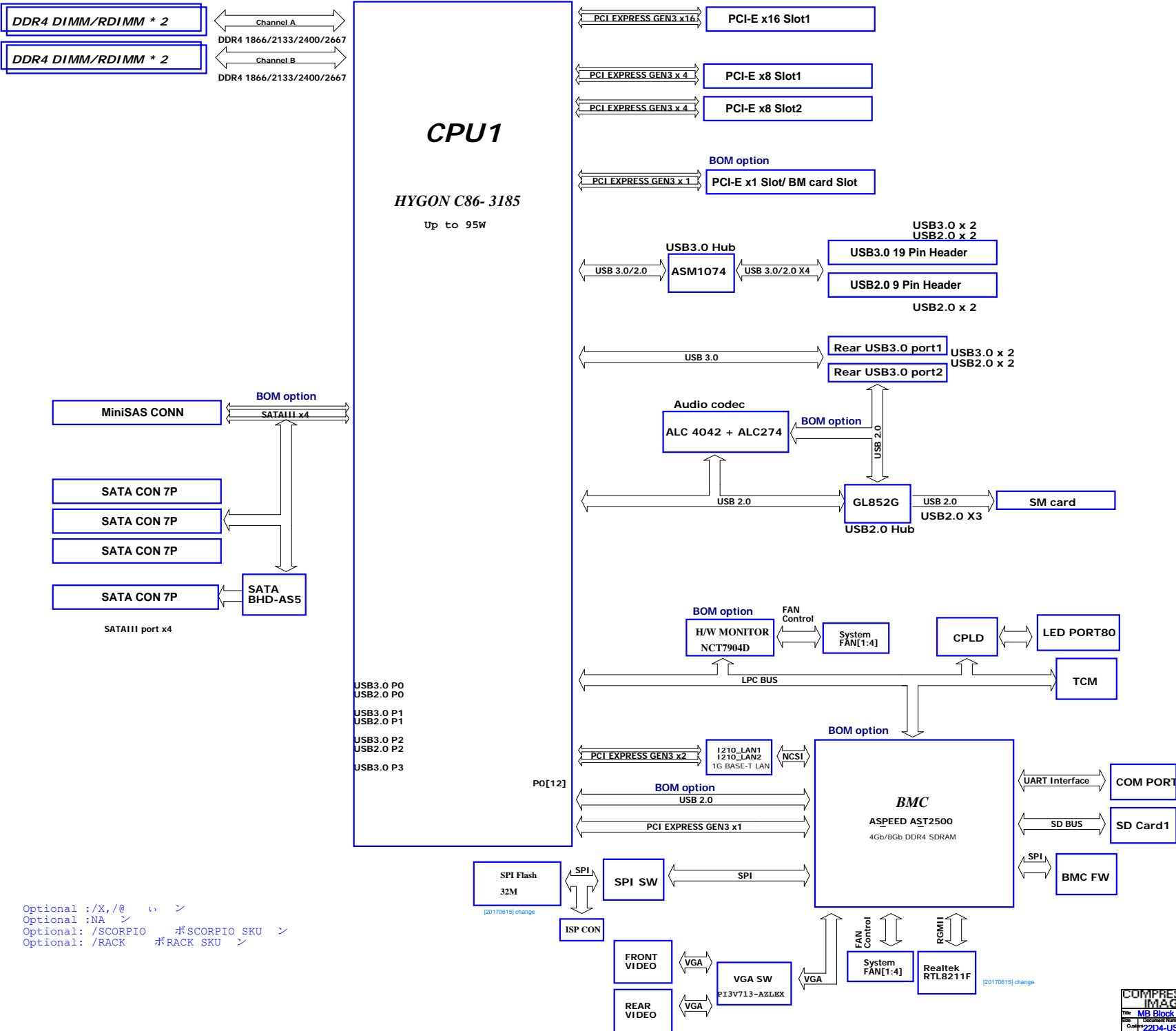


001 Index	039 N/A	077 ASM1074-3(PWR)	116 N/A
002 MB Block Diagram	040 N/A	078 ASM1074-4(EMI/ESD)	117 +5V_DUAL2
003 CHANGE HISTORY	041 CPU POWER_SEQUENCE	079 ASM1074-5(USB CONN)	118 +3V_DUAL
004 Clock Distribution	042 TCM SSX44-B	080 N/A	119 +1.8V_DUAL
005 SMBus	043 AUDIO_ALC4042+ALC274	081 GL852G-1	120 PWR_AST2500
006 BM_CARD_&_SPI_BUS_TOPOLOGY	044 AUDIO_BACK+FRONT Conn.	082 GL852G-2(EMI/ESD)	121 +3.3V_VDD
007 N/A	045 AUDIO_LDO	083 SM Pin header	122 +1.2V_SATA
008 POWER_SEQ_DIAGRAM	046 N/A	084 N/A	123 N/A
009 N/A	047 MINI SAS HD & SATA Conn.	085 N/A	124 +1.8V_VDD
010 CLK BUFF-1(33/50Mhz)	048 SATA BHD5-AS5	086 N/A	125 +VCORE1 (IR35201)
011 CLK BUFF-2(100Mhz)	049 N/A	087 N/A	126 +VCORE1 (Phase 1&2)
012 CPU_DDR4_CHA	050 PCIEX16 Slot1	088 AST2500 - PCIE/DDR4/LPC/I2C	127 +VCORE1 (Phase 3&4)
013 CPU_DDR4_CHB	051 PCIEX 4 Slot1	089 AST2500 - SPI/UART/MAC	128 +VSOC1 (Phase 1&2)
014 CPU_PCIE_SATA	052 PCIEX 4 Slot2	090 AST2500 - VGA/USB/GPIO	129 +VCORE1\VSOC1_Caps
015 CPU_USB_CLK_SPI_LPC	053 PCIEX 1 Slot with BM Card	091 AST2500 - RTL8211E	130 +VDDIO_AB (IR35201)
016 CPU_UART_SD_I2C_GPIO	054 LAN1-I210_NCSI	092 AST2500 - TRAPPING	131 +VDDIO_AB (Phase 1&2)
017 CPU_THERM_SVID_JTAG	055 DM_LAN1_USB3_12	093 AST2500 - POWER/GND	132 +VDDIO_Caps
018 CPU_POWER	056 LAN2-I210	094 P_PCIE/SATA SW	133 +VPPDDR_AB
019 CPU_GND	057 LAN1_LAN2_CONN	094 VGA Switch	134 +VTTDDR_AB
020 HDT CONNECTOR	058 NCT6796D(MAIN,HW MONITOR)	095 N/A	135 DECOUPLING CAP
021 N/A	059 NCT6796D(PORT 80 LED)	096 SD CARD	136 N/A
022 DDR4_CHA_DIMM0	060 NCT6796D(FAN)	097 SYSTEM_LED	137 N/A
023 DDR4_CHA_DIMM1	061 NCT6796D(COM)1CONN+1HEADER	098 N/A	138 FP HEADER & BUTTON
024 DDR4_CHB_DIMM0	062 TEMP Sensor	099 N/A	139 BMC_System_BTN_FRU&_IPMB
025 DDR4_CHB_DIMM1	063 Rear USB3 (EMI/ESD/OC)	100 N/A	140 SYS_SKU_ID
026 N/A	064 CPLD	101 N/A	141 CURRENTMONITOR-1
027 N/A	065 N/A	102 CPU/BMC/CPLD/JTAG	142 N/A
028 N/A	066 N/A	103 N/A	143 DIMM ERROR LED
029 N/A	067 N/A	104 N/A	144 N/A
030 N/A	068 N/A	105 N/A	145 N/A
031 N/A	069 N/A	106 N/A	146 N/A
032 N/A	070 N/A	107 N/A	147 Screw Hole
033 N/A	071 N/A	108 N/A	148 PCB
034 N/A	072 RTC BATTERY	109 N/A	149 EMI_CAP
035 N/A	073 BIOS ROM	110 Powe_Block_Diagram	150 N/A
036 N/A	074 POWER CONNECTOR	111 N/A	
037 N/A	075 ASM1074-1	112 N/A	
038 N/A	076 ASM1074-2(OC)	113 N/A	
		114 +0.9V_VDDCR_SOC_S5	
		115 +5VSB	

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Optional :/X,/@ い ン
Optional :NA ン
Optional: /SCORPIO ボ SCORPIO SKU ン
Optional: /RACK ボ RACK SKU ン

Schematics Change History

Version	Date / Author	Comments
V1.00		1. First Init.
V1.01		

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IMAGE

Title **CHANGE HISTORY**

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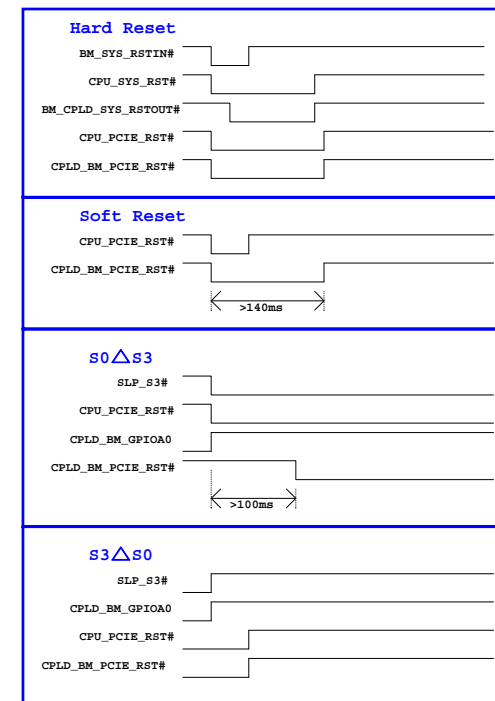
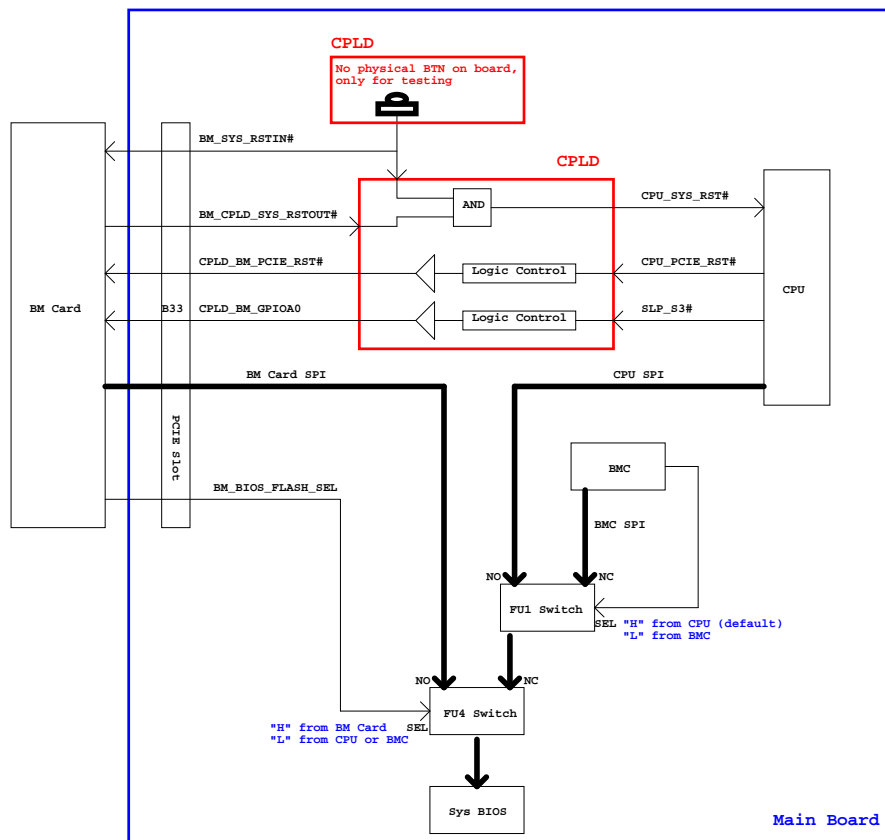
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IMAGE

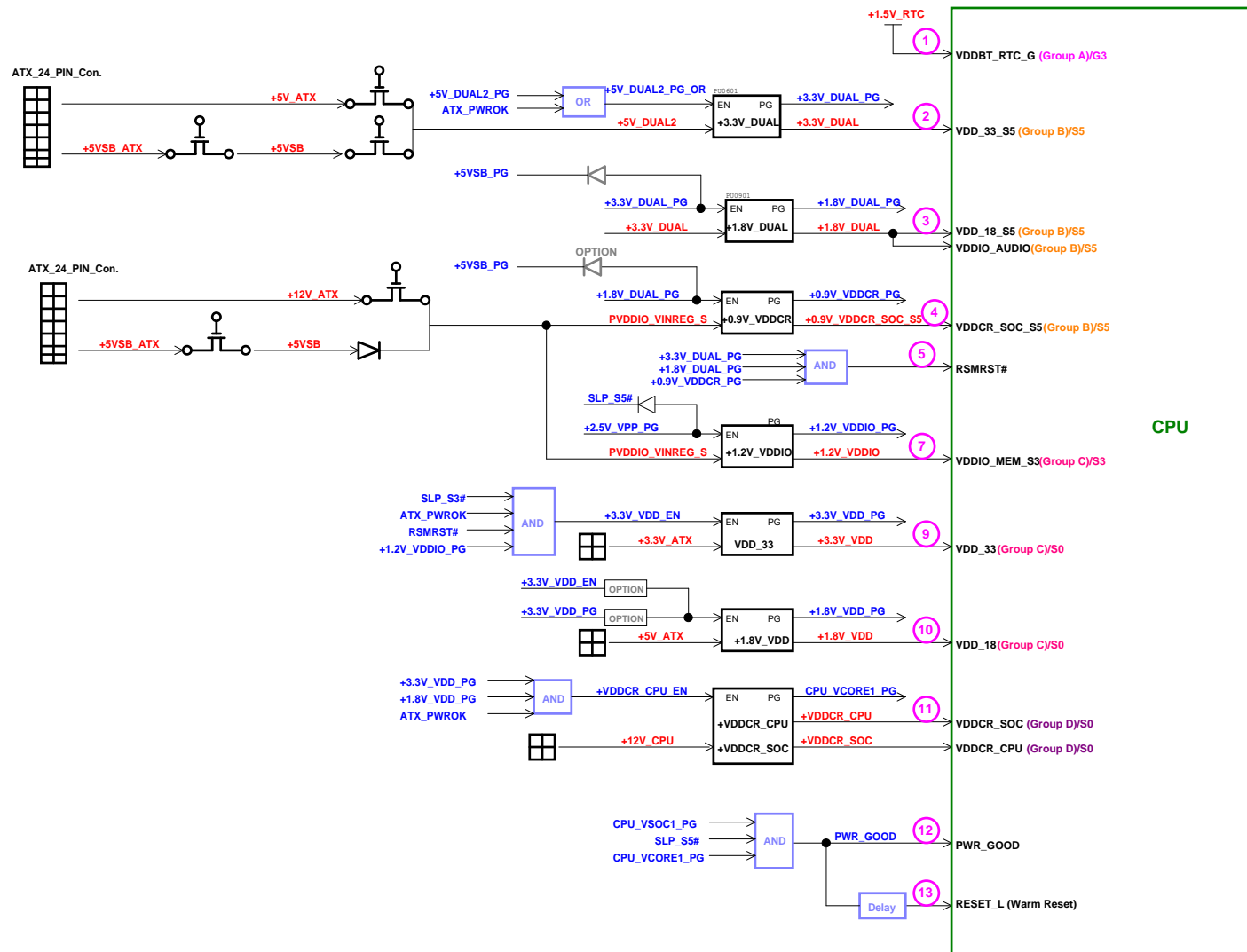
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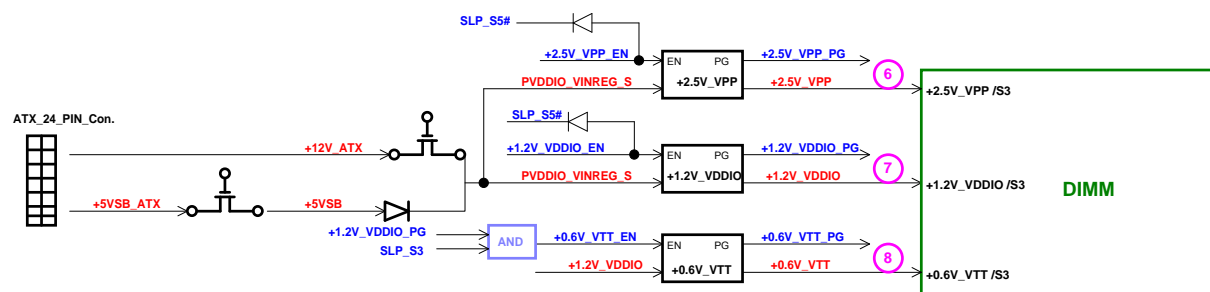




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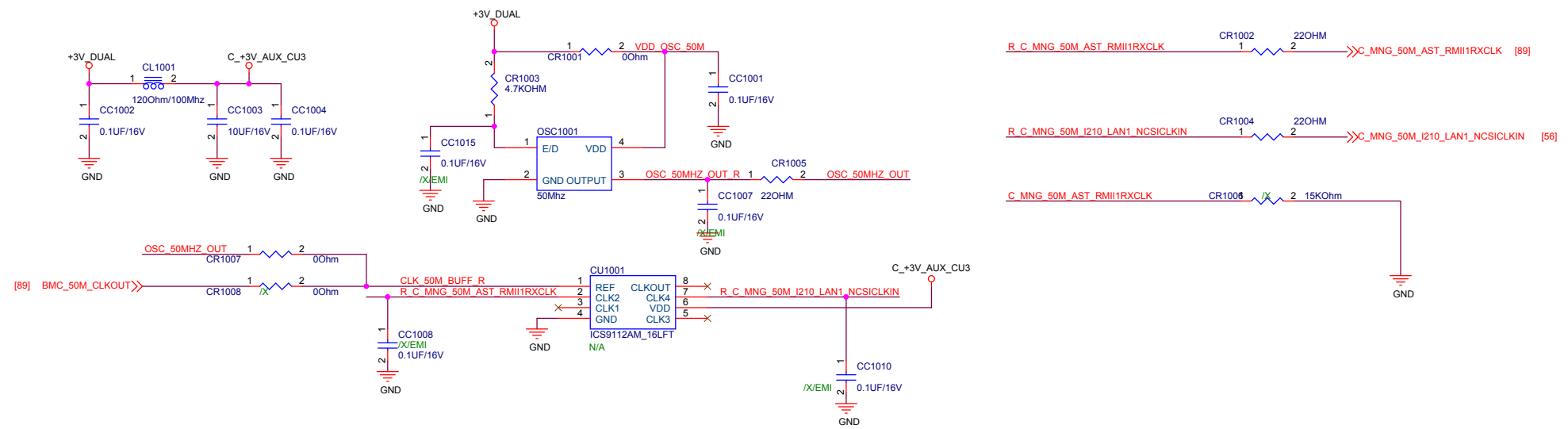


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POWER SEQ DIAGRAM			
Time	Document Number	Rev	
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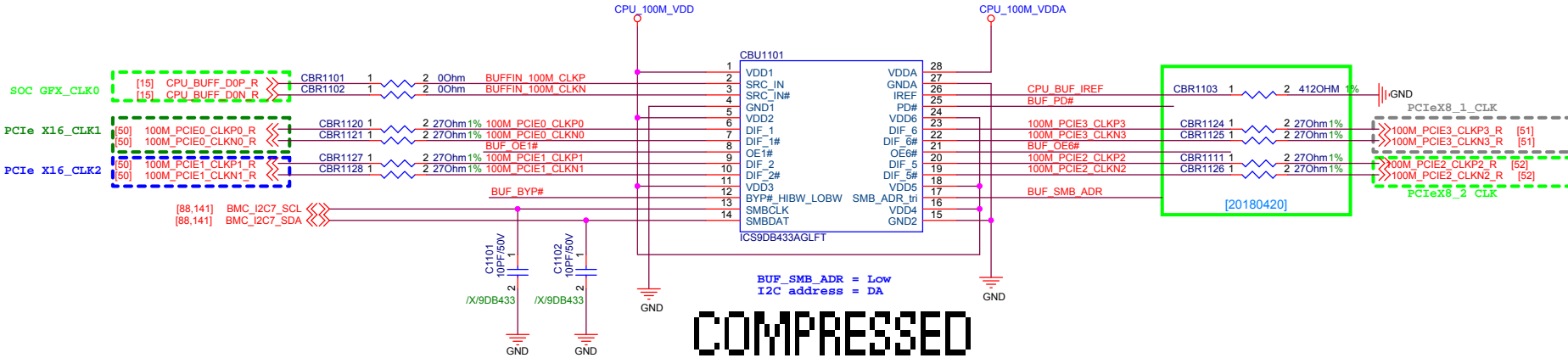
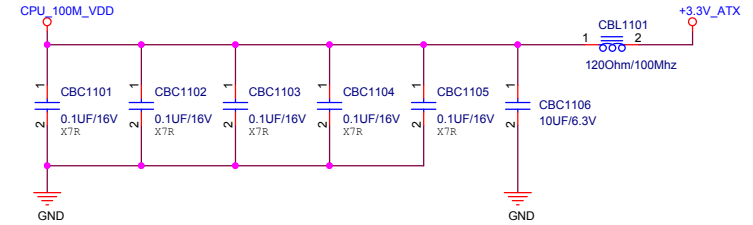
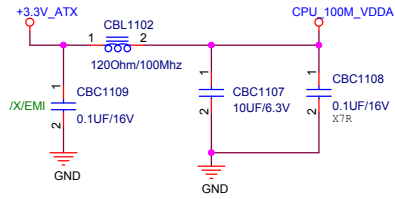


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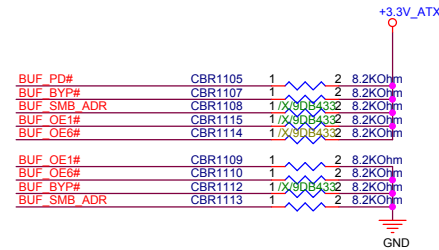
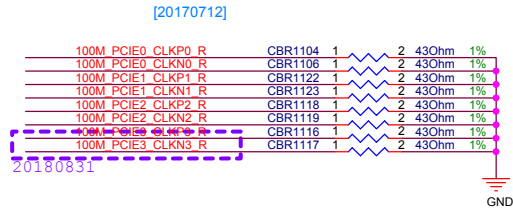
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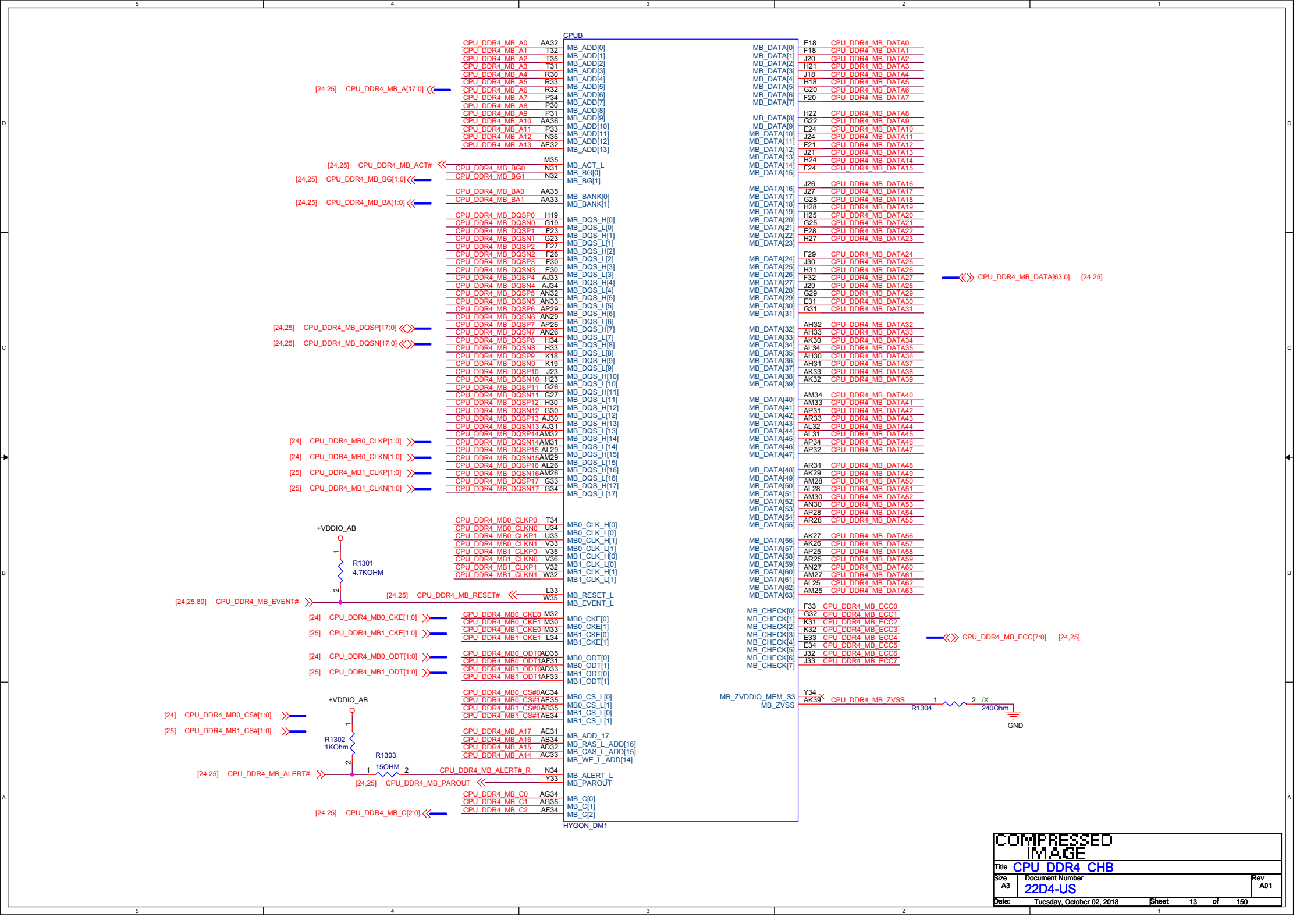


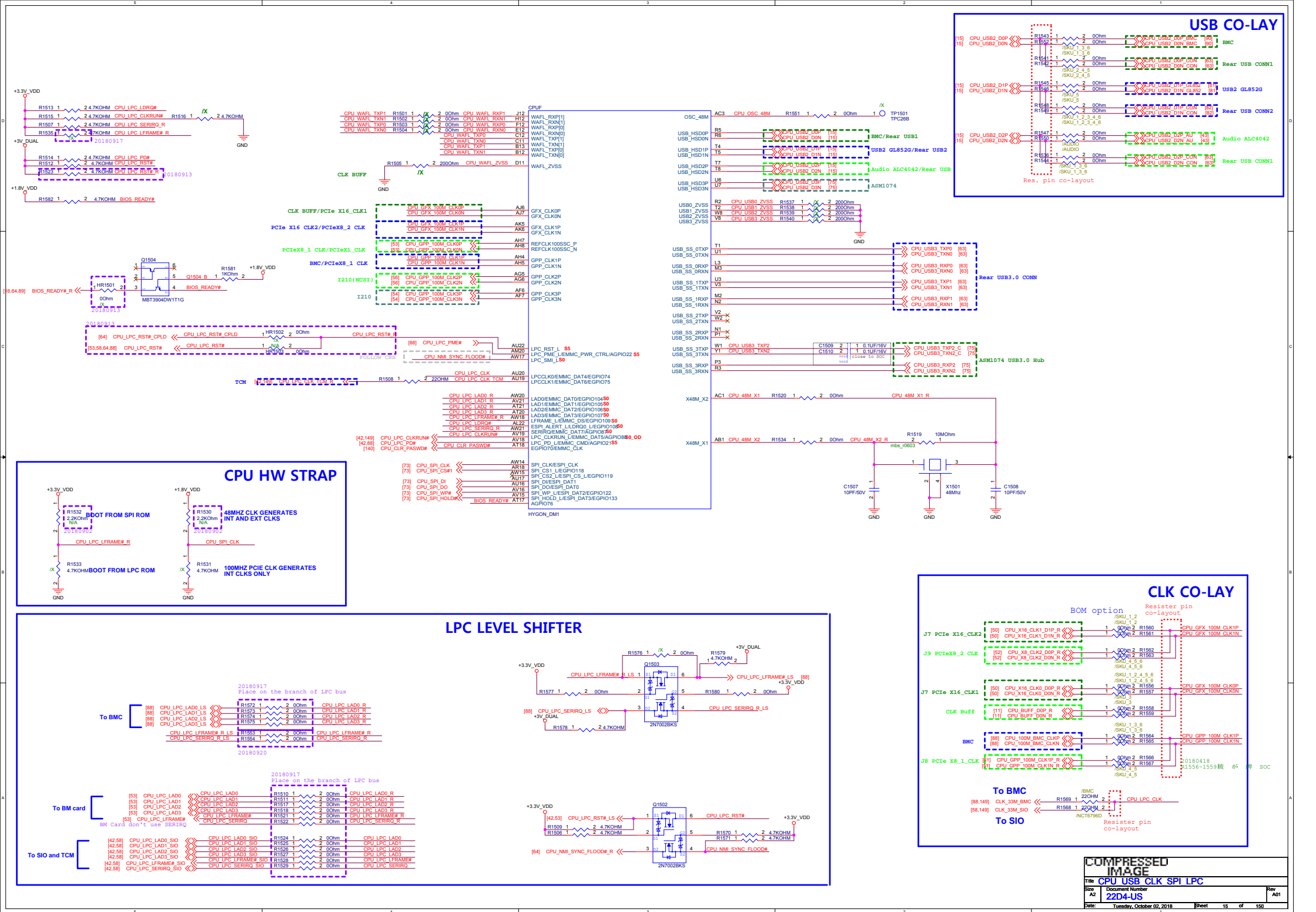
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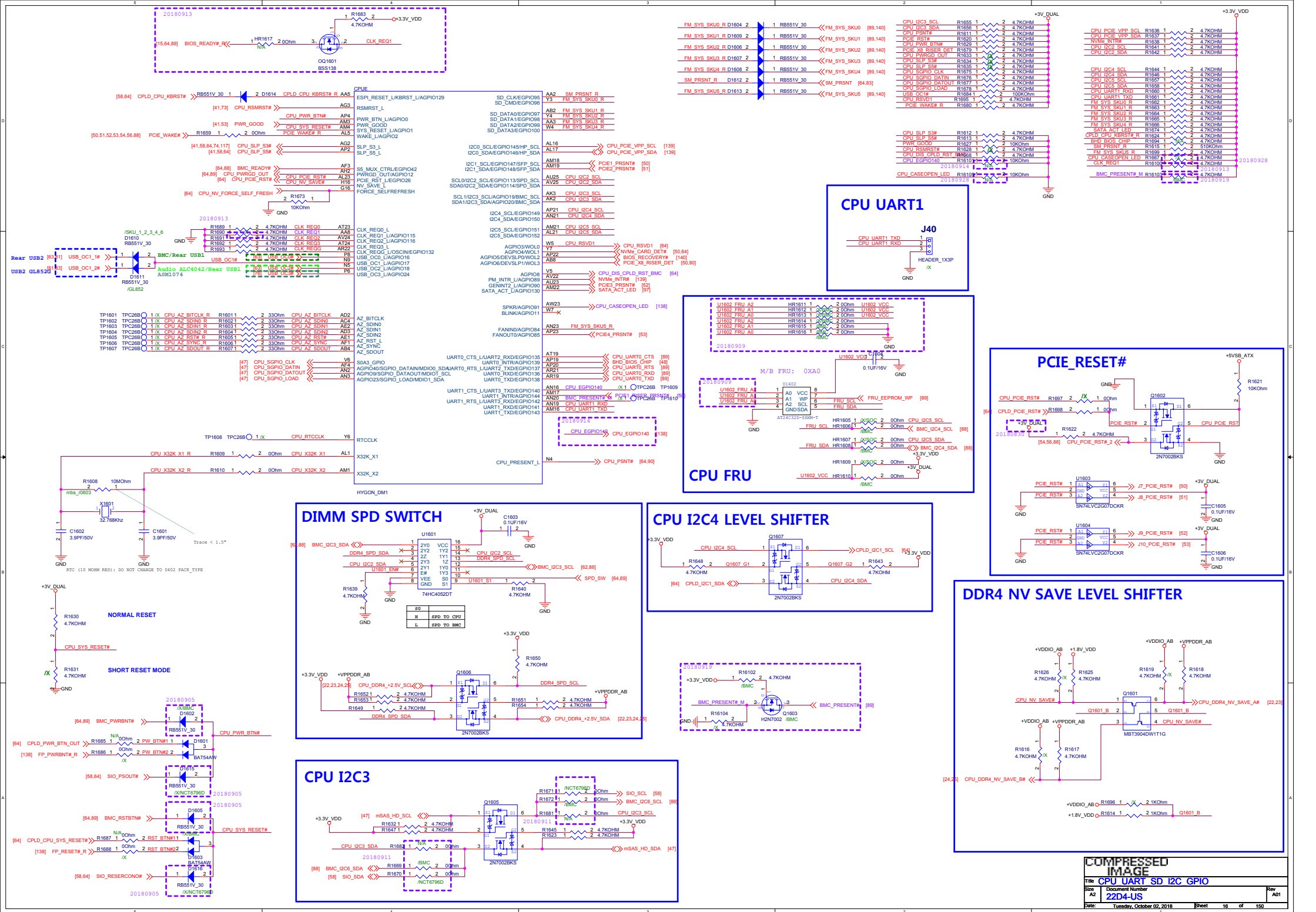


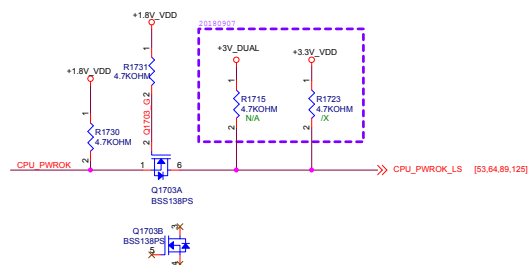
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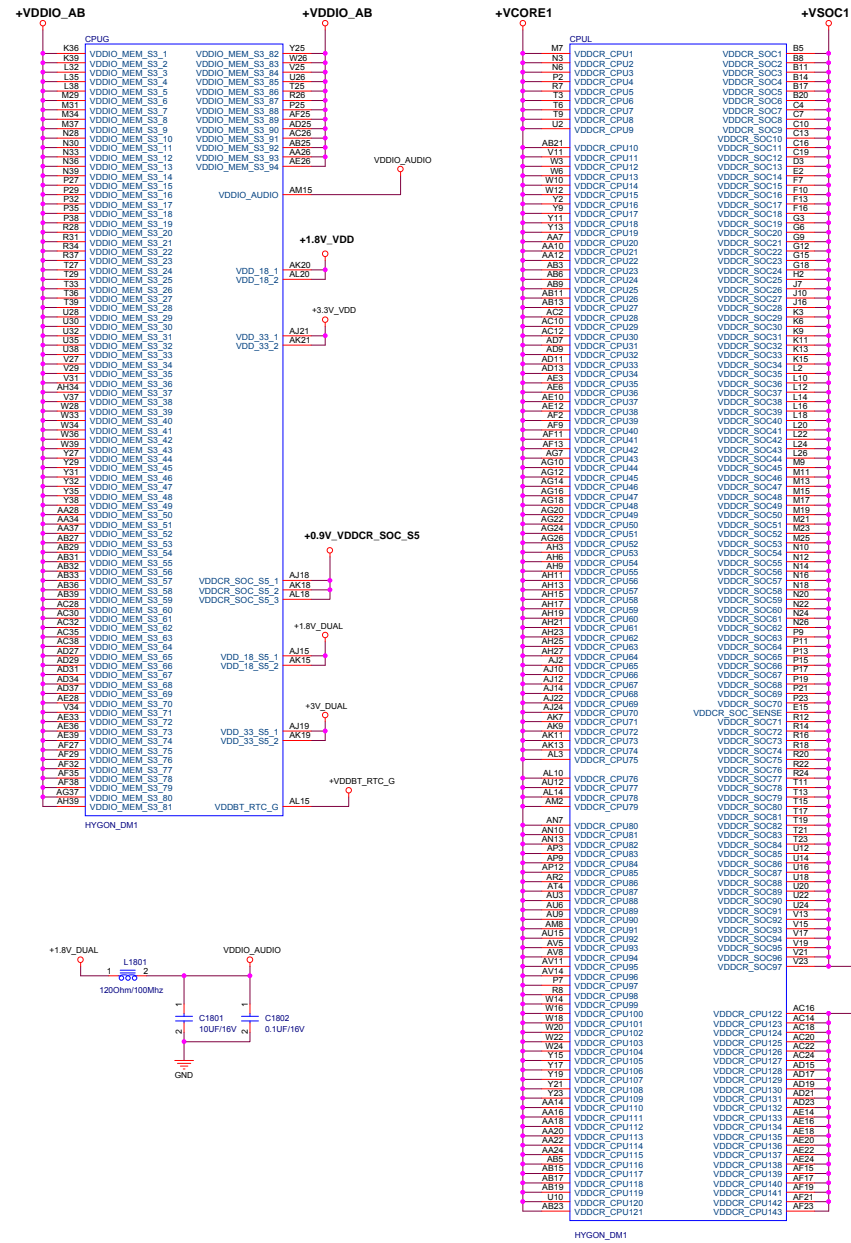


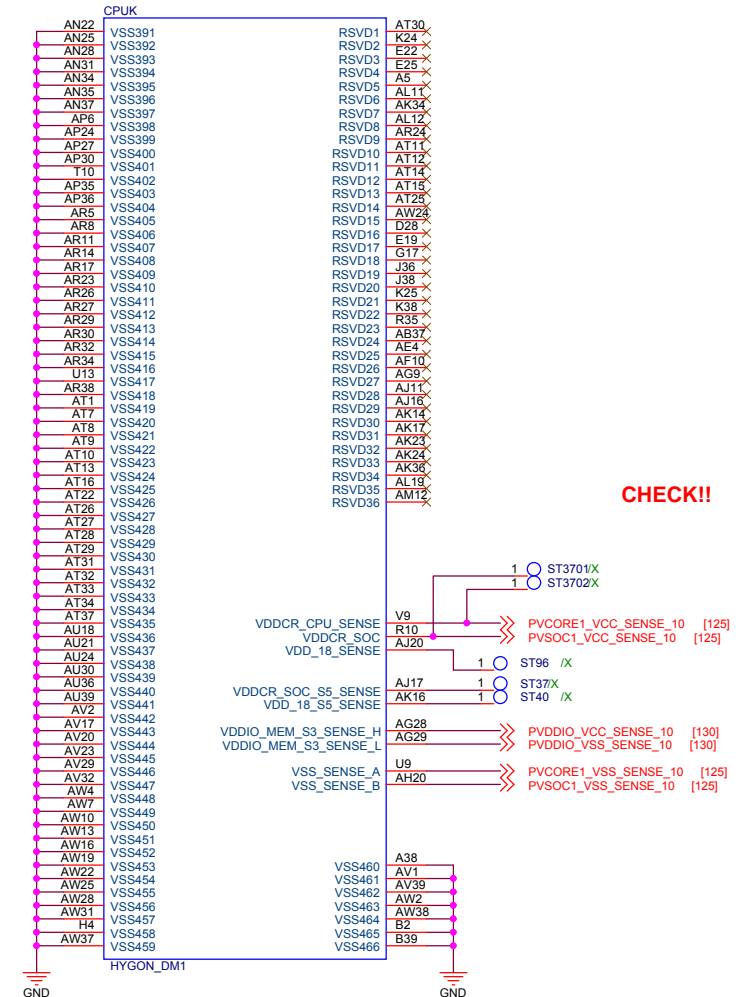
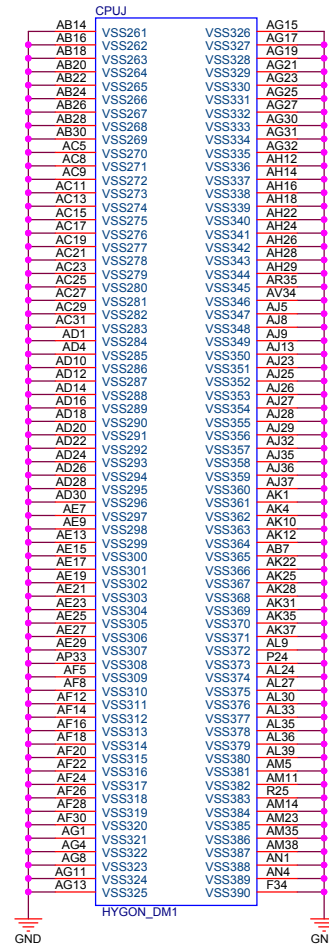
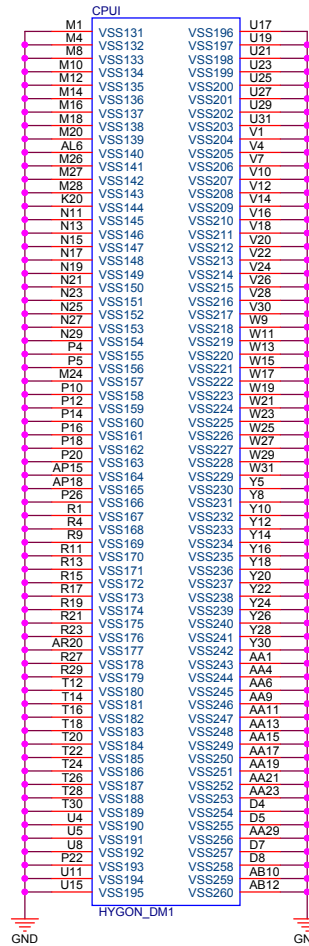
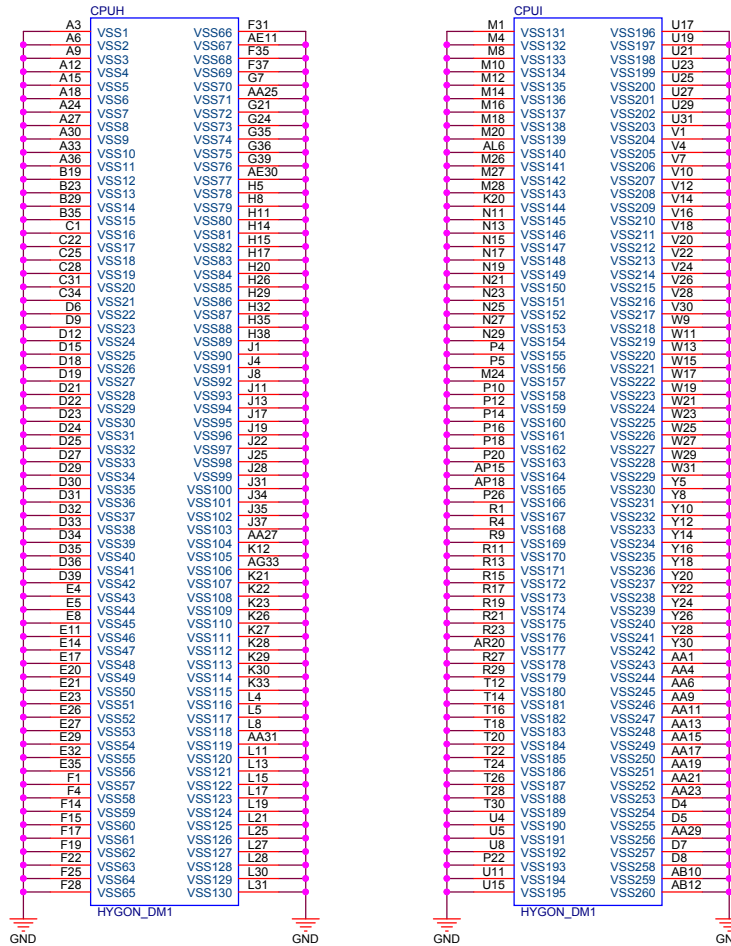




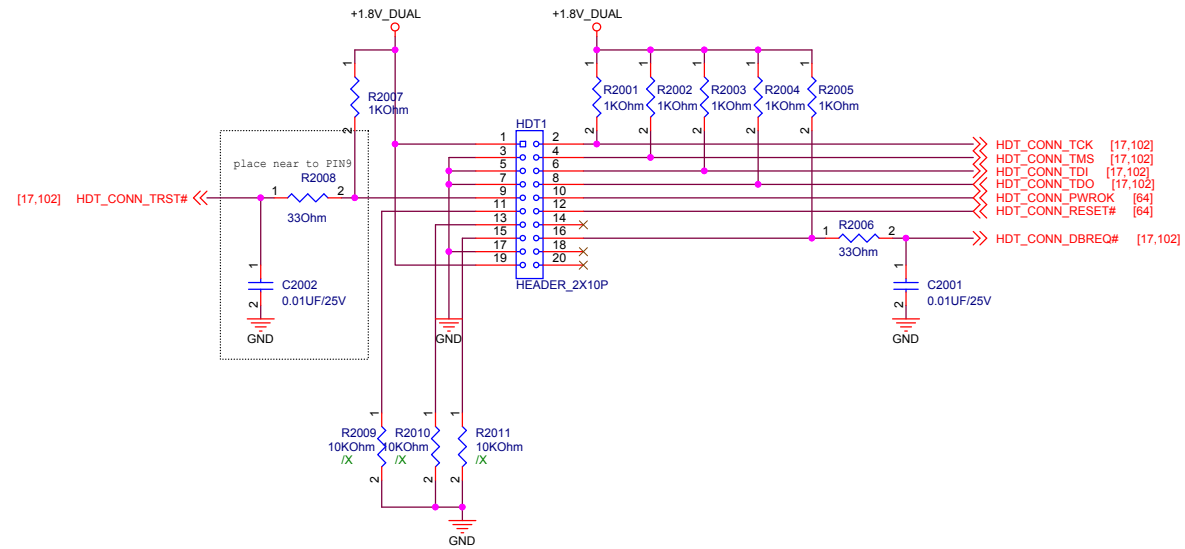








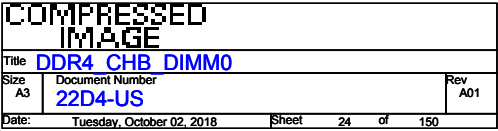
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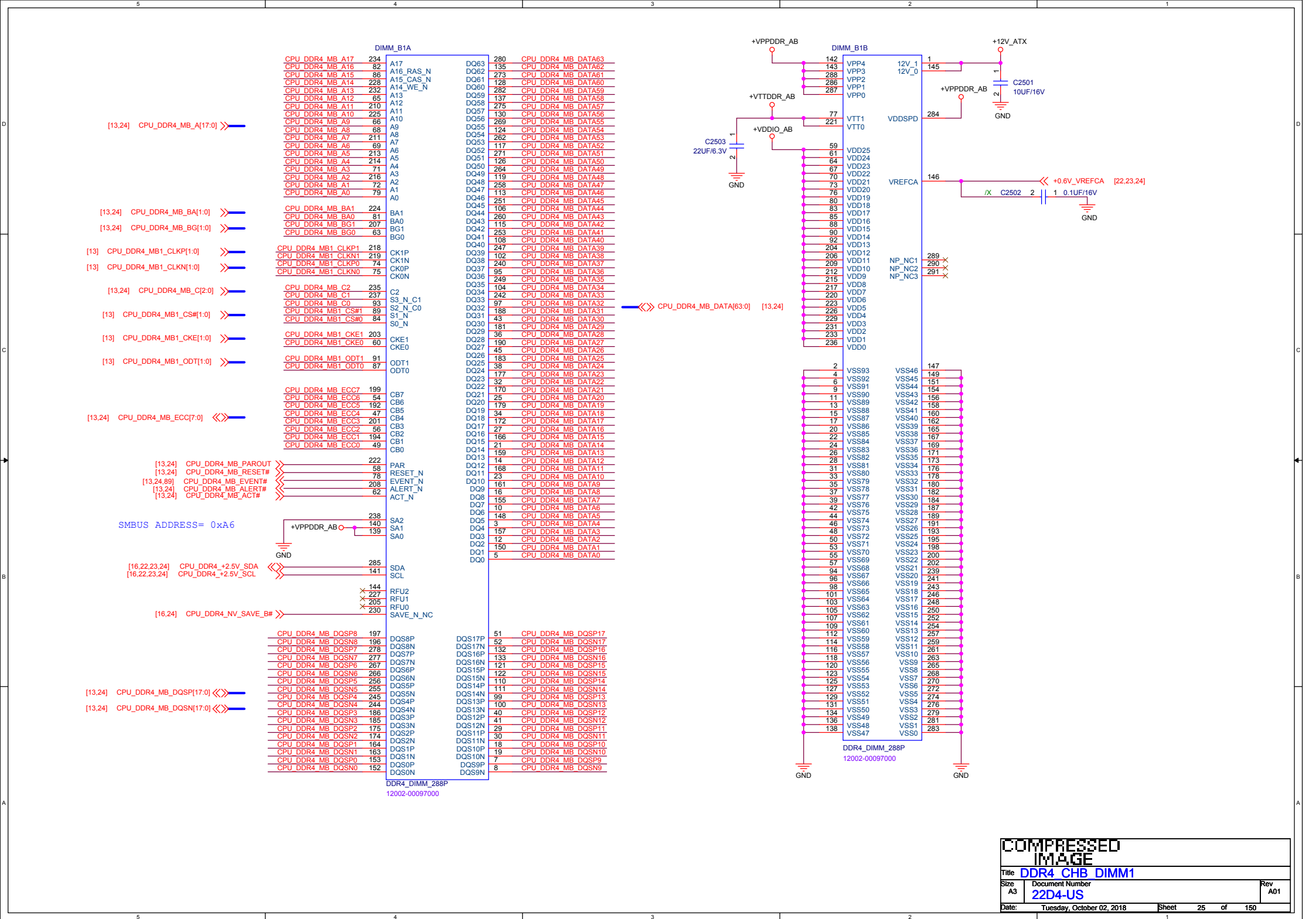




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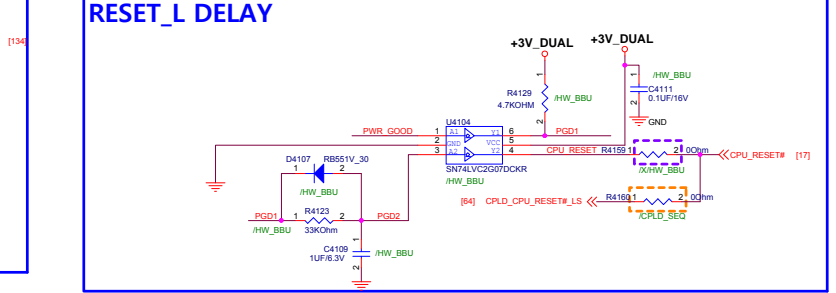
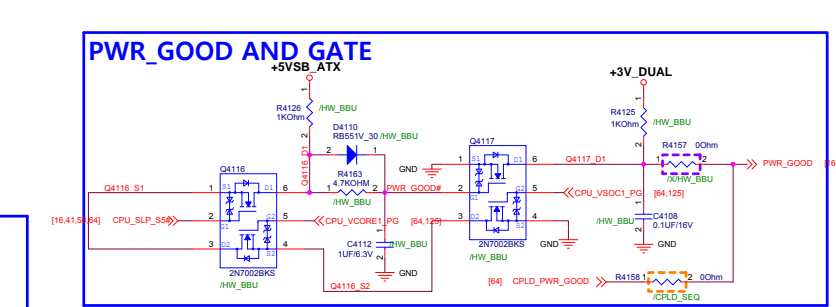
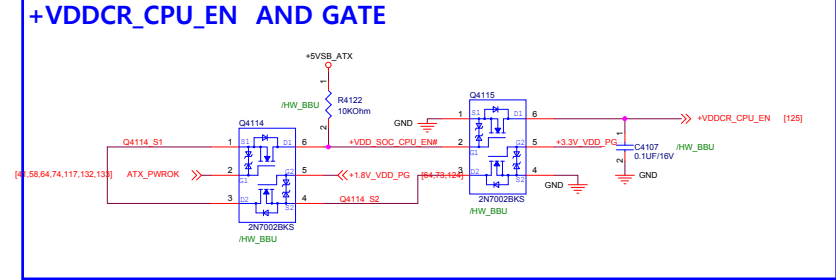
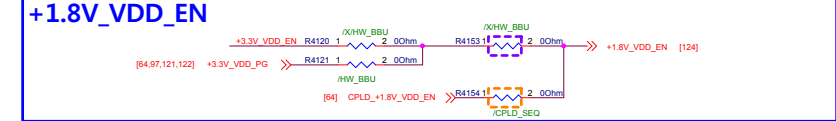
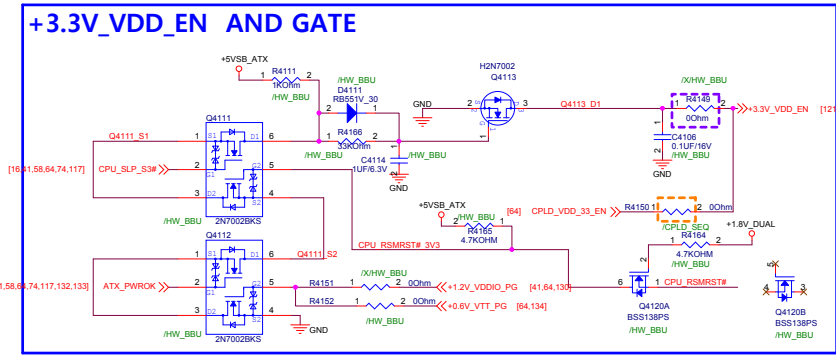
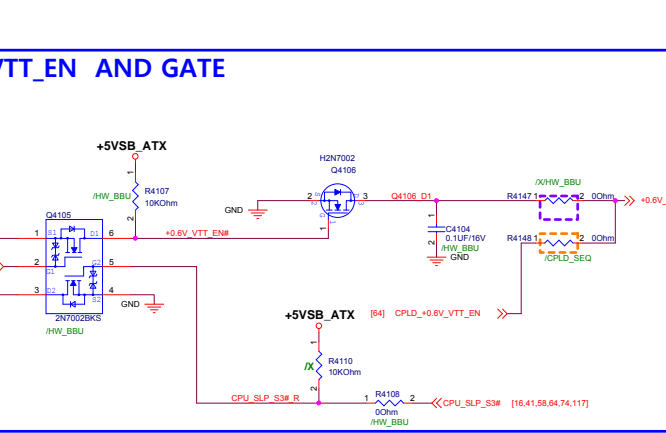
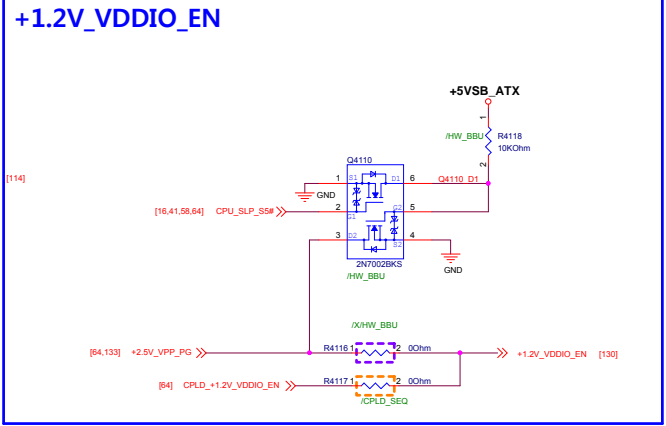
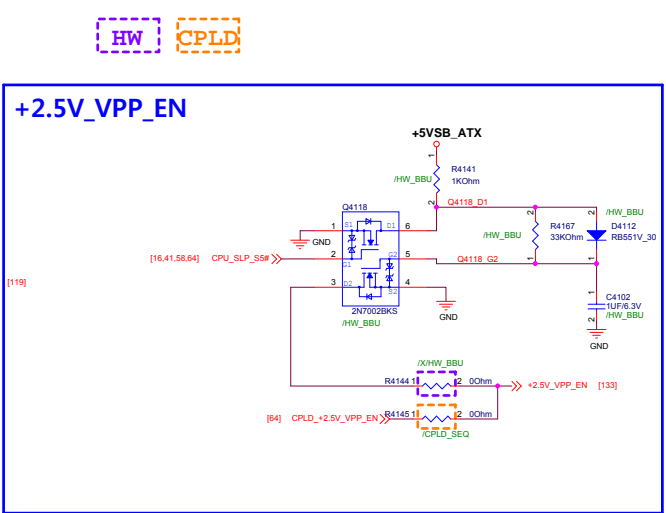
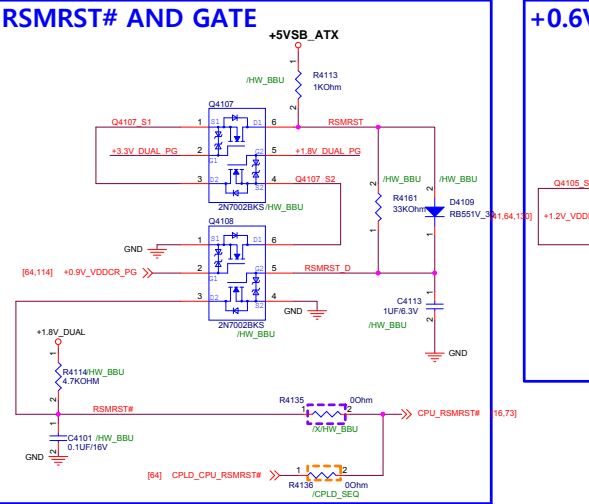
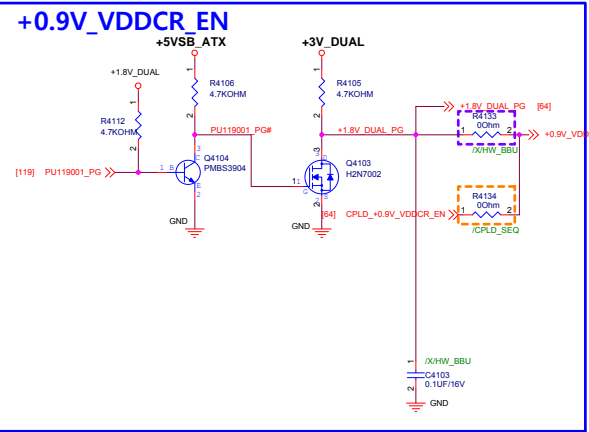
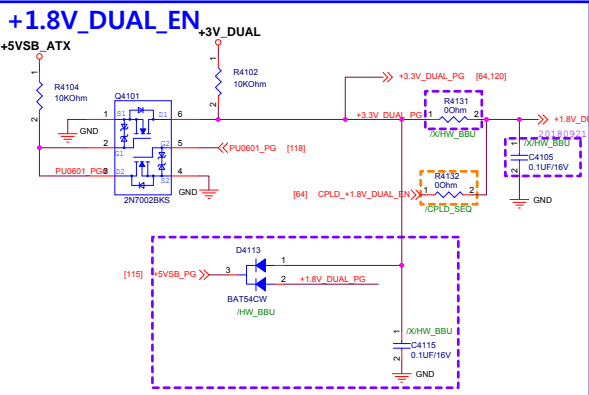
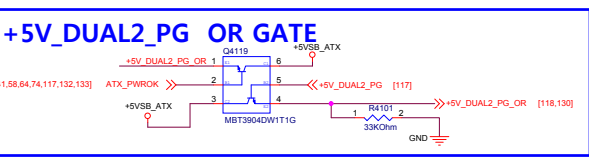
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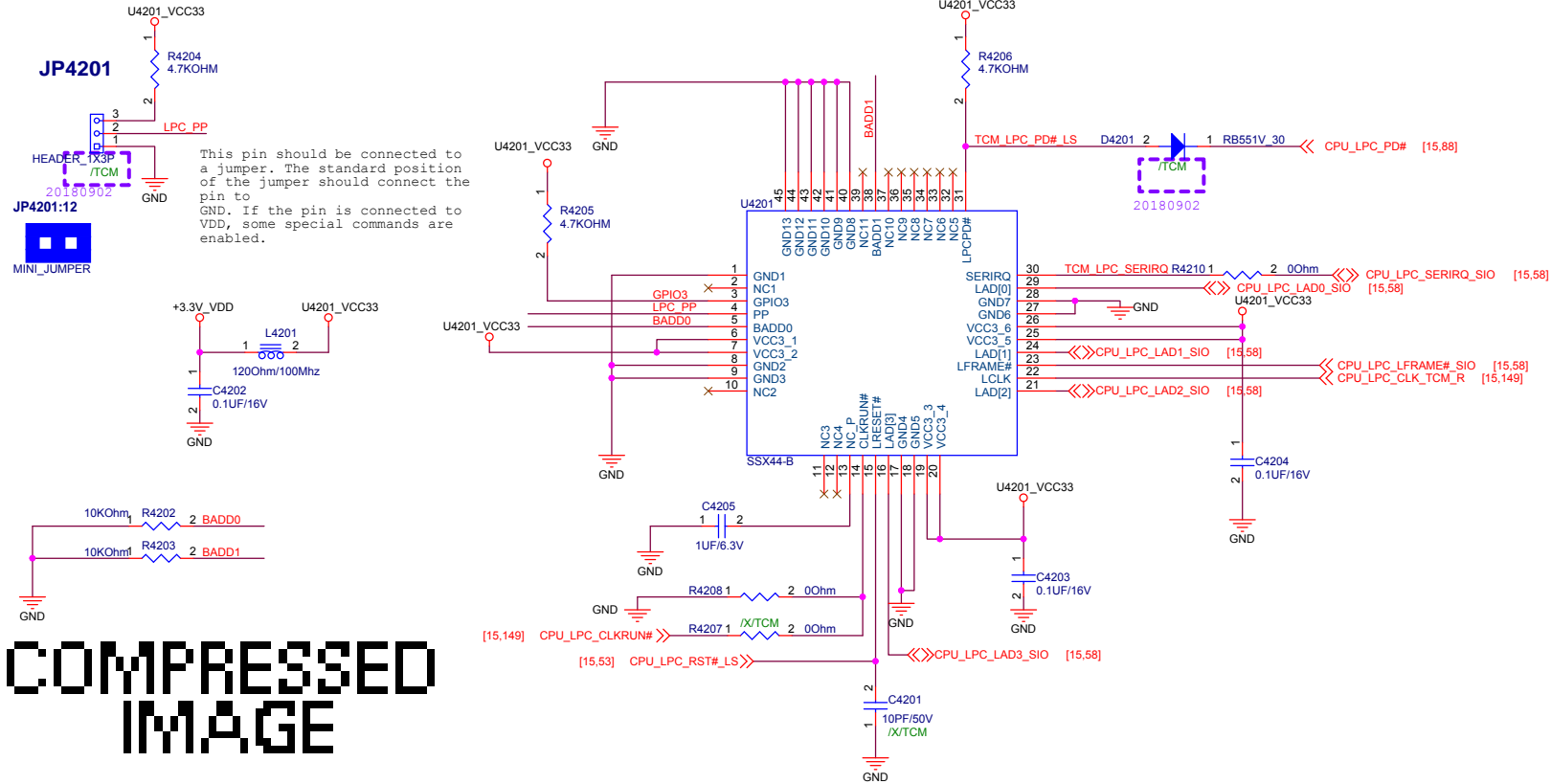
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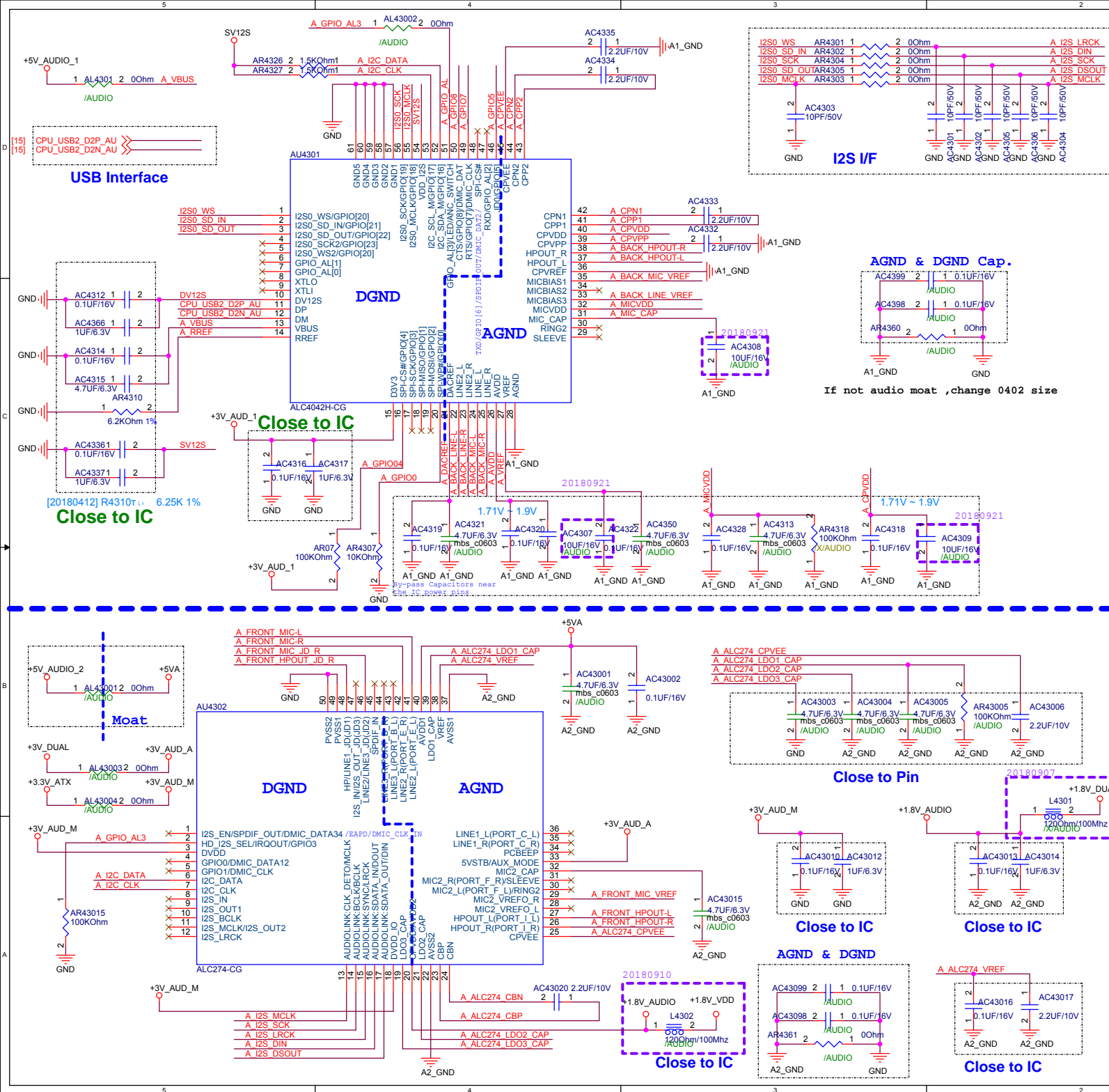


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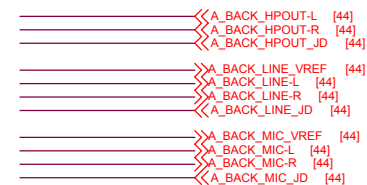
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Title TCM SSX44-B			
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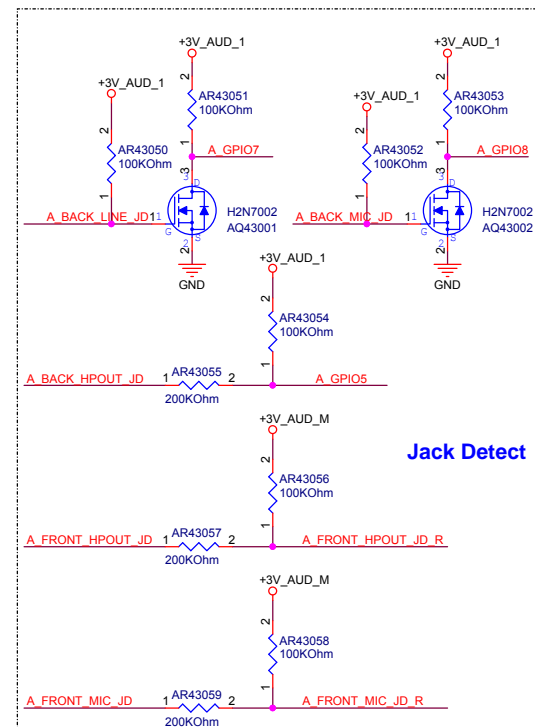
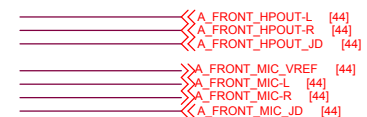


Front / Back	Function	Source
Front Panel IN1	MIC_IN2	ALC274
Front Panel OUT1	HPOUT2	ALC274
Back Panel Jack1	MIC_IN1	ALC4042H
Back Panel Jack2	HPOUT1	ALC4042H
Back Panel Jack3	LINE_IN	ALC4042H

To BACK AUDIO Jack



To FRONT AUDIO Header



Jack Detect

COMPRESSED
IMAGE

Title **AUDIO ALC4042+ALC274**

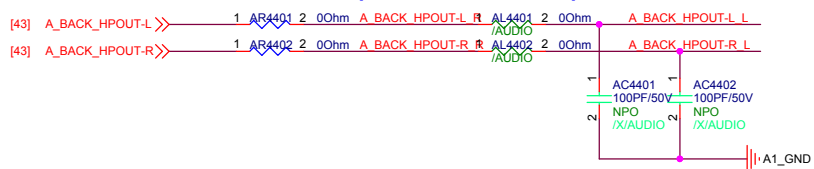
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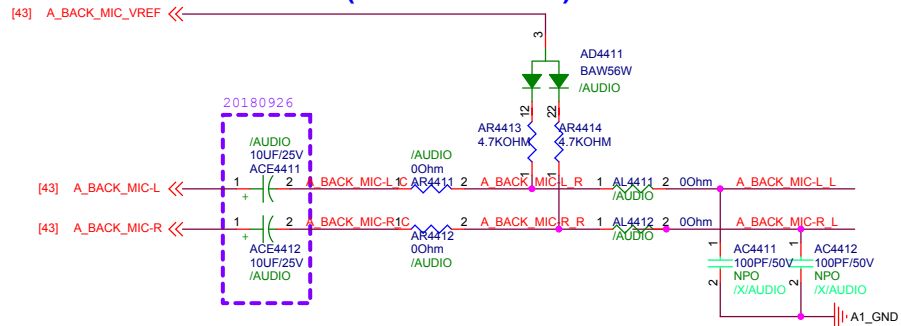
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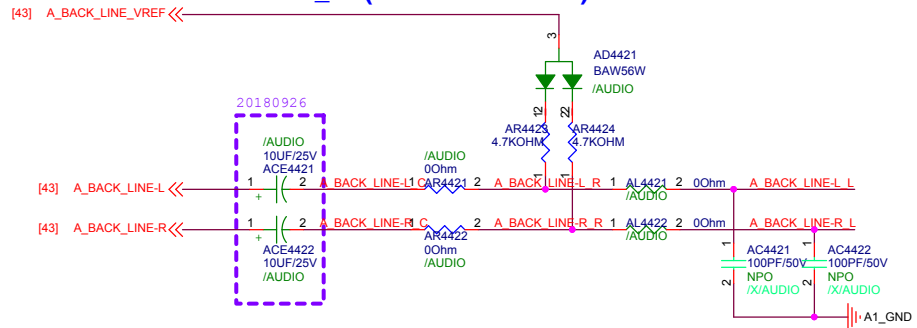
Back HPOUT (From ALC4042H)



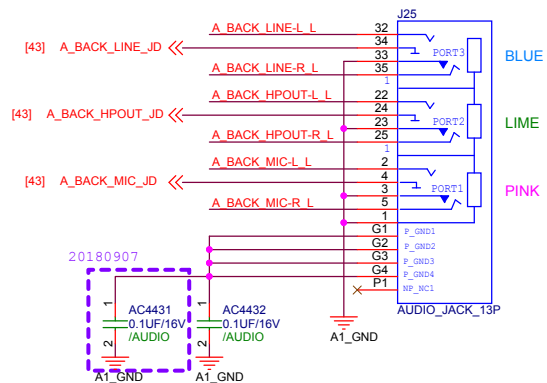
Back MIC-IN (From ALC4042H)



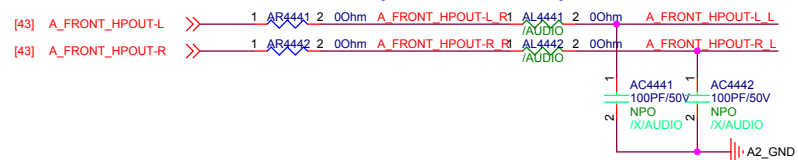
Back LINE IN (From ALC4042H)



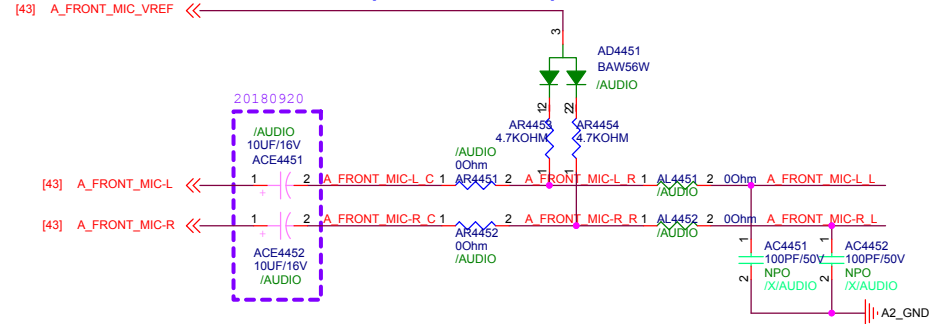
125 AUDIO JACK



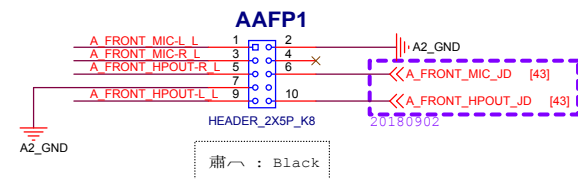
Front HPOUT (From ALC274)



Front MIC-IN (From ALC274)



AUDIO FRONT Panel (Header)



COMPRESSED
IMAGE

Title **AUDIO_BACK+FRONT Conn.**

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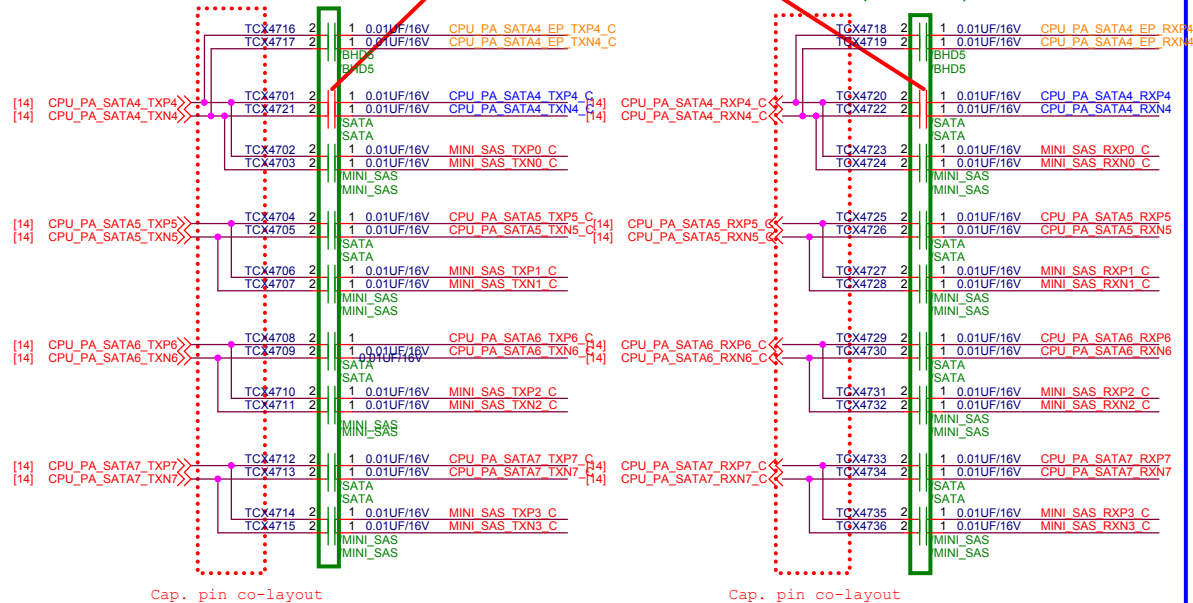
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Part NO change to resistor

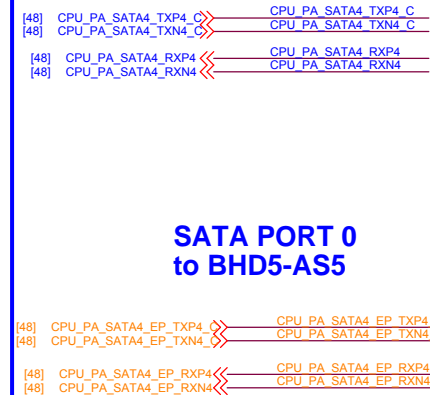
SATA & MINI SAS BOM Option

(vioid)

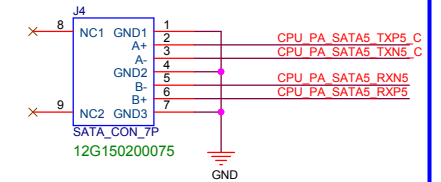
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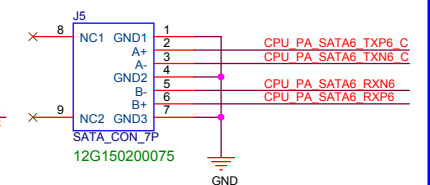
SATA PORT 0



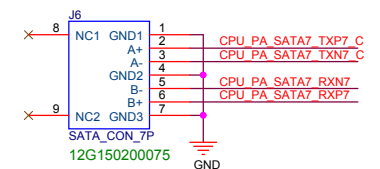
J4 SATA PORT 1



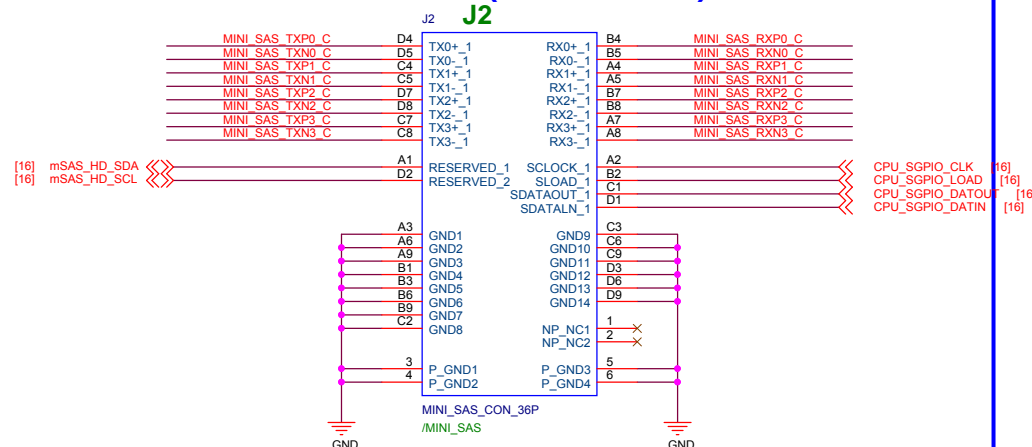
J5 SATA PORT 2

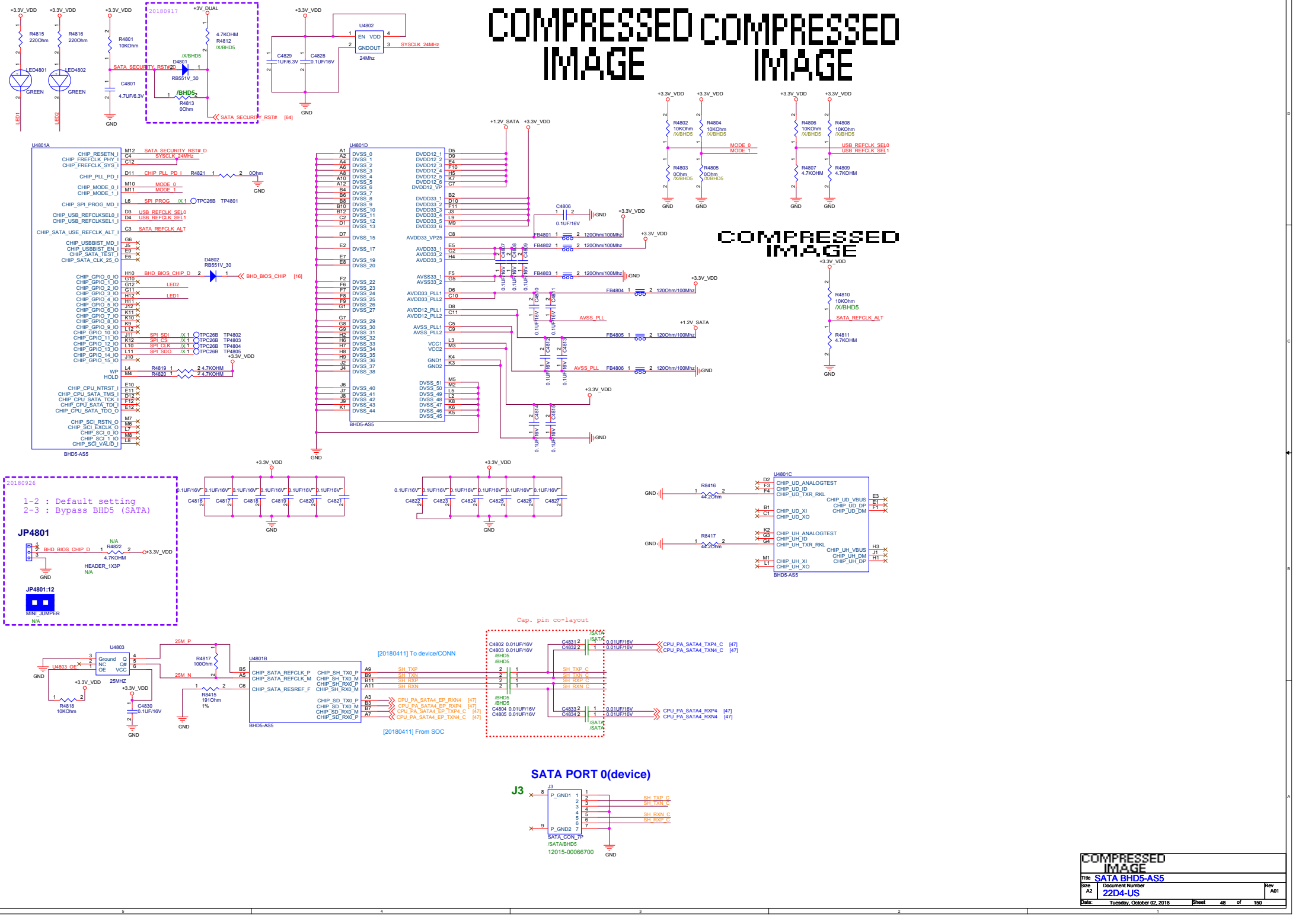


J6 SATA PORT 3



MiniAS HD (Vertical)





COMPRESSED
IMAGE

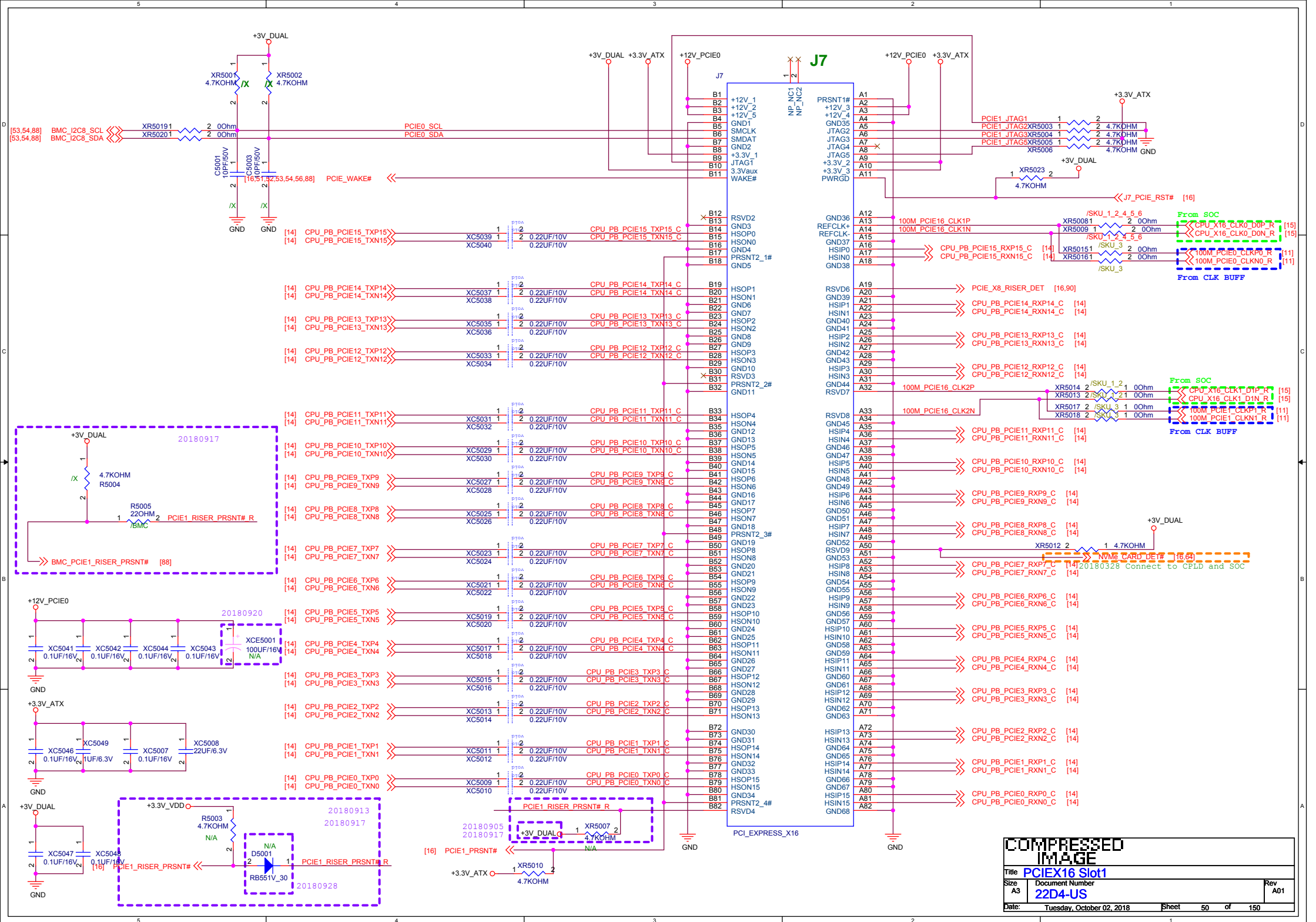
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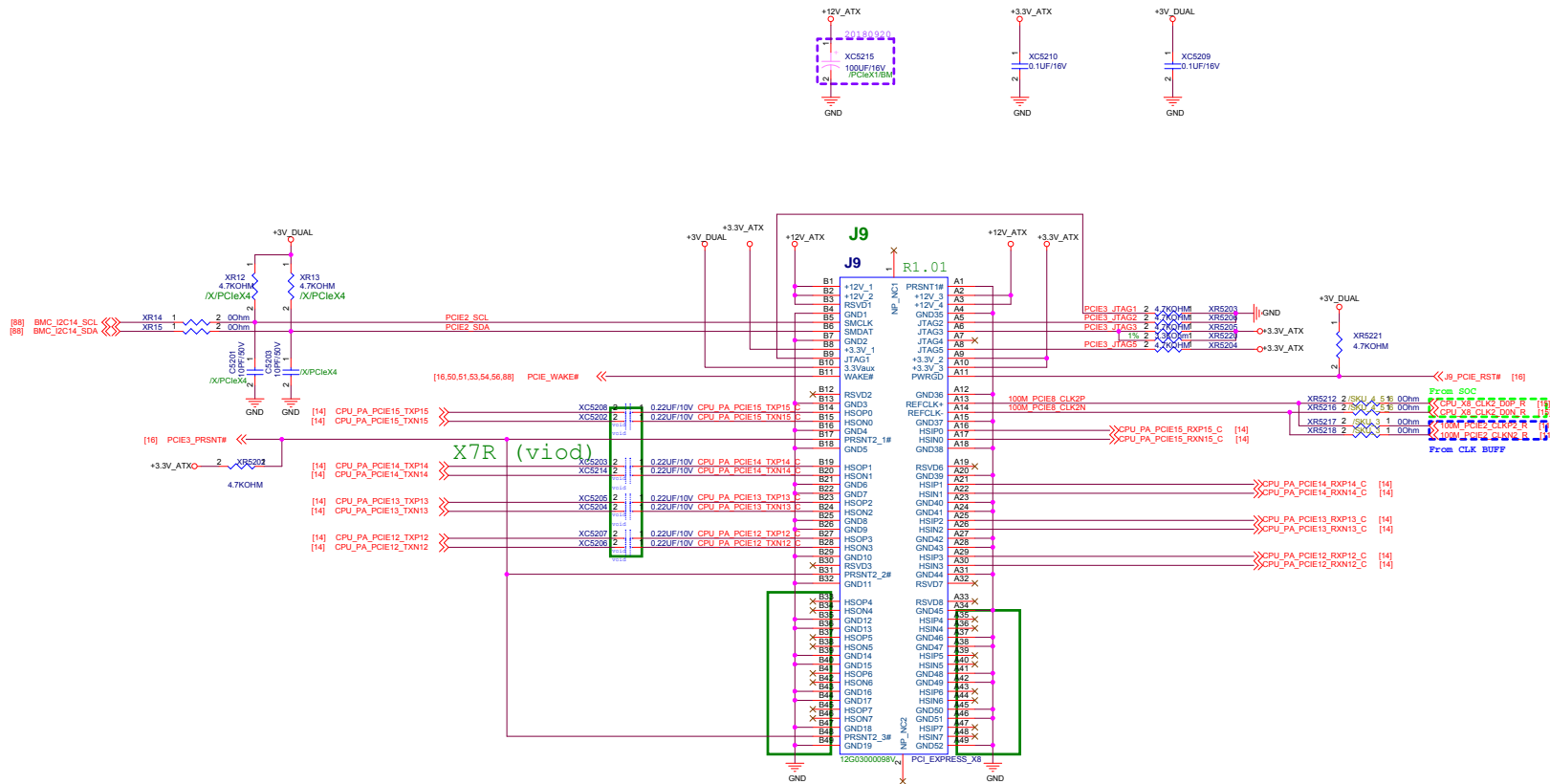
SATA PORT 0(device)

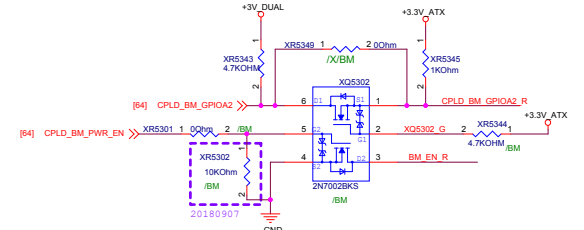
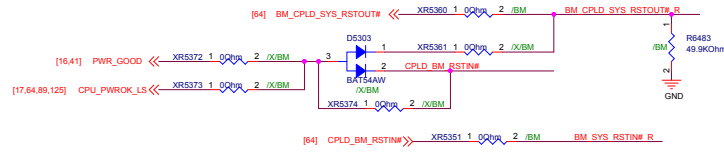
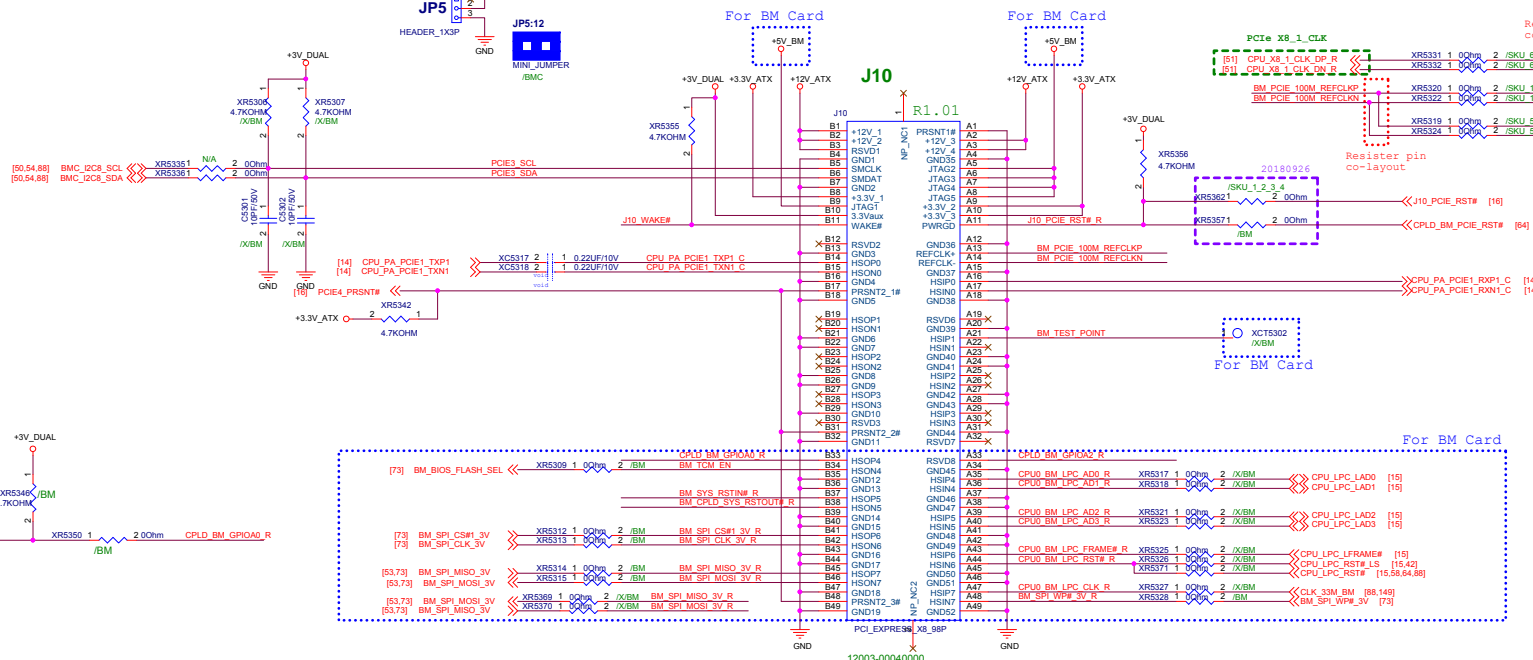
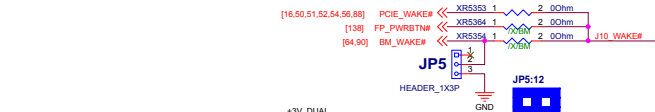
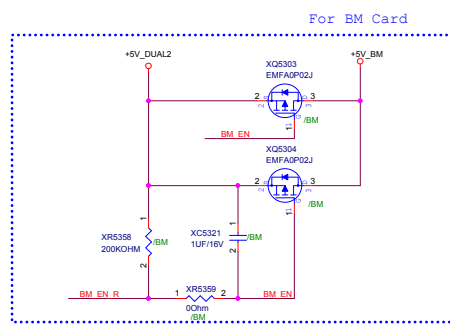
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Size	22D4-US		
Date	Tuesday, October 02, 2018	Sheet	48 of 150
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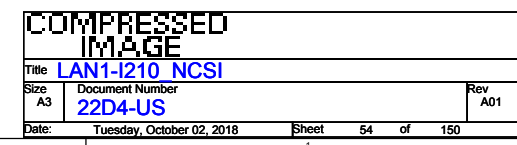


COMPRESSED IMAGE		
Title N/A		
Size A3	Document Number 22D4-US	Rev A01
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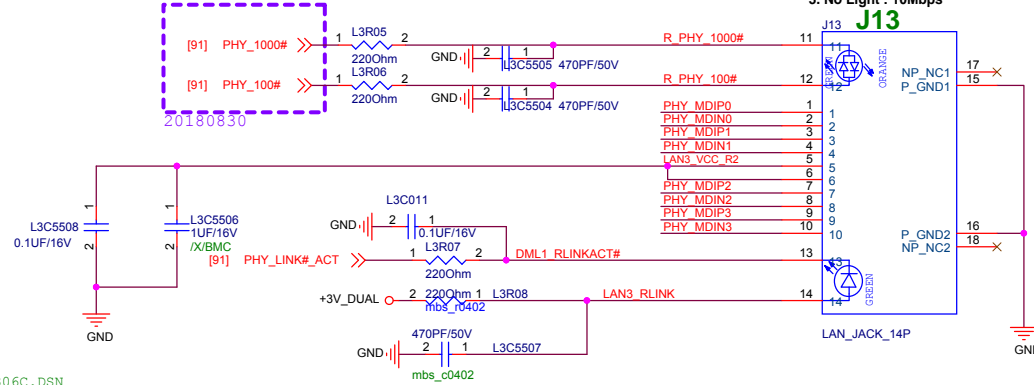






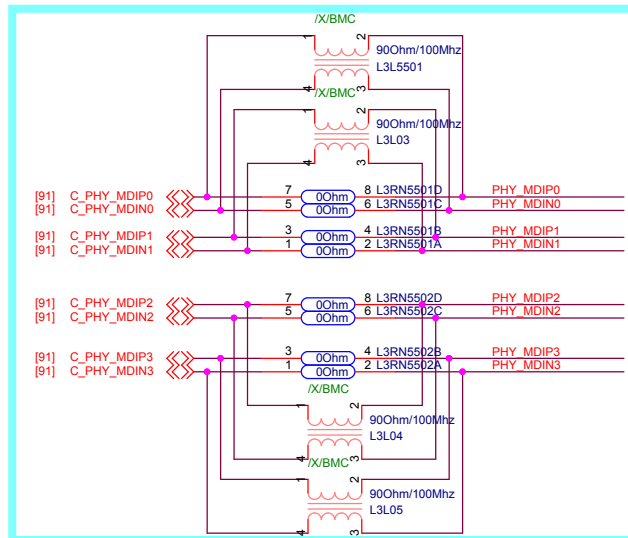
20180413 ㊟DM_LAN1_USB3_12 腹

Lan dedicate Interface



SPEED LED:
1. GREEN : 100Mbps
2. ORANGE : 1000Mbps
3. No Light : 10Mbps

20170306: 把o211PG-D24_IFX_0306C.DSN
20170306: swap for 抖結



**COMPRESSED
IMAGE**

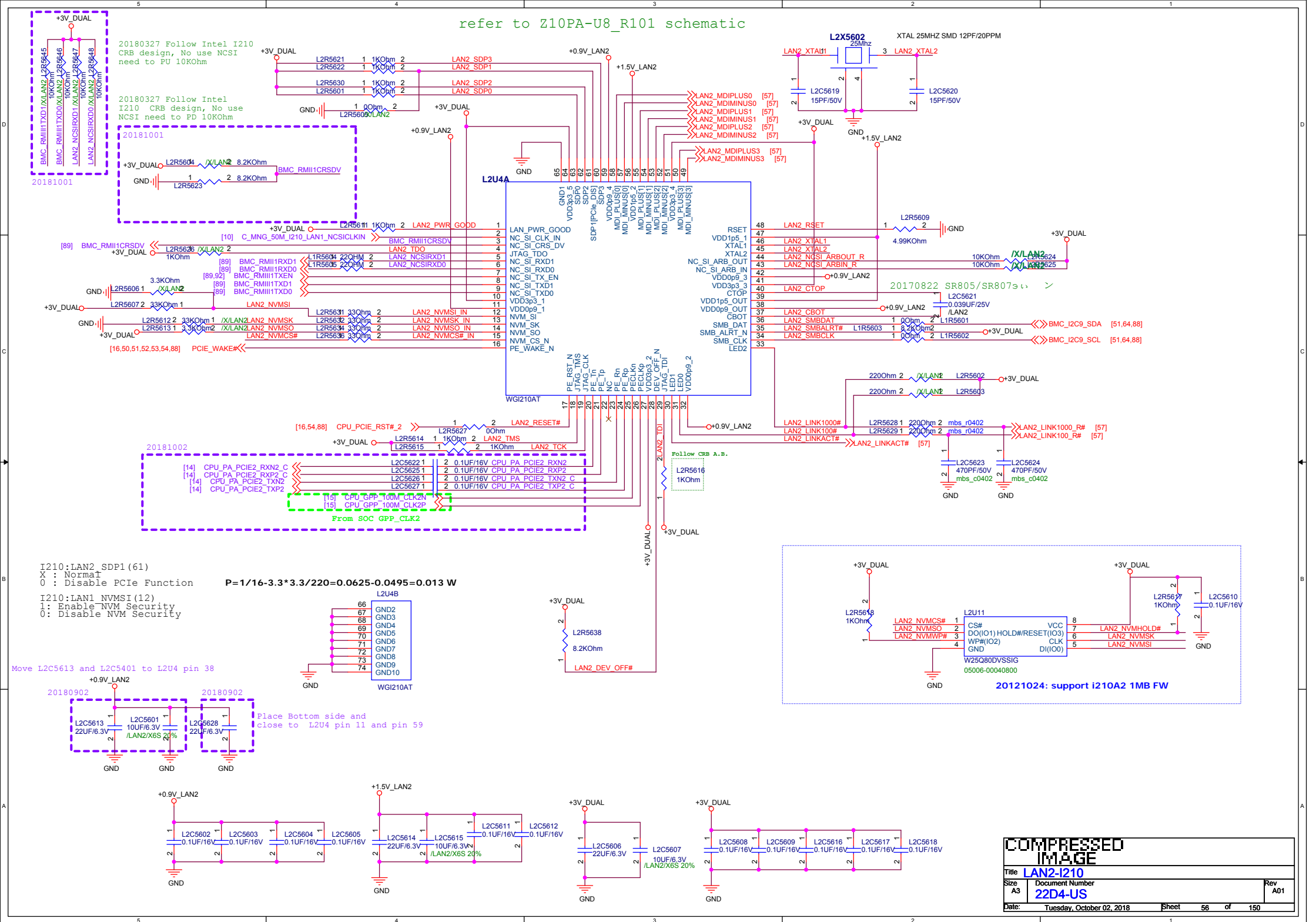
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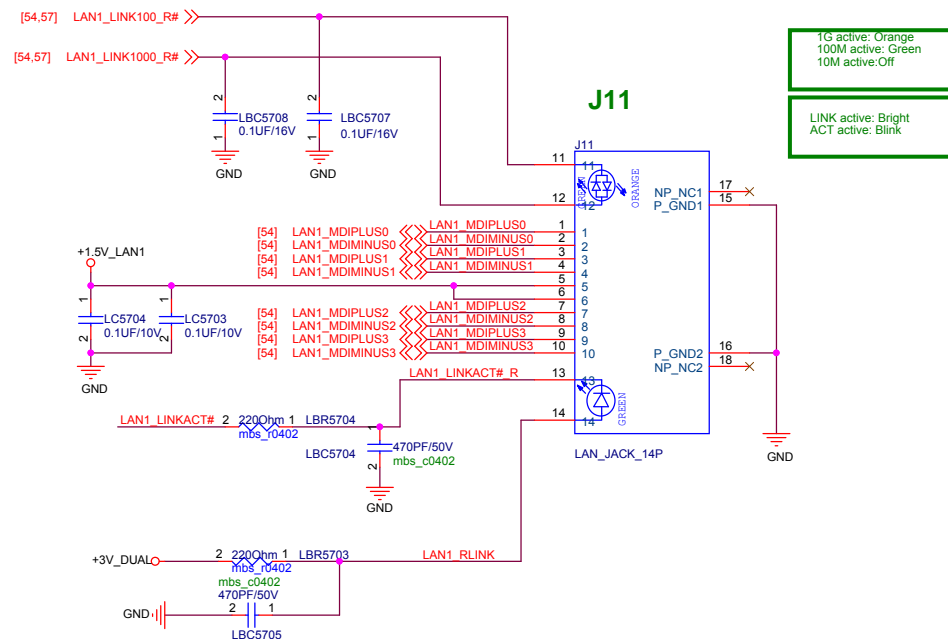
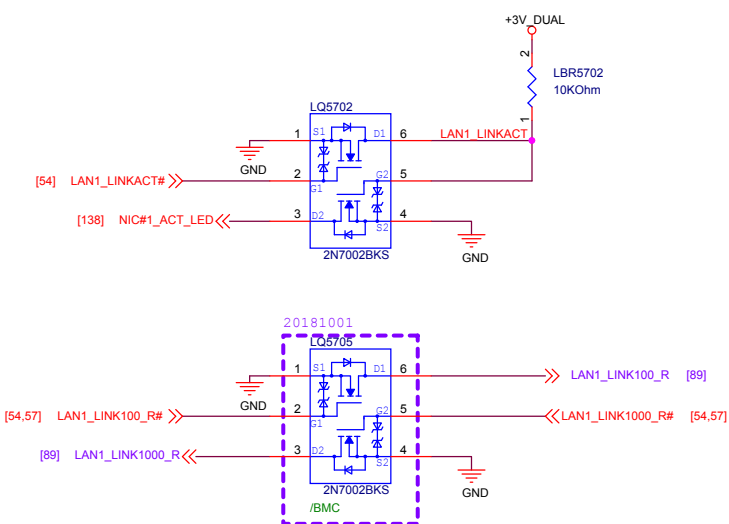
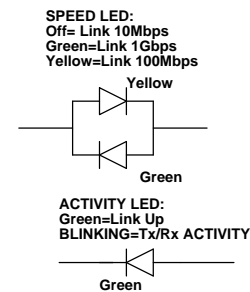
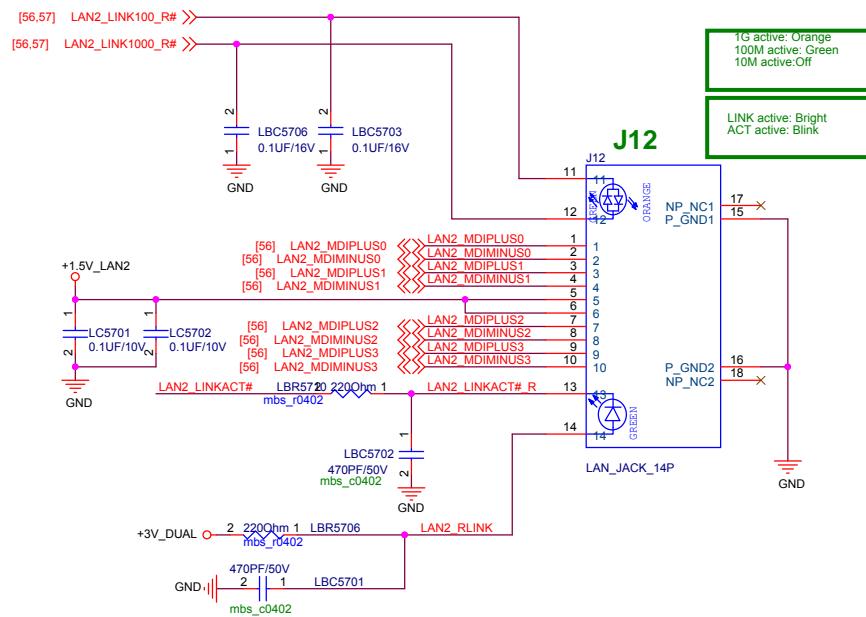
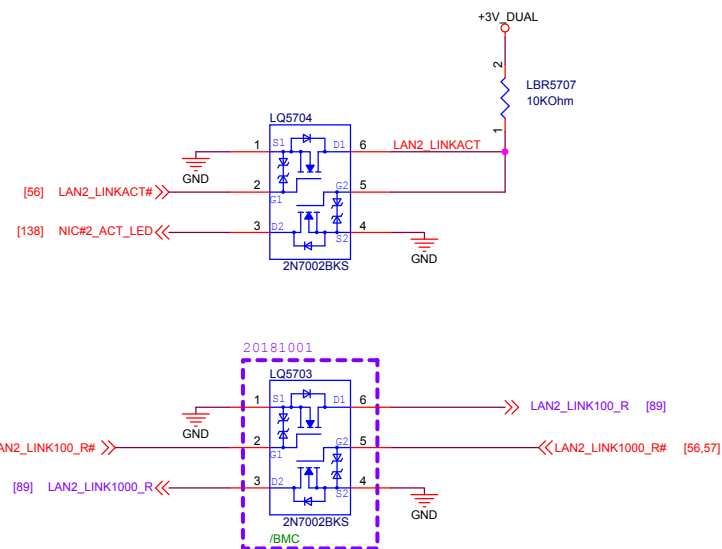
Size **A3** Document Number
22D4-US

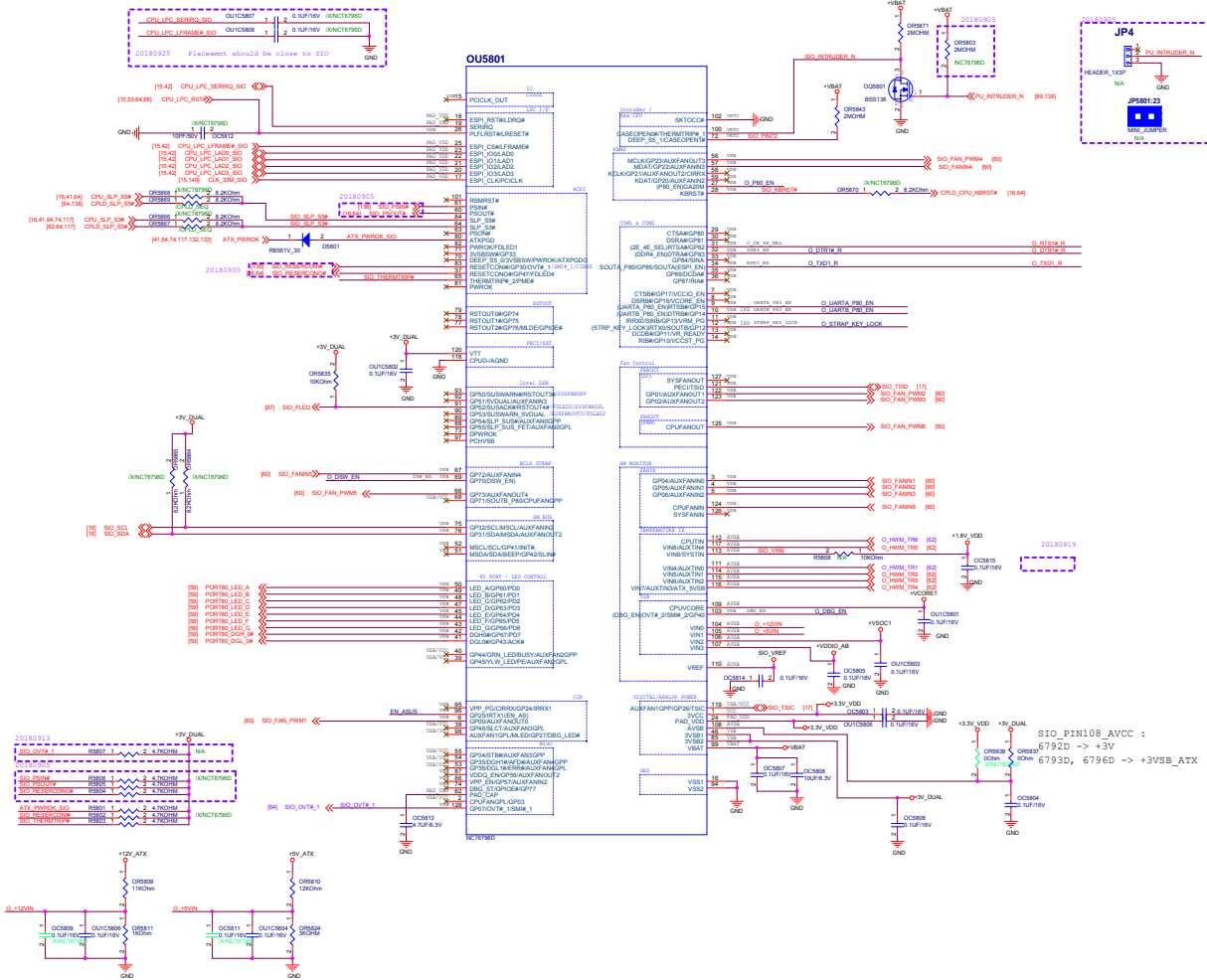
Rev
A01

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refer to Z10PA-U8_R101 schematic







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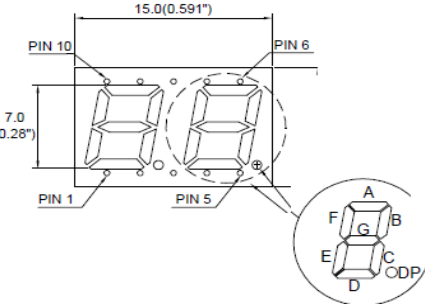
COMPRESSED
IMAGE

COMPRESSED
IMAGE

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IMAGE

Port 80 (7 Segment). SIO is common athode.

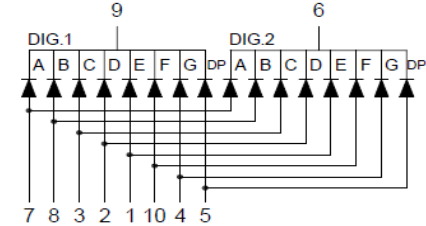
Package Dimensions



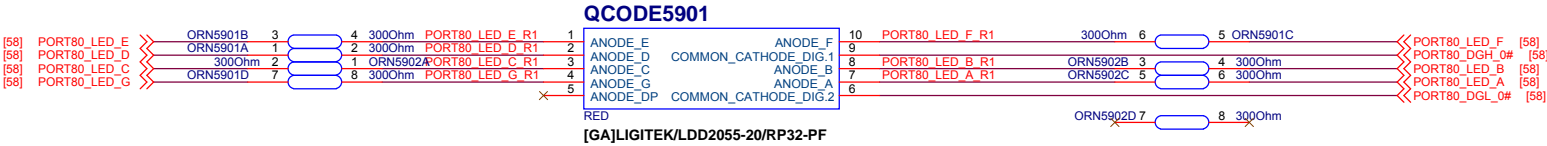
Electrical Connection

PIN NO.	LDD2055-20/RP32-PF
1	Anode E
2	Anode D
3	Anode C
4	Anode G
5	Anode DP
6	Common Cathode Dig.2
7	Anode A
8	Anode B
9	Common Cathode Dig.1
10	Anode F

Internal Circuit Diagram
LDD2055-20/RP32-PF

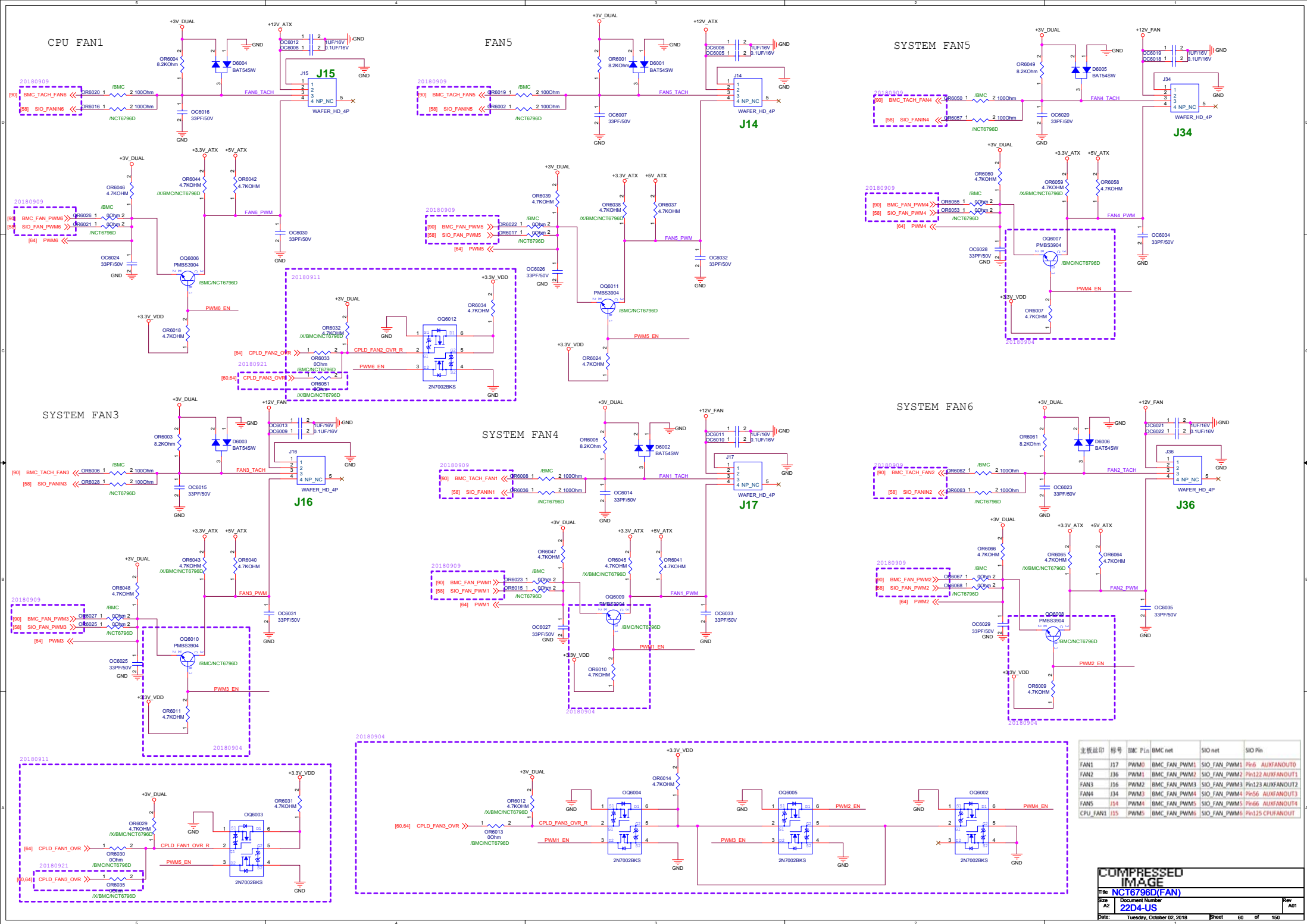


Q_CODE_low byte



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IMAGE

Title	NCT6796D(PORT 80 LED)		
Size	Document Number	Rev	
A3	22D4-US	A01	
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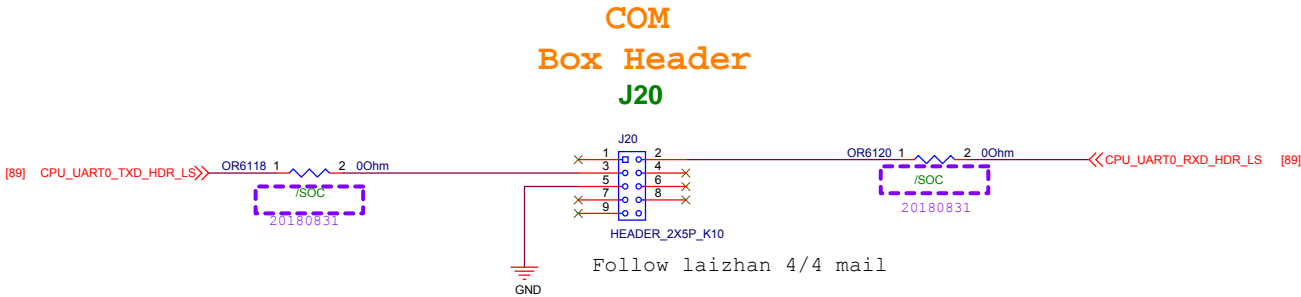
主板丝印	标号	BMC Pin	BMC net	SIO net	SIO Pin
FAN1	J17	PWM0	BMC_FAN_PWM1	SIO_FAN_PWM1	Pin6 AUXFANOUT0
FAN2	J36	PWM1	BMC_FAN_PWM2	SIO_FAN_PWM2	Pin122 AUXFANOUT1
FAN3	J16	PWM2	BMC_FAN_PWM3	SIO_FAN_PWM3	Pin123 AUXFANOUT2
FAN4	J34	PWM3	BMC_FAN_PWM4	SIO_FAN_PWM4	Pin66 AUXFANOUT3
FAN5	J14	PWM4	BMC_FAN_PWM5	SIO_FAN_PWM5	Pin66 AUXFANOUT4
CPU_FAN1	J15	PWM5	BMC_FAN_PWM6	SIO_FAN_PWM6	Pin125 CPUFANOUT

COMPRESSED IMAGE

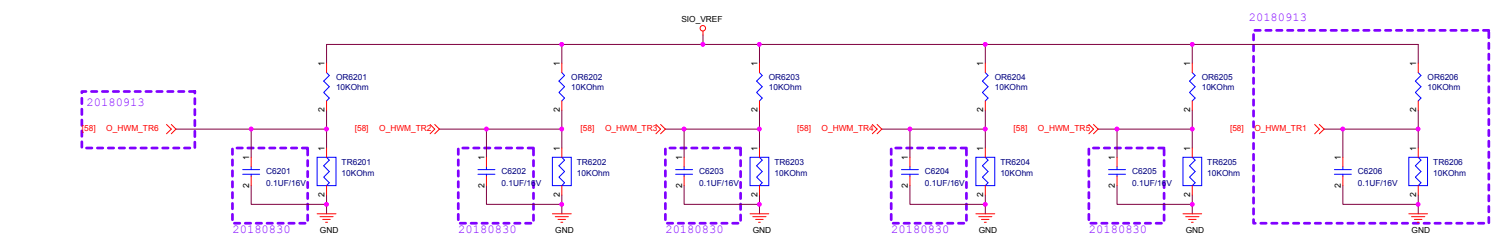
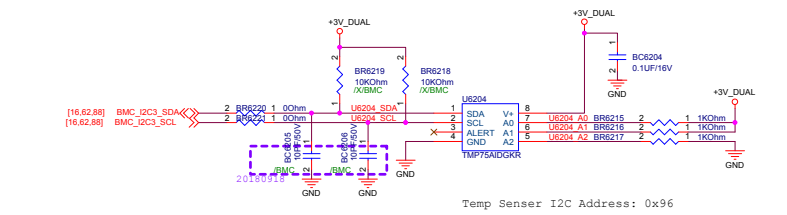
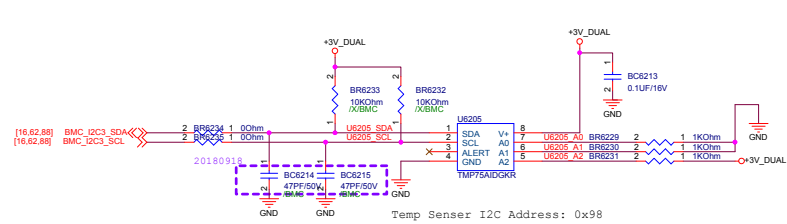
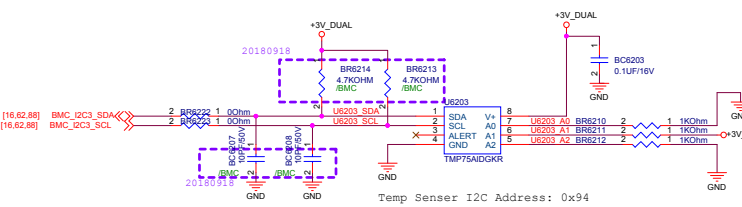
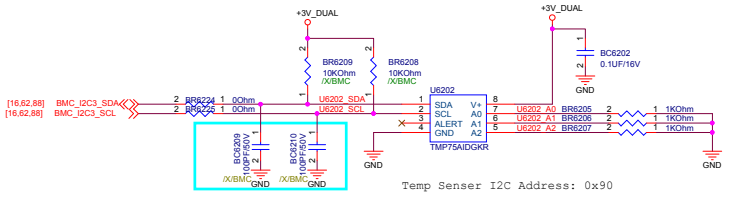
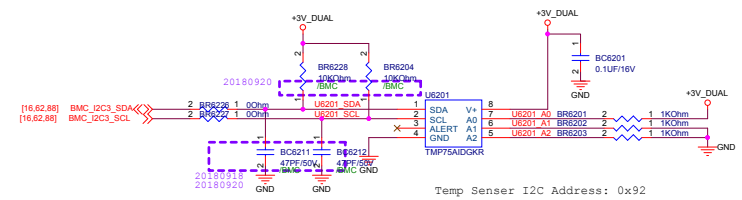
Time: NCT6796D(FAN)
Size: 22D4-US
Date: Tuesday, October 02, 2018
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COM 1



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Size A3	Document Number 22D4-US	Rev A01
Date: Tuesday, October 02, 2018	Sheet 61 of 150	

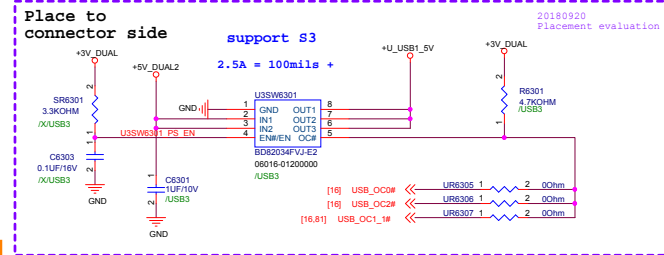
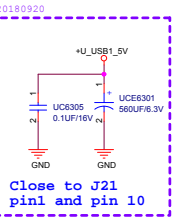
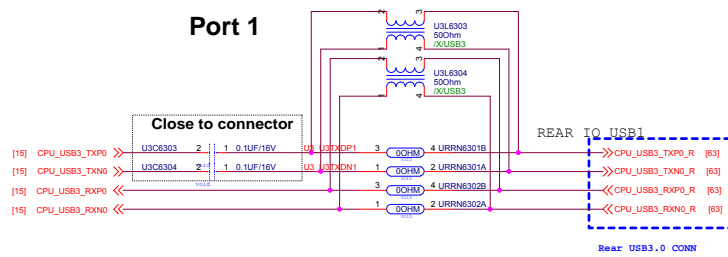


location5: address 0x98 change to 0x9E

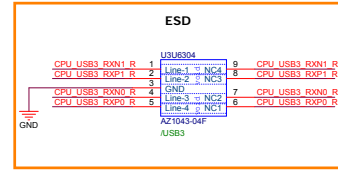
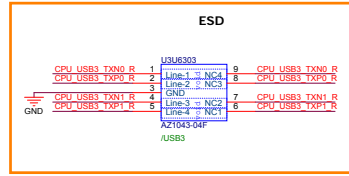
A2	A1	A0	SLAVE ADDRESS	
0	0	0	1001000	0x90
0	0	1	1001001	0x92
0	1	0	1001010	0x94
0	1	1	1001011	0x96
1	0	0	1001100	0x98
1	0	1	1001101	0x9A
1	1	0	1001110	0x9C
1	1	1	1001111	

Table 12. Address Pins and Slave Addresses for the TMP75

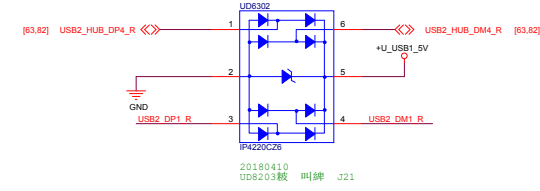
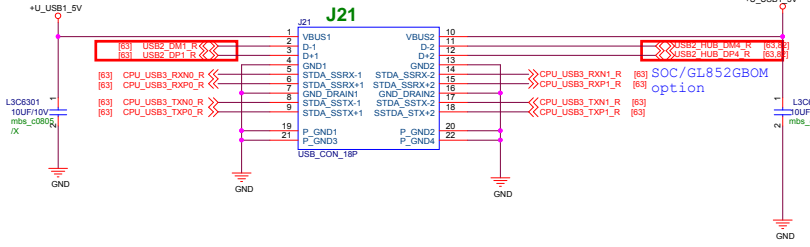
Port 1



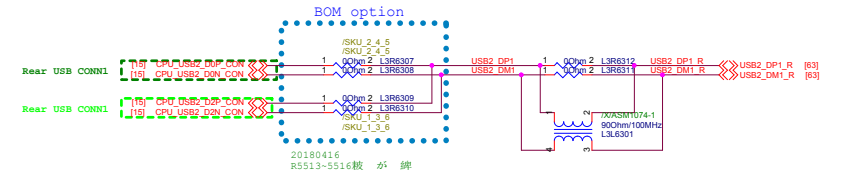
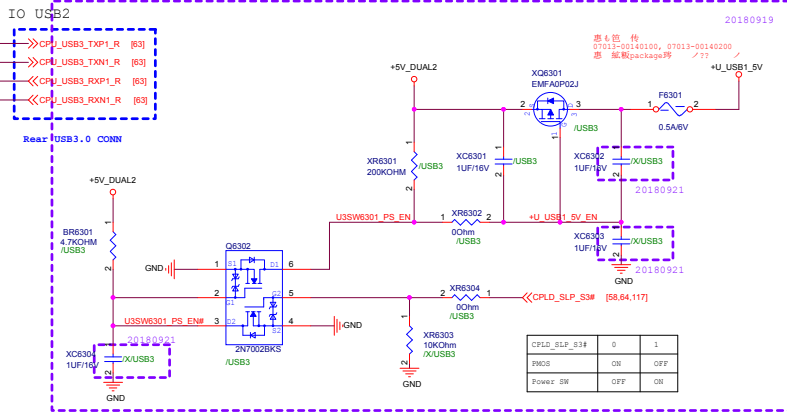
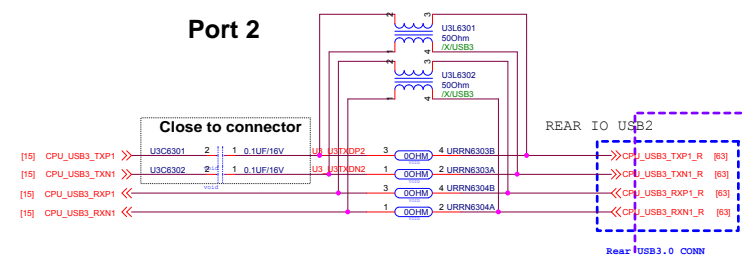
PCH USB3.0
1. 900 mA for each port
2. two port for one OCH & VBUS PWR
3. make sure connector VBUS PWR netname



USB Interface

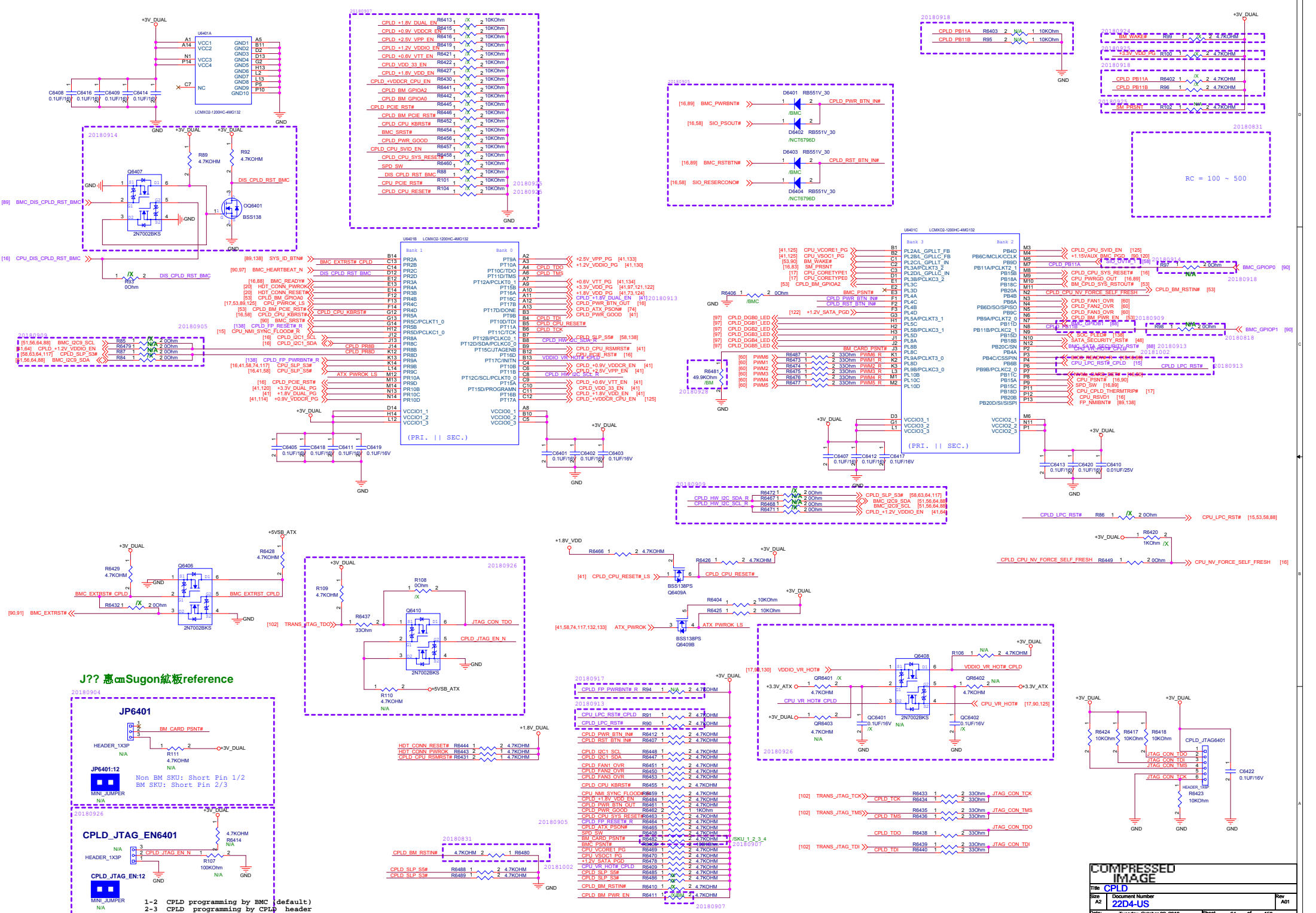


Port 2

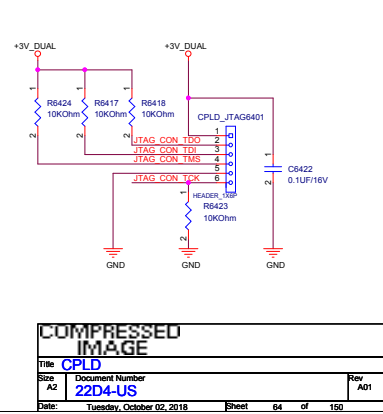
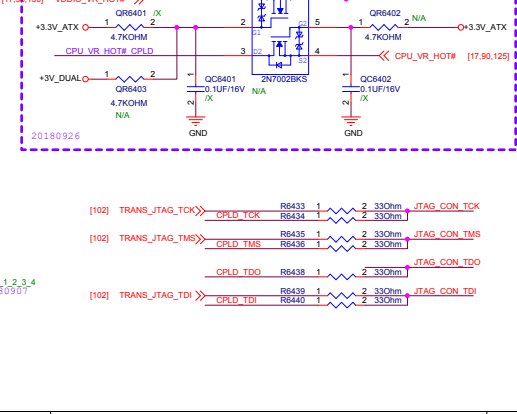
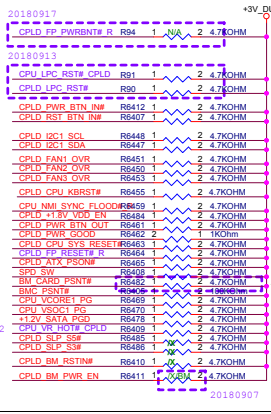
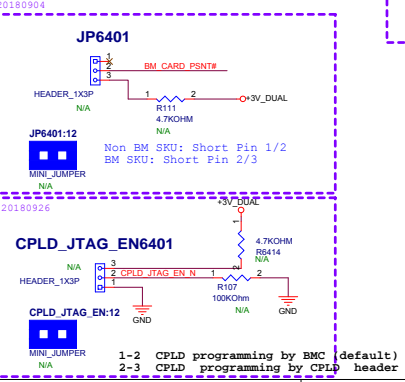


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Title	Rear USB3.0 (EMI/ESD)/OC		
Size	Document Number	Rev	
A2	22D4-US	A01	
Date:	Tuesday, October 02, 2018	Sheet	63 of 150



J?? 惠mSugon板reference



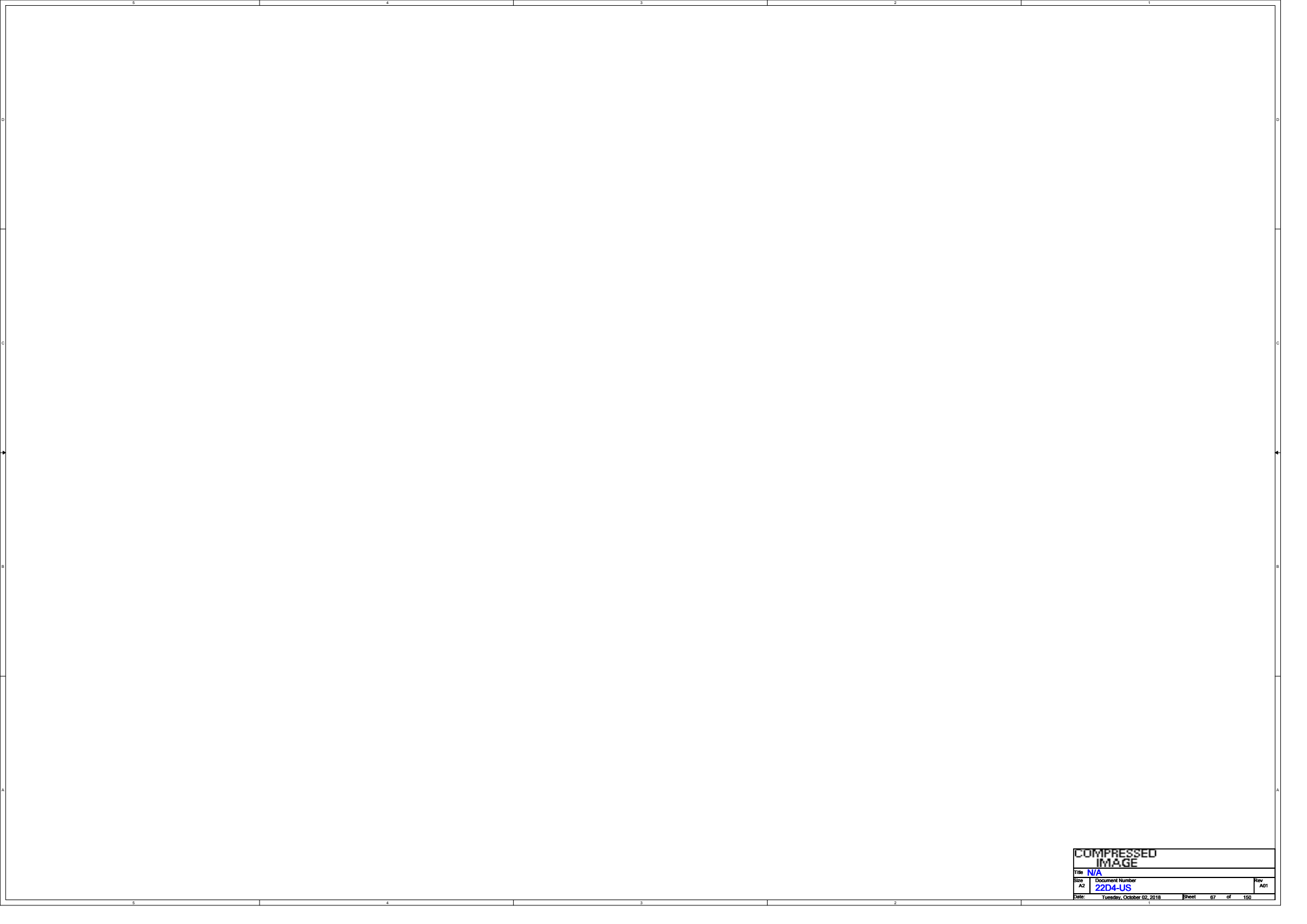
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File	CPD	Document Number	Rev
Size	2204-US		A01
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Size	Document Number	
A2	22D4-US	Rev A01
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Size	Document Number		Rev
A2	22D4-US		A01
Date:		Tuesday, October 02, 2018	Sheet 66 of 150



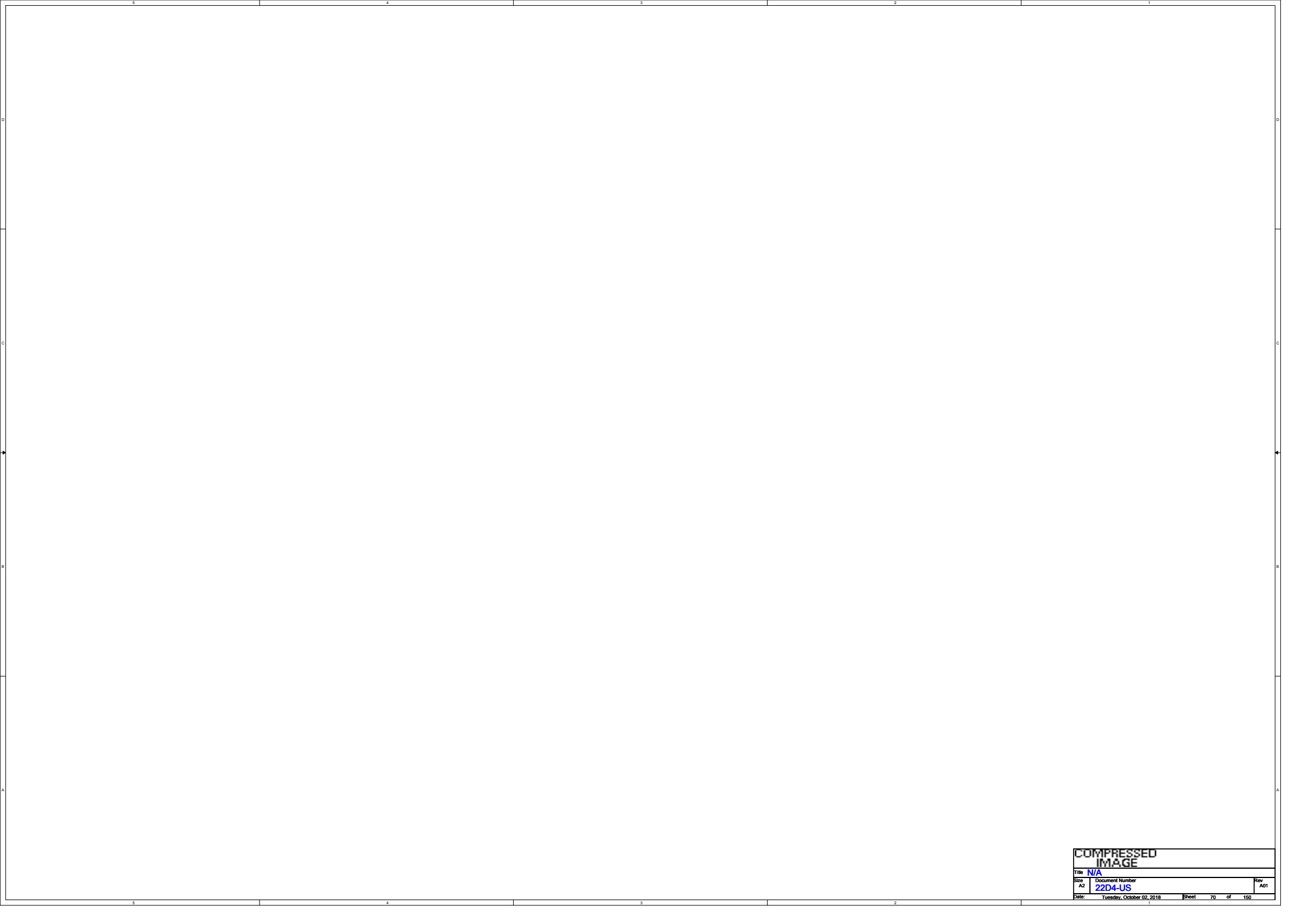
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Date:	Tuesday, October 02, 2018		Sheet 67 of 150



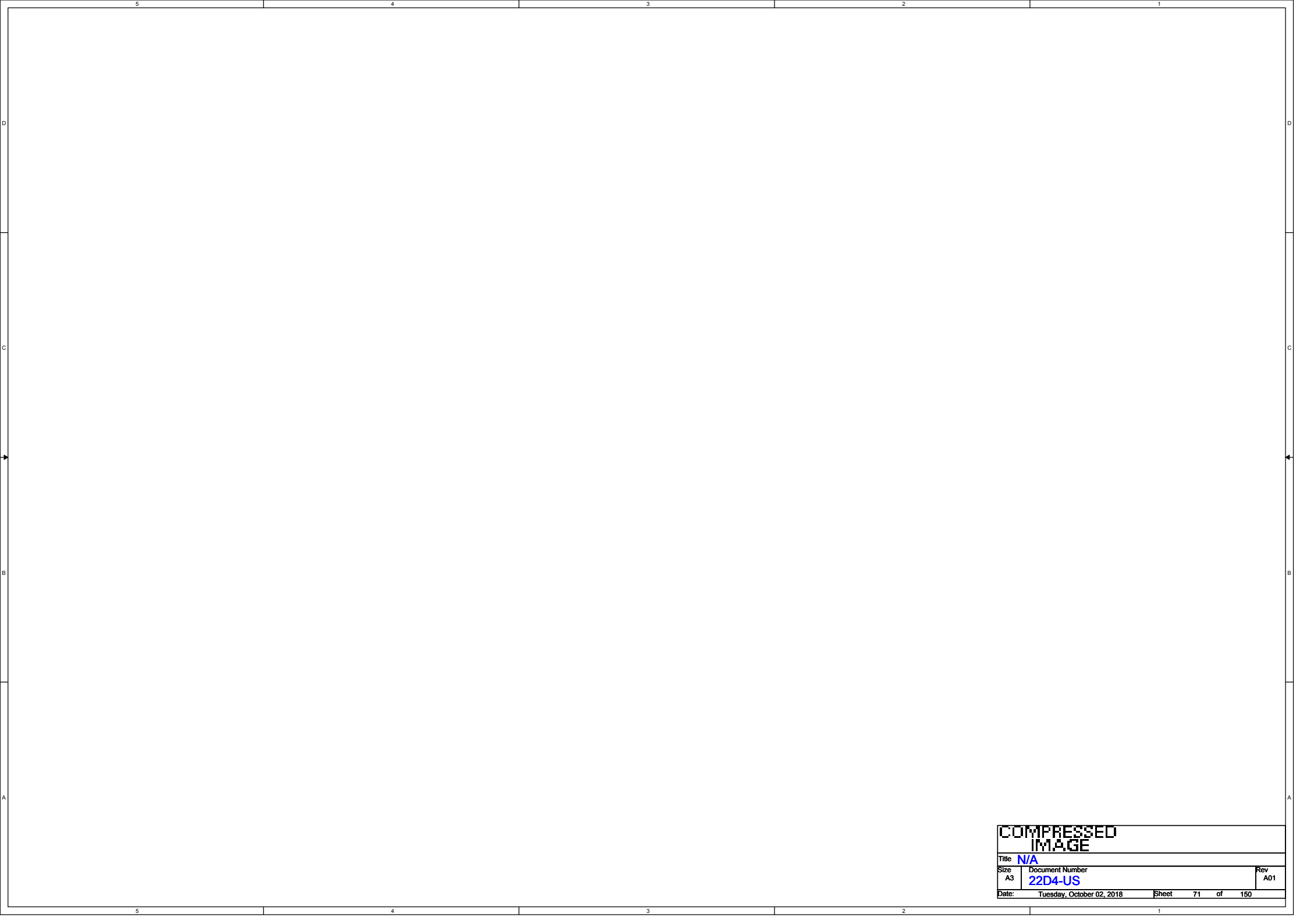
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Size A2	Document Number 22D4-US
Date: Tuesday, October 02, 2018	Sheet 68 of 150
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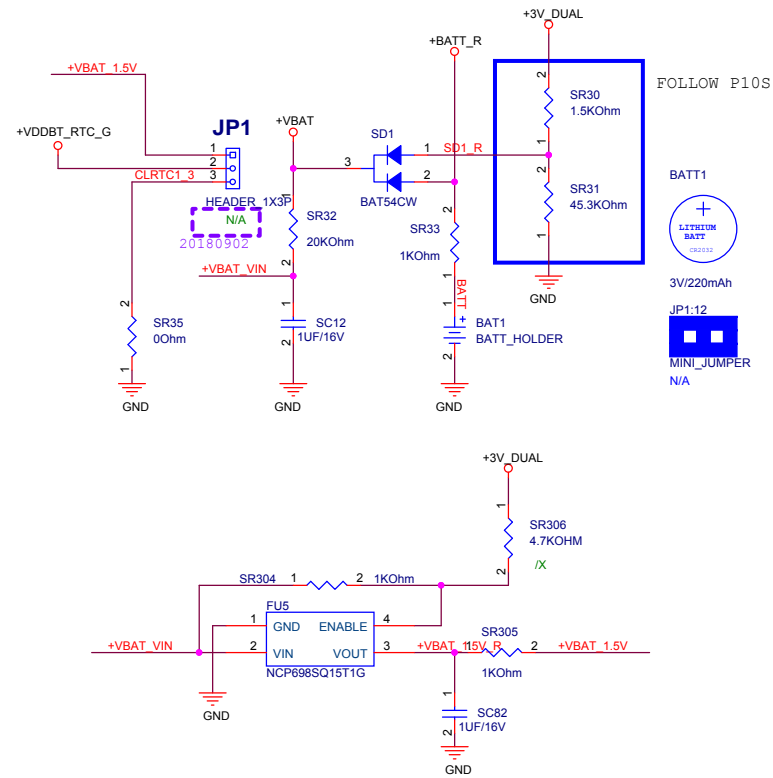
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Rev	A01	
Date:	Tuesday, October 02, 2018	Sheet 08 of 156

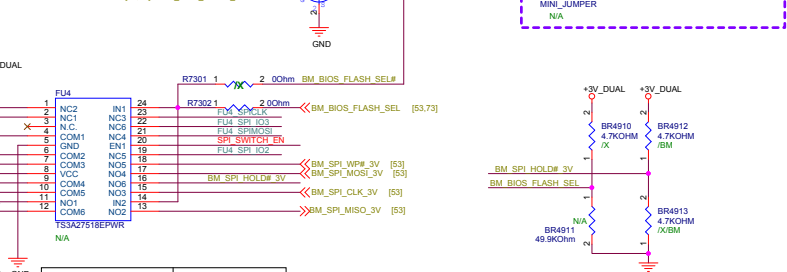
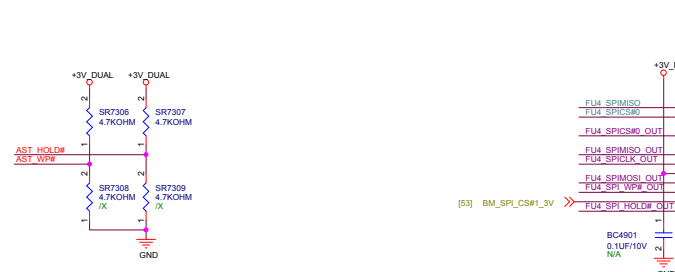
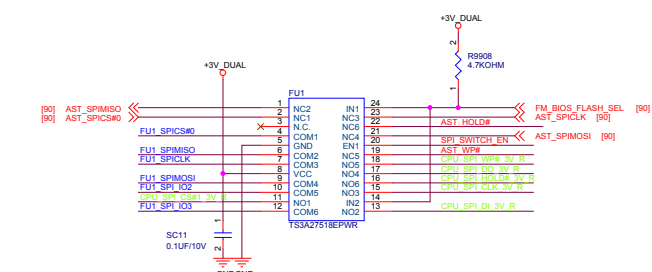
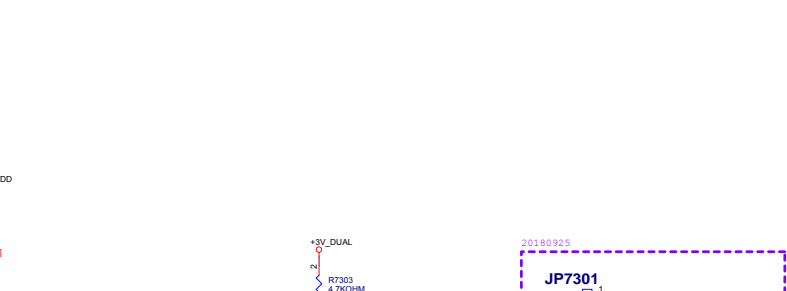
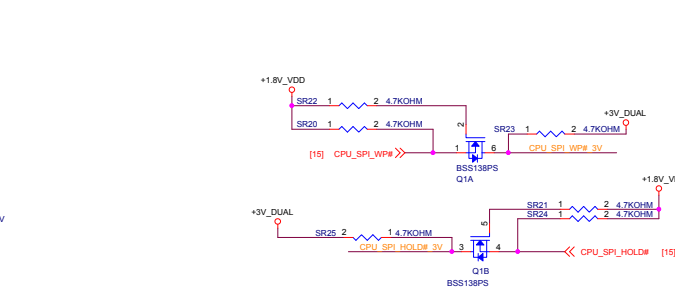
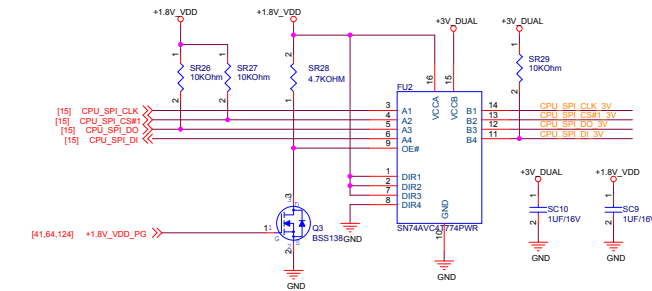


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Title	N/A		
Size	Document Number		Rev
A2	22D4-US		A01
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Size A3	Document Number 22D4-US		
Date:	Tuesday, October 02, 2018	Sheet 71 of 150	Rev A01

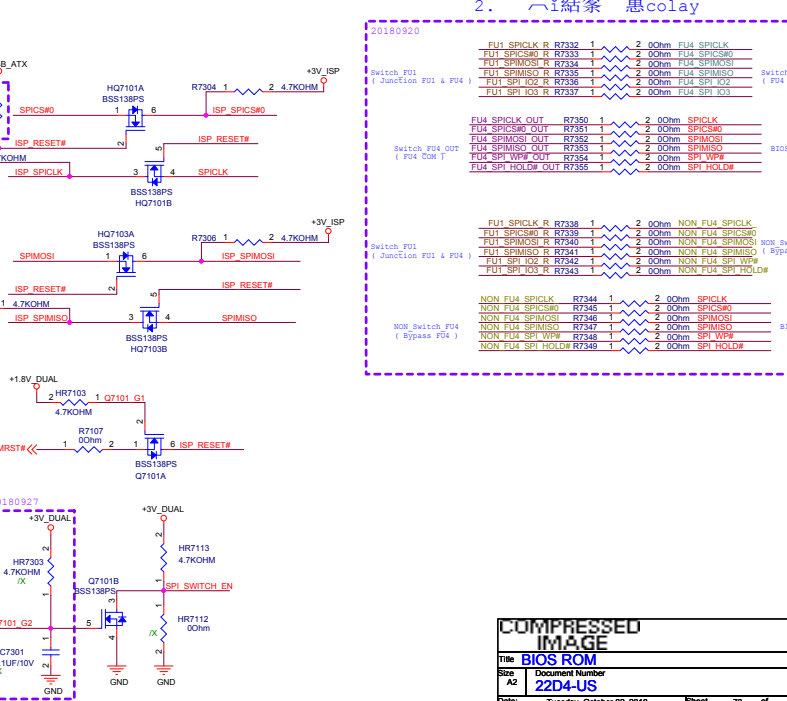
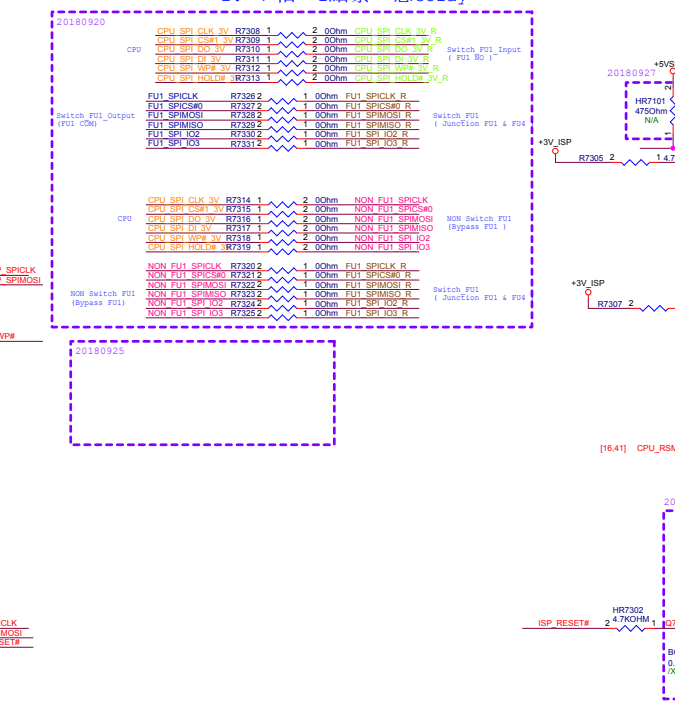
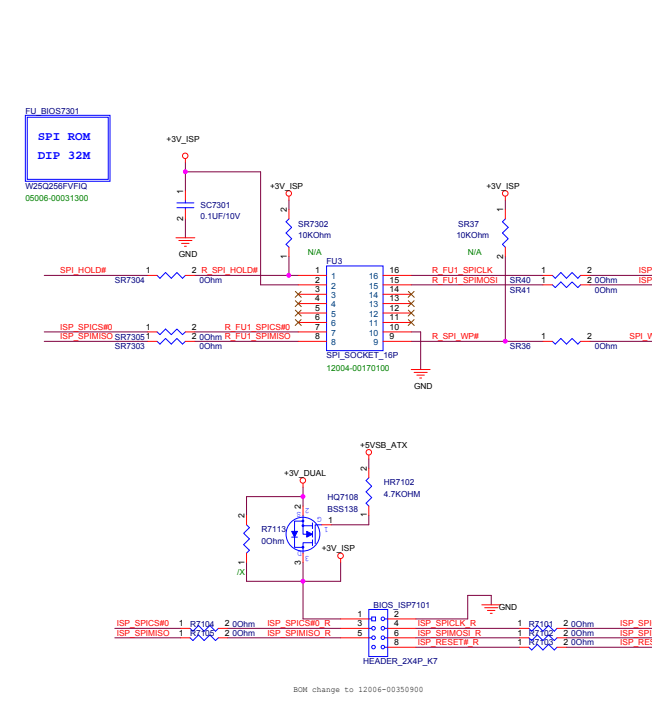




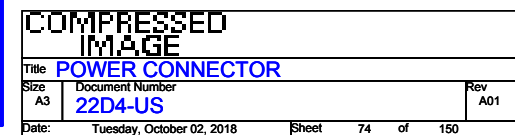
FM_BIOS_FLASH_SEL	FU1_SPI
H	CPU_SPI
L	BMC_SPI

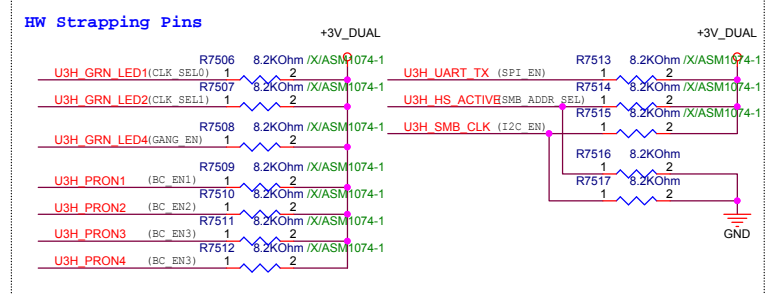
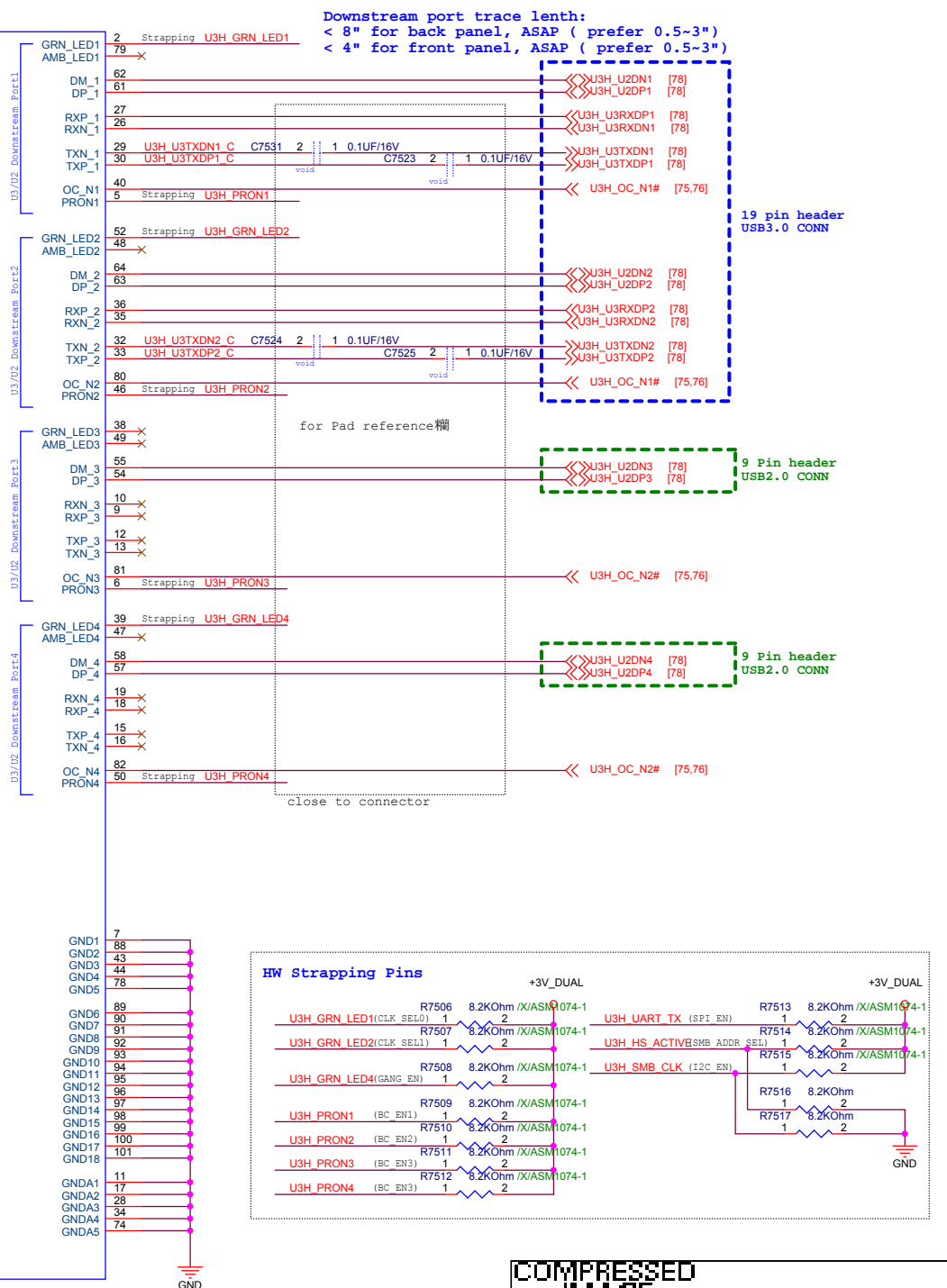
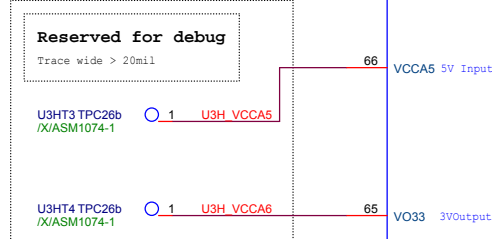
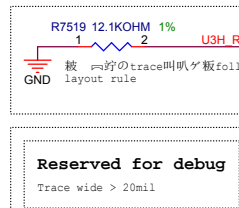
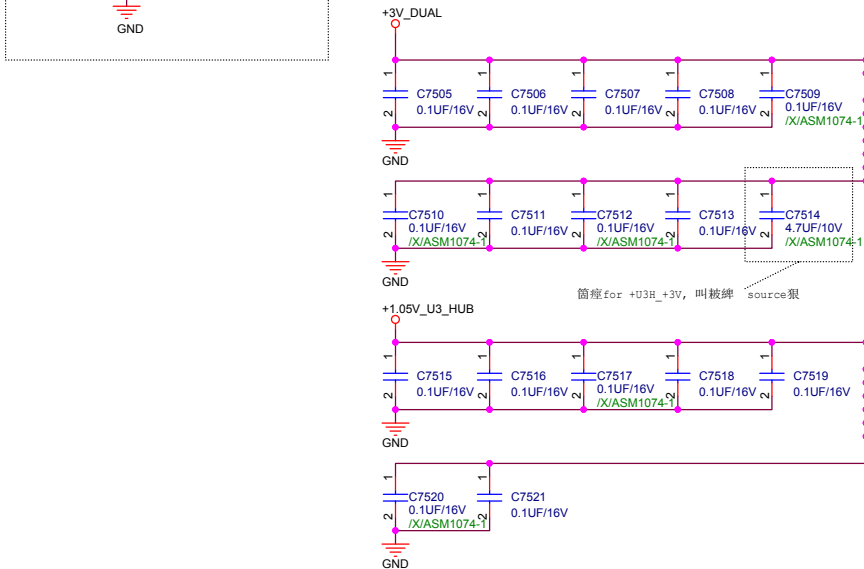
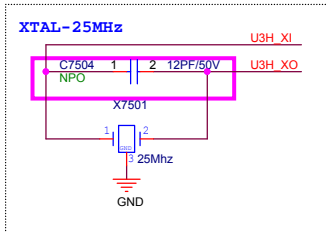
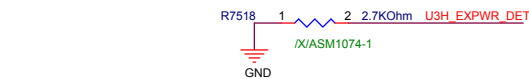
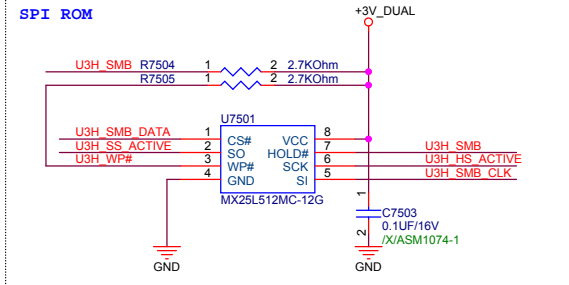
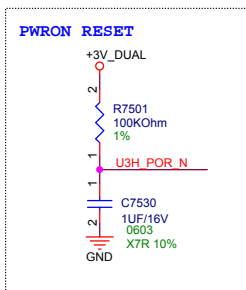
EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	X	X	ON	ON	ON	ON
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

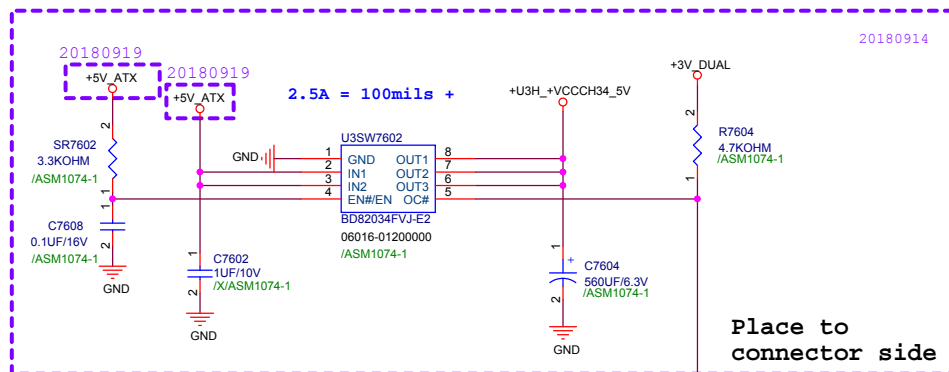
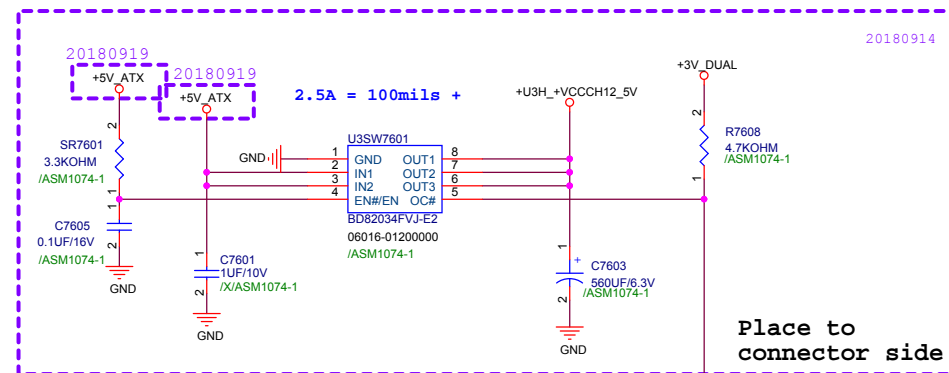
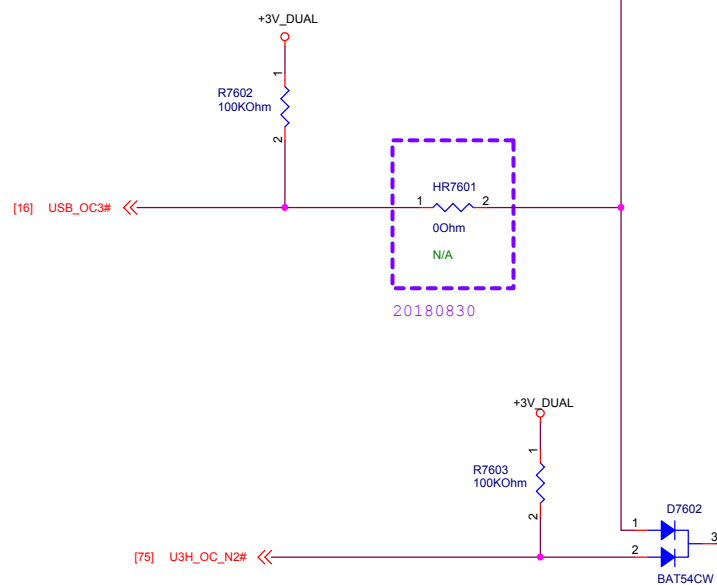
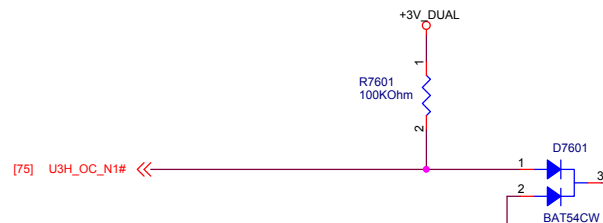
BM_BIOS_FLASH_SEL	FU4_SPI
L	CPU/BMC_SPI
H	BM_CARD_SPI

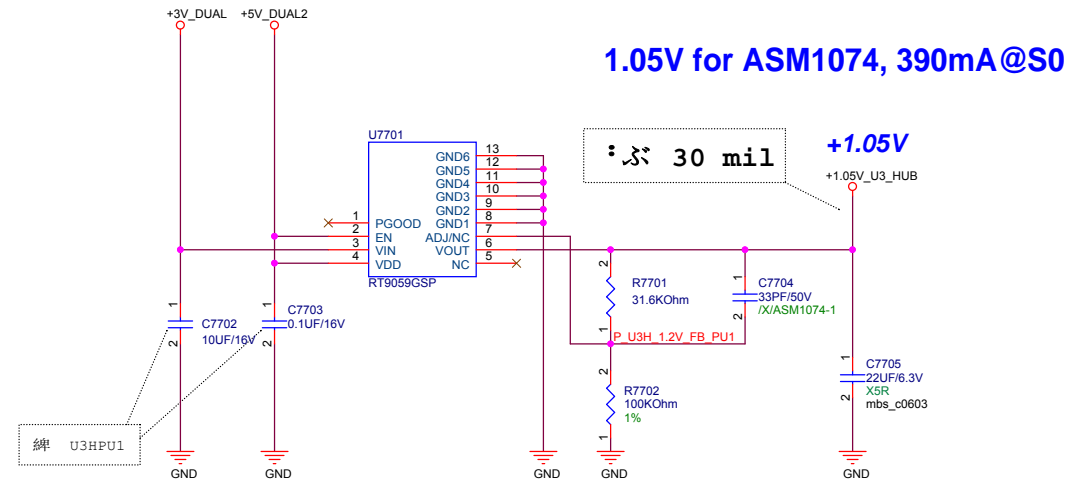


A diagram illustrating the concept of image compression. It shows two overlapping images of the text "COMPRESSED IMAGE". The top image is labeled "B" and the bottom image is labeled "A". The images are offset, with "A" shifted to the left and down relative to "B".









7. Timing Diagram

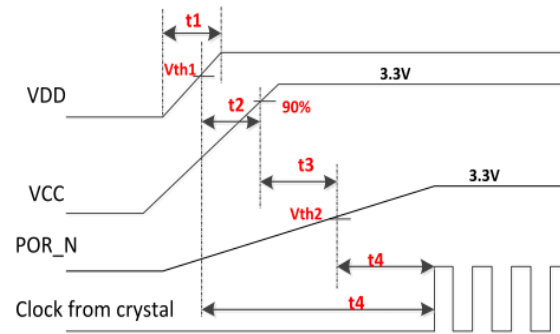


Figure 5: Power on Sequence for crystal mode

Power on Sequence Timing Specification for crystal mode

Symbols	Parameter	Min	Typ	Max	Unit	Remark
Vth1	The threshold of VDD internal power detect	0.49	0.7	0.92	V	
Vth2	The threshold of POR_N signal detect		0.5*VCC		V	
t1	Settling time of VDD stable power			6	ms	Measure from 10% to 90%
t2	The maximum delay timing of VCC power ready after the threshold of VDD	N/A		6	ms	Measure the timing between the point of Vth1 to 90% of VCC
t3	POR_N goes high after VCC power ready	0		N/A	ms	Measure the timing between the 90% of VCC to Vth2 of POR# (If without external POR_N circuit, this rule could be skipped)
t4	Maximum delay of stable clock available after the latest available point of Vth1 or Vth2			26	ms	Measure the timing between the point of Vth to stable clock available (self-powered mode)
				151	ms	Measure the timing between the point of Vth to stable clock available (bus-powered mode)

**COMPRESSED
IMAGE**

Title **ASM1074-3(PWR)**

Size A3 Document Number

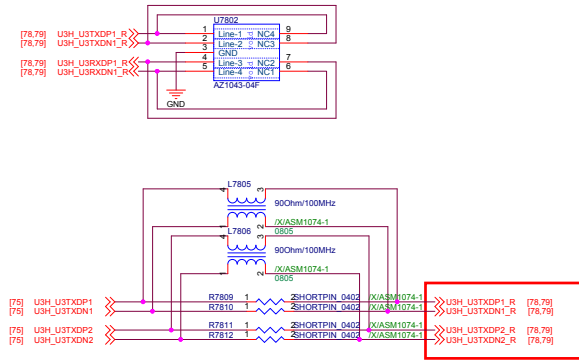
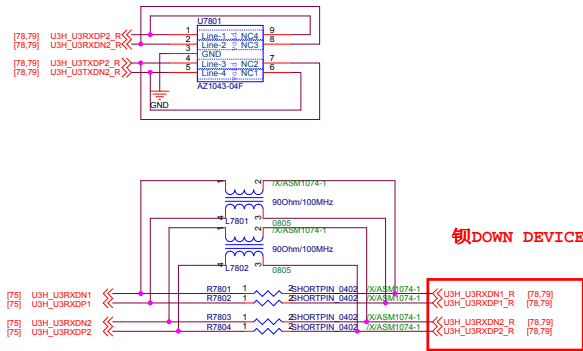
22D4-US

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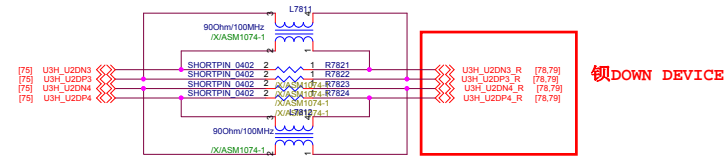
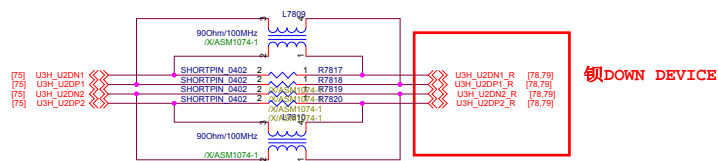
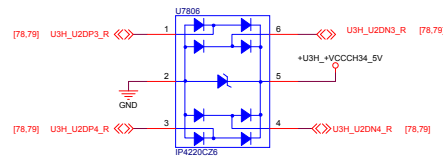
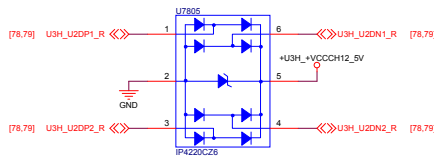
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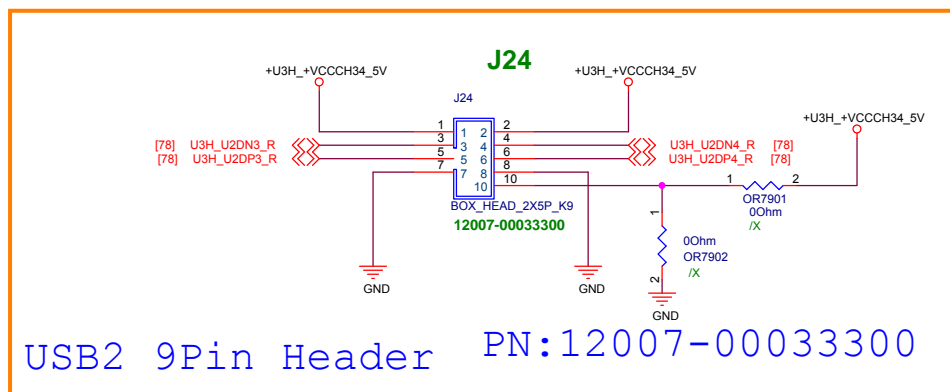
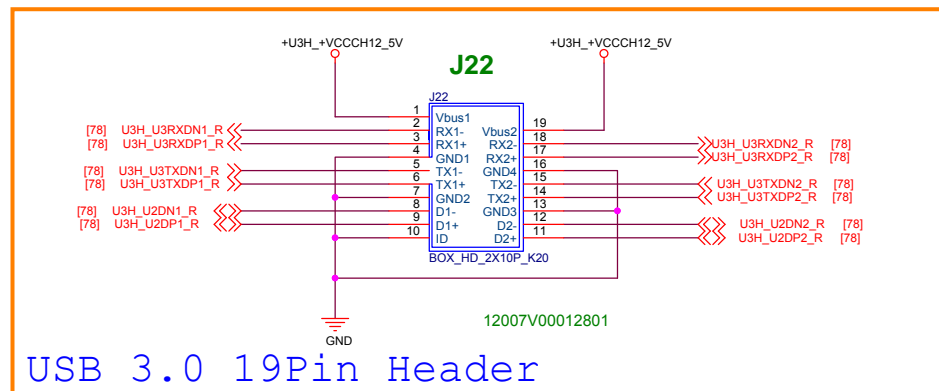
Rev A01

USB3.0



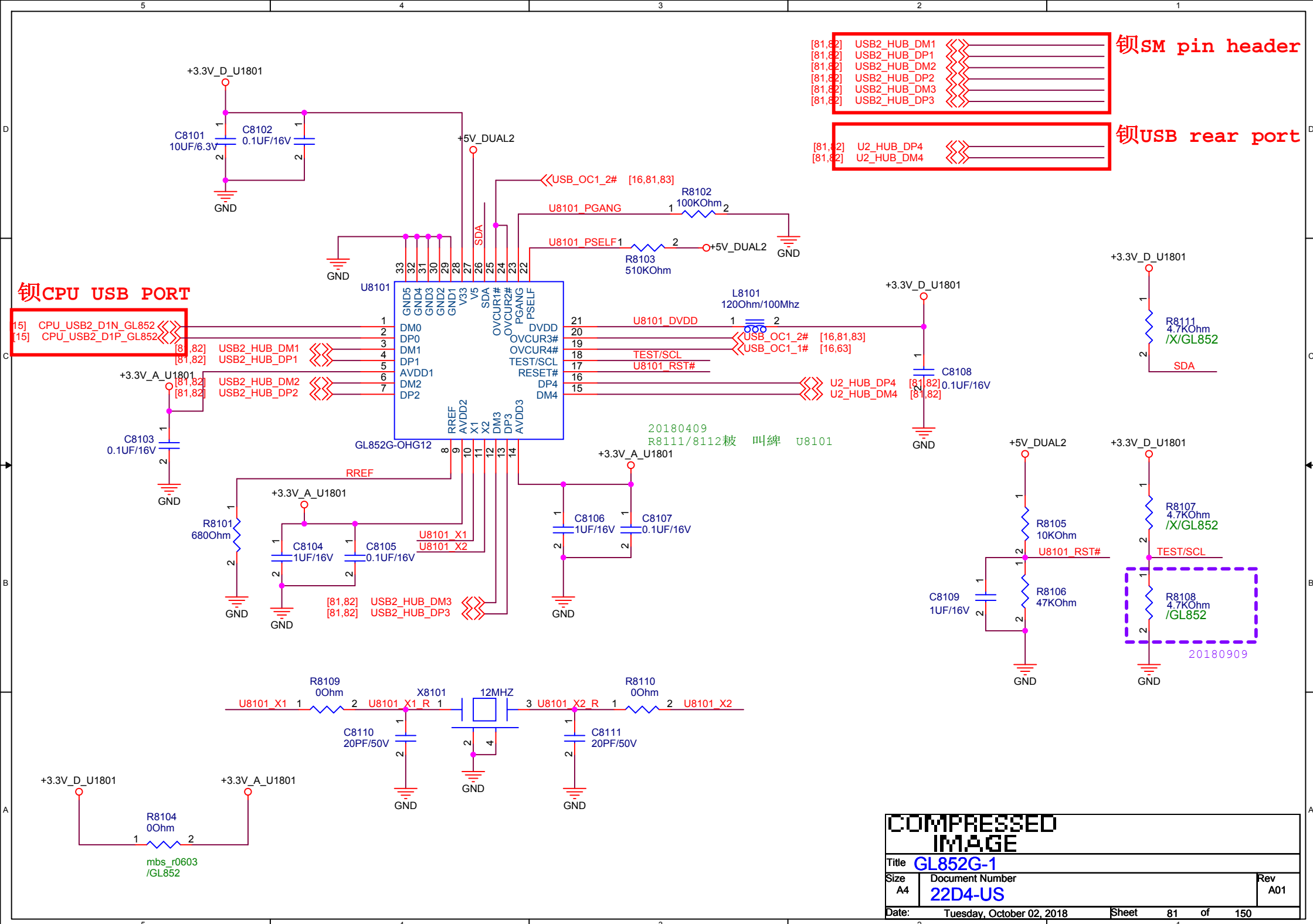
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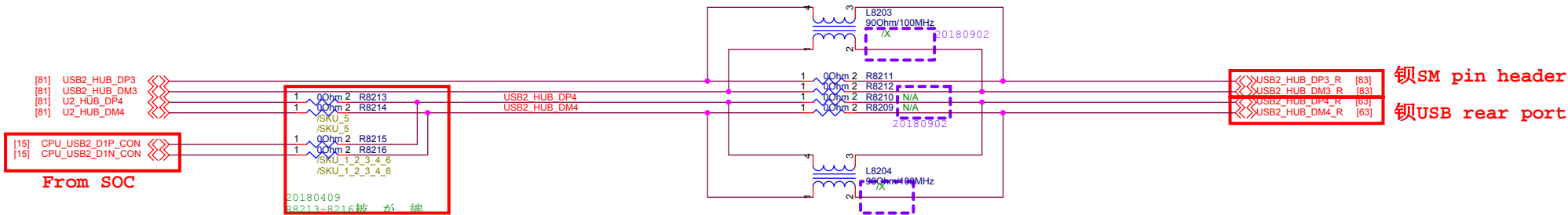
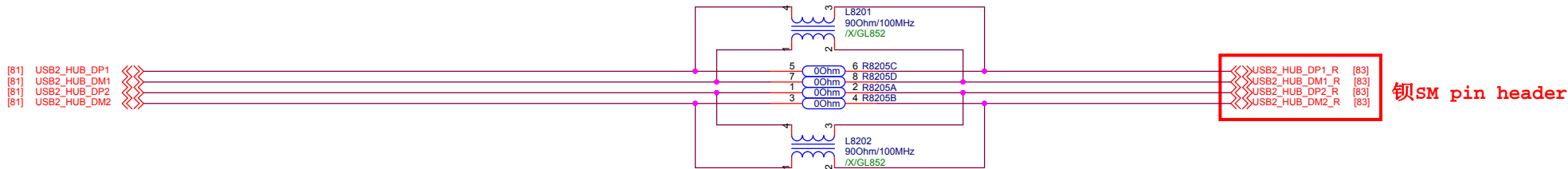






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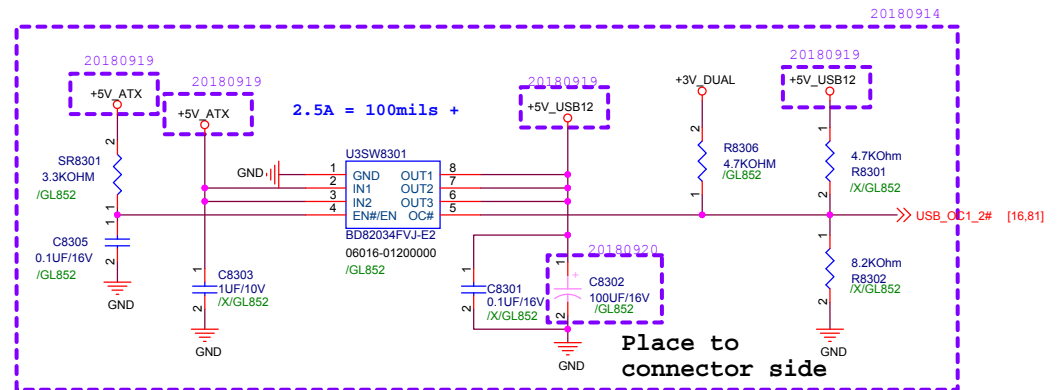
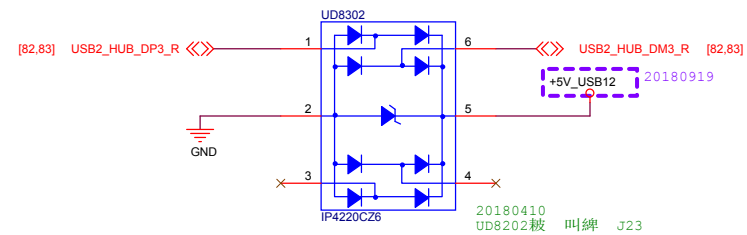
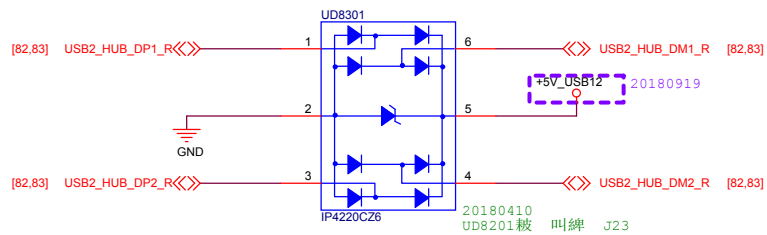
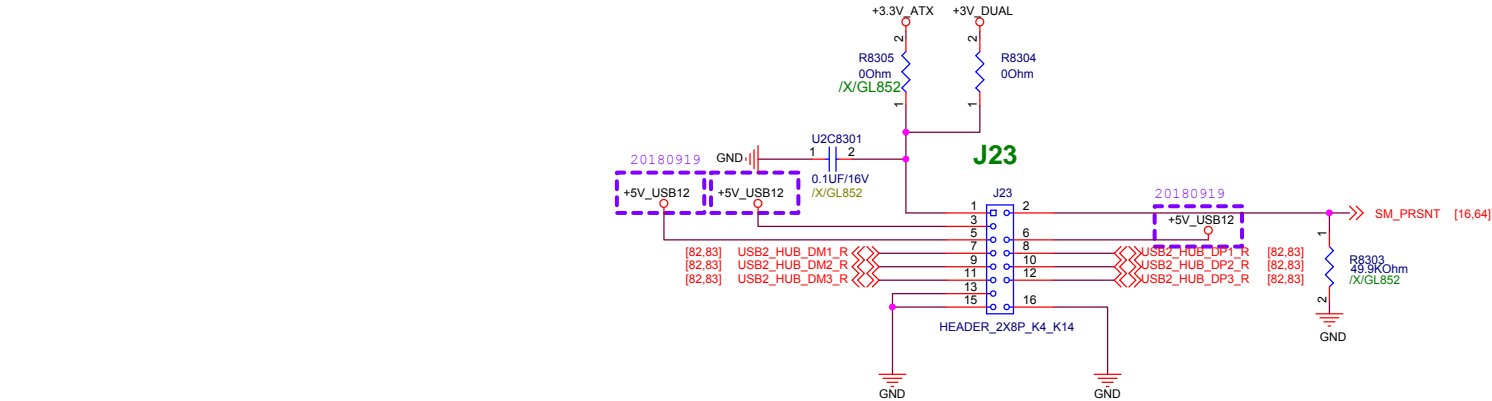
[15] CPU_USB2_D1P_CON
[15] CPU_USB2_D1N_CON

From SOC

1 0Ohm 2 R8213
1 0Ohm 2 R8214
1 /SKU_5
1 0Ohm 2 R8215
1 0Ohm 2 R8216
1 /SKU_1_2_3_4_6
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20180409
R8213~R8216 被 叫 牌

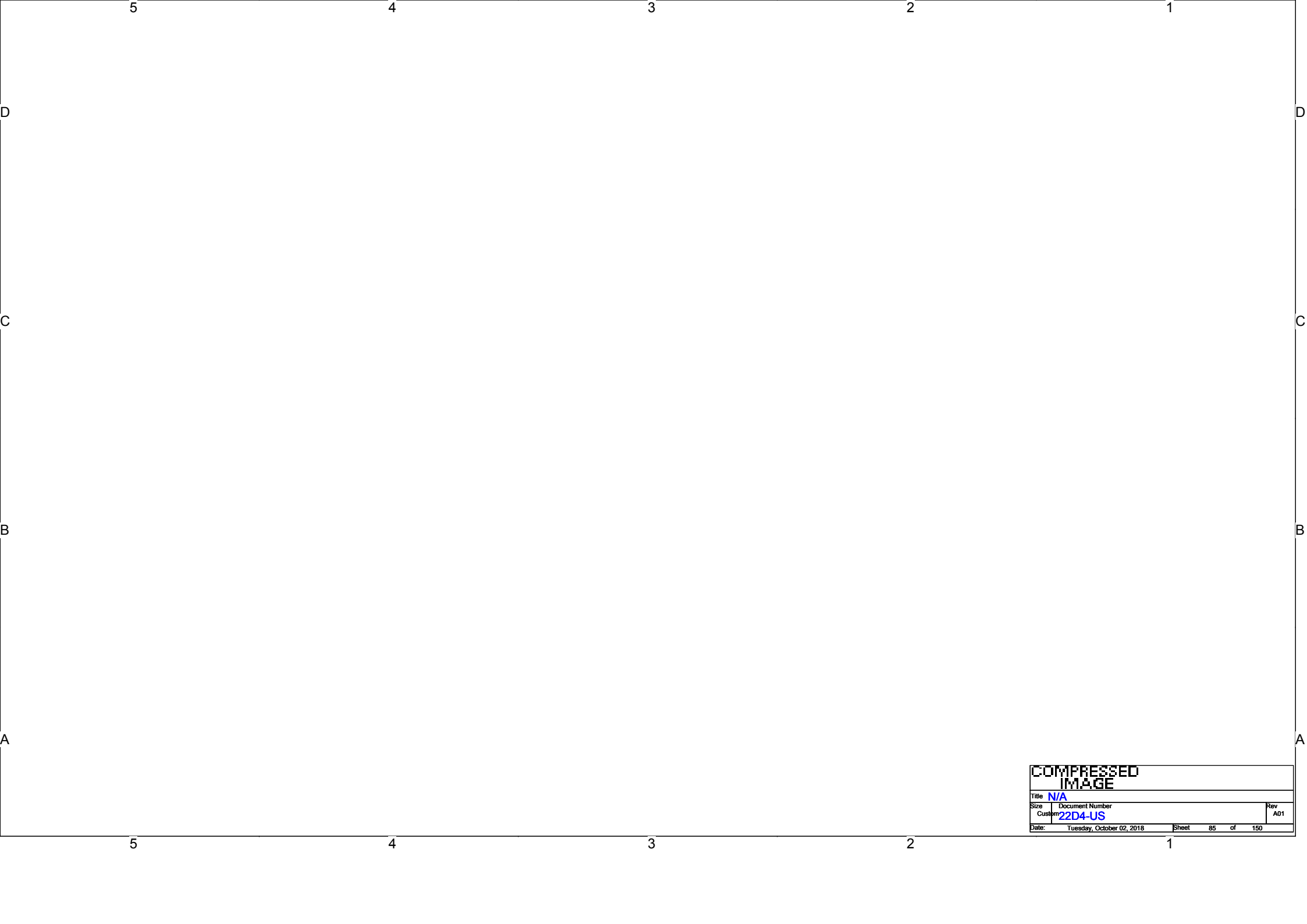
20180409
R8210/R8209/L8204 被 叫 牌 J21

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IMAGE





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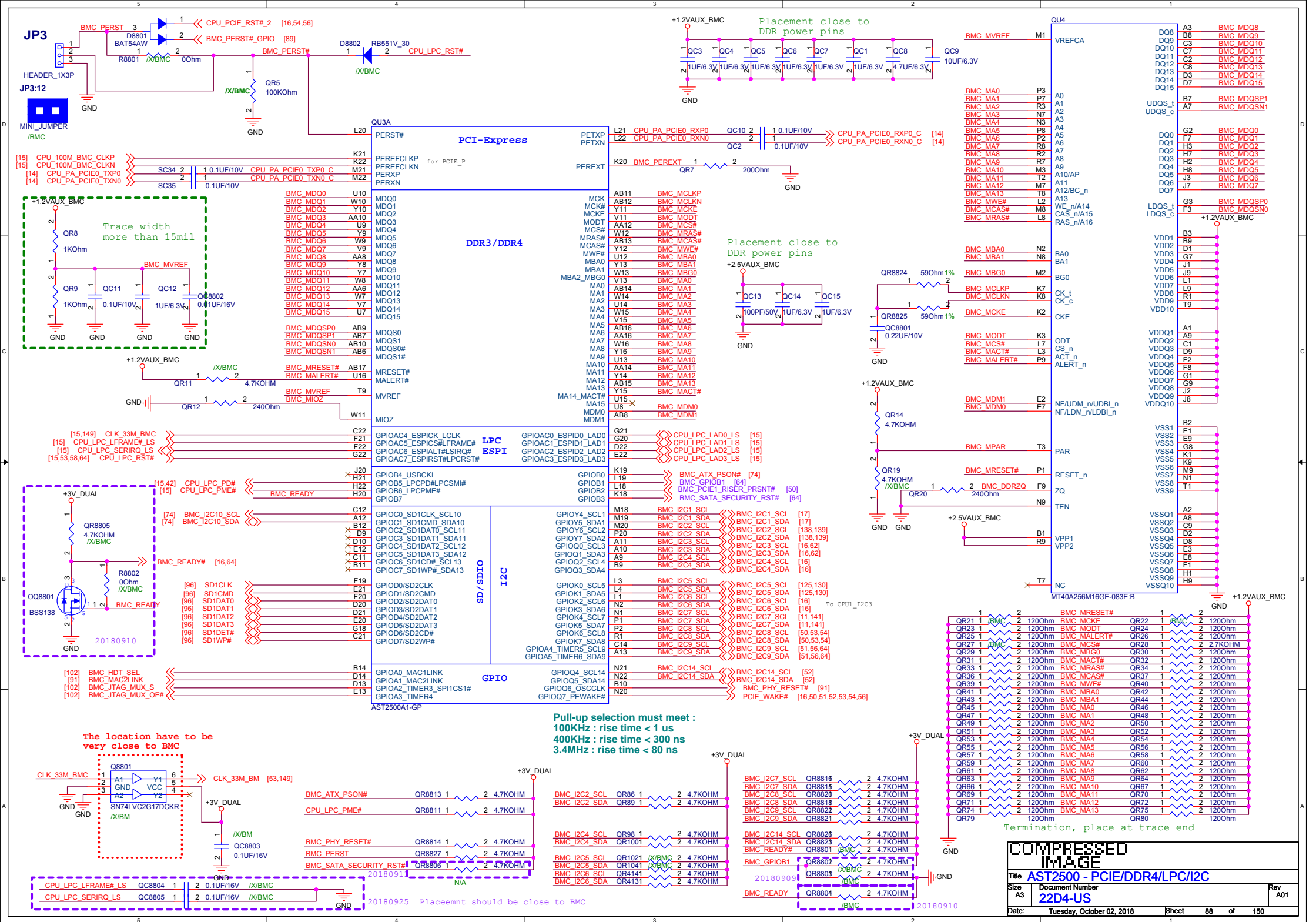
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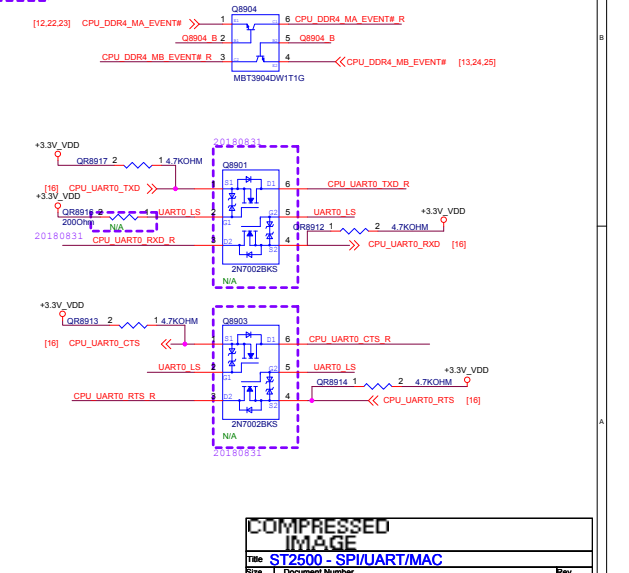
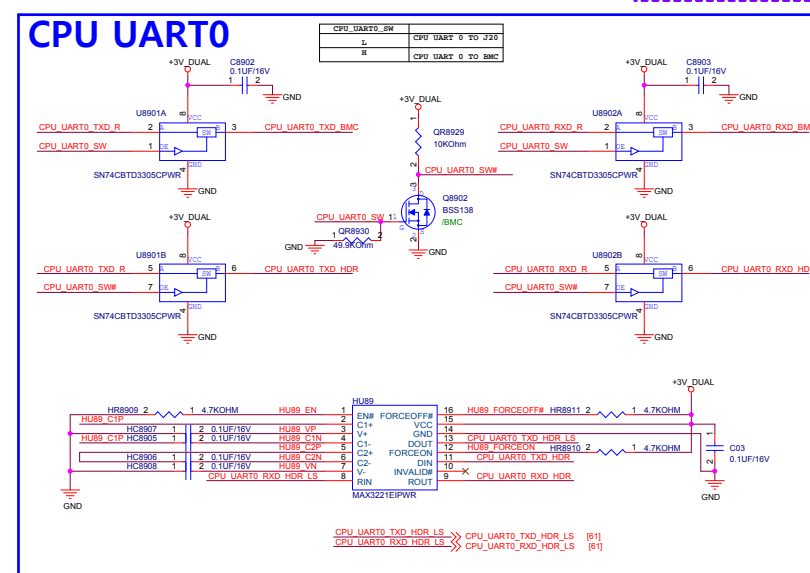
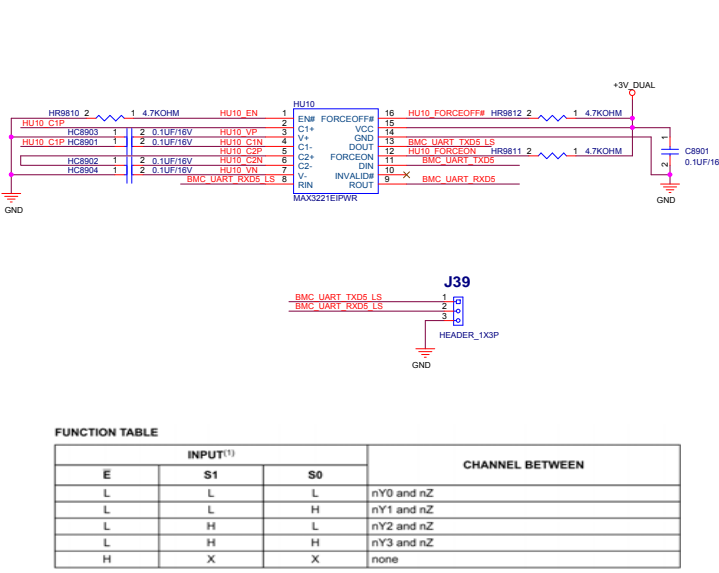
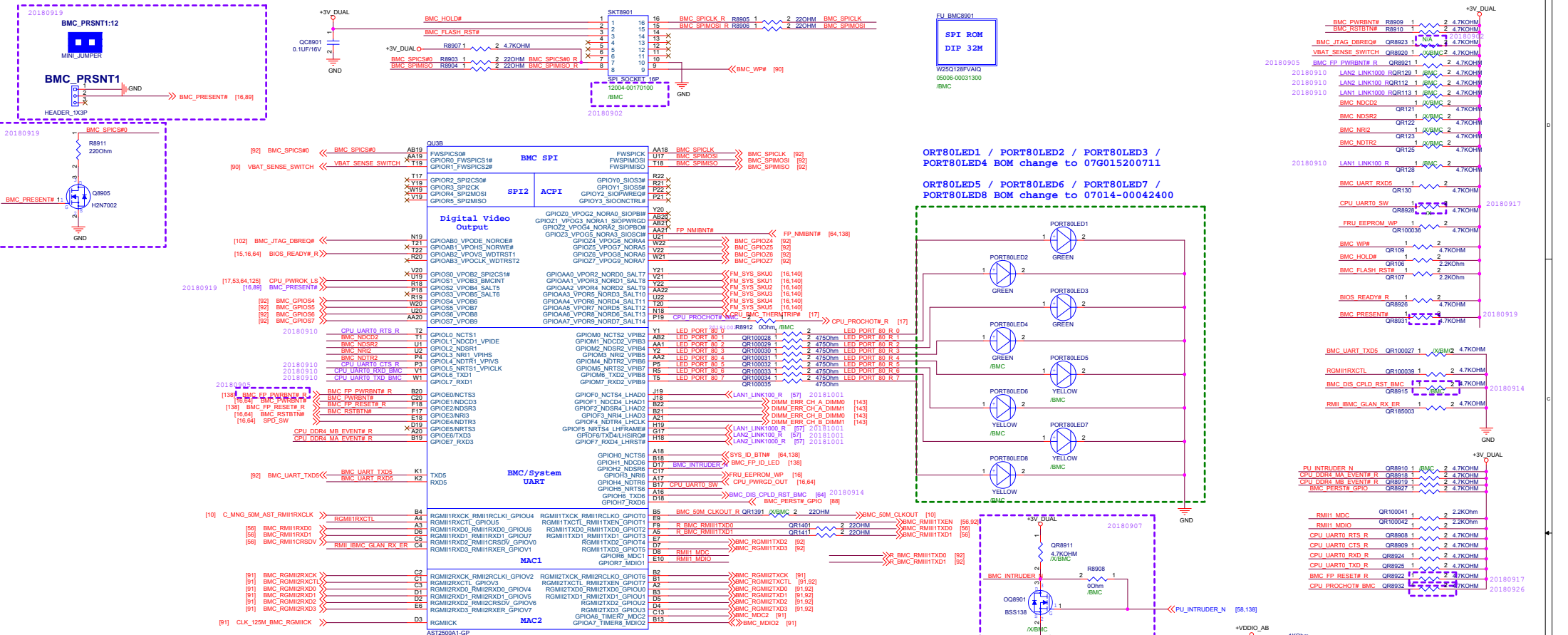
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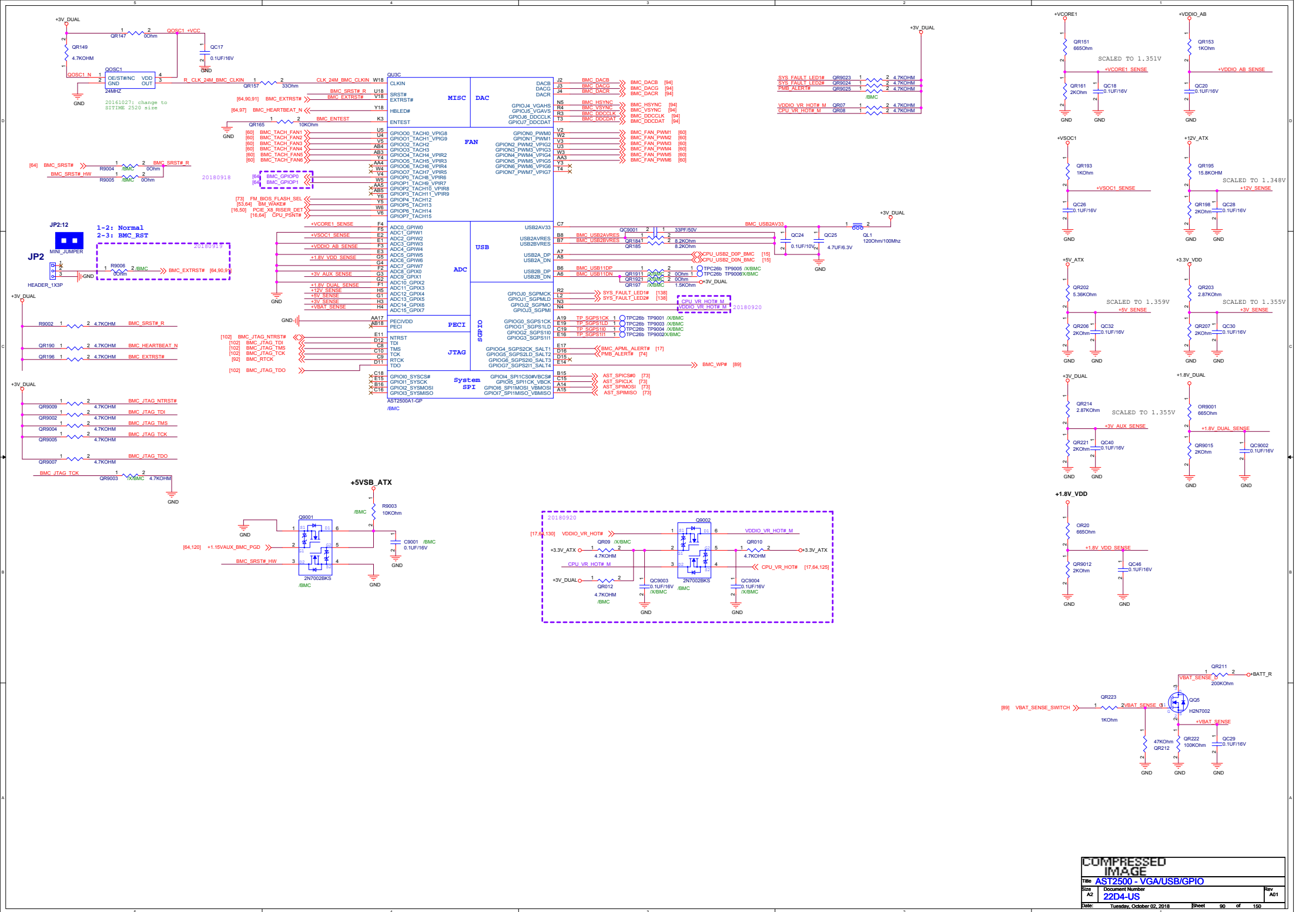
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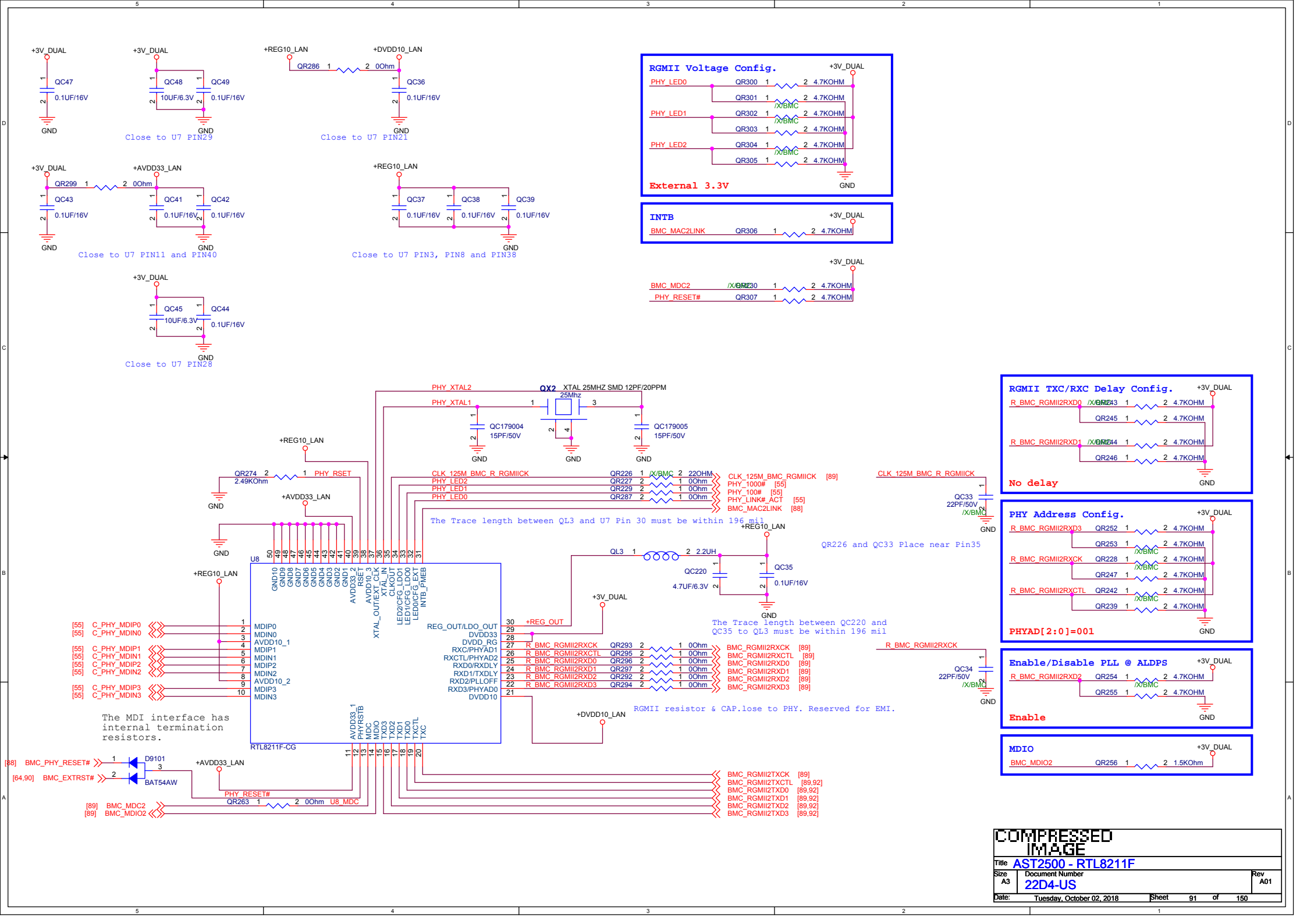
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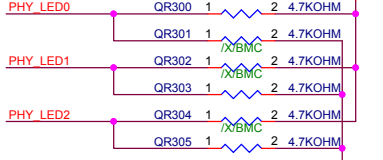






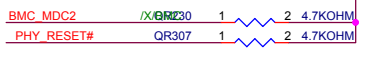


RGMII Voltage Config.

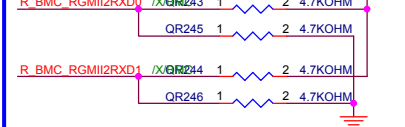


External 3.3v

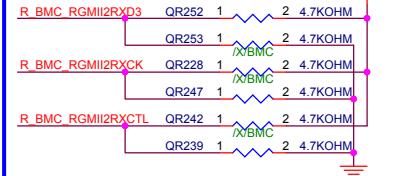
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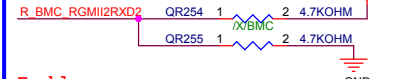
RGMII TXC/RXC Delay Config.



PHY Address Config.



Enable/Disable PLL @ ALDPS



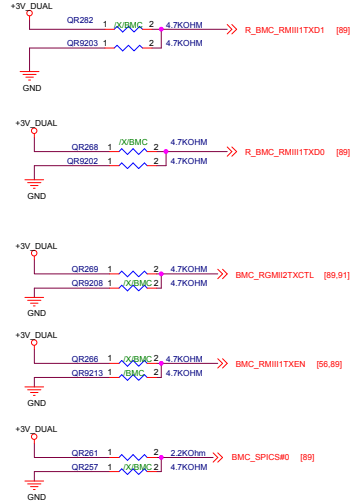
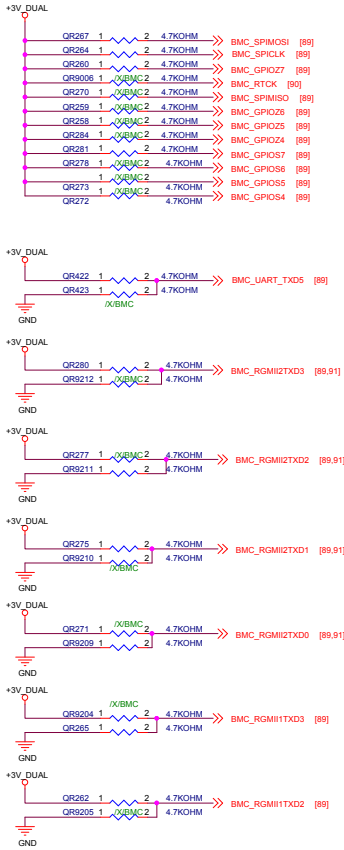
MDIO

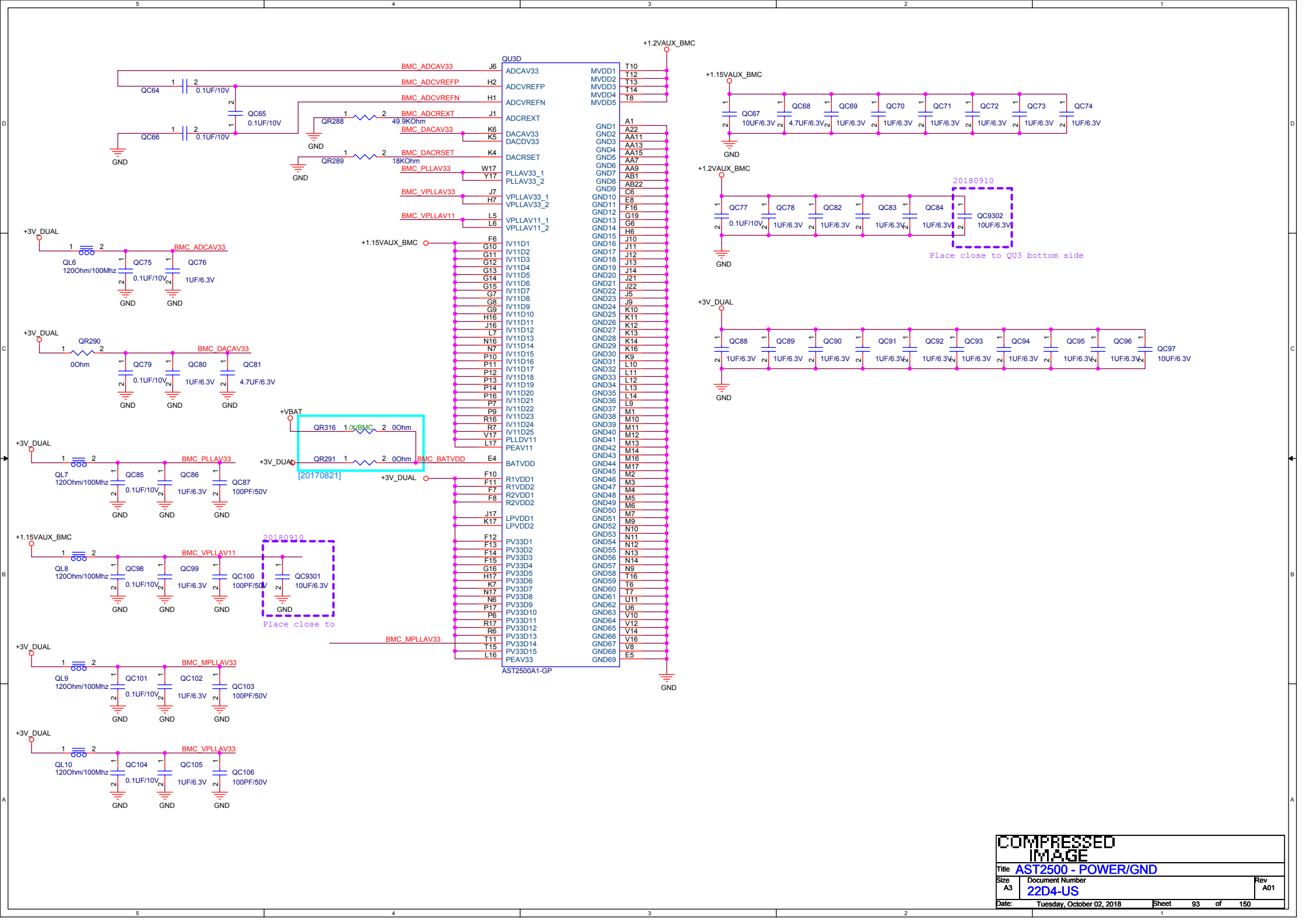


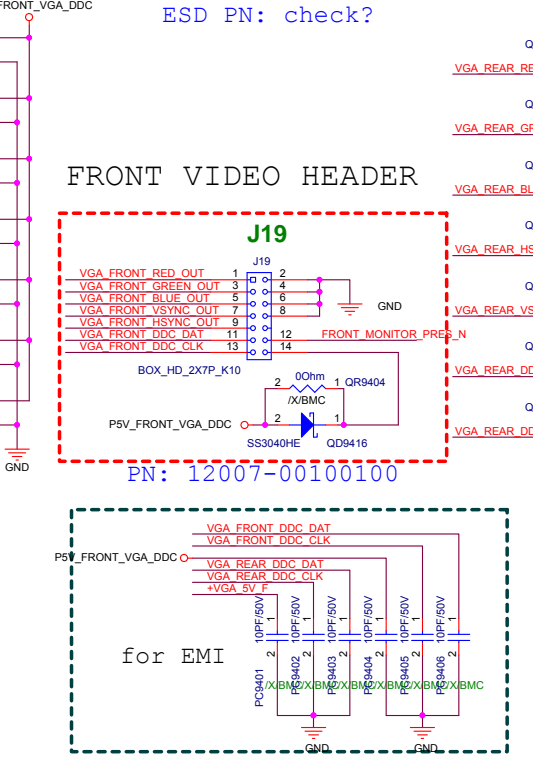
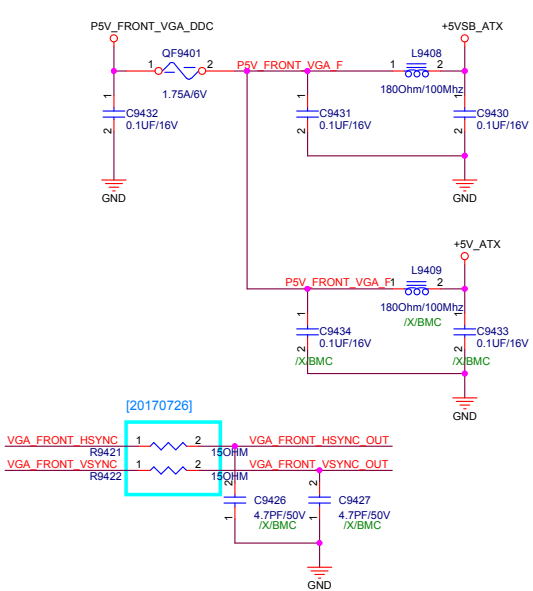
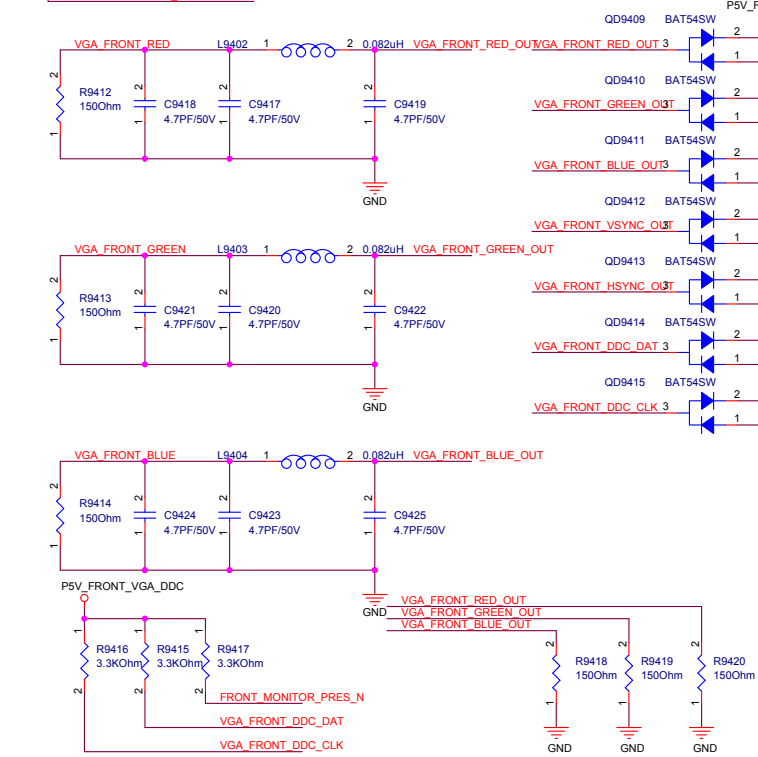
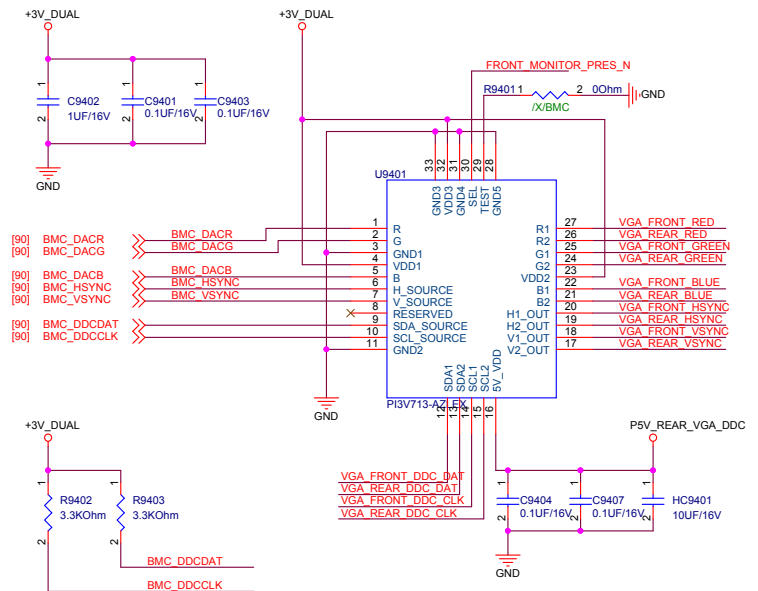
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0x1E6E2070 Bit#	BALL NUM	BALL NAME	DESCRIPTION
31	U17	FWSPIMOSI	ENABLE SPI FLASH STRAP AUTO FETCH MODE 0: DISABLE 1: ENABLE (DFLT)
30	AA18	FWSPICK	ENABLE GPIO STRAP MODE 0: DISABLE 1: ENABLE (DFLT)
29	K1	TXD5	SELECT UART DEBUG PORT (IT CAN SUPPORT FIRMWARE UPDATE CAPABILITY) 0: SELECT UART1 AS BMC CONSOLE PORT 1: SELECT UART5 AS BMC CONSOLE PORT (DFLT)
27	W21	GPIOZ7	ENABLE FAST RESET MODE FOR ARM ICE DEBUGGER 0: LONG RESET MODE, NORMAL OPERATION (DFLT) 1: FAST RESET MODE, FOR ICE DEBUGGER CONNECTION
26	C9	RTCK	ENABLE ESPI FLASH MODE (BIT VALID ONLY WHEN ESPI MODE IS ENABLE) 0: ESPI RESPOND WITH NO FLASH ATTACHED (DFLT) 1: ESPI RESPOND WITH FLASH ATTACHED
25	T18	FWSPIMISO	ENABLE ESPI MODE 0: LPC MODE 1: ESPI MODE (DFLT)
24	D4	RGMII2TXD3	SELECT DDR4 SDRAM 0: DDR3 SDRAM 1: DDR4 SDRAM (DFLT)
23	D5	RGMII2TXD2	SELECT 25MHZ REFERENCE CLOCK INPUT MODE 0: CLKIN IS 24MHZ AND USBCKI NOT USED 1: CLKIN IS 25MHZ AND USBCKI = 24/48MHZ (DFLT)
22	B3	RGMII2TXD1	ENABLE GPIOE PASS-THROUGH MODE 0: DISABLE 1: ENABLE PASS-THRU AT POWER ON (DFLT)
21	A2	RGMII2TXD0	ENABLE GPIOD PASS-THROUGH MODE 0: DISABLE 1: ENABLE PASS-THRU AT POWER ON (DFLT)
20	A2	GPIOZ6	Disable LPC to decode SuperIO0x2E/0x4E address 0: Enable address decoding(DFLT) 1: Disable address decoding
19	D7	RGMII1TXD3	ENABLE ACPI FUNCTION 0: DISABLE ACPI 1: ENABLE ACPI (DFLT)
18	W22	GPIOZ5	SELECT USBCKI INPUT FREQUENCY 0: 24MHZ 1: 48MHZ (DFLT)
17	U21	GPIOZ4	ENABLE BMC 2ND BOOT WATCHDOG TIMER 0: DISABLE (DFLT) 1: ENABLE TIMER START COUNTING AT POWER UP
16	E7	RGMII1TXD2	SUPER-IO CONFIGURATION ADDRESS SELECTION 0: DECODE 0X2E (DFLT) 1: DECODE 0X4E
15	AA20	GPIO57	VGA CLASS CODE SELECTION 0: SELECT THE CLASS CODE FOR VIDEO DEVICE 1: SELECT THE CLASS CODE FOR VGA DEVICE (DFLT)
13	A5	RGMII1TXD1	SPI MODE SELECTION [13:12] (RELATED TO GPIO[7:4]) 00: DISABLE SPI INTERFACE (DFLT) 01: ENABLE SPI MASTER
12	F9	RGMII1TXD0	10: ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE 11: ENABLE SPI PASS-THROUGH
07	B1	RGMII2TXCTL	DEFINE MAC2 INTERFACE 0: RMII/NCsI 1: RGMII (DFLT)
06	E9	RGMII1TXCTL	DFINE MAC1 INTERFACE 0: RMII/NCsI (DFLT) 1: RGMII
05	U20	GPIO56	ENABLE DEICATED VGA BIOS ROM 0: NO VGA BIOS ROM, VGA BIOS IS MERGED IN THE SYSTEM BIOS (DFLT) 1: ENABLE DEDICATED VGA BIOS ROM
04	W20	GPIO55	RESERVED (0)
03	R19	GPIO54	VGA MEMORY SIZE [3:2] (ALONG WITH SOFT STRAP 2) 00: SELECT 8MB VGA MEMORY 01: SELECT 16MB VGA MEMORY (DFLT) 10: SELECT 32MB VGA MEMORY 11: SELECT 64MB VGA MEMORY
00	AB19	FWSPICS0#	DISABLE CPU BOOT 0: ENABLE BOOT (DFLT) 1: DISABLE CPU OPERATION, WHEN NO FIRMWARE EXIST

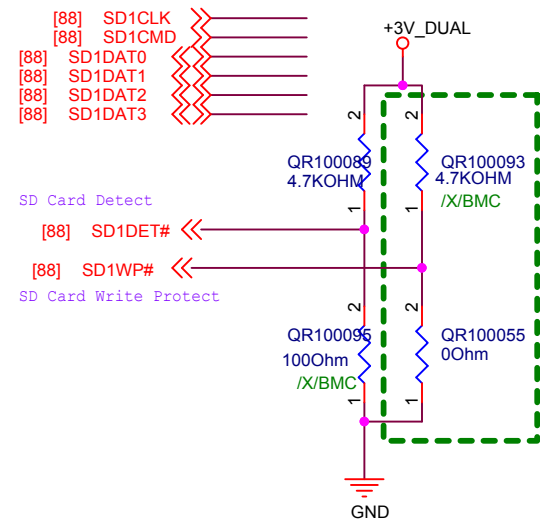
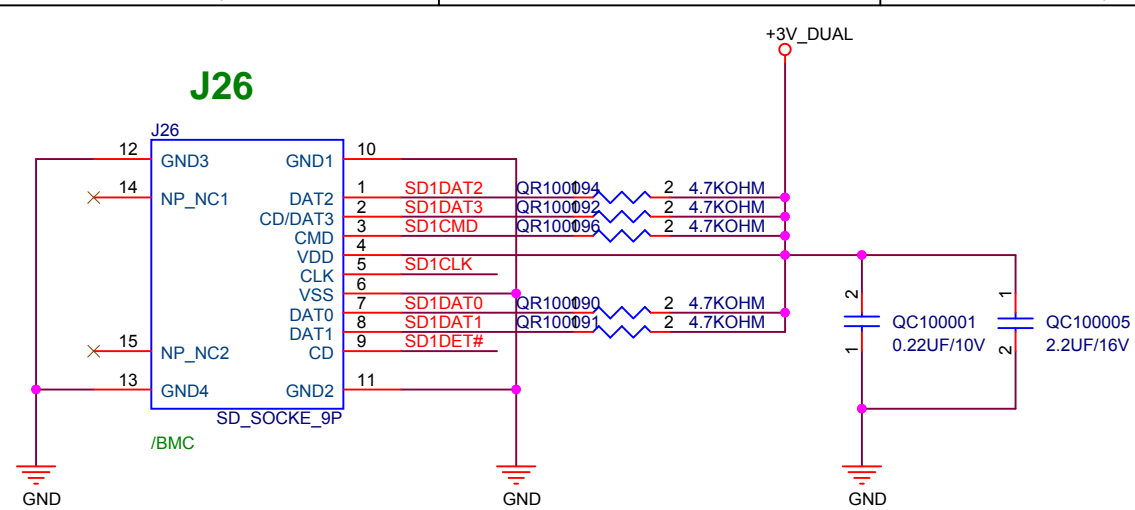








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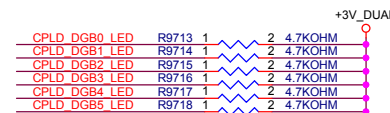
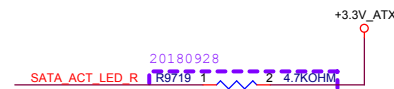
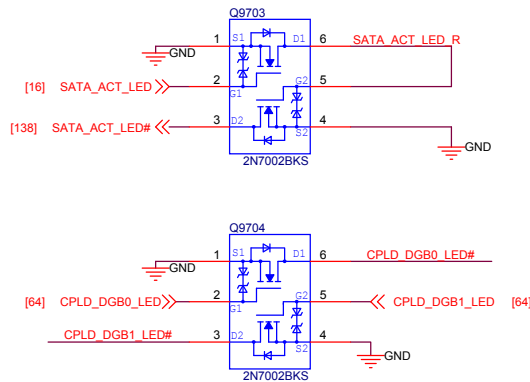
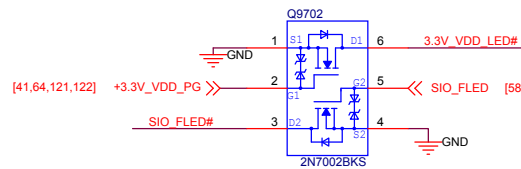
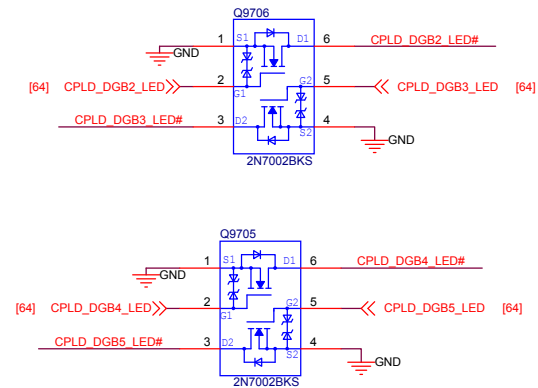
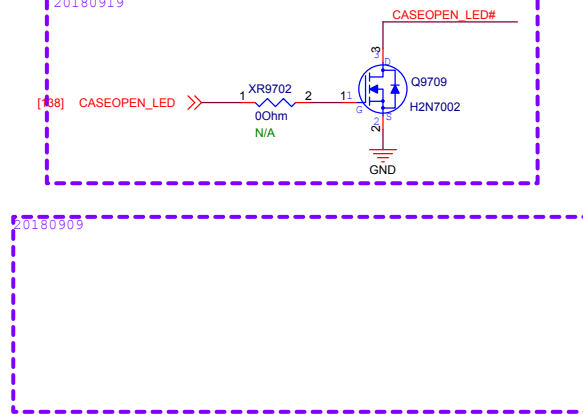
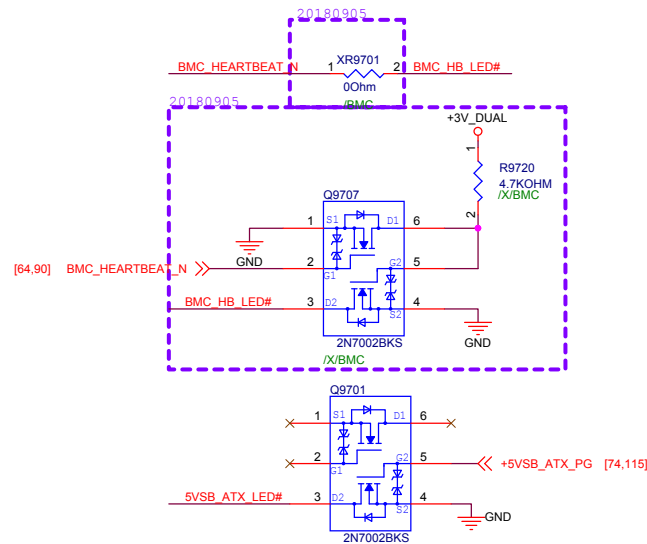
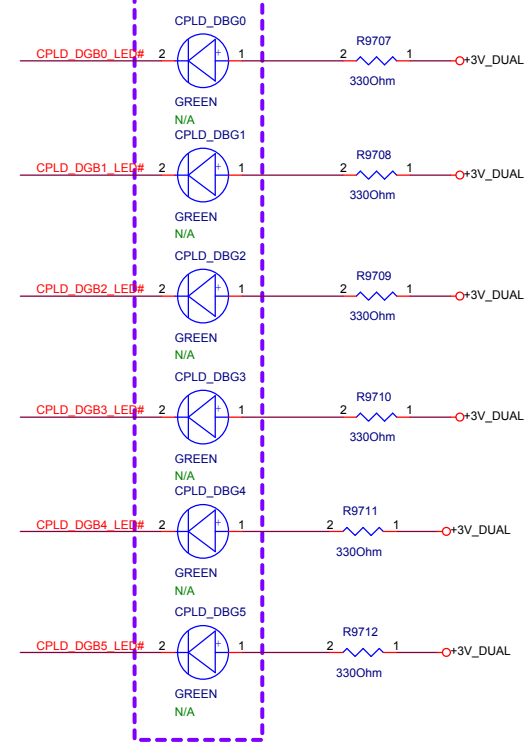
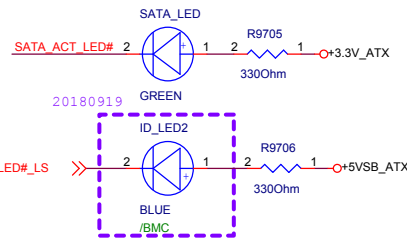
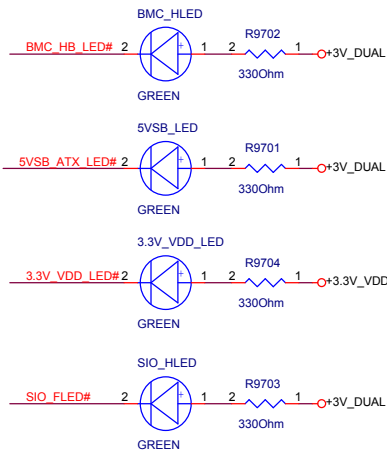
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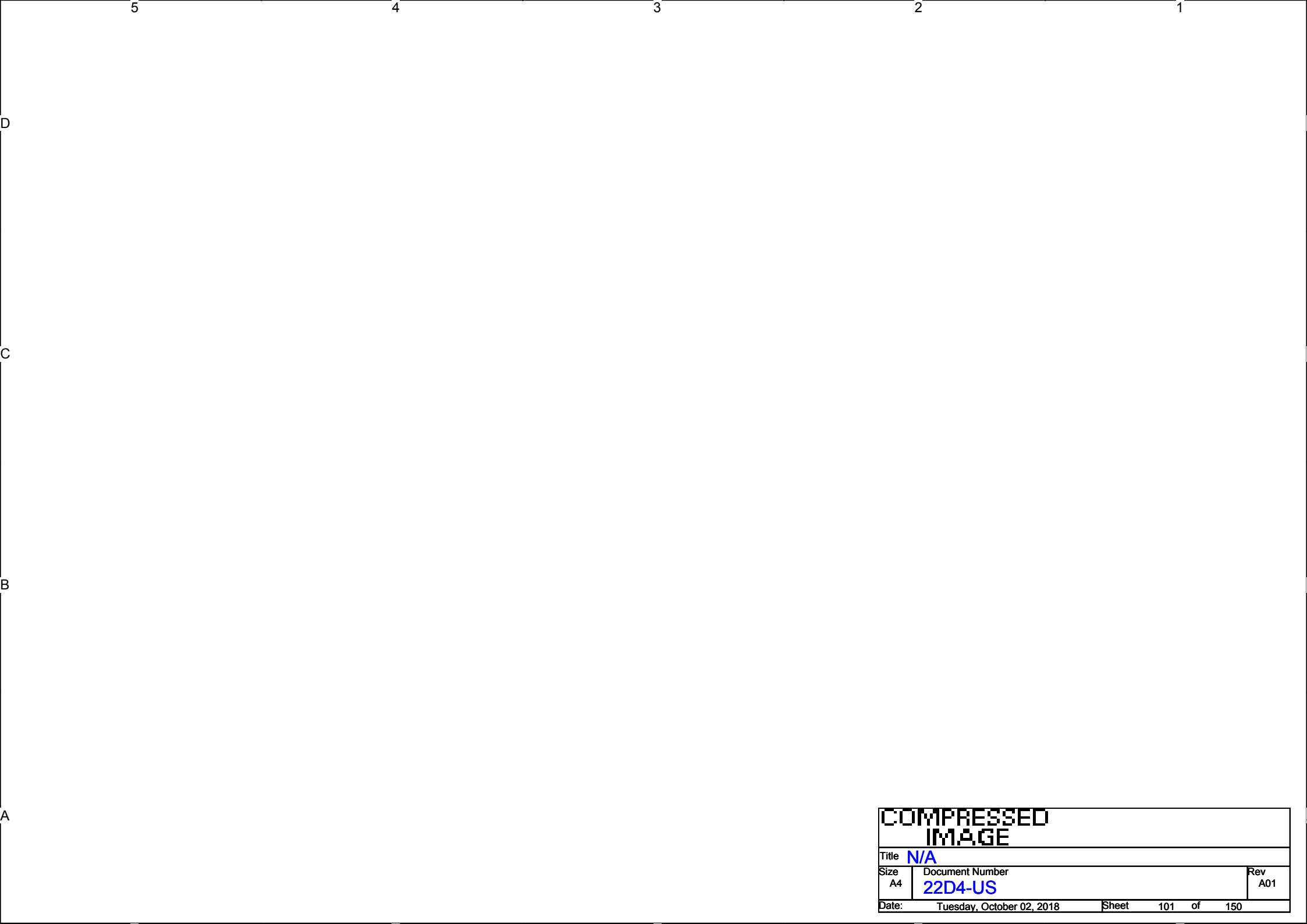
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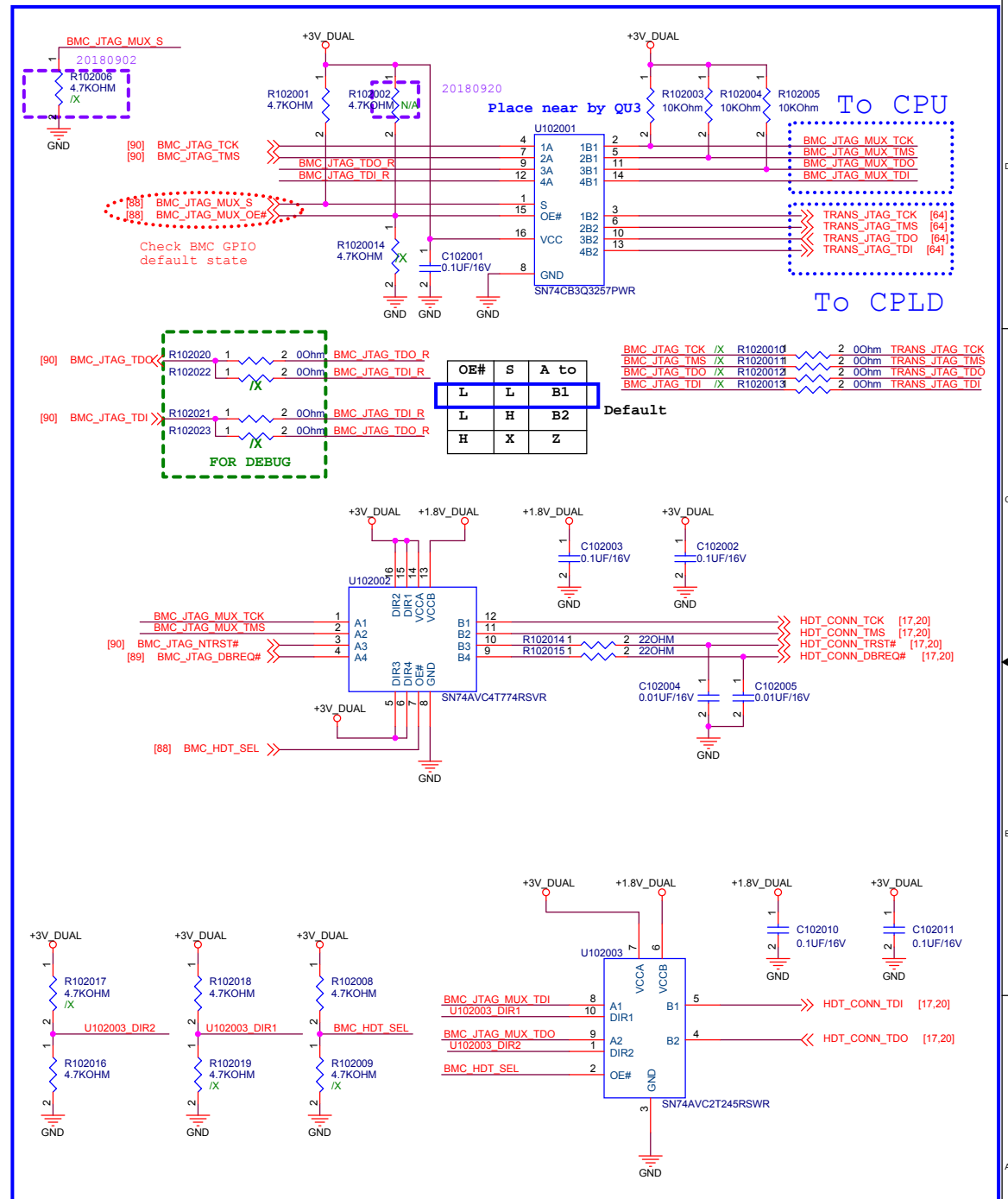
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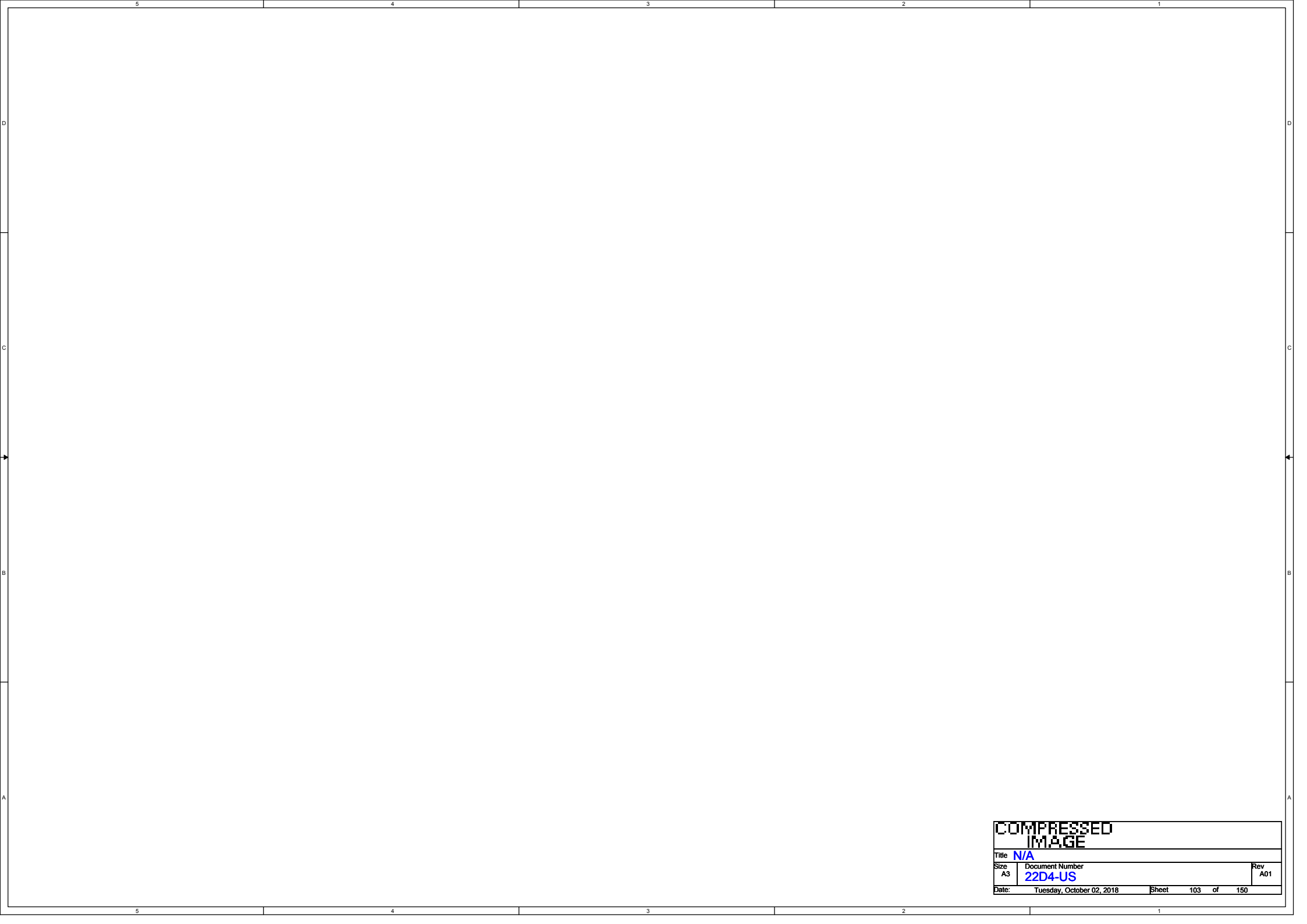
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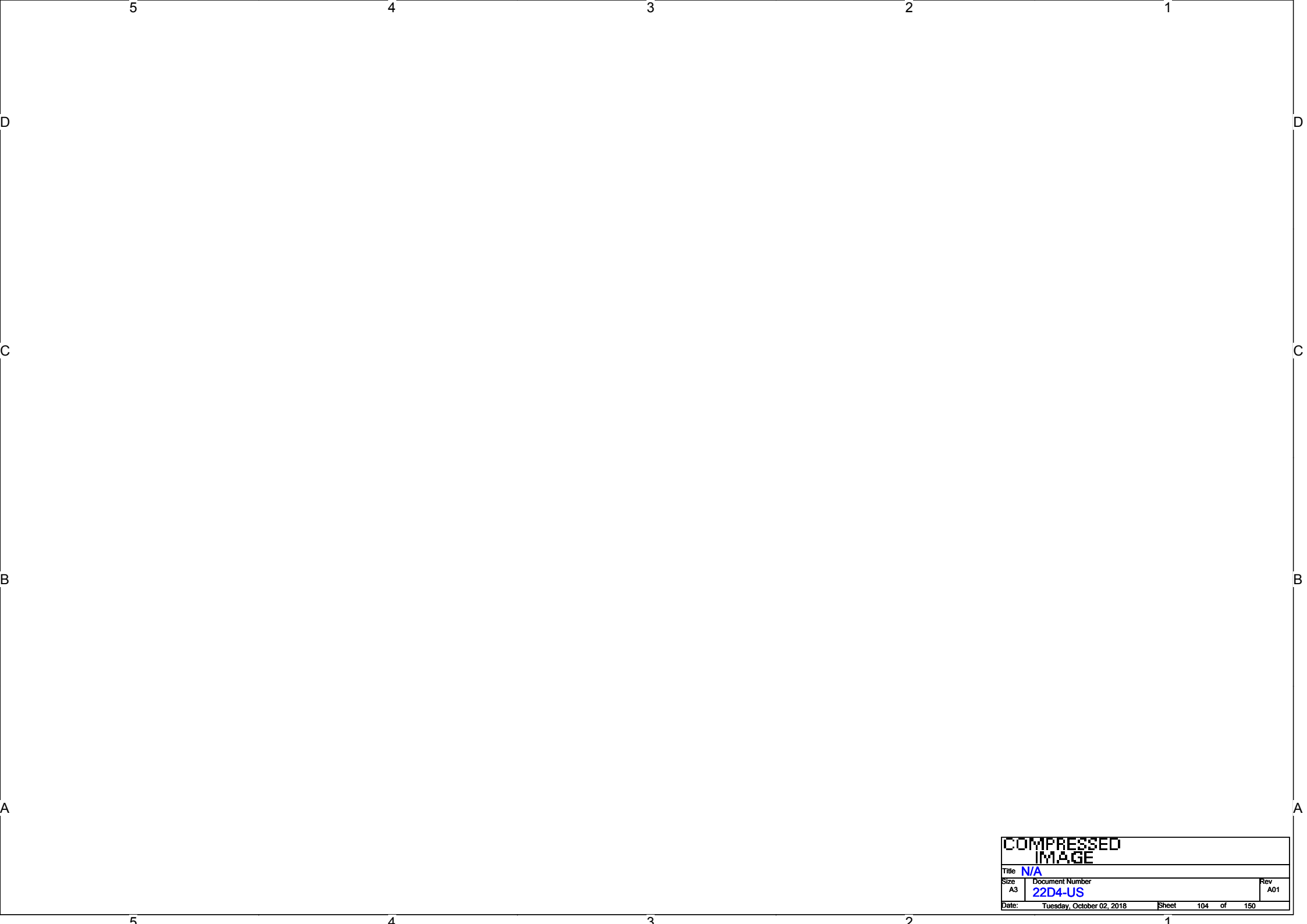
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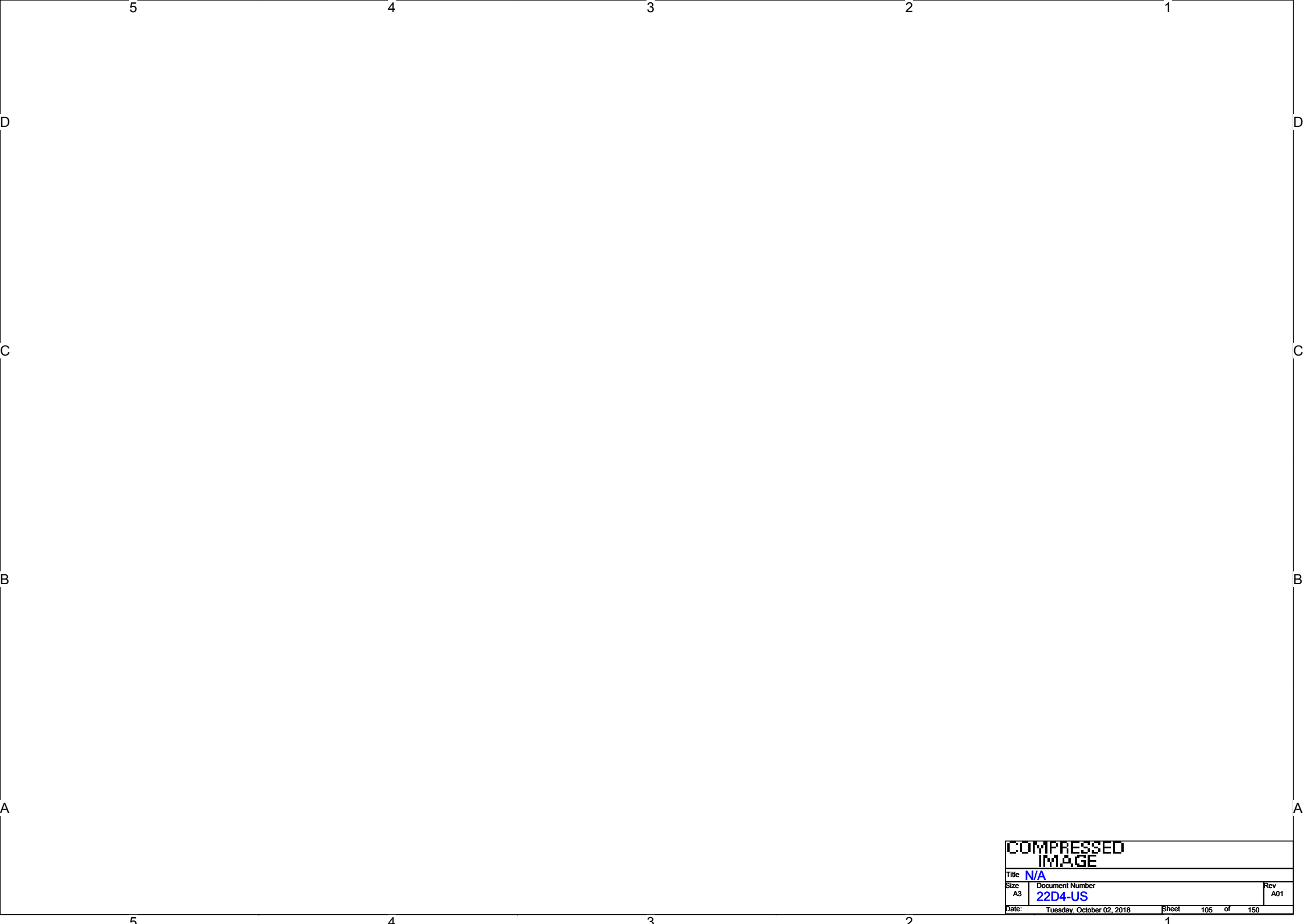
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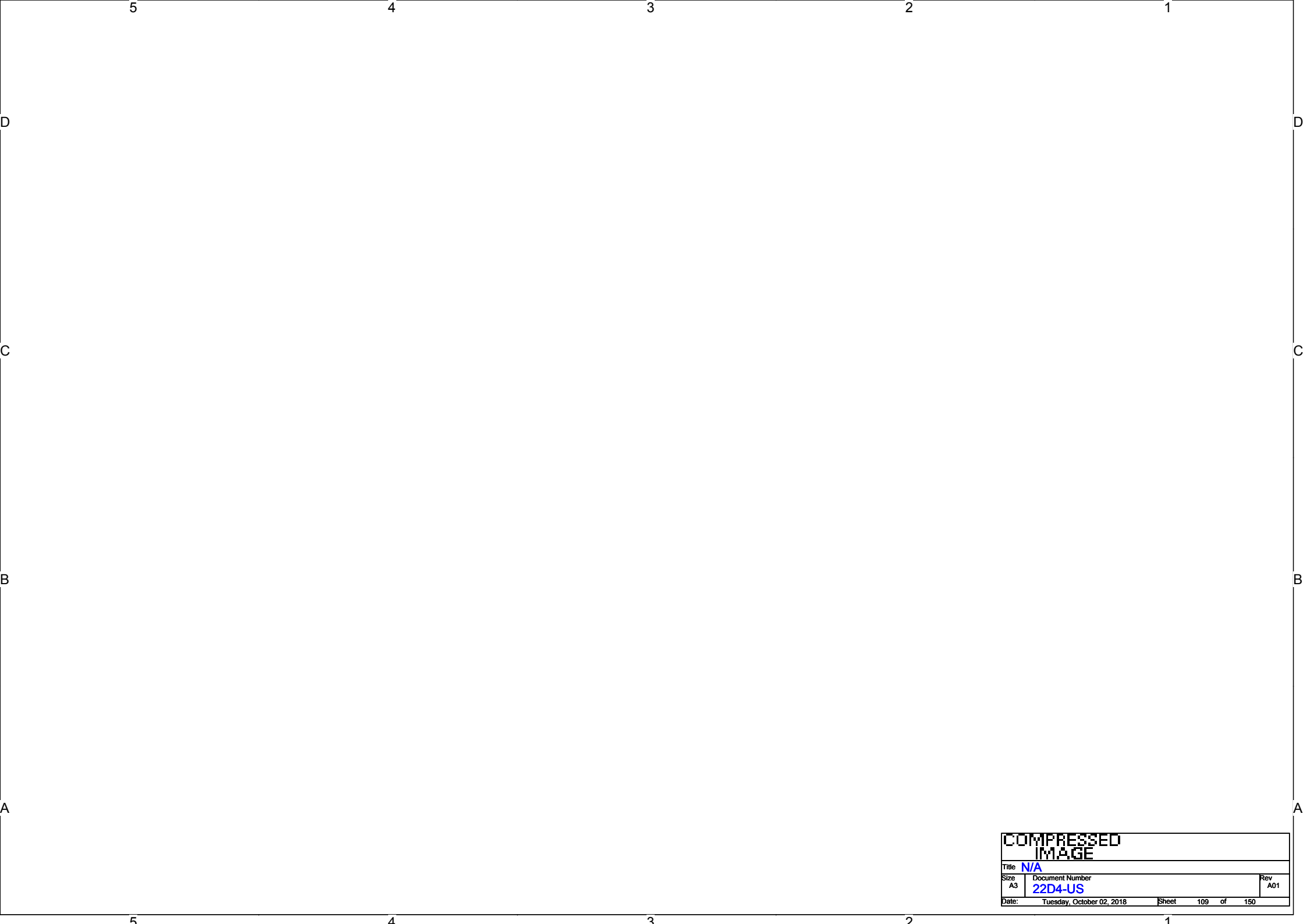
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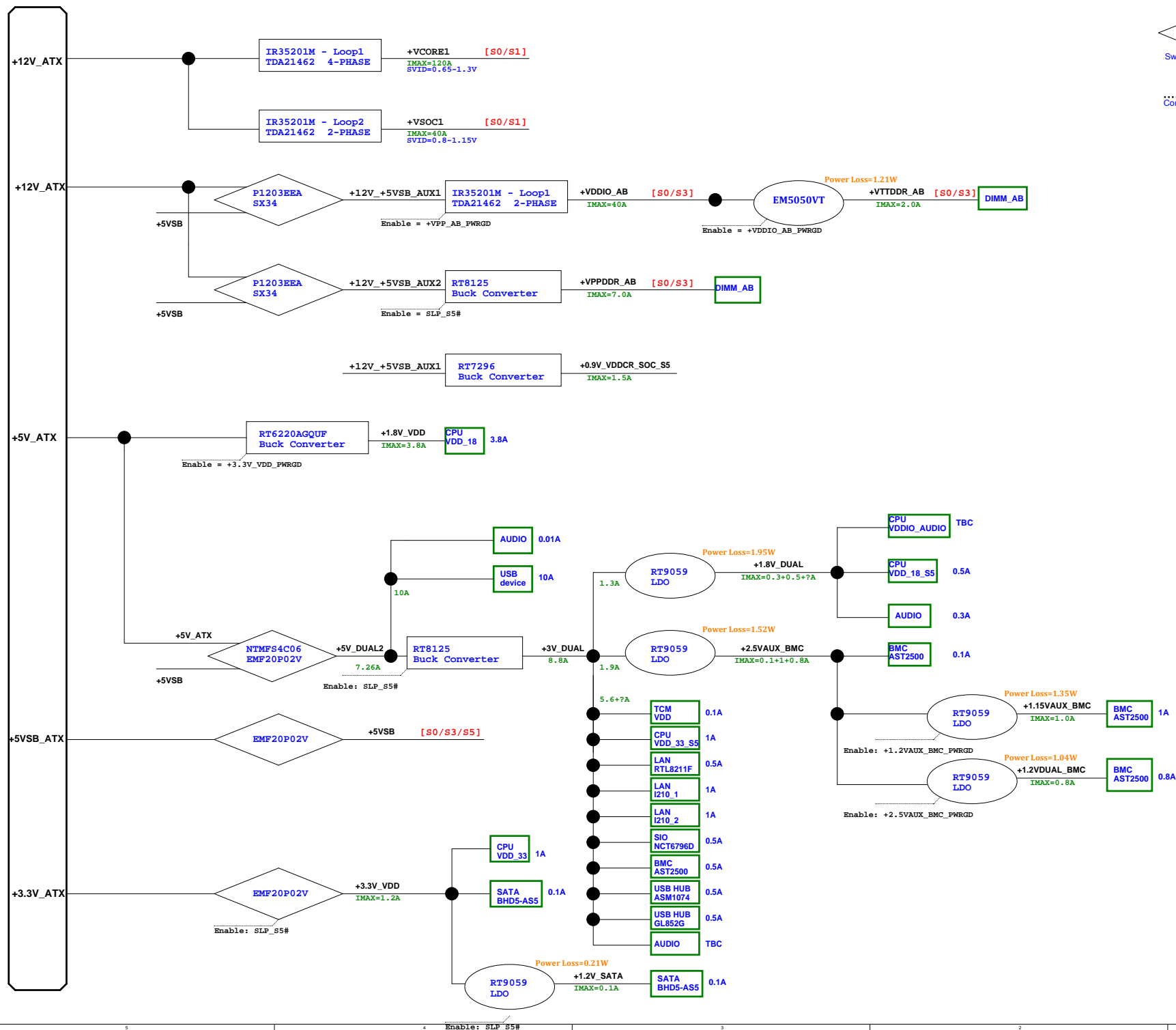
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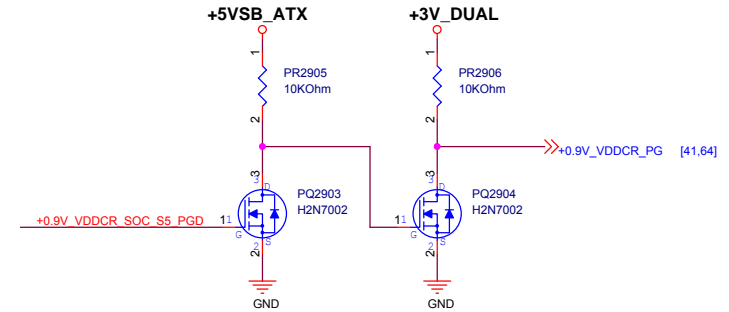
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IMAGE

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+0.9V_VDDCR_SOC_S5_PWRGD



$$D = V_{out}/V_{in} = 0.9/12 = 0.075$$

$$I_{ripple} = 1.5 * (D * 1 - D) = 1.5 * ((0.075) * (0.925)) = 0.395A$$

$$I = ((V_{in} - V_{out}) * D_{duty}) / (L_{out} * f_{sw})$$

$$= ((12V - 0.9V) * (0.9V/12V)) / (2.2 * 500KHz) = 0.756A$$

$$I_{(L(peak))} = I_{o(rms)} + I \quad I/2 = 1.5A + 0.378A = 1.878A$$

$$\text{Output } ESR < V_o(\text{ripple}) / I$$

$$= 70mV / 0.758A = 92.6m$$

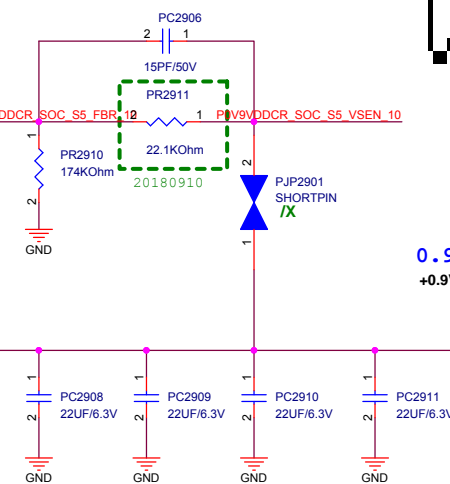
$$C = I_{out} * t_{off} / \Delta V$$

$$= 1.878 * [(1/500kHz) * ((12 - 0.9)/12)] / 50mV$$

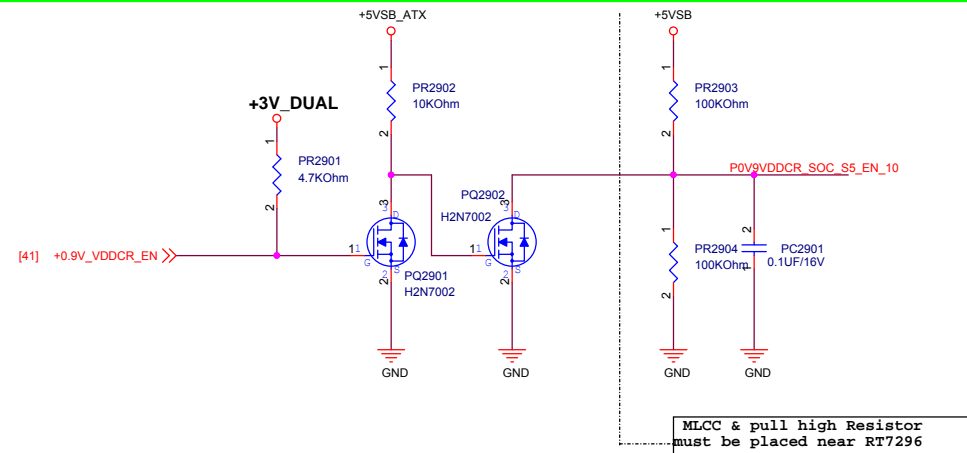
$$\Delta C = 69.49\mu F$$

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IMAGE

0.9V/1.5A
+0.9V_VDDCR_SOC_S5

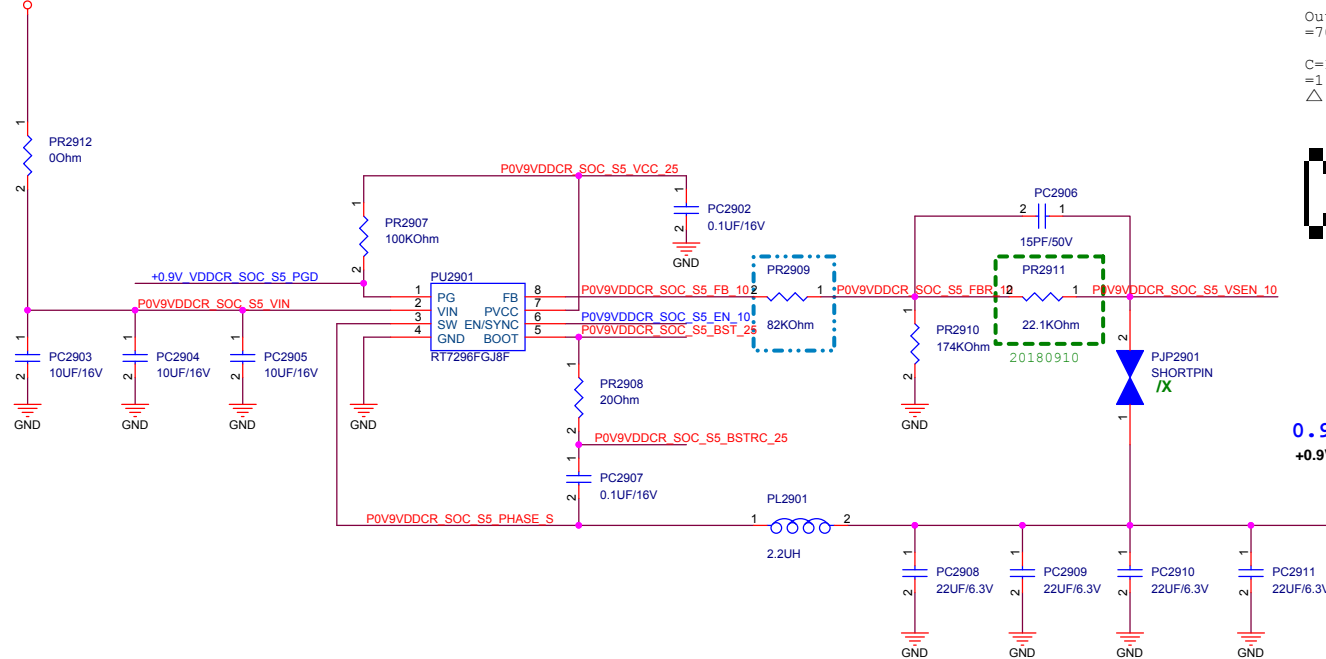


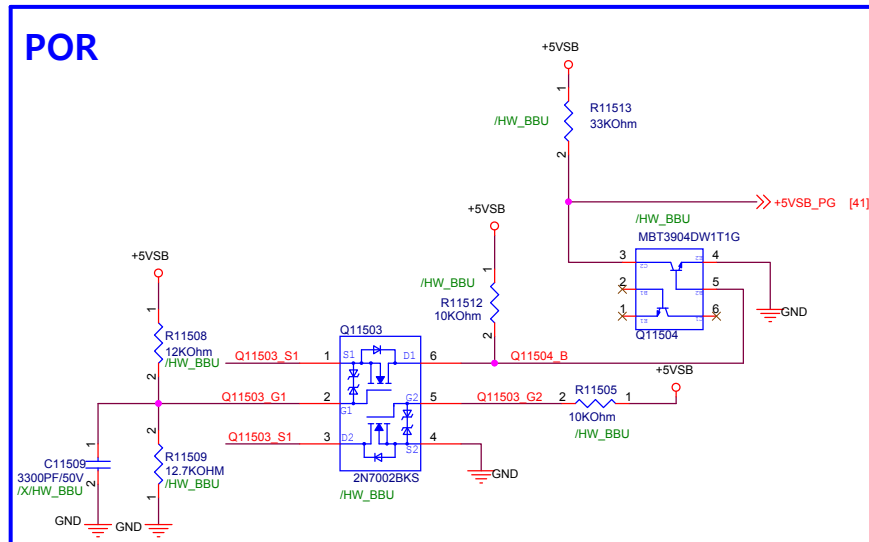
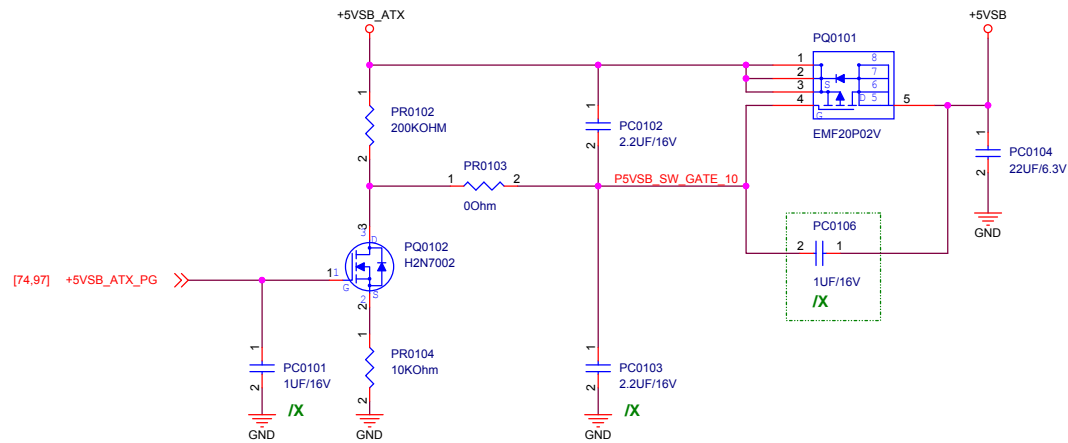
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MLCC & pull high Resistor must be placed near RT7296

PVDDIO_VINREG_S

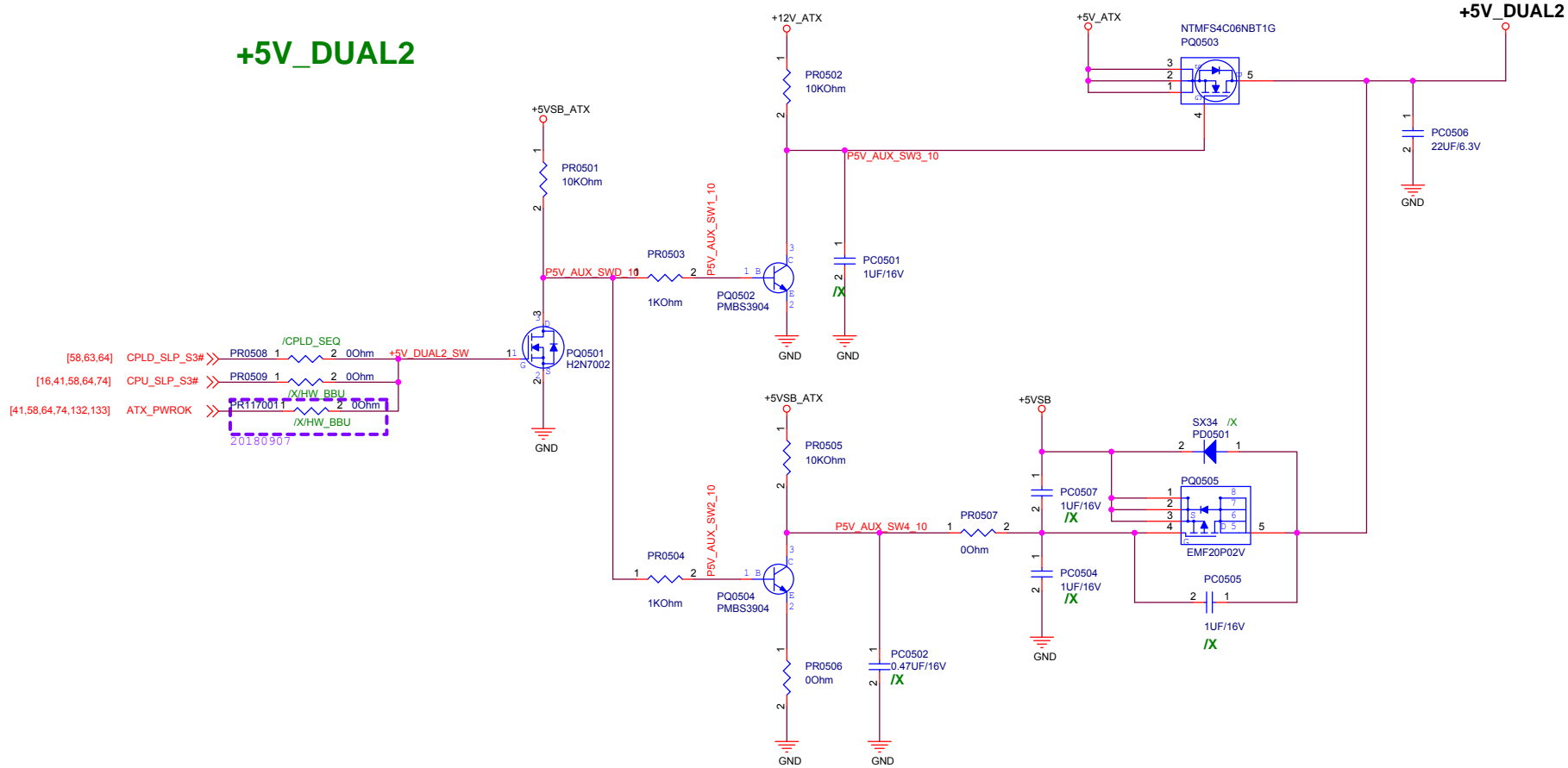




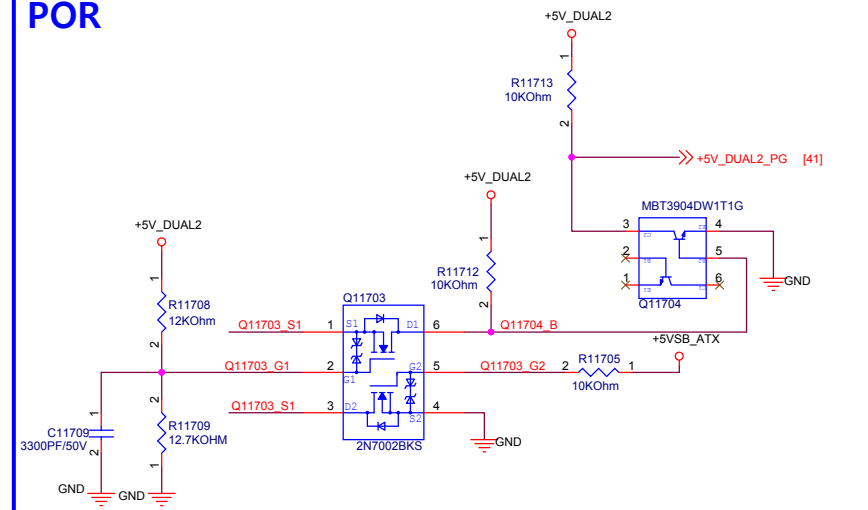


COMPRESSED IMAGE			
Title	N/A		
Size	A2		
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Rev	A01		

+5V_DUAL2



POR



COMPRESSED
IMAGE

Title +5V_DUAL2		Rev A01
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+5V_DUAL2

COMPRESSED
IMAGE

FEUB063T-R33MS
DCR=3.5mohm
IDC=21A, ISAT=25A
7x7x3

PL0601
0.33uH

P5VDUAL2_VINREG_S

PC0603
1uF/16V

PCE0601
270uF/16V

PR0601
0Ohm

P3VDUAL_BSTR_25

PR0603
0Ohm

PC0606
0.1uF/16V

P3VDUAL_UGR_25

PR0604
10KOhm

P3VDUAL_UG_25

PR0605
0Ohm

P3VDUAL_VCC_25

PC0607
1uF/16V

P3VDUAL_LG_25

PR0606
15.8KOhm

P3VDUAL_LG_25

PC0608
1000PF/50V

P3VDUAL_SNRC_25

PR0607
10Ohm

P3VDUAL_VSEN_10

P3VDUAL_REFOUT_10

PR0602
1KOhm

P3VDUAL_REFIN_10

PC0604
1000PF/50V

PC0605
1000PF/50V

+3V_DUAL

20180910

PR0614
10KOhm

[41] PU0601_PG <<

RT8125DGQW

GND3

GND2

GND1

REFOUT

REFIN

PGOOD

EN

LGATE/OCSET

VCC

FB

BOOT

UGATE

PHASE

FB

VCC

FB

VCC

Enable: Open Drain
Disable: Low

[41,130] +5V_DUAL2_PG_OR >>

PC0612
0.01uF/16V

PR0612
82.5KOhm

PC0611
10PF/50V

PR0611
10KOhm

PC0610
100PF/50V

PR0608
0Ohm

P3VDUAL_FB_10

PR0610
0Ohm

P3VDUAL_FBR_10

PR0609
32.4KOhm

P3VDUAL_FBR_10

PR0608
0Ohm

P3VDUAL_FB_10

PC0610
100PF/50V

P3VDUAL_FB_10

PR0608
0Ohm

P3VDUAL_FB_10

PC0610
100PF/50V

P3VDUAL_FB_10

PR0608
0Ohm

P3VDUAL_FB_10

PC0610
100PF/50V

P3VDUAL_FB_10

PR0608
0Ohm

P3VDUAL_FB_10

PC0610
100PF/50V

P3VDUAL_FB_10

PR0608
0Ohm

P3VDUAL_FB_10

PC0610
100PF/50V

P3VDUAL_FB_10

Vout = 0.8V * (1 + 32.4k / 10k) = 3.396V

+3V_DUAL Power rail - Output MLCC
(close to CPU Power Rail)

Output capacitors
(Place at the VR output)

Output capacitors
(Close to I/O)

+3V_DUAL

PC0613
22uF/6.3V

PC0614
22uF/6.3V

PC0615
22uF/6.3V

PC0616
22uF/6.3V

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

N/A

COMPRESSED
IMAGE

Title +3V_DUAL

Size A3

Document Number

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Rev

A01

$D = V_{out}/V_{in} = 3.3/5 = 0.66$
 $I_{ripple} = I_o * (D * 1 - D) = 9 * ((0.66) * (0.34)) = 4.27A$
 $I = ((V_{in} - V_{out}) * D * Duty) / (L * Out * F_{sw})$
 $= ((5V - 3.396V) * (3.396V / 5V)) / (1 * 300KHz) = 3.63A$
 $I_{(L(peak))} = I_o(rms) + I/2 = 9A + 1.815A = 10.82A$
 $Output\ ESR < V_o(ripple) / I$
 $= 50mV / 3.63A = 13.78m$
 $C = I_{out} * t_{off} / V = 9 * [(1 / 300KHz) * (1 - D)] / 50mV$
 $\Delta C = 137.49\ \mu F$

Io=9.0A
Io_limit=16.3A

Io_limit=Rocset*10uA/Rdson
=15.8k*10uA/10.8m = 14.63A

PQH0601
NTMFS4C10NB1G
BMRBAS0606301R0MA1
DCR=6.1mohm
IDC=12A, ISAT=15A
7x7x3

COMPRESSED
IMAGE

PL0602
1uH

+3V_DUAL

PC0609
1000PF/50V

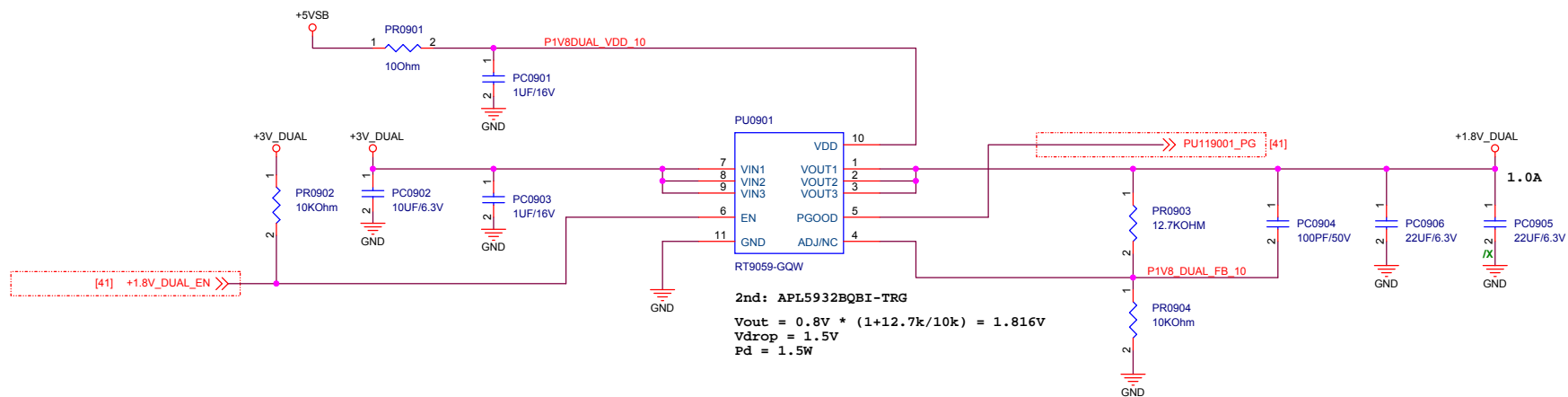
P3VDUAL_SNRC_25

PR0607
10Ohm

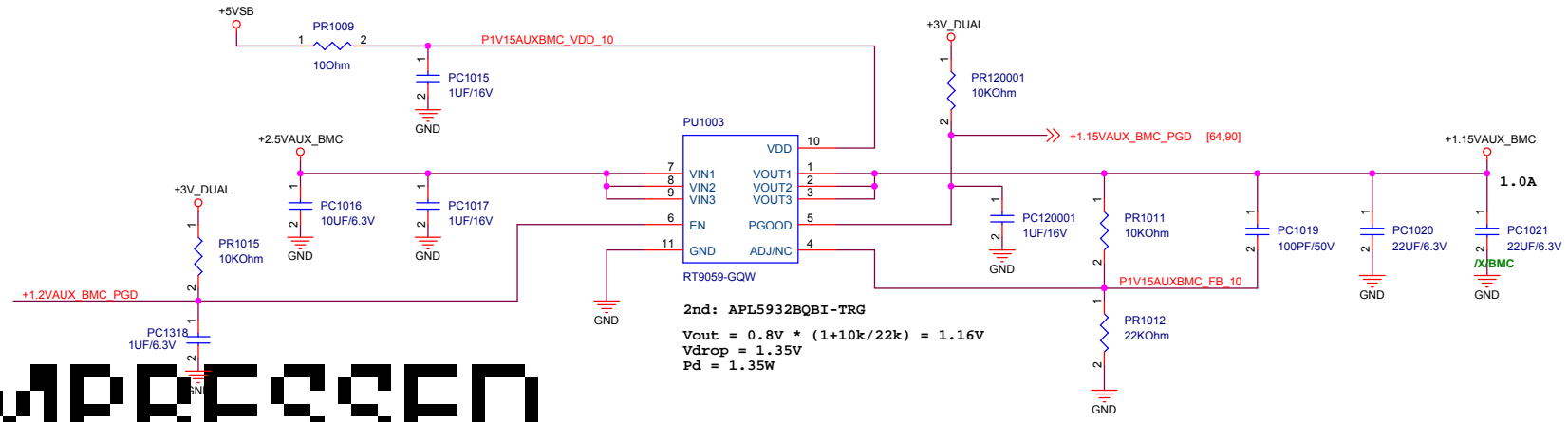
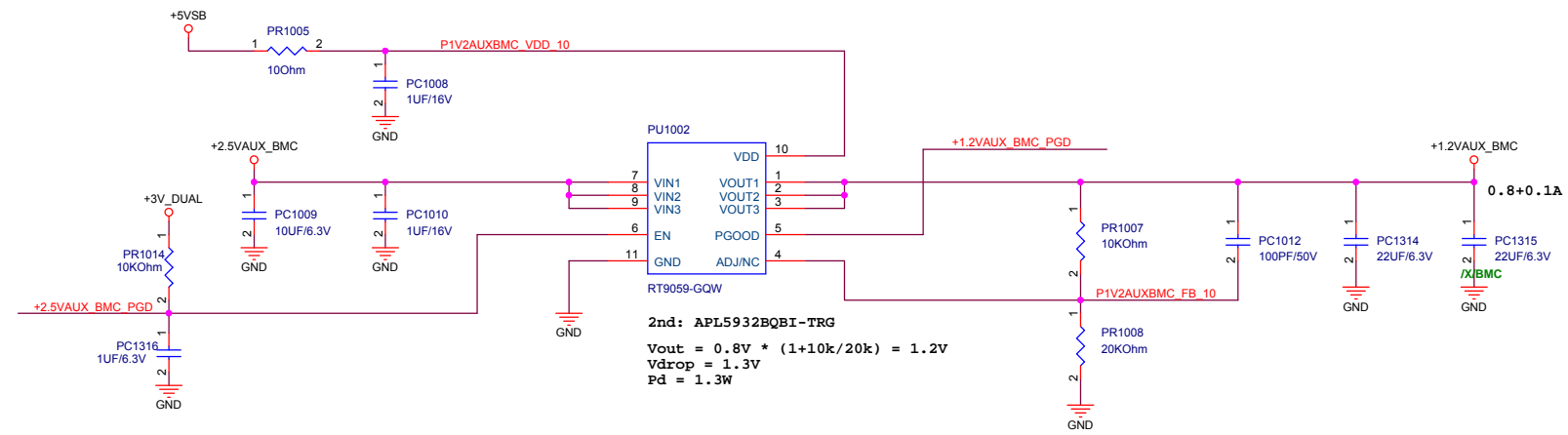
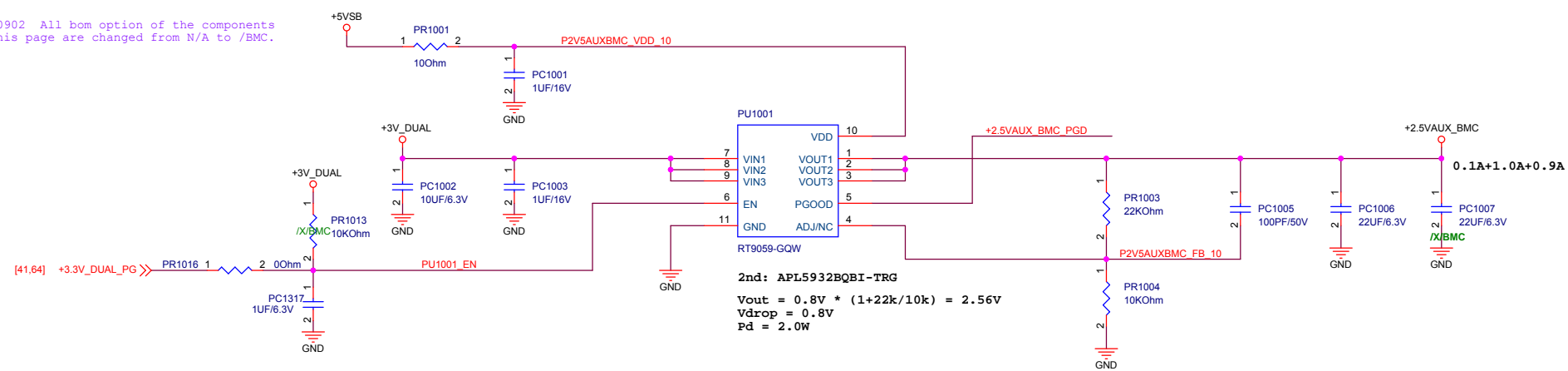
P3VDUAL_VSEN_10

PJP0601
SHORTPIN

/X

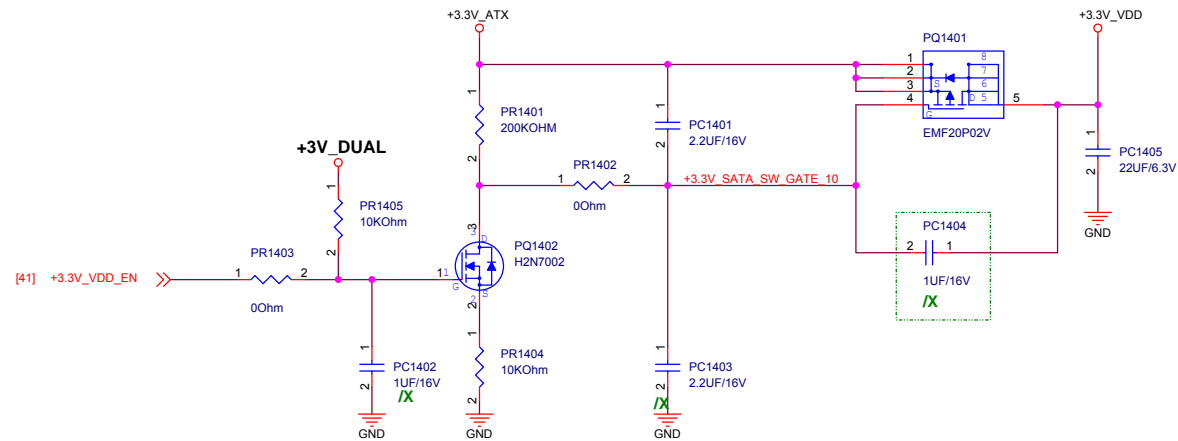


20180902 All bom option of the components
in this page are changed from N/A to /BMC.



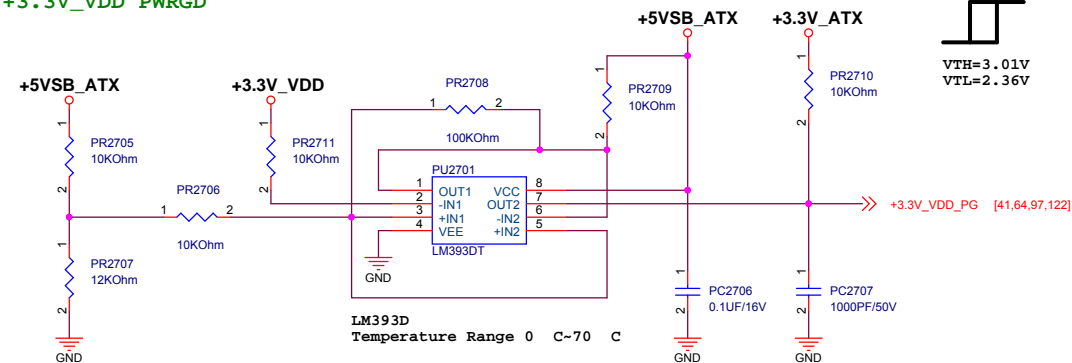
COMPRESSED
IMAGE

COMPRESSED IMAGE		
Title	PWR AST2500	
Size	Document Number	Rev
A3	22D4-US	A01
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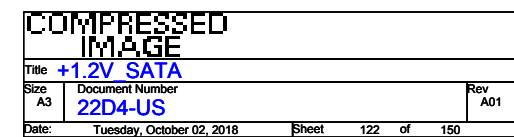
ROOM: +3.3V_VDD
Ref. Schematic: N/A

+3.3V_VDD PWRGD



COMPRESSED
IMAGE

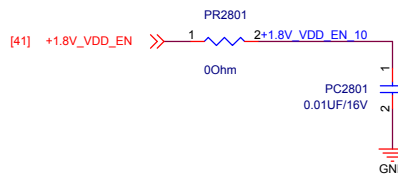
Title		+3.3V_VDD	
Size	Document Number	Rev	
A3	22D4-US	A01	
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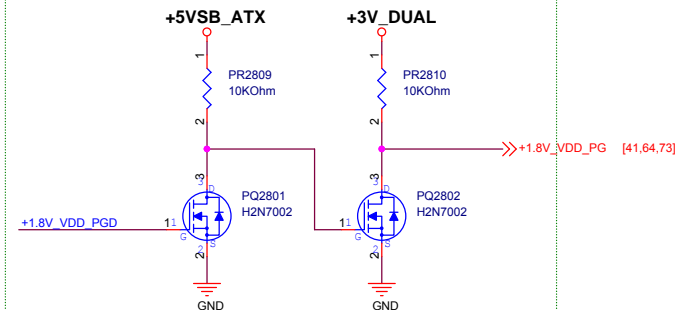


COMPRESSED IMAGE			
Title N/A			
Size A3	Document Number 22D4-US		Rev A01
Date:	Tuesday, October 02, 2018	Sheet 123 of 150	

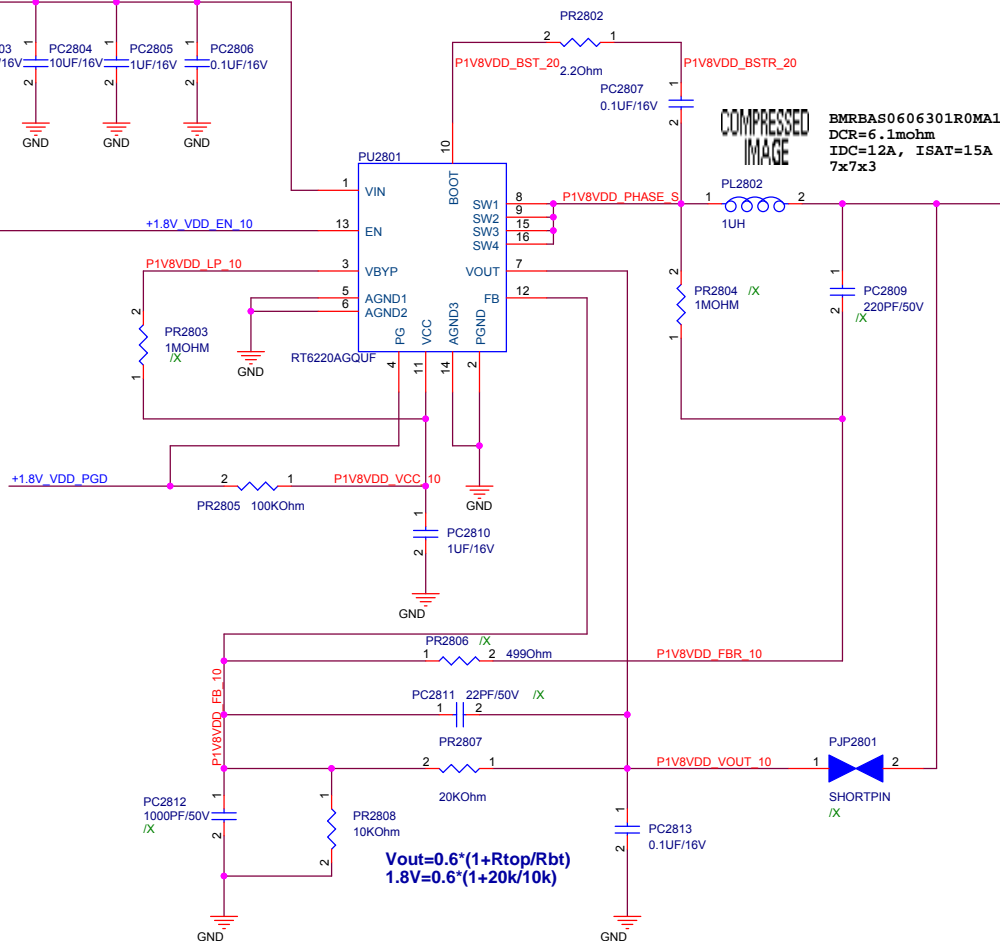
ENABLE



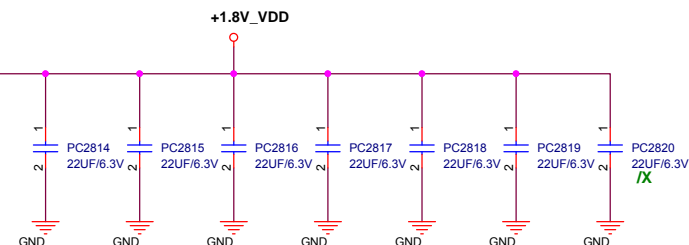
+1.8V_VDD PGD



+5V_ATX



+1.8V_VDD(3.8A)



$$D = V_{out}/V_{in} = 1.8/5 = 0.36$$

$$I_{ripple} = I_o * (D * (1-D)) = 3.8 * ((1.8/5) * (3.2/5)) = 1.824A$$

$$I = ((V_{in} - V_{out}) * Duty) / (L * f_{sw}) = ((5V - 1.8V) * (1.8V/5V)) / (1 \mu H * 500KHz) = 2.304A$$

$$I_{(L(peak))} = I_o(rms) + I/2 = 3.8A + 1.152A = 4.952A$$

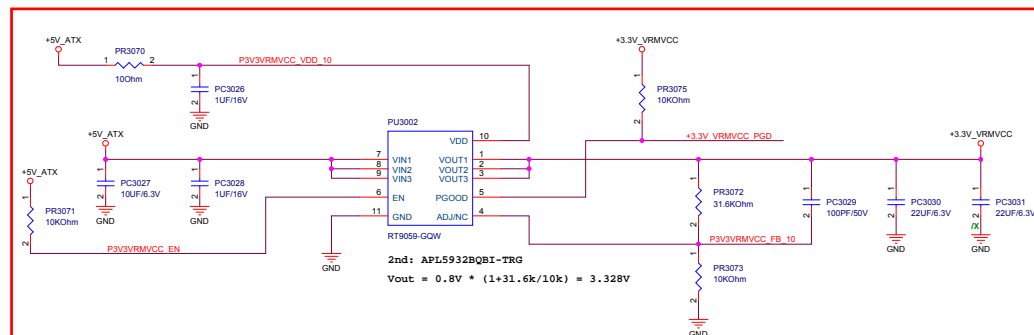
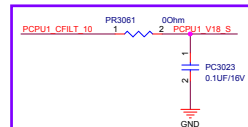
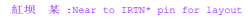
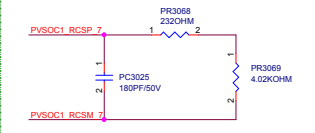
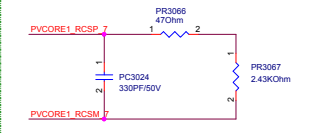
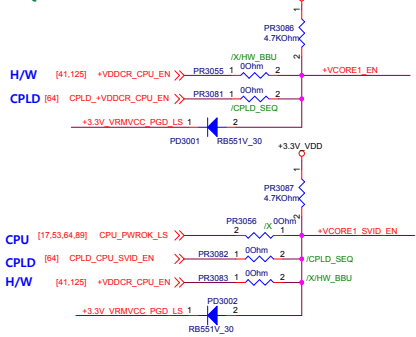
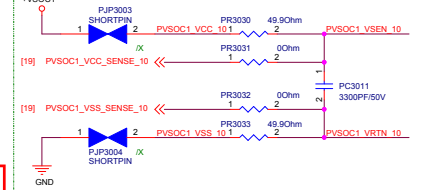
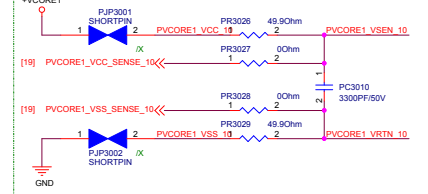
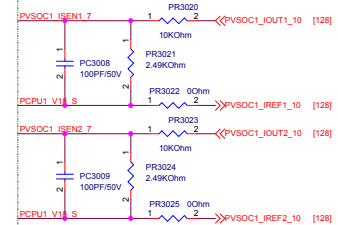
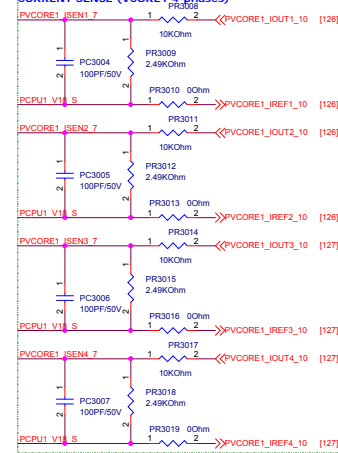
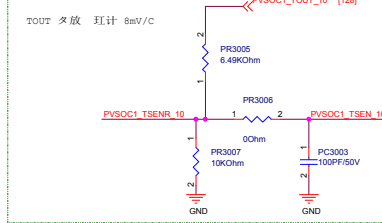
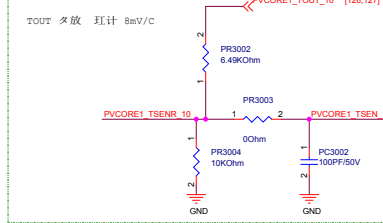
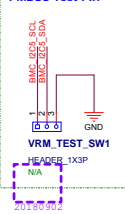
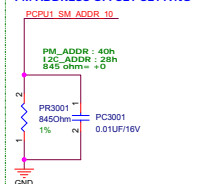
$$\text{Output ESR} < V_o(ripple) / I = 70mV / 2.304A = 30.34m$$

$$C = I_{out} * t_{off} / \Delta V = 3.8 * [(1/500kHz) * (1.8/5)] / 50mV$$

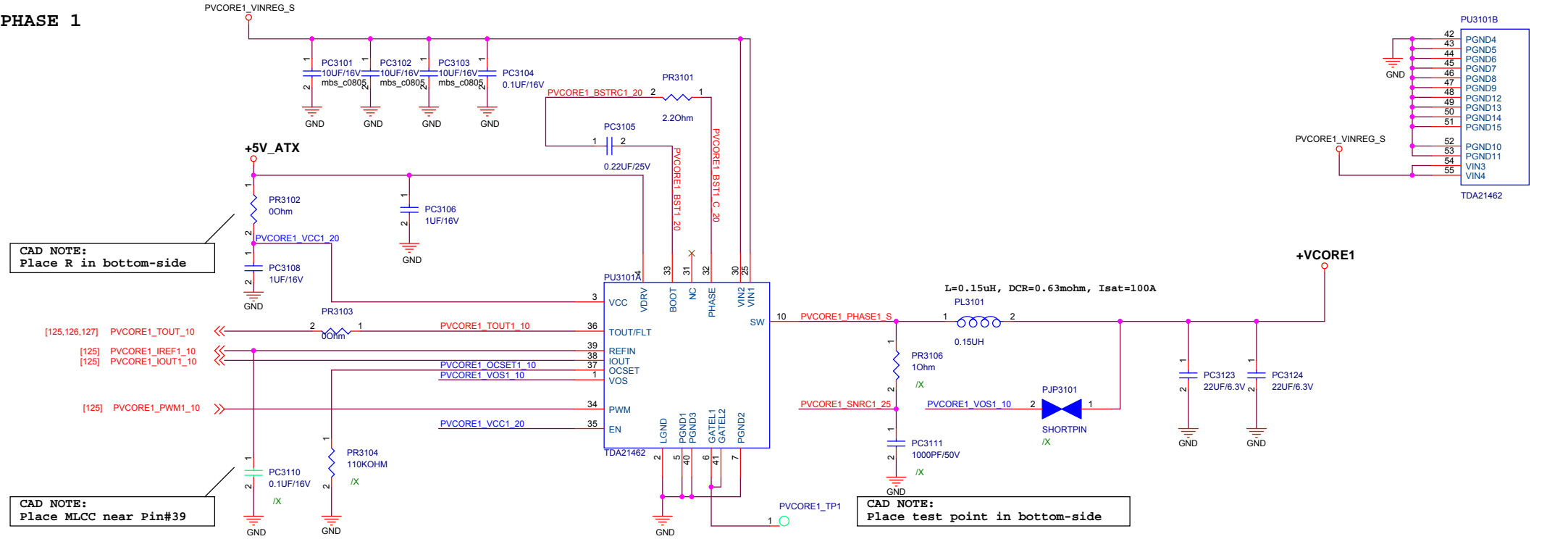
$$\Delta C = 97.28 \mu F$$

COMPRESSED IMAGE

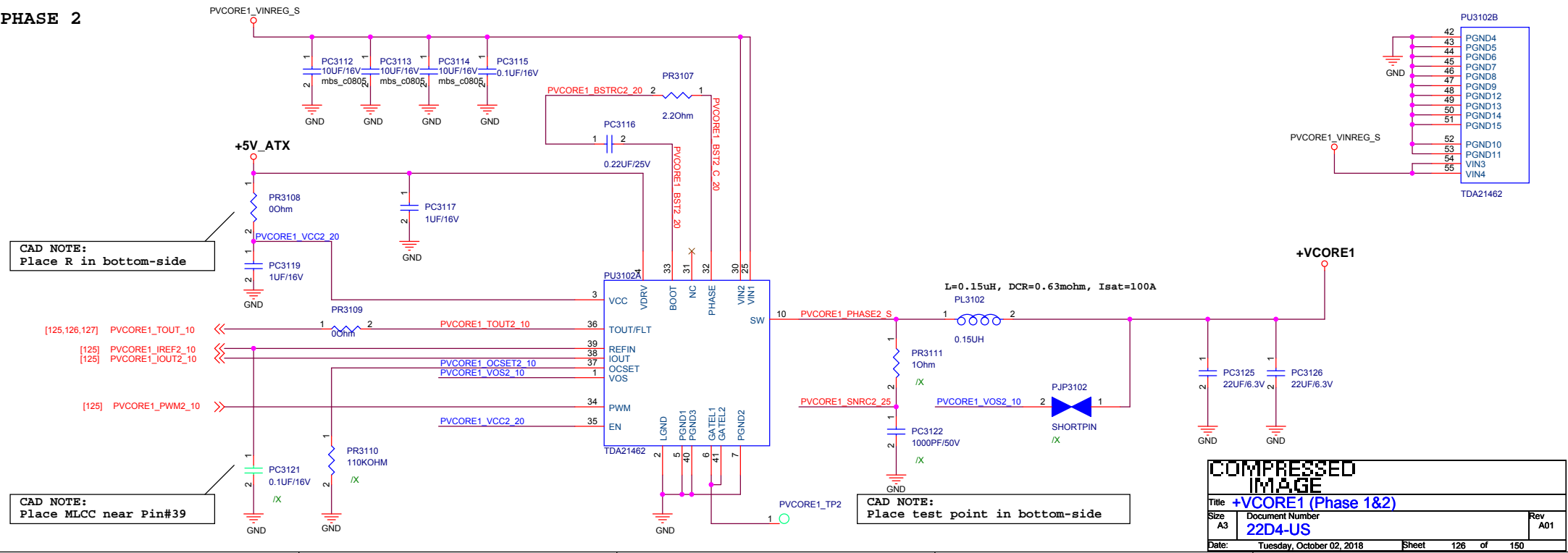
Title	+1.8V_VDD	
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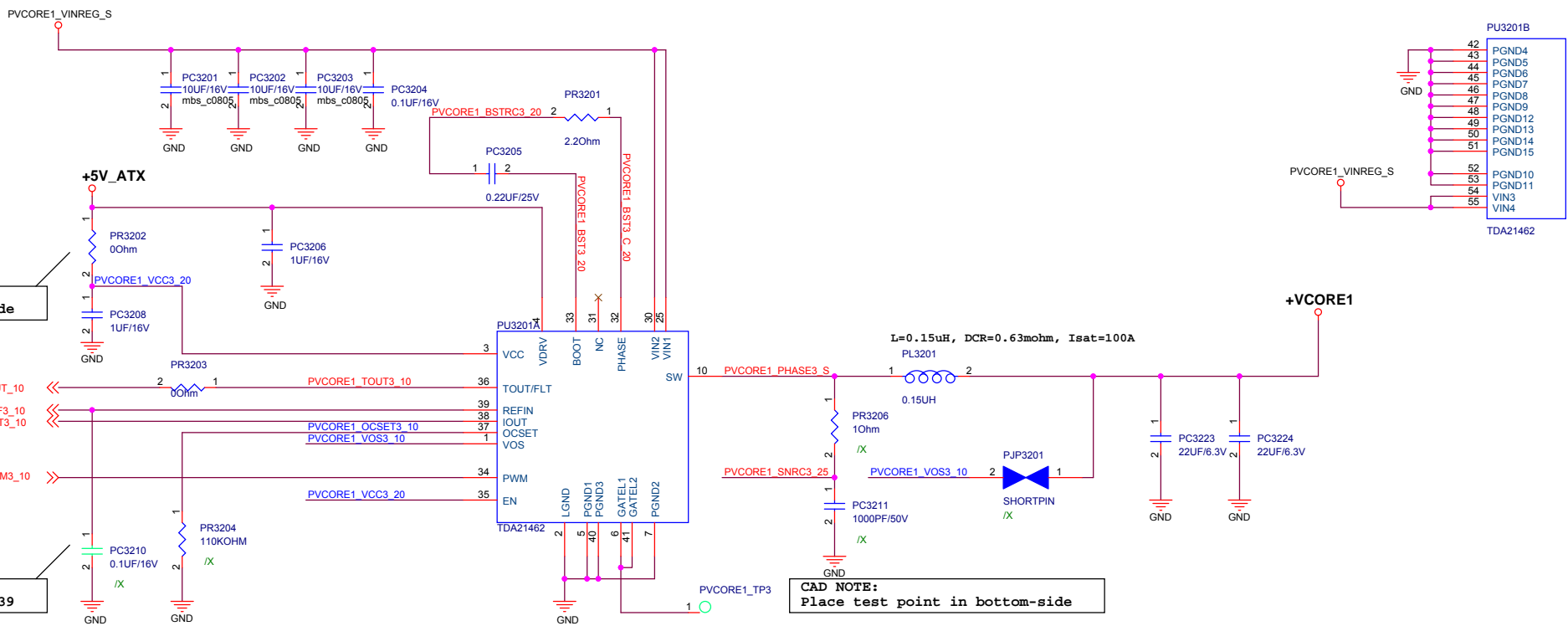
PHASE 1



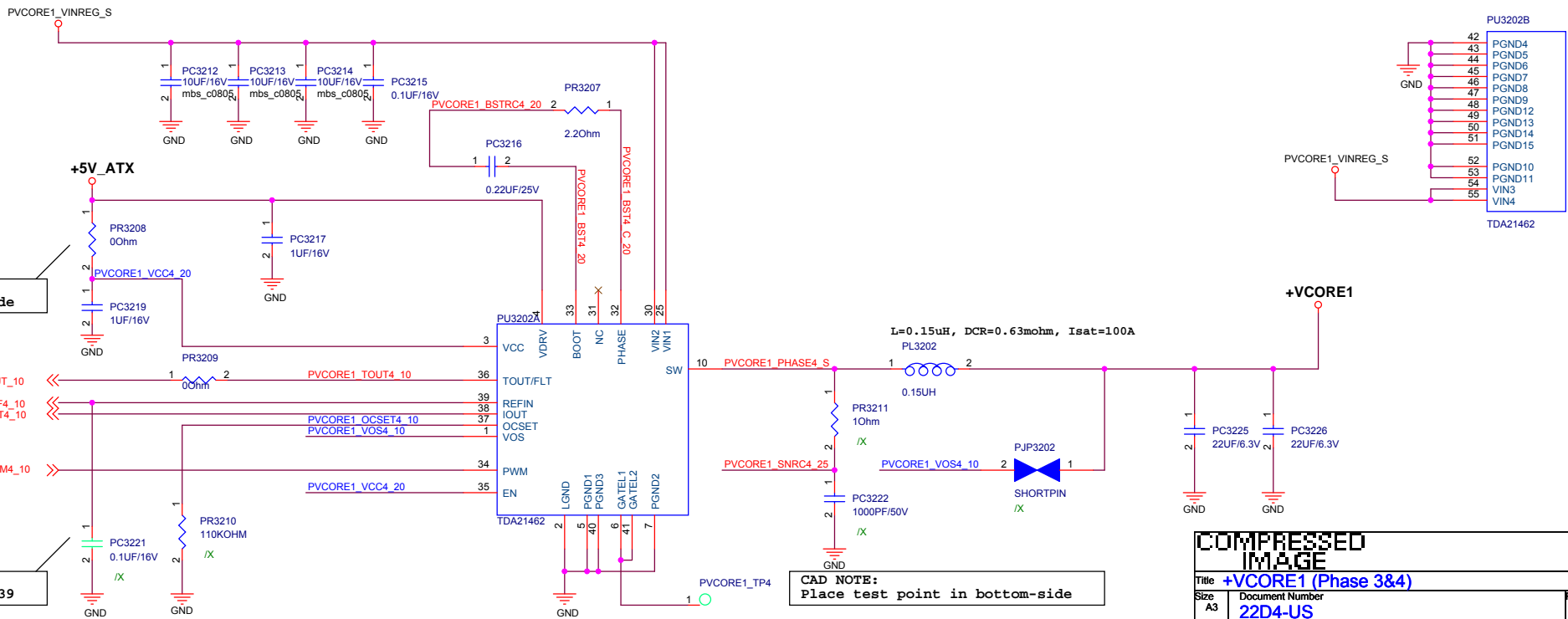
PHASE 2



PHASE 3

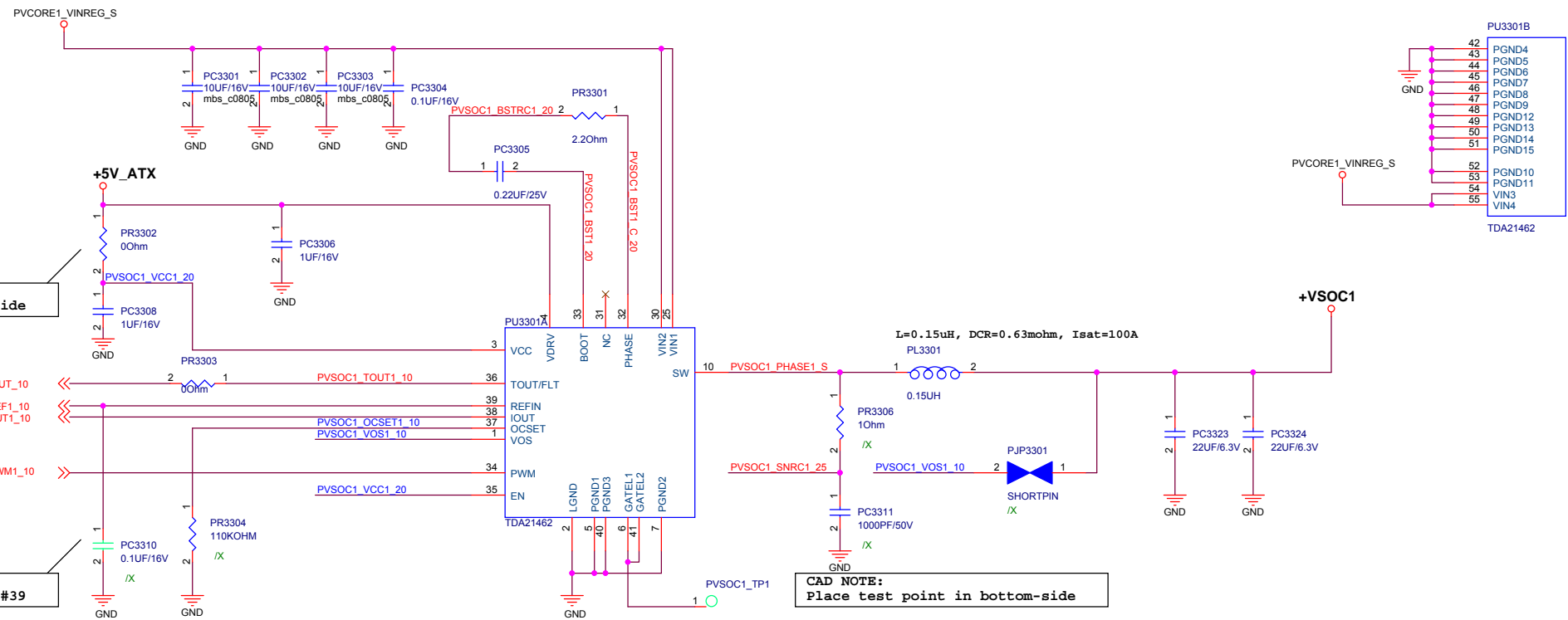


PHASE 4

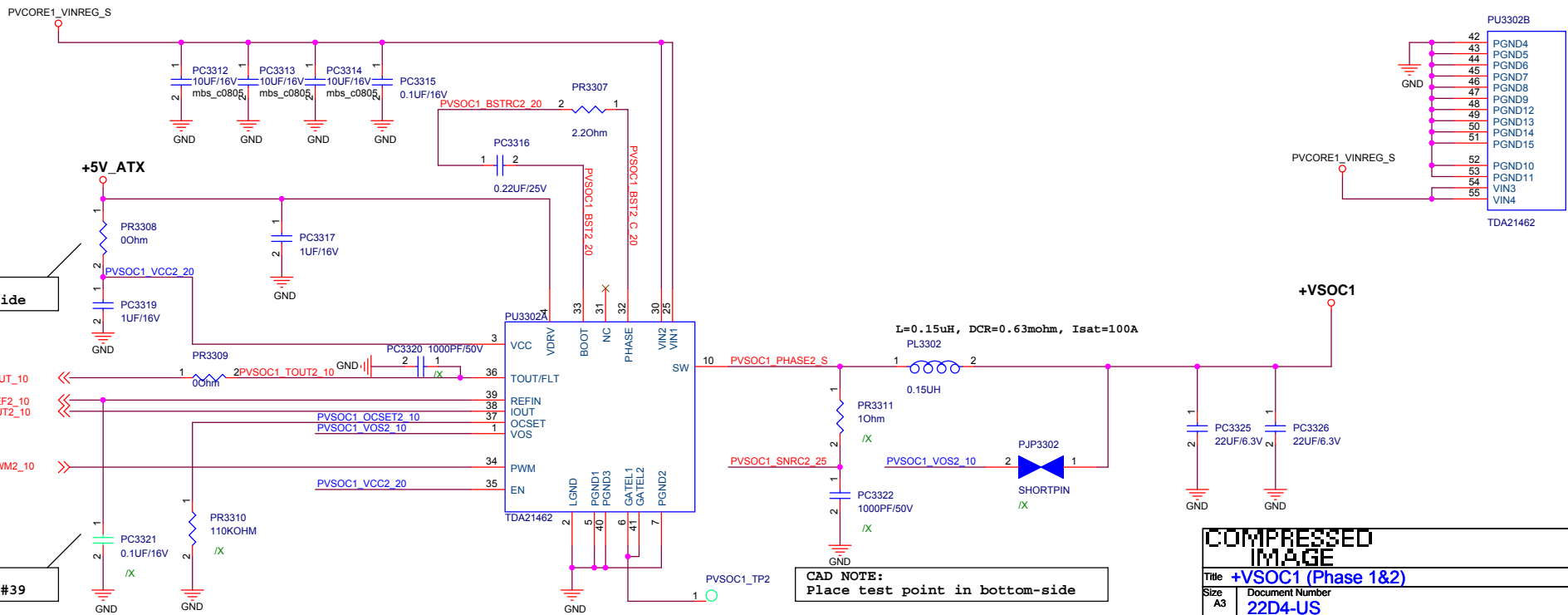


COMPRESSED IMAGE		
Title	+VCORE1 (Phase 3&4)	
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PHASE 1



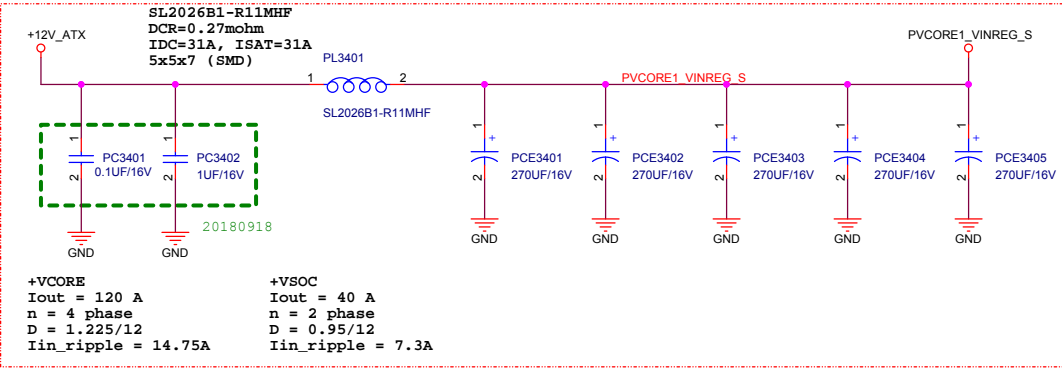
PHASE 2



**COMPRESSED
IMAGE**

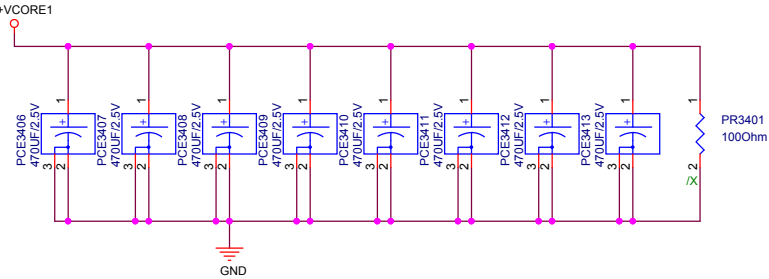
Title +VSOC1 (Phase 1&2)			
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+VCORE & +VSOC Power rail - Input Filter

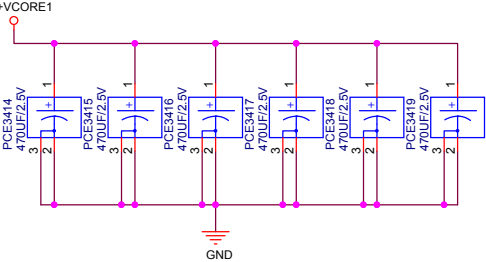


VCORE Output Caps

Output capacitors
(Placed at the BOT of VR output)
8 x 470uF (SP-CAP) replaced by 3 mOhm

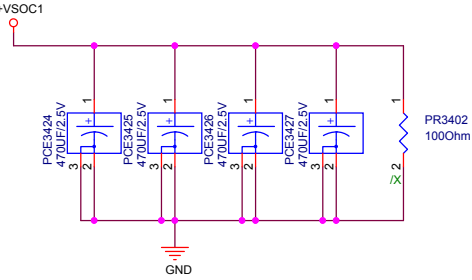


Output capacitors
(Placed at the TOP of VR output)
6 x 470uF (SP-CAP) replaced by 3 mOhm



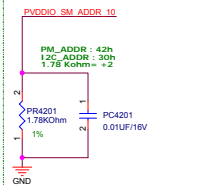
VSOC Output Caps

Output capacitors
(Placed at the BOT of VR output)
4 x 470uF (SP-CAP) replaced by 3 mOhm

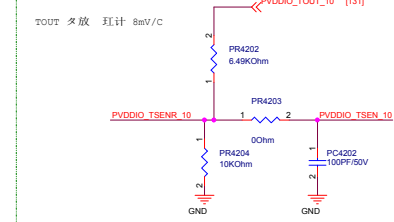


COMPRESSED IMAGE		
Title +VCORE1VSOC1_Caps		
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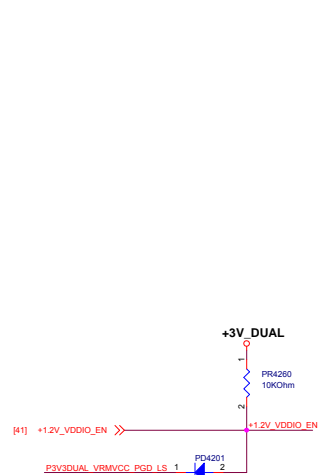
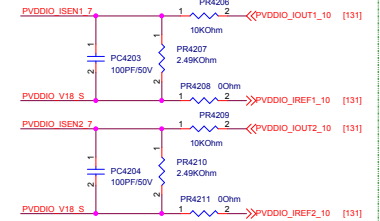
PM ADDRESS OFFSET SETTING



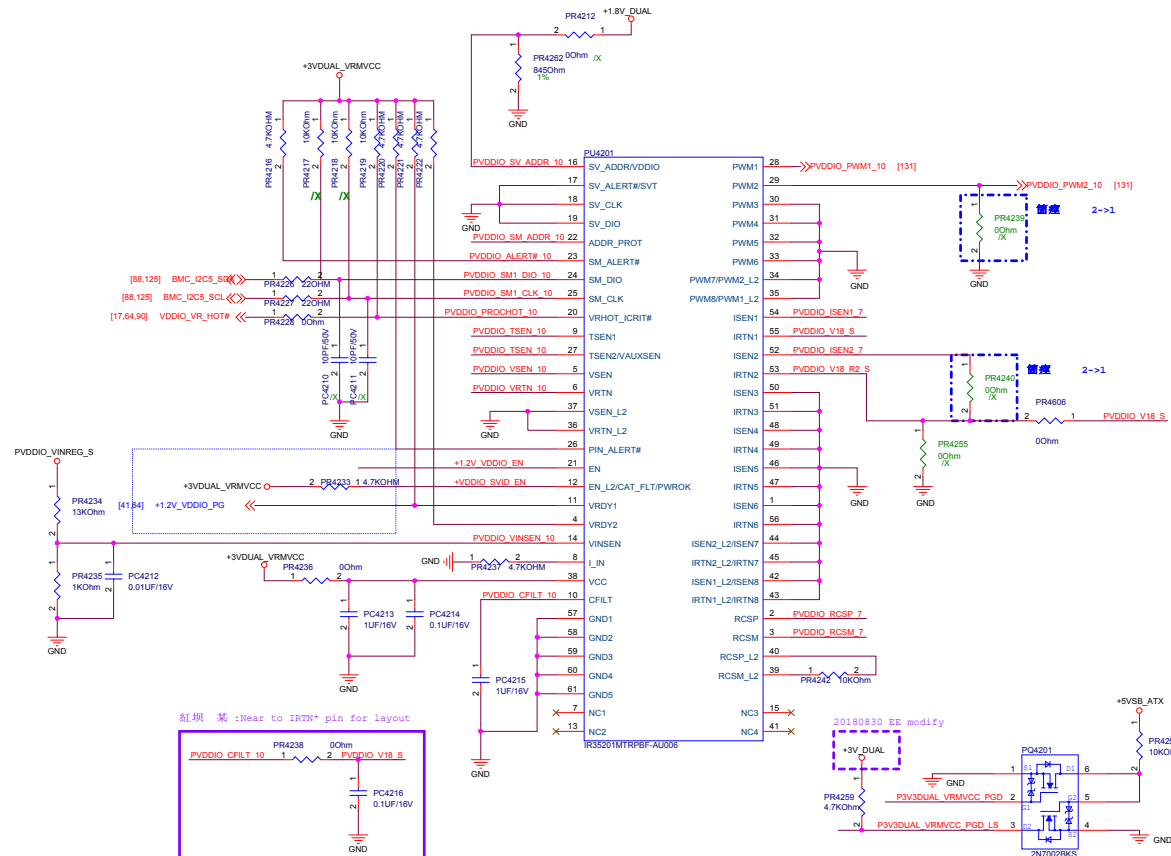
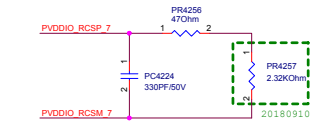
VCCIN TEMPERATURE SENSE



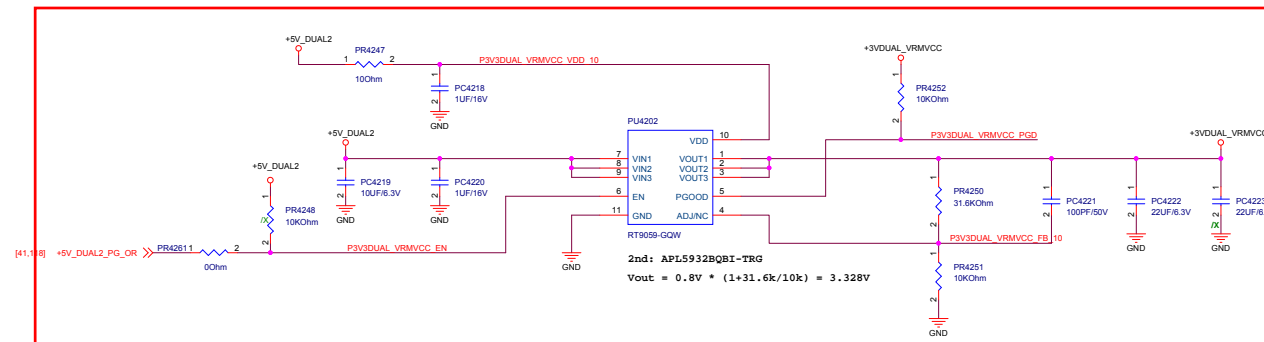
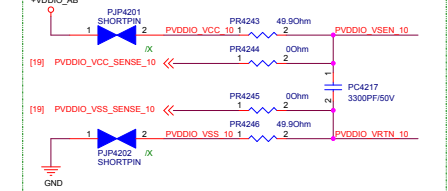
CURRENT SENSE (VDDIO 2-phases)



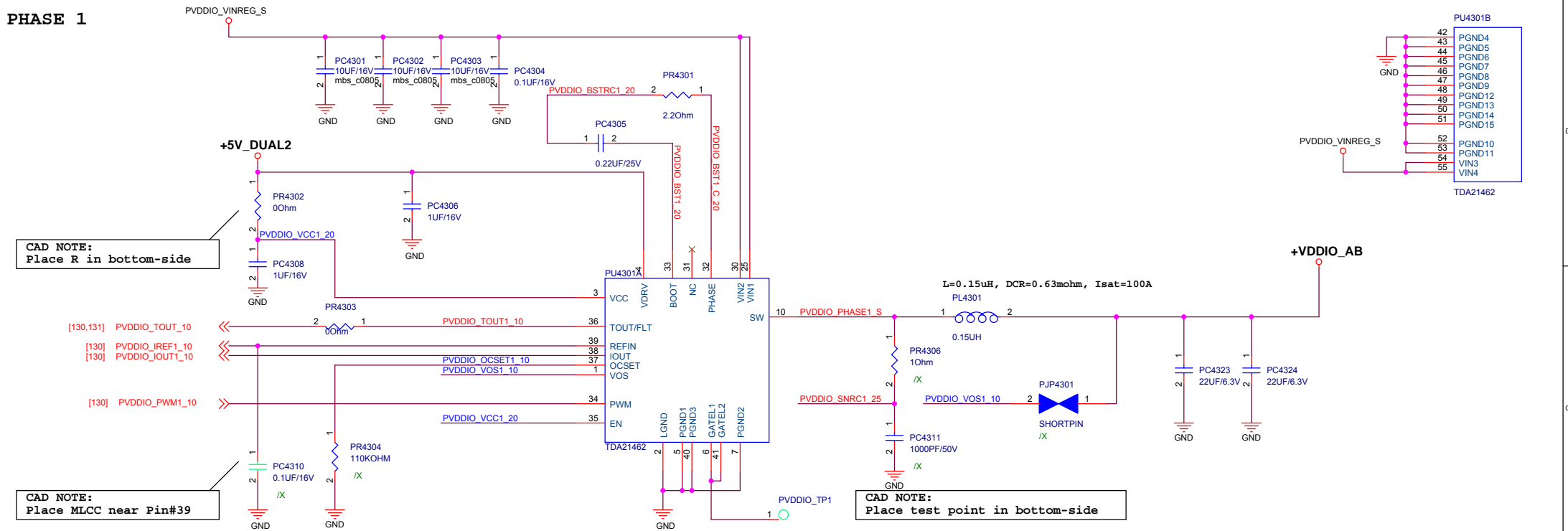
LOADLINE (VDDIO)



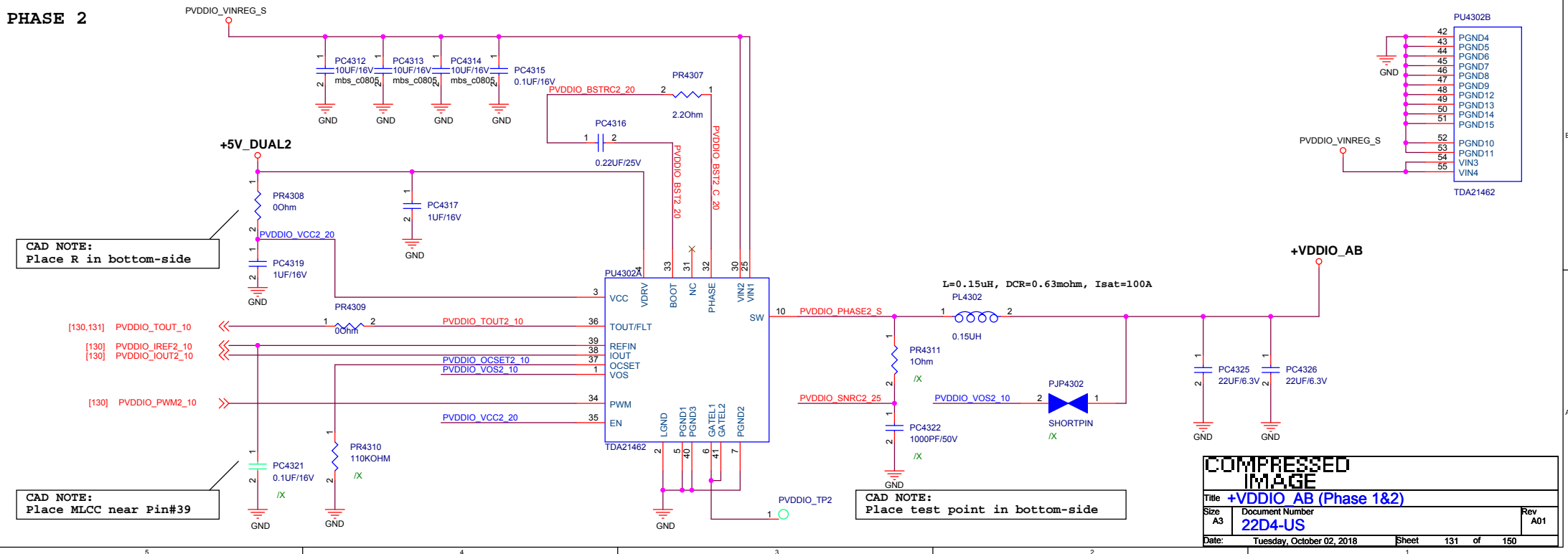
VCORE_REMOTE_SENSE



PHASE 1



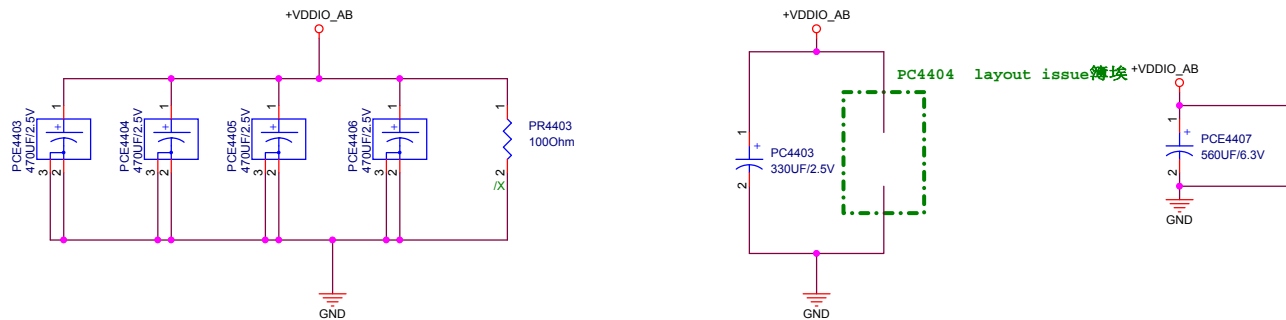
PHASE 2



COMPRESSED IMAGE		
Title	+VDDIO_AB (Phase 1&2)	
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[illegible]

Output capacitors
(Placed at the BOT of VR output)
4 x 470uF (SP-CAP) replaced by 3 mOhm



Title +VDDIO_Caps			
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Modify 0904 (EE Request)

[41,58,64,74,117,132] ATX_PWROK<>

Enable: Open Drain
Disable: Low

[41,64] +2.5V_VPP_PG

[41] +2.5V_VPP_EN

+VPPDDR Power rail - Output MLCC

22uF (06.3) 6pcs@VR

Output capacitors
(Place at the VR output)

$D = V_{out}/V_{in} = 2.572/12 = 0.214$
 $I_{ripple} = I_o * (D * 1 - D) = 7 * ((0.214) * (0.786)) = 2.871A$
 $I = ((V_{in} - V_{out}) * Duty) / (L_{out} * F_{sw})$
 $= ((12V - 2.572V) * (2.572V / 12V)) / (1 \mu H * 300KHz) = 6.74A$
 $I_{(L(peak))} = I_o(rms) + I$
 $I/2 = 7A + 3.37A = 10.37A$
Output $ESR < V_o(ripple) / I$
 $= 50mV / 6.74A = 7.418m$
 $C = I_{out} * t_{off} / V$
 $= 9 * [(1 / 300KHz) * (1 - D)] / 50mV$
 $\Delta C = 366.644 \mu F$

$I_o = 7.0A$
 $I_o_limit = 9.56A$

$I_o_limit = R_{ocset} * 10\mu A / R_{dson}$
 $= 6.65k * 10\mu A / 6.95m = 9.56A$

$V_{out} = 0.8V * (1 + 22.2k / 10k) = 2.576V$

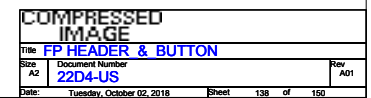
COMPRESSED IMAGE		
Title +VPPDDR AB		
Size A3	Document Number 22D4-US	Rev A01
Date: Tuesday, October 02, 2018	Sheet 133	of 150



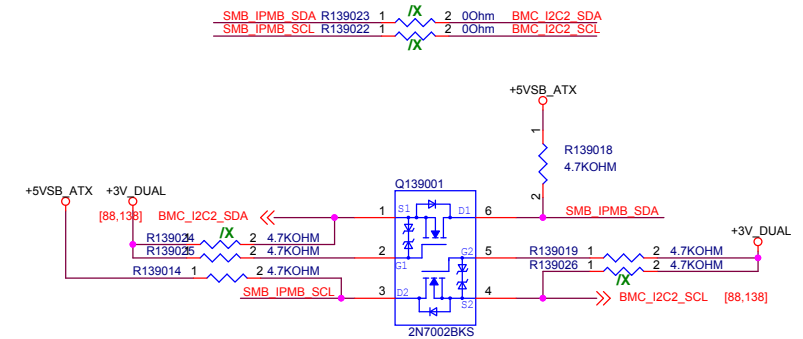
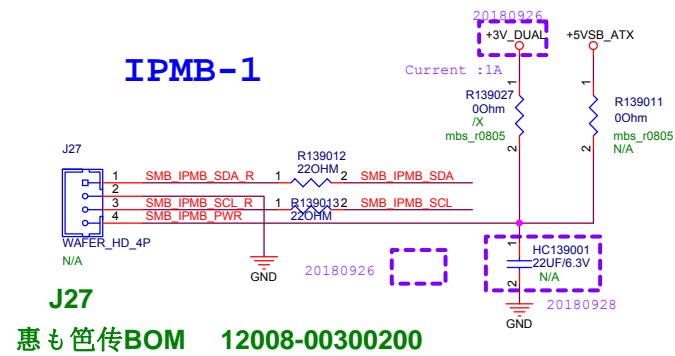
COMPRESSED IMAGE			
Title N/A			
Size A3	Document Number 22D4-US		Rev A01
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COMPRESSED IMAGE			
Title		N/A	
Size	Document Number		Rev
A3	22D4-US		A01
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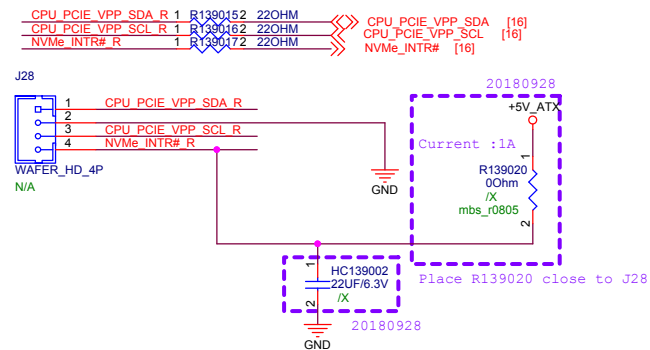


```
W330 : +12V_ATX ( R139027,C139001 ン / R139011, HC139001い ン)
others +5VSB_ATX ( R139027,C139001 い ン / R139011,HC139001 ン)
```



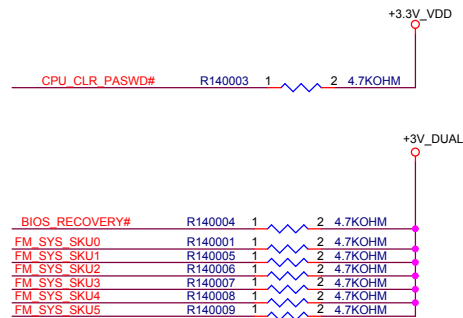
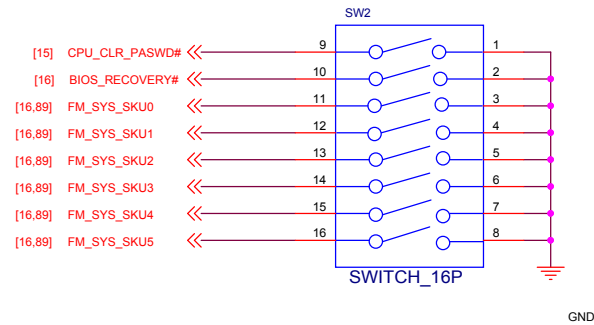
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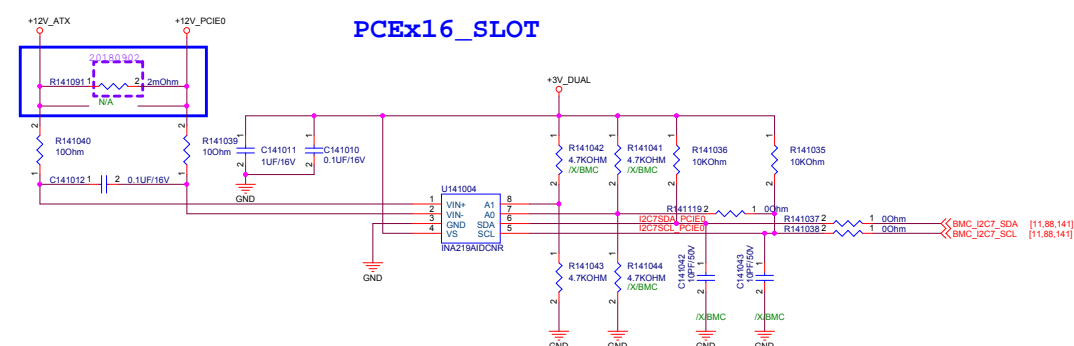
J28
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IMAGE

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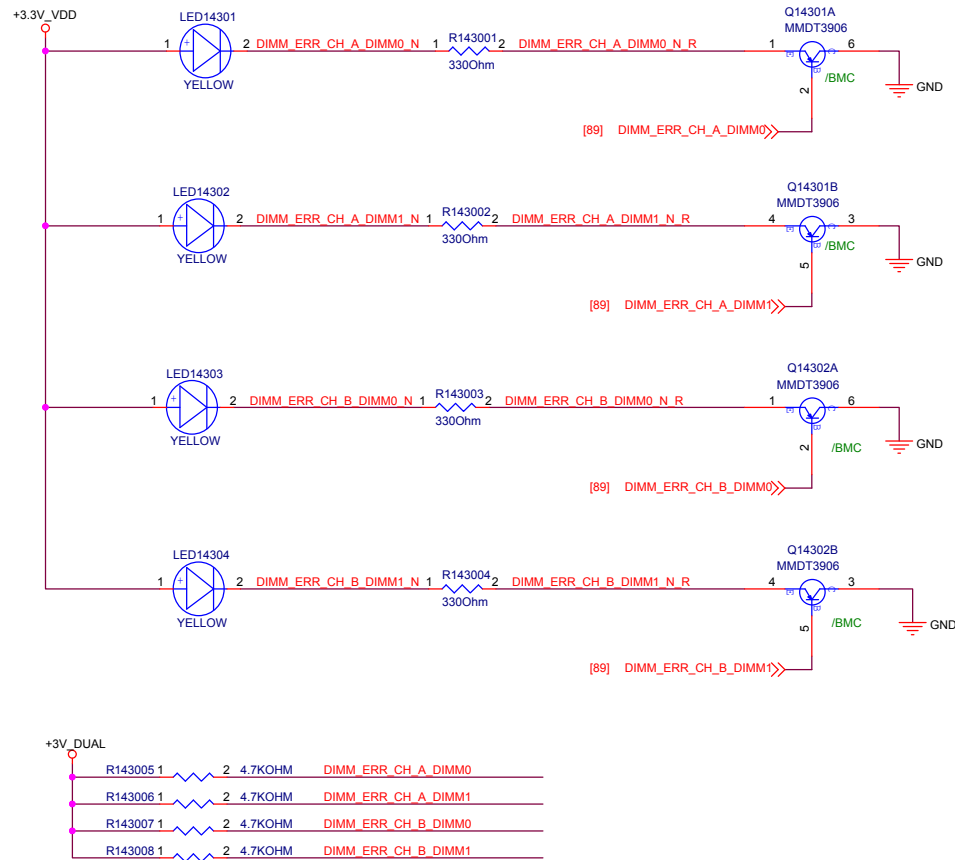


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GND	SCL	1000011
V _{SS}	GND	1000100
V _{SS}	V _{SS}	1000101
V _{SS}	SDA	1000110
V _{SS}	SCL	1000111
SDA	GND	1001000
SDA	V _{SS}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _{SS}	1001101
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Title	CURRENTMONITOR-1
Size	Document Number
Custom	22D4-US



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5					4					3					2					1				
D																								
C																								
B																								
A																								

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IMAGE

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5

4

3

2

1

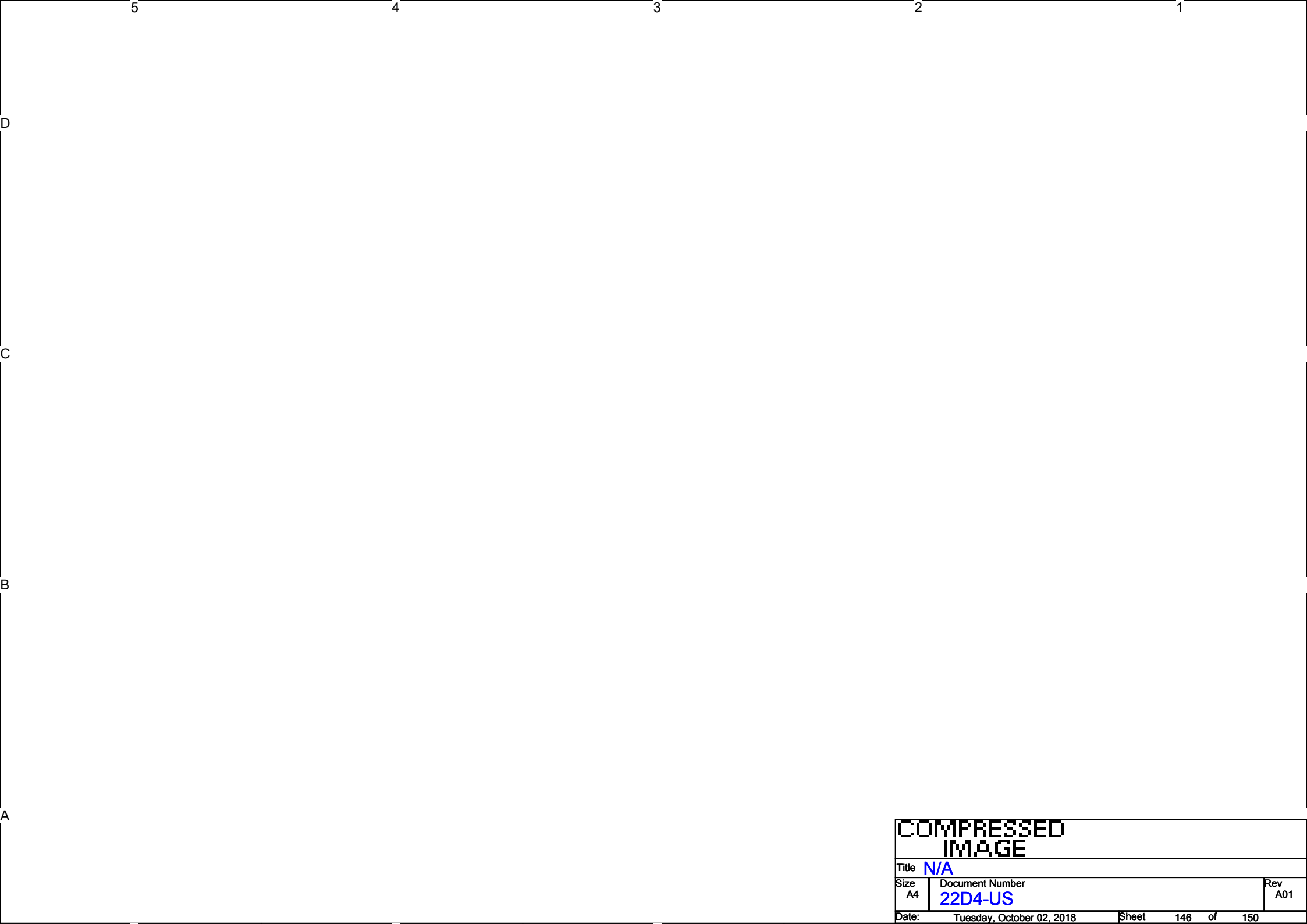
D

C

B

A

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5

4

3

2

1

D

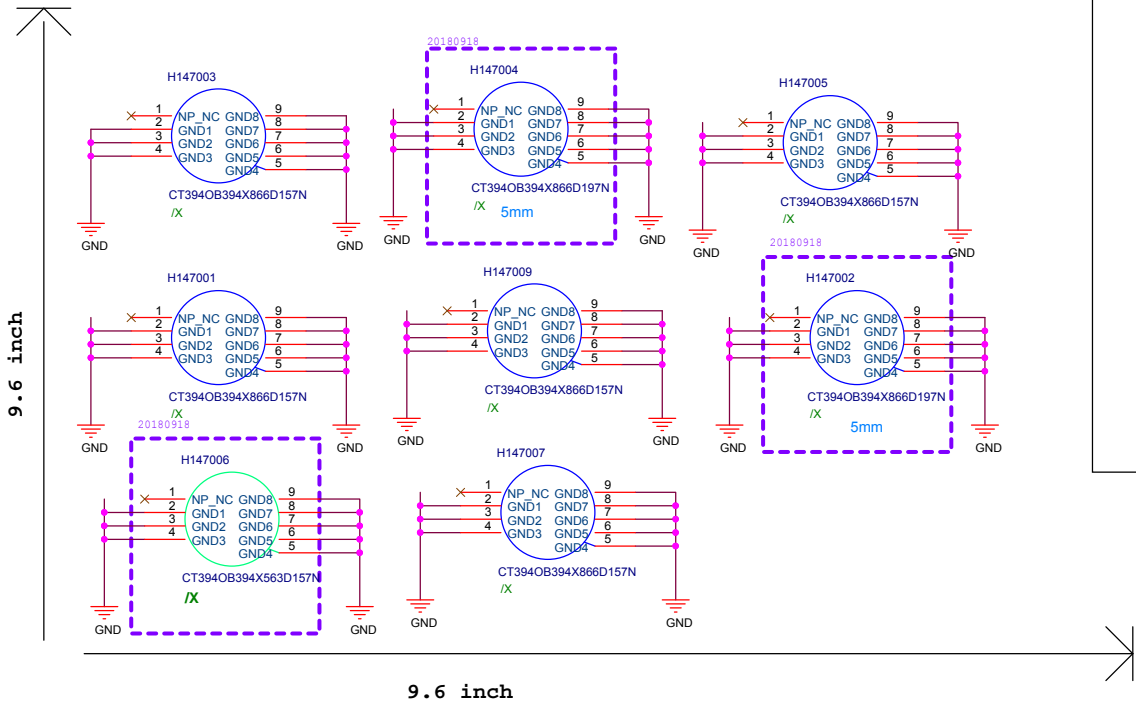
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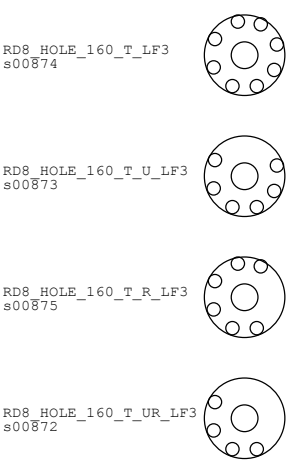
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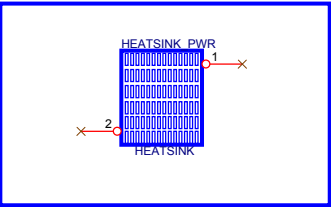
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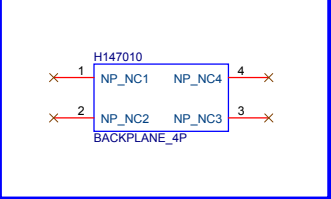
MB SCREW FOOTPRINT



POWER HEATSINK



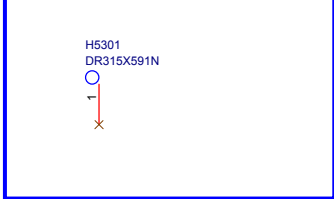
CPU HOLE



PCIEx16 HOLE



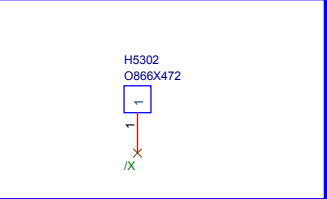
BM CARD hole



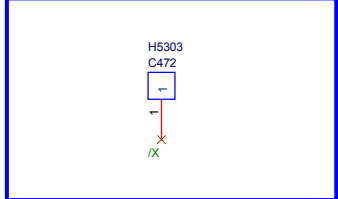
Fiducial Mask



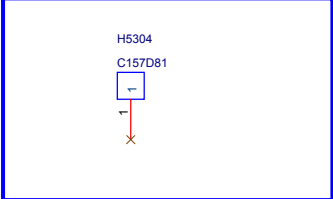
CPU PAD



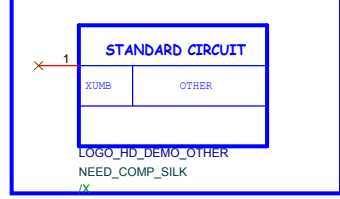
Board PAD



Guide pin



Text Frame



PCB1

22D4-US
承(TTL)
R1.0

Fake part
08001-12030000

PCB2

22D4-US
⊖瀬
(TRUSTECH)
R1.0

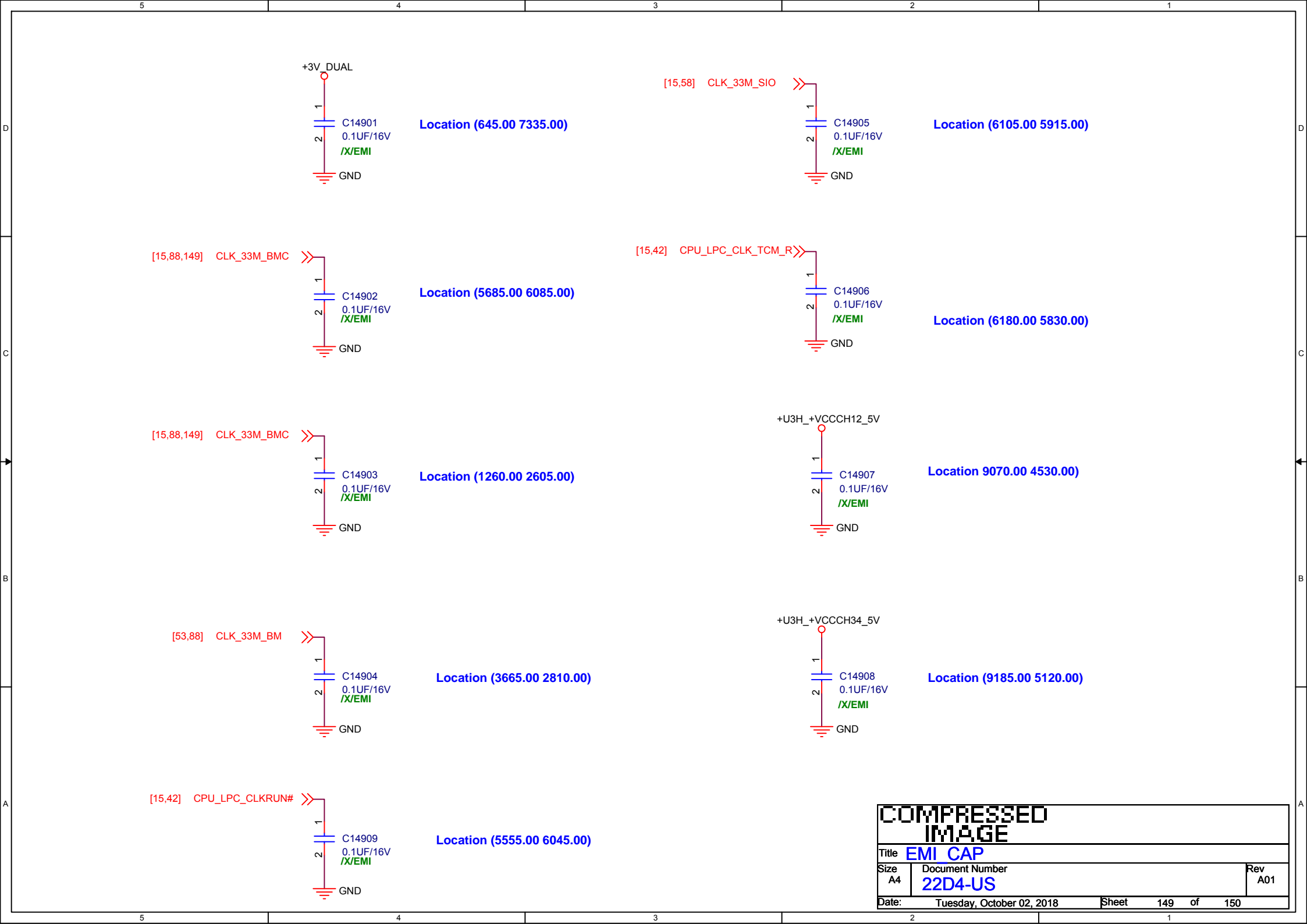
Fake part
08001-12030100

PCB3

22D4-US
秤山
(VICTORY)
R1.0

Fake part
08001-12030200

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