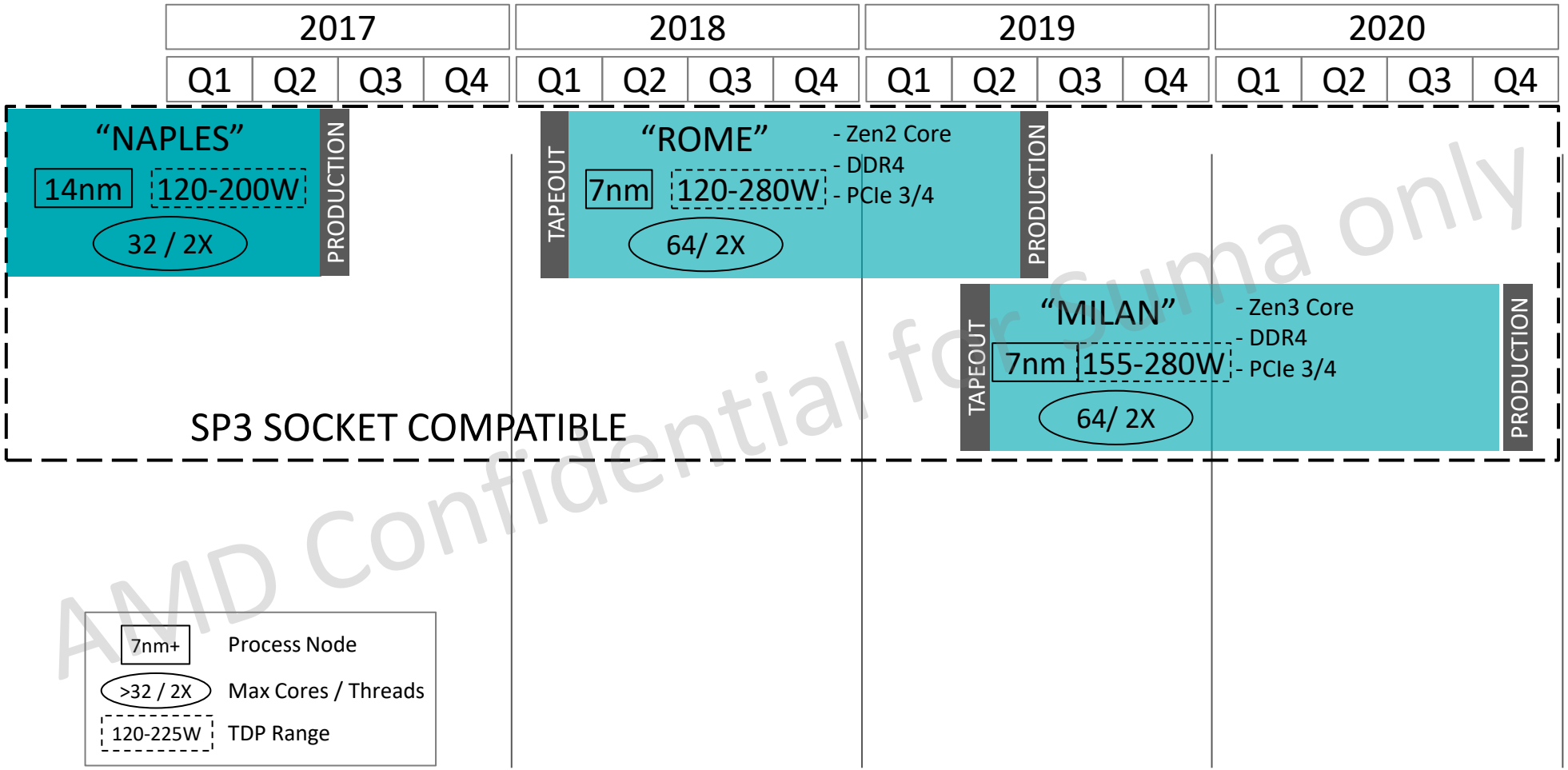
AMD EPYC™ PROCESSOR
FAMILY 19H MODELS 00H-0FH SP3 "MILAN"

REV 2021.06.28

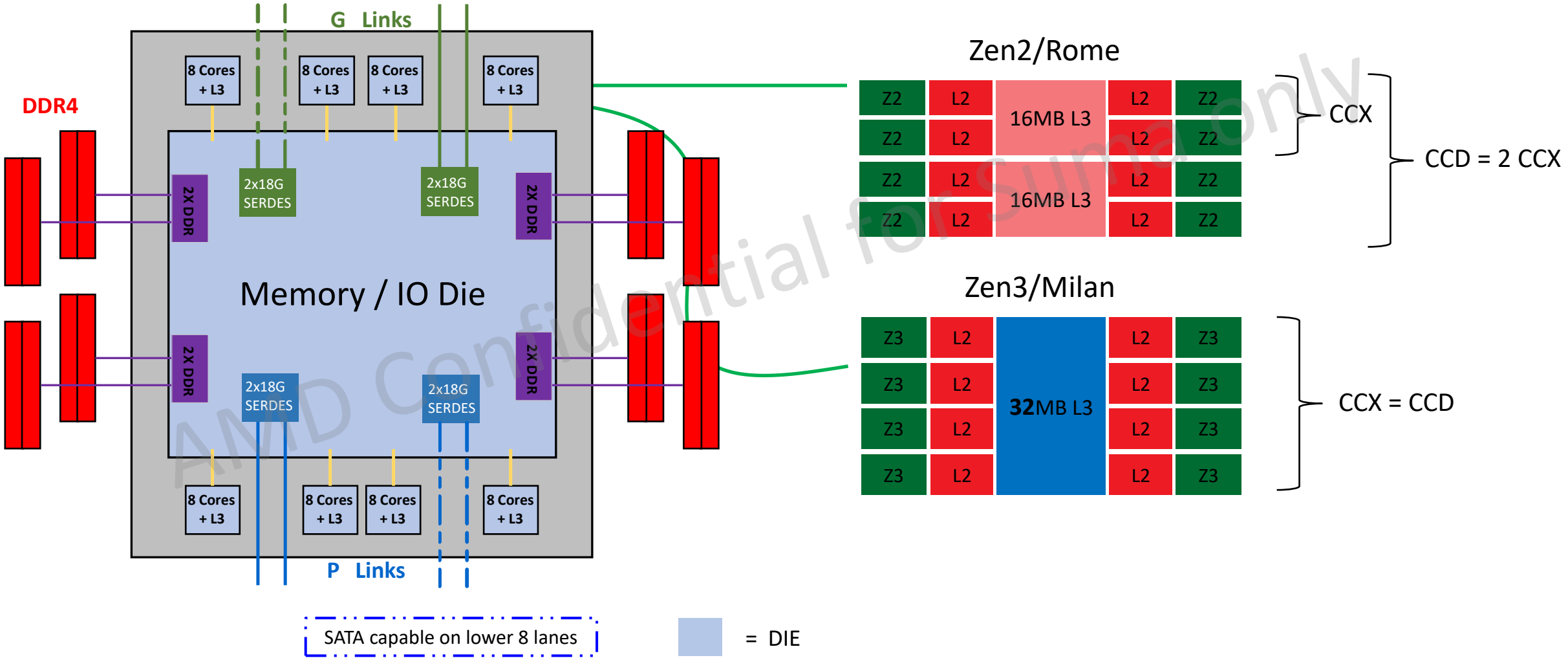
AMD EPYC™ ROADMAP



PERFORMANCE LEADERSHIP | CONTINUOUS INNOVATION

“ROME” AND “MILAN” BLOCK DIAGRAM

UP TO 9 DIE MCM: UP TO 8 CCD PLUS 1 IO DIE



“MILAN” KEY PRODUCT FEATURES

AMD

- Socket Compatible with Improved Performance:
  - Milan supported in Rome platforms with BIOS update
  - 64 Zen3 cores/128 threads per socket
  - 32MB L3 shared by 8 cores/CCD
  - Improved single core performance
  - Improved throughput performance
  - Additional AOCC compiler improvements

AMD EPYC™ ROADMAP: PLATFORM COMPATIBILITY

	"Rome"	"Milan"
Socket	SP3	SP3
xGMI	Rome Optimized: xGMI2 up to 18 GT/s Naples Compatible: xGMI1 10.6 GT/s	Rome/Milan Optimized: xGMI2 up to 18 GT/s
Memory	Rome Optimized: up to DDR4-3200 Naples Compatible: up to DDR4-2666	Rome/Milan Optimized: up to DDR4-3200 *(note: internal fabric clock coupled to the memory clock at max of 1600MHz for improved latency with DDR4-3200)*
IO	Rome Optimized: PCIeGen4: 16 GT/s Naples Compatible: PCIeGen3: 8 GT/s	Rome/Milan Optimized: PCIe4: 16 GT/s
BIOS	Based on AGESA RomePI-SP3	Based on AGESA MilanPI-SP3

“MILAN” MAXIMUM MEMORY FREQUENCY AND CAPACITY – 1 DIMM PER CHANNEL

REFER TO PID 55898, PROCESSOR PROGRAMMING REFERENCE (PPR) AS THE OFFICIAL SOURCE FOR THE MEMORY SUPPORT MATRIX

	DIMM Population	DDR4 Frequency MT/s	Capacity (8 Gbit x4 devices)	Capacity (16 Gbit x4 devices)
DIMM Type	DIMM 0	Rome/Milan platforms	1 channel / 8 channels	1 channel / 8 channels
RDIMM	1R (1 rank)	3200	16GB / 128GB	32GB / 256GB
	2R or 2DR (2 ranks)	3200	32GB / 256GB	64GB / 512GB
LRDIMM (dual die package devices)	4DR (4 ranks)	3200	64GB / 512GB	128GB / 1TB
LRDIMM (3DS devices)	2S2R (4 ranks)	3200	64GB / 512GB	128GB / 1TB
	2S4R (8 ranks)	3200	128GB / 1TB	256GB / 2TB
3DS RDIMM	2S2R (4 ranks)	3200	64GB / 512GB	128GB / 1TB
	2S4R (8 ranks)	3200	128GB / 1TB	256GB / 2TB

“MILAN” MAXIMUM MEMORY FREQUENCY AND CAPACITY – 2 DIMM PER CHANNEL

REFER TO PID 55898, PROCESSOR PROGRAMMING REFERENCE (PPR) AS THE OFFICIAL SOURCE FOR THE MEMORY SUPPORT MATRIX

	DIMM Population / Chan		DDR4 Frequency MT/s	Capacity (8Gbit x4 devices)	Capacity (16Gbit x4 devices)
DIMM Type	DIMM 0	DIMM 1	Rome/Milan platforms	1 channel / 8 channels	1 channel / 8 channels
RDIMM	-	1R	3200	16GB / 128GB	32GB / 256GB
	1R	1R	2933	32GB / 256GB	64GB / 512GB
	-	2R or 2DR	3200	32GB / 256GB	64GB / 512GB
	1R	2R or 2DR	2933	48GB / 384GB	96GB / 768GB
	2R or 2DR	2R or 2DR	2933	64GB / 512GB	128GB / 1TB
LRDIMM (dual die package devices)	-	4DR	3200	64GB / 512GB	128GB / 1TB
	4DR	4DR	2933	128GB / 1TB	256GB / 2TB
LRDIMM (3DS devices)	-	2S2R (4 ranks)	3200	64GB / 512GB	128GB / 1TB
	-	2S4R (8 ranks)	3200	128GB / 1TB	256GB / 2TB
	2S2R (4 ranks)	2S2R (4 ranks)	2933	128GB / 1TB	256GB / 2TB
	2S2R (4 ranks)	2S4R (8 ranks)	2933	192GB / 1.5TB	384GB / 3TB
	2S4R (8 ranks)	2S4R (8 ranks)	2933	256GB / 2TB	512GB / 4TB
3DS RDIMM	-	2S2R (4 ranks)	2933	64GB / 512GB	128GB / 1TB
	2S2R (4 ranks)	2S2R (4 ranks)	2666	128GB / 1TB	256GB / 2TB
	-	2S4R (8 ranks)	2933	128GB / 1TB	256GB / 2TB
	2S2R (4 ranks)	2S4R (8 ranks)	2666	192GB / 1.5TB	384GB / 3TB
	2S4R (8 ranks)	2S4R (8 ranks)	2666	256GB / 2TB	512GB / 4TB

“MILAN” KEY PROCESSOR SAMPLES MILESTONES

Milestone	Release<ed>	Availability	Customer Usage
A0 ES2: Eng Samples	<03/2020>	2 OPNs 64C, 32C Fused non-secure	BIOS development, System Validation
B1 PR Wave 1: Production Ready Samples	Starts shipping late <10/2020>	6 OPNs Fused secure	Final system validation regressions, Final thermal tests, Certification tests, Production solutions, Benchmark testing, Pilot support
B1 PR Wave 2: Production Ready Samples	Starts shipping <12/2020>	13 OPNs Fused secure	
AMD Production Ramp	Starts shipping 3 weeks after each OPN PR	Fused secure	Production

Contact your customer support team for details regarding using Rome parts for Milan thermal testing

- Dates reflect start in sampling ship date
- Updates from previous revisions are marked in blue font
- <date> Reflects completed milestone
- Please contact your AMD sales representative for details on sample shipment quantities and dates

MILAN PR SAMPLE WAVES

AMD

- Wave 1:
  - 64 core 225W (2P/1P), Production OPN 100-000000344, PR samples will contain -00 suffix
  - 32 core 225W (2P/1P), Production OPN 100-000000345, PR samples will contain -00 suffix
  - 64 core 280W (2P/1P), Production OPN 100-000000312, PR samples will contain -00 suffix
  - 24 core 180W (2P/1P), Production OPN 100-000000323, PR samples will contain -00 suffix
  - 16 core 155W (2P/1P), Production OPN 100-000000329, PR samples will contain -00 suffix
  - 32 core 280W (2P/1P), Production OPN 100-000000313, PR samples will contain -00 suffix
- Wave 2:
  - 8 core 180W (2P/1P), Production OPN 100-000000327, PR samples will contain -00 suffix
  - 64 core 225W (1P), Production OPN 100-000000337, PR samples will contain -00 suffix
  - 24 core 240W (2P/1P), Production OPN 100-000000317, PR samples will contain -00 suffix
  - 56 core 240W (2P/1P), Production OPN 100-000000318, PR samples will contain -00 suffix
  - 32 core 200W (2P/1P), Production OPN 100-000000334, PR samples will contain -00 suffix
  - 16 core 190W (2P/1P), Production OPN 100-000000338, PR samples will contain -00 suffix
  - 28 core 225W (2P/1P), Production OPN 100-000000319, PR samples will contain -00 suffix
  - 16 core 155W (1P), Production OPN 100-000000339, PR samples will contain -00 suffix
  - 16 core 240W (2P/1P), Production OPN 100-000000321, PR samples will contain -00 suffix
  - 24 core 200W (2P/1P), Production OPN 100-000000340, PR samples will contain -00 suffix
  - 32 core 225W (1P), Production OPN 100-000000341, PR samples will contain -00 suffix
  - 24 core 200W (1P), Production OPN 100-000000342, PR samples will contain -00 suffix
  - 48 core 225W (2P/1P), Production OPN 100-000000326, PR samples will contain -00 suffix

“MILAN” PROCESSOR PRODUCT STACK

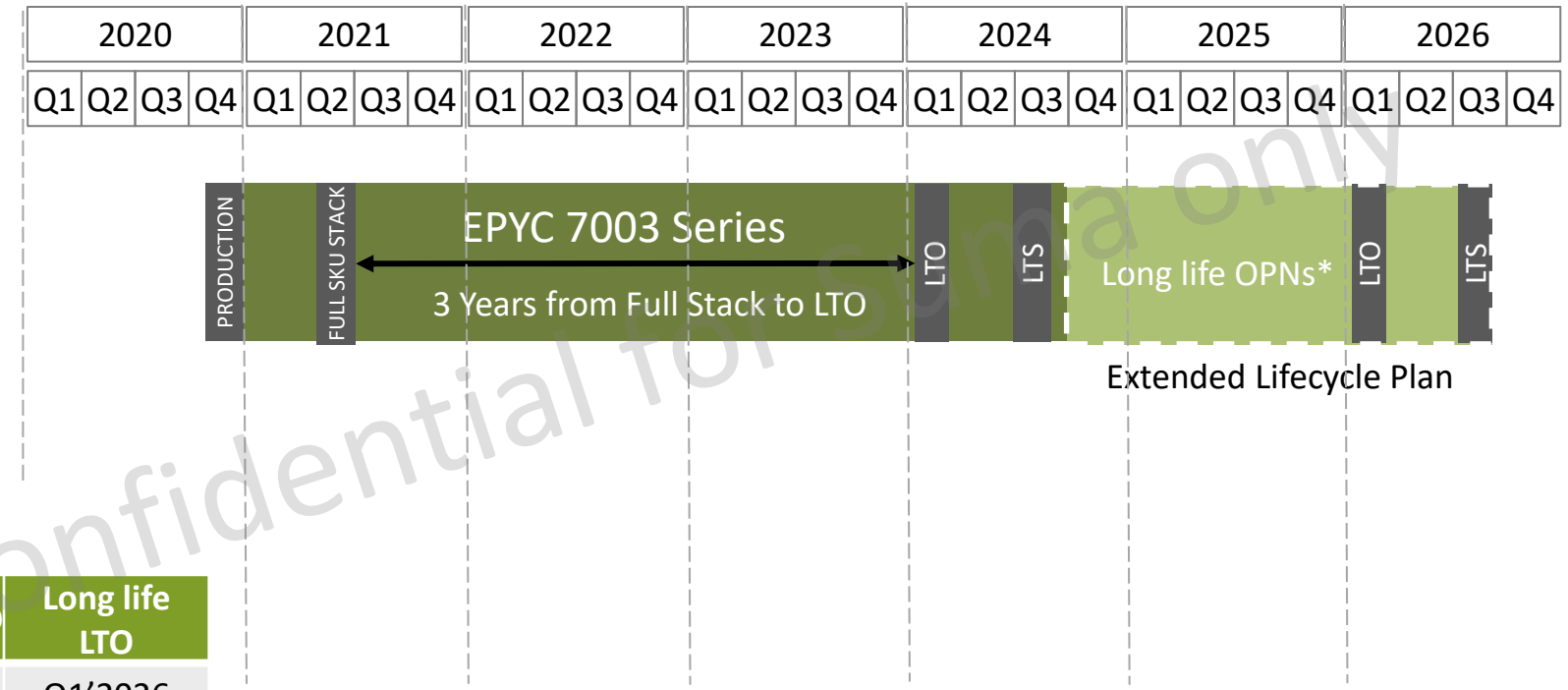
REFERENCE PID 56958 POWER AND THERMAL DATA SHEET FOR DETAILS

2P/1P	Model	Production OPN*	Default TDP (W)	cTDP Min (W)	cTDP Max (W)	Cores	Threads	Base Freq (GHz)	Max. Boost Freq (GHz)	L3 Cache (MB)	DDR Channels	Max DDR Freq (1 DPC)	PCIe
2P/1P	7763	100-000000312	280	225	280	64	128	2.45	3.5	256	8	3200	x128
2P/1P	7713	100-000000344	225	225	240	64	128	2.0	3.675	256	8	3200	X128
1P	7713P	100-000000337	225	225	240	64	128	2.0	3.675	256	8	3200	X128
2P/1P	7663	100-000000318	240	225	240	56	112	2.0	3.5	256	8	3200	X128
2P/1P	7643	100-000000326	225	225	240	48	96	2.3	3.6	256	8	3200	X128
2P/1P	75F3	100-000000313	280	225	280	32	64	2.950	4.0	256	8	3200	X128
2P/1P	7543	100-000000345	225	225	240	32	64	2.8	3.7	256	8	3200	X128
1P	7543P	100-000000341	225	225	240	32	64	2.8	3.7	256	8	3200	X128
2P/1P	7513	100-000000334	200	165	200	32	64	2.6	3.650	128	8	3200	X128
2P/1P	7453	100-000000319	225	225	240	28	56	2.75	3.450	64	8	3200	X128
2P/1P	74F3	100-000000317	240	225	240	24	48	3.2	4.0	256	8	3200	X128
2P/1P	7443	100-000000340	200	165	200	24	48	2.850	4.0	128	8	3200	X128
1P	7443P	100-000000342	200	165	200	24	48	2.850	4.0	128	8	3200	X128
2P/1P	7413	100-000000323	180	165	200	24	48	2.65	3.6	128	8	3200	X128
2P/1P	73F3	100-000000321	240	225	240	16	32	3.5	4.0	256	8	3200	X128
2P/1P	7343	100-000000338	190	165	200	16	32	3.2	3.9	128	8	3200	X128
2P/1P	7313	100-000000329	155	155	180	16	32	3.0	3.7	128	8	3200	X128
1P	7313P	100-000000339	155	155	180	16	32	3.0	3.7	128	8	3200	X128
2P/1P	72F3	100-000000327	180	165	200	8	16	3.7	4.1	256	8	3200	X128

PR OPNs will contain -00 suffix

LIFECYCLE AVAILABILITY AMD EPYC™ 7003 SERIES CPUS

LTO – Last Time Order
LTS – Last Time Ship



EPYC Series	Initial Production	Standard LTO	Long life LTO
EPYC 7003	4Q'2020	Q1'2024	Q1'2026

Supply subject to availability
Please contact our AMD sales representative for more information

AMD EPYC™ 7003 EXTENDED AVAILABILITY OPNS

Cores	EPYC 7003 1P CPUs	Extended Availability OPNs
64	7713P	7713P
32	7543P	7543P
24	7443P	- - -
16	7313P	7313P

Cores	Hi Perf / Core OPNs	Extended Availability OPNs
32	75F3	- - -
24	74F3	- - -
16	73F3	- - -
8	72F3	- - -

Cores	EPYC 7003 1P/2P CPUs	Extended Availability OPNs
64	7763	- - -
	7713	7713
56	7763	- - -
48	7643	- - -
32	7543	7543
	7513	- - -
28	7453	7453
24	7443	- - -
	7413	7413
16	7343	- - -
	7313	7313

Supply subject to availability
Please contact our AMD sales representative for more information

“MILAN” AGESA SCHEDULE

- AGESA will release at an approximate monthly cadence from first samples
- AGESA dates are dependent upon sample availability
- BIOS Partners: AMI, Insyde, BMC Partners: AMI, Insyde
- AMD enables IBVs to provide core BIOS. Please contact your IBV for platform BIOS release schedules. In general, IBV code is available 1-2 weeks after AGESA release.

AGESA release	Release Date	Milan Samples Alignment	Comments
MilanPI-SP3_1.0.0.0	<12/04/2020>		Production Release
MilanPI-SP3_1.0.0.1	<02/05/2021>		
MilanPI-SP3_1.0.0.2	<04/05/2021>		See following slide for key updates
MilanPI-SP3_1.0.0.3	<05/22/2021>		MilanPI-SP3_1.0.0.3 also adds support for a future Milan-X product. Milan-X uses the same I/O die as Milan, plus the B2 revision of the CCD die to update silicon vias for stacked L3. B2 code will only be applied to Milan-X OPNs. See following slide for key updates
MilanPI-SP3_1.0.0.4	<06/25/2021>		See following slide for key updates
MilanPI-SP3_1.0.0.5	08/2021		

MILANPI-SP3_1.0.0.4 KEY UPDATES

AMD

- SEV-SNP feature enhancements

- B0, B1 and B2 uCode updates to resolves Erratum #1361 which will be published in the Rev 1.04 Milan Revision Guide (PID 56683)
  - B0 Milan microcode 0x0A001046, B1 Milan microcode 0x0A001137, B2 Milan-X microcode 0x0A00121D
  - The .bin files of these microcde patches will also be available on DevHub by the end of June for use with MilanPI-SP3_1.0.0.2 and MilanPI-SP3_1.0.0.3

- Erratum 1361: Processor May Hang When Switching Between Instruction Cache and Op Cache
  - Erratum Description: Under a highly specific and detailed set of internal timing conditions, running a program with a code footprint that exceeds 32 KB may cause the processor to hang while switching between code regions that consistently miss the instruction cache and code regions that are contained within the Op Cache.
  - Additional background: AMD observed EX WDT failures on some nodes running multi-node workloads during at-scale testing.
  - Potential Effect on System: System may hang or reset

MILANPI-SP3_1.0.0.3 KEY UPDATES

- Adds support for a future Milan-X product
- Provides AzSHCI V2 support with Windows Server 2022
- B1 and B2 uCode updates to resolve the following Errata which will be published in the next Milan Revision Guide (PID 56683)
- B1 Milan microcode 0x0A001133, B2 Milan-X microcode 0x0A00121A
  - 1336: RMPUPDATE May Fail to Return Error Code For 2M Guest Page
  - 1343: Executing VMRUN When a Reserved Bit Is Set in MXCSR May Cause Unpredictable Behavior
  - 1350: Unexpected Interrupt May Happen After AVIC (Advanced Virtual Interrupt Controller) Doorbell Received
  - 1352: Processor May Fail to Lock RMP (Reverse Map Table) Entry For vAPIC (Virtual Advanced Programmable Interrupt Controller) Backing Page

MILANPI-SP3_1.0.0.2 KEY UPDATES

- Improved performance for HPC applications which use 200G IB NIC as interconnect. With prior production AGESA releases, workloads may show significant impact to IB bandwidth with MPI message sizes > 8K.
- Added option to control DDR4 DIMM Registering Clock Driver weak drive feature from JEDEC spec with default set to Disabled. AMD recommends disabling RCD weak drive due to increased risk of memory errors.
- Updated power calculation parameter to fix an incorrectly reported CPU power issue when running iperf/FIO on systems using Power Capping.
- Added option to set DLWM to (x8/x16) to optimize the performance of workloads with limited cross node traffic. The default DLWM setting for Milan remains as (x2/x8/x16).
- B1 microcode update to 0x0A00111D for Errata #1329 and #1330 which will be published in the next Milan Revision Guide (PID 56683)
  - #1329: Hypervisor with Encrypted SVM (Secure Virtual Machine) Related Pages May Experience Unpredictable Behavior If Guest Enables LBR (Last Branch Record)
  - #1330: SEV-SNP (Secure Encrypted Virtualization - Secure Nested Paging) Guests With Last Branch Record Enabled May Experience Incorrect Alternate Injection Behavior

CONFIGURABLE EDC WITH MILAN IRM GROUP X OPNS AND MILANPI-SP3_0.0.9.1

AMD

Configurable EDC (cEDC)

- Configurable EDC (cEDC) capability is available for Milan Group X OPNs and MilanPI-SP3_0.0.9.1 and later
- Select OPNs will support IRM Group X and will be documented in the Power and Thermal Datasheet (PID 56958)
- cEDC offers performance benefits with increased EDC above 255A, **with maximum value at 300A**

PCDs Customization

- **PcdCfgPlatformEDC**
  - Specifies the **Maximum EDC limit** that the platform can support based on electrical and thermal characterization of the platform.
  - Value range in hex is (0x00 - 0x12C) and decimal is (0-300).
- **PcdCfgEDC**
  - Specifies the **desired EDC limit** on the platform.
  - In order to increase EDC Limit, **BOTH** PcdCfgEDC and PcdCfgPlatformEDC must be configured.
  - The maximum allowed is 300A. AMD recommends discrete values of 255A, 280A, or 300A.
  - Value range in hex is (0x00 - 0x12C) and decimal is (0-300).

Note: cEDC value should be configured based on the characterization and settings of your Milan platform.

Configuring the cEDC value higher than your platform capability could lead to unexpected shutdowns.

DUAL ROME/MILAN BIOS SUPPORT WITH MILAN B0

FIRST SUPPORT IN MILANPI-SP3_0.0.8.0

- Provides the ability to combine Rome and Milan B0 BIOS images in a singular BIOS flash image
- Rome and Milan binaries are generated separately
  - Rome from RomePI
  - Milan from MilanPI
- Re-validation and QA efforts on Rome are minimized given leverage of previous Rome validation/BIOS
  - Customers will still need to confirm Rome production support with new dual image
- Dual BIOS 32MB binary image is generated by concatenating 16MB of latest Rome image with 16MB Milan PI-0.0.8.0 or later image
  - To build a dual BIOS image which supports Rome and Milan B0 silicon:
    - Rome (16MB) EFS[0x24] = 0xFE // EFS Offset 0x24, Bit0 (Second_GEN_EFS) must be set to 0
    - Milan (16MB) EFS[0x24] = 0xFC // EFS Offset 0x24, Bit0 and Bit1 (Multi_GEN_EFS) must be set to 0
    - Milan image must be in the upper 16MB and Rome image must be in the lower 16MB
  - Example of command to concatenate Rome and Milan Image: COPY /B ROMEB0_16MB.FD + MILANB0_16MB.FD DUAL_32MB.FD
- Reference PID#55758: “AMD Platform Security Processor BIOS Architecture Design Guide for AMD Family 17h and 19h Processors”

SINGLE BIOS IMAGE TO SUPPORT MILAN A0 AND B0

- For a single BIOS image which supports both Milan A0 and B0, the following offsets are required:
  - Milan (16MB) EFS[0x24] = 0xFC // EFS Offset 0x24, Bit1 (Multi_GEN_EFS) must be set to 0 to support Milan B0 silicon
    // EFS Offset 0x24, Bit0 (Second_GEN_EFS) must be set to 0 to support Milan A0 silicon
- A single 32MB BIOS image for Rome B0, Milan A0 and Milan B0 silicon is not supported

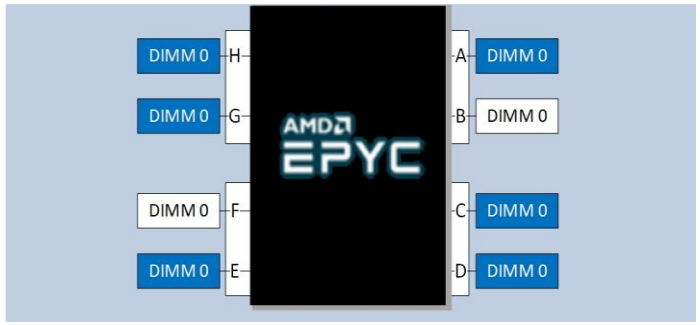
"MILAN" FEATURE ENABLEMENT

Functional Area	Feature Enablement with MilanPI-SP3_0.0.7.0	MilanPI-SP3_0.0.7.1	MilanPI-SP3_0.0.7.2	MilanPI-SP3_0.0.8.0	MilanPI-SP3_0.0.8.1	MilanPI-SP3_0.0.9.0	MilanPI-SP3_0.0.9.1 and later
Sample Support	225W 64C, 1.6GHz base, 3.0GHz boost 180W 32C, 1.8GHz base, 3.0GHz boost			B0 support dual BIOS support w/ B0		PR	
Power Management	Core C-states, C-state Boost, P-states, CC6, DF C-states, Prochot						
xGMI	xGMI: up 18 GT/s, 3 and 4 link support (platform dependent)						
Memory	POR memory speeds for RDIMM, LRDIMM, LRDIMM 3DS, RDIMM 3DS Memory p-states, DRAM thermal throttling	MBIST	NVDIMM-N		6 channel memory interleaving with B0		
PCIe	Up to Gen4 x16, bifurcation, de-emphasis, IOMMU, Preferred I/O					LCLK Freq Control	
SATA	Up to Gen3						
USB	USB2, USB3.1 gen1						
RAS	MCA, MCA thresholding, MCA address translation, Data poisoning, DRAM ECC & scrubbers, DRAM UECC retry, DRAM A/C Parity and Write Data CRC, NBIO RAS, PCIe AER & ECRC, Link RAS, All watchdog timers, USB/SATA ECC, SOC parity (FCH, SMN), WHEA, PFEH, GHES assist, Post Package Repair (Soft & Hard)	AGESA memory tester	Error Disconnect Recovery (EDR), Surprise Down				
NVMe hot plug	Legacy OS-First Hotplug, Legacy FW-first Hotplug						
APML	SB-TSI, SB-RMI						
SPI lock			ROM Armor				

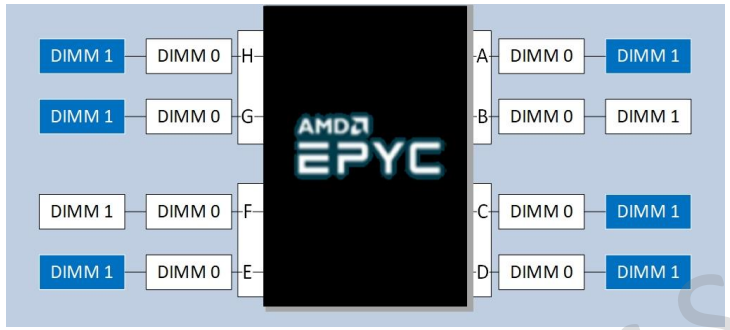
For LCLK Feq Control Information, see PID 56970 AMD SP3 Family 19h Models 00h–0Fh Infinity Fabric Options

6-CHANNEL INTERLEAVING SUPPORT WITH MILAN B0 AND MILANPI-SP3_0.0.8.1

6-Channel Interleaving DIMM Configuration



Six DIMM Population in 1DPC Configuration



Six DIMM Population in 2DPC Configuration

Twelve DIMM Population in 2DPC Configuration

6-Channel Interleaving Rules

- Channels ACDEGH are the only channels capable of six-way interleaving. No other channels may be populated
- All DIMM must be of the same capacity, and only with ≤ 256GB per channel
- Six-way support requires that the interleaving size be 2KB or 4KB.
- Six-way interleaving is supported in NPS=1 only.
- Supported only on Milan B0 and requires AGESA 0.0.8.1 or newer release
- 6 channel interleaving is a feature that is supported across all Milan OPNs

6-channel interleaving documentation reference

- 6 DIMM Configuration section in "*Memory Population Guidelines for AMD EPYC™ 7003 Series Processors" Pub* 56873 Rev 0.60 or newer.
- Interleaving Options section in "*Socket SP3 Platform NUMA Topology for AMD Family 19h Models 00h–0Fh" Pub* 56795 Rev 1.10 or newer
- D18F0x110...D18F0x188 [DRAM Base Address] (DF::DramBaseAddress) in "PPR Vol 2 for AMD Family 19h Model 00h A0" Pub 55898 Rev 0.92 or newer

“MILAN” TOOLS CAPABILITIES

Tool	Current Version	Comments
AMD SST (ASST)	• Version 7.4.10 for Windows • Version 7.4.13 for Linux	
MemEye	• Version 1.26.45	• MemEye Training Guide v 1.3
AMD XpressIO	• Version 3.1.2.0 for Windows • Version 3.1.2.0 for Linux	• Adds SystemDeck functionality • AMD XpressIO (AMDXIO) Training Guide v 1.2
AMD XpressIO Margin Visualization (AMV)	• Version 1.50	
AMD Compliance Pattern Recipe Tool	• Version 1.2	
Machine Error Decode Tool	• Version 2.8.19 for Windows • Version 2.8.19 for Linux RPM • Version 2.8.19 for Linux Debian	
RAS	• Version 1.8.5.211 for Windows • Version 1.8.5.482 for Linux RPM • Version 1.8.5.481 for Linux Debian	• RAS Error Injection Tool Platform Guidance v 2.40
AMD Validation Toolkit (AVT)	• Version 2.7.14 for Windows • Version 2.7.14 for Linux	
HDT	• Version 20.6.71.5117	• HDT20 version 20.2.21.4778 or greater is required for Milan B0
SDLE-2	• Version 2.9.14	• Analysis spreadsheets and batch files v2.08 • DDR4 SDLE-2 Load Pod Installation Guide v1.0
Net Tool Database for SPE Server	• Version 1.0.2.20200803	
AMD Server Schematic Checker	• Version 1.13	

SP3 “MILAN” TECHNICAL DOCUMENTATION

“Milan” shares some documentation with “Rome” and “Naples”.
“Naples” is Family 17h models 00h-0Fh, “Rome” is Family 17h models 30h-3Fh, “Milan” is Family 19h models 00h-0Fh

PID	TITLE	Release<ed>
Product Documents		
55426	Socket SP3 Processor Functional Data Sheet	<Rev: 1.04 Oct 2020>
55441	Socket SP3 Processor Electrical Data Sheet (EDS)	<Rev: 0.65 July 2020>
56683	Revision Guide for AMD Family 19h Models 00h-0Fh Processors	<Rev: 1.03 Jun 2021>
56789	AMD Family 19h Models 00h–0Fh Processor Engineering Sample Information	<Rev: 0.72 Feb 2020>
56873	Memory Population Guidelines for AMD EPYC™ 7003 Series Processors	<Rev: 0.80 Mar 2021>
56795	Socket SP3 Platform NUMA Topology for AMD Family 19h Models 00h–0Fh	<Rev: 1.10 May 2020>
56970	AMD SP3 Family 19h Models 00h–0Fh Infinity Fabric Options	<Rev: 0.75 Nov 2020>
56958	Power and Thermal Data Sheet for AMD Family 19h Models 00h–0Fh Socket SP3 Processors	<Rev: 1.10 Jun 2021>

SP3 “MILAN” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
Platform Design		
55423	Thermal Design Guide for Socket SP3 Processors	<Rev: 1.05 Jun 2019>
55423	Thermal Design Guide for SP3 Processors (PUBLIC)	<Rev: 3.00 Nov 2017>
55424	Flotherm Thermal Model for Socket SP3 Processors User’s Guide	<Rev: 1.08 Oct 2020>
56211	Socket SP3 Thermal Test User’s Guide	<Rev: 0.16 Feb 2020>
55949	Socket SP3 Thermal Test Slug (TTS) User’s Guide	<Rev: 0.84 Aug 2020>
55260	Socket SP3 Design Specification	<Rev: 1.15 Mar 2020>
55414	Preliminary Socket SP3 Processor Motherboard Design Guide	<Rev: 1.10 Nov 2020>
55421	Socket SP3 Processor Motherboard Schematic Checklist	<Rev: 3.02 May 2020>
55422	Socket SP3 Processor Motherboard Layout Checklist	<Rev: 3.01 May 2020>
56412	AMD Socket SP3 Processor IO Configuration Guide	<Rev: 0.78 June 2020>
56799	Server System Validation Manual for Socket SP3 Family 19h Models 00h–0Fh Processors	<Rev: 0.79 Jan 2021>
56744	Socket SP3 NVME Hotplug Specification for Family 19h 00h-0Fh	<Rev: 0.91 July 2020>
56832	SP3 Hardware Bringup Checklist	<Rev: 1.60 Feb 2020>
56862	Performance Validation Guide for Family 19h Models 00h0Fh Processors	<Rev: 1.62 Aug 2020>
56856	Socket SP3 Validated Memory for Family 19h Models 00h-0Fh	<Rev: 0.22 May 2021>

SP3 “MILAN” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
Infrastructure		
48022	AMD Serial VID Interface 2.0 (SVI2) Specification	<Rev: 1.10 Feb 2020>
55823	Socket SP3 Post Reflow Assembly & Package Insertion Procedure	<Rev: 1.10 Feb 2018>
55821	SP3 Carrier Frame Installation Procedure	<Rev: 1.00 June 2016>
55418	Infrastructure Roadmap (IRM) for Socket SP3	<Rev: 1.18 Nov 2020>
Reference Platform		
Ethanol-X (EATX, 2P, 1DPC)		Rev A
Ethanol Debug X (EATX+, 2P, 2DPC)		Rev A
Diesel Power Reference		Rev A
Daytona XT (2U Rackmount, 2P, 2DPC)		Rev B
2U Rackmount Rome-based System with SMT DIMMs Paper Study		Rev A

SP3 “MILAN” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
Software Docs		
55898	Processor Programming Reference (PPR) for AMD Family 19h Models 00h-0Fh Processors, Revision A0	<Rev: 0.92 June 2020>
55898	Processor Programming Reference (PPR) for AMD Family 19h Models 00h-0Fh Processors, Revision B1	<Rev: 0.50 Jun 2021>
55483	AMD Generic Encapsulated Software Architecture (AGESA) V9 Interface Specification	<Rev: 1.64 Jun 2021>
55730	Common Platform Module Implementation Guide	<Rev: 1.22 Apr 2020>
56796	AMD Family 19h, Models 00h–0Fh, ACPI v6.3 Porting Guide	<Rev: 1.00 Jan 2020>
55758	AMD Platform Security Processor BIOS Architecture Design Guide for AMD Family 17h and 19h Processors	<Rev: 1.13 Jun 2021>
48882	AMD I/O Virtualization Technology (IOMMU) Specification	<Rev: 3.06 Apr 2021>
56732	Socket SP3 RAS Platform Specification and Implementation Guide for AMD Family 19h Models 00h–0Fh	<Rev: 1.30 Feb 2021>
56534	Enabling Platform Secure Boot for AMD Family 17h Models 00h–0Fh and 30h–3Fh and Family 19h Models 00h–0Fh Processor-Based Server Platforms	<Rev: 0.91 Jan 2021>
24592	AMD64 Architecture Programmer's Manual Volume 1: Application Programming (PUBLIC)	<Rev: 3.23 Oct 2020>
24593	AMD64 Architecture Programmer's Manual Volume 2: System Programming (PUBLIC)	<Rev: 3.37 Mar 2021>
24594	AMD64 Architecture Programmer's Manual Volume 3: General Purpose and System Programming Instructions (PUBLIC)	<Rev: 3.32 Mar 2021>
26568	AMD64 Architecture Programmer's Manual Volume 4: 128-Bit and 256-Bit Media Instructions (PUBLIC)	<Rev: 3.24 May 2020>
26569	AMD64 Architecture Programmer's Manual Volume 5: 64-Bit Media and x87 Floating Point Instructions (PUBLIC)	<Rev: 3.15 May 2018>
40332	AMD64 Architecture Programmer’s Manual: Volumes 1-5	<Rev: 4.03 Mar 2021>
55766	Secure Encrypted Virtualization API (PUBLIC)	<Rev: 3.24 Apr 2020>
56860	SEV Secure Nested Paging Firmware ABI Specification (PUBLIC)	<Rev: 0.90 Apr 2021>
56946	Seasim Training Guide	<Rev: 1.00 July 2020>

SP3 “MILAN” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
Application Notes		
57084	Java Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57080	NVMe Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57071	Couchbase Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57091	High Performance Computing (HPC) Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57087	Microsoft SQL Server Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57072	MongoDB Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57088	RedHat Linux Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57075	AMD EPYC™ 7003 Series Processors’ Microarchitecture	<Rev: 2.00 Mar 2021>
57086	Opensource RDMBS Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57070	Apache Cassandra Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57078	Container Tuning Guide on Kubernetes for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57083	Data Plan Development Kit (DPDK) Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57090	Microsoft Windows Server Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57079	VMware vSAN Tuning Guide for AMD EPYC™ 7003 Series Processors	<Rev: 2.00 Mar 2021>
57089	VMware vSphere Tuning Guide for AMD EPYC™ 7003 Series Processor s	<Rev: 2.00 Mar 2021>
57081	VMware Network Tuning Guide for AMD EPYC™ 7003 Series Processor Based Servers	<Rev: 2.00 Mar 2021>
57076	Linux Network Tuning Guide for AMD EPYC™ 7003 Series Processor Based Servers	<Rev: 2.00 Mar 2021>
57085	Hadoop Tuning Guide for AMD EPYC™ 7003 Series Processor Based Servers	<Rev: 2.00 Mar 2021>
57011	Workload Tuning Guide for AMD EPYC™ 7003 Series Processor Based Servers	<Rev: 1.00 Apr 2021>
56882	AMD Family 19h Models 00h-0Fh SP3 Platform Performance and Power Optimization Guide (PPOG)	<Rev: 1.02 May 2021>
56534	Enabling Platform Secure Boot for AMD Family 17h Models 00h–0Fh and 30h–3Fh and Family 19h Models 00h–0Fh Processor-Based Server Platforms	<Rev: 0.91 Jan 2022>

SP3 “MILAN” TECHNICAL DOCUMENTATION (CONTINUED)

PID	TITLE	Release<ed>
Software Downloads		
MilanPI-SP3	MilanPI-SP3 Platform Initialization Package	<Rev: 1.0.0.4 Jun 2021>
MilanPI_Rel_Notes	MilanPI-SP3 Release Notes	<Rev: 1.0.0.4 Jun 2021>
EthanolX_RM_BIOS	Ethanol-X Milan BIOS	<Rev: RXM1004C Jun 2021>
DaytonaX_RM_BIOS	Daytona-X Milan BIOS	<Rev: RYM1004C Jun 2021>
Insyde_BMC	Insyde Universal BMC Binary for AMD CRBs	<Rev: 3.54 Nov 2020>
Windows IO drivers	SP3 Windows Peripheral-IO Drivers SP3 Windows PSHED Plug-in Driver	<Rev: 2.18.17.254 Jun 2021> <Rev: 2.18.08.444 Jun 2021>
xGMI Model	SEASIM xGMI Model for SP3 Milan	<July 2020>
PCIe Model	SEASIM PCIe Model for SP3 Milan	<July 2020>
SEASIM	SEASIM Tool	<July 2020>
uProf	AMD uProf 3.4	<Rev: 3.4 Apr 2021>
AOCC Linux	AMD Optimized CPU Libraries (AOCLv3.0)	<Feb 2021>
AOCC Compiler	AOCC 3.0 Compiler	<Feb 2021>

SP3 “MILAN” TARGETED OPERATING SYSTEMS & HYPERVISORS

	N - 1	Launch (N)
Microsoft	Server 2016	Server 2019 & 2022 Azure Stack HCI v1
vmware	vSphere 6.7u3 P03	vSphere 7.0u1
redhat	see notes	RHEL 8.3
SUSE	SLES 12 SP5 Requires maintenance update (Mar 4, 2020 Kernel 4.12.14-122.17)	SLES 15 SP2
CANONICAL	Ubuntu 18.04.5	Ubuntu 20.04
CITRIX		Hypervisor 8.2
CentOS		8.3 CentOS 8 updates end in 2021 https://centos.org/distro-faq
ORACLE	UEK 5.5	UEK 6.1

Windows note:

- X2APIC/256T not supported in 2016
- Sept 2019 Media Refresh & beyond provides full 256T/x2APIC support

RedHat notes:

- RHEL 7.x is in maintenance mode – not taking new features, therefore will not support Milan
- Milan users will need to upgrade to RHEL 8.3 (Nov 2020)
- RHEL uses a whitelist to check for known hardware configurations. RHEL versions that work for Rome are expected to boot and run, but the end-user will see the message “Unsupported Hardware Detected”.

DEVICES TESTED BY PARTNERS WITH MILAN

PLEASE CONTACT THE RESPECTIVE PARTNER FOR MORE INFORMATION

Category	Partner	Devices
Connectivity (NIC, FC)	Mellanox (NIC)	25G: MCX4121A-ACAT, MCX512A-ACAT 100G: MCX556A-EDAT (Gen 4), MCX623106AE-CDAT (Gen 4) 200G: MCX653106A (Gen 4)
	Broadcom (NIC)	1G: BCM5720-2P 25G: BCM957414A4142CC 100G: BCM957508-P2100G
	Broadcom (FC)	32G: LPe36000
	Marvell (NIC & FC)	NIC: QL41262HLCU, QL41212HLCU-CK FC: QLE2764, QLE2772
	Cornelis (NIC)	100G Omni-Path: 100HFA016FS

DEVICES TESTED BY PARTNERS WITH MILAN

PLEASE CONTACT THE RESPECTIVE PARTNER FOR MORE INFORMATION

Category	Partner	Devices
	Broadcom (RAID/HBA)	• 9400 (Gen 3) and 9500 (Gen 4) series
Storage	Kioxia	• CM6 and CD6 (Gen4)
	Micron	• 9300 (Gen 3) • 7300 (Gen 3) • 2300 M.2 (Gen 3)
	Samsung	• PM1733, PM9A3 (Gen 4) • PM1725b, PM983 (Gen 3)
	SK Hynix	• PE8010 (Gen 4)
	Western Digital	• Ultrastar DC SN640 (Gen 3) • Ultrastar DC SN840 (Gen 3)
Accelerator (dGPU, FPGA)	NVIDIA	• Tesla - V100
	AMD Radeon GPU's	• MI25, MI50, MI60, MI100
	Xilinx	• Alveo: U50, U200, U250, U280, Versal

DISCLAIMER & ATTRIBUTION

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions and typographical errors.

The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes.

AMD MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE CONTENTS HEREOF AND ASSUMES NO RESPONSIBILITY FOR ANY INACCURACIES, ERRORS OR OMISSIONS THAT MAY APPEAR IN THIS INFORMATION.

AMD SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL AMD BE LIABLE TO ANY PERSON FOR ANY DIRECT, INDIRECT, SPECIAL OR OTHER CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF ANY INFORMATION CONTAINED HEREIN, EVEN IF AMD IS EXPRESSLY ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

ATTRIBUTION