## Reading questions

Pre-class answer

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1. A given program spends 10% of its time in an initial startup

phase, and then 90% of its time in work that can be easily

parallelized. Assuming a machine with homogeneous cores, plot the

idealized speedup and parallel efficiency of the overall code

according to Amdahl's law for up to 128 cores. If you know how,

you should use a script to produce this plot, with both the serial

fraction and the maximum number of cores as parameters.

**Strong scaling:**

Assume time to run the program is T

For p=128 cores, Tser=T, Tpara­=0.1\*T+0.9\*T/128

Max Speed up S(p)=

efficiency = S(p)/p = 9.34/128

**Weak scaling:**



efficiency = S(p)/p 

2. Suppose a particular program can be partitioned into perfectly

independent tasks, each of which takes time tau. Tasks are

set up, scheduled, and communicated to p workers at a (serial)

central server; this takes an overhead time alpha per task.

What is the theoretically achievable throughput (tasks/time)?

k tasks

(T/p+alpha)\*k

when p goes to infinity

it is tasks/time = k/(T/p+alpha)\*k =1/alpha

3. Under what circumstances is it best to not tune?

It best to not tune When the tuning is not so important and when the tuning is hard to implement or in the case that the codes is likely to be changed (frequently) in the future and the tuning will make it difficult to revise the code.

4. The class cluster consists of eight nodes and fifteen Xeon Phi

accelerator boards. Based on an online search for information on

these systems, what do you think is the theoretical peak flop rate

(double-precision floating point operations per second)? Show how

you computed this, and give URLs for where you got the parameters

in your calculation. (We will return to this question again after

we cover some computer architecture.)

From the course website, we know the machine has “fifteen Xeon Phi 5110P boards hosted in eight 12-core compute nodes consisting of Intel Xeon E5-2620 v3 processors”. I think the hosts should not be counted into the theoretical peak flop rate as their job is to distribute the work to the Xeon Phi 5110P boards

from: http://www.intel.com/content/www/us/en/benchmarks/server/xeon-phi/xeon-phi-theoretical-maximums.html

we know that flops of Theoretical Peak single precision FLOPS of a Xeon Phi 5110P is 32 FLOPS/clock x 60 cores x 1.053 GHz = 2021.76 GF/s.

So For 15 Xeon Phi 5110P, the Theoretical Peak (single precision) FLOPS is 15\*1021.76GF/s=15326.4 GF/s

5. What is the approximate theoretical peak flop rate for your own machine?

My machine is using Intel® Core™ i5-3230M Processor.

From:

http://ark.intel.com/products/72056/Intel-Core-i5-3230M-Processor-3M-Cache-up-to-3\_20-GHz-BGA

8 FLOPS/clock x 2 cores x 2.6 GHz = 41.6 FLOPS