Preliminary Research Presentation

A Bottom-to-Top Optimized Design of Compact Neural Readout

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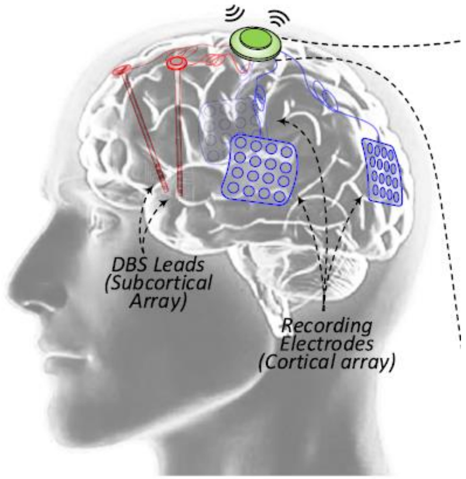
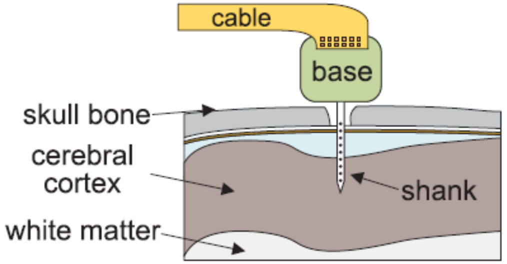
- M.S. in biomedical engineering
    - Extensive training in circuit design
        - AFE (LNA, VGA, ADC)
        - Neuromorphic computing, analog MAC
        - Spiking neural network
        - …
    - Knowledge foundation in bioelectronics
        - Bioelectronics and biosensors
        - MEMS
        - Optics
        - …
- The presentation is customized based on my background
- The ideas are immature, any thoughts and suggestions are welcome

Outline

- Background
- Proposal 1: improve the AFE-Embedded NS SAR
- Proposal 2: improve the analog-to-feature conversion
- Conclusion

Importance of Compact Neural Readout

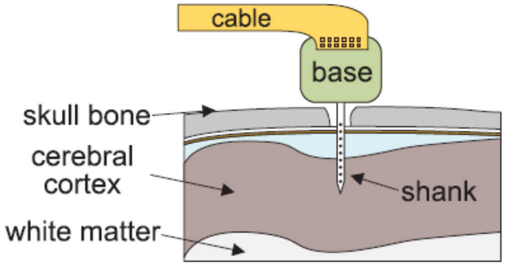


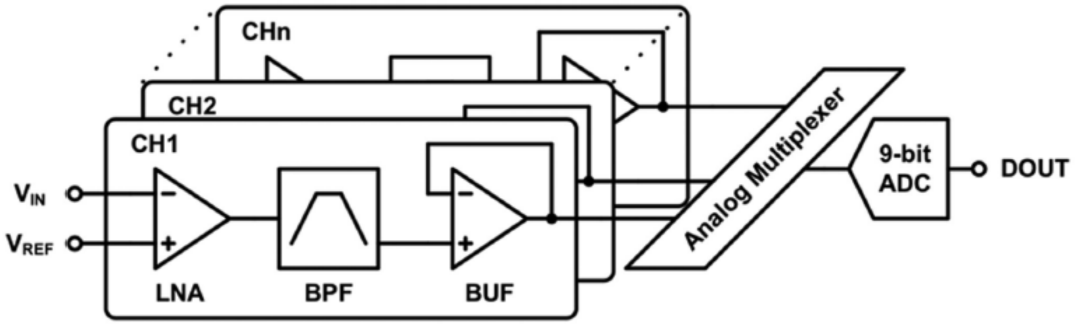


- Neural interface is important!
- Compactness is crucial in neural recording front-end
- Compact
  - Physically
    - Small area, low noise, low power, artifacts tolerance
  - Functionally
    - Machine learning function

Ref: Pazhouhandeh JSSC 2021, Dorigo JSSC 2018, Kim TBioCAS 2018

Neural interface design challenge





- Conventional neural AFE faces significant challenges
- Physically compact
  - Front-end saturation
- Functionally compact
  - Excessive data rate
- Improvements are needed!

Ref: Pazhouhandeh JSSC 2021, Dorigo JSSC 2018, Kim TBioCAS 2018

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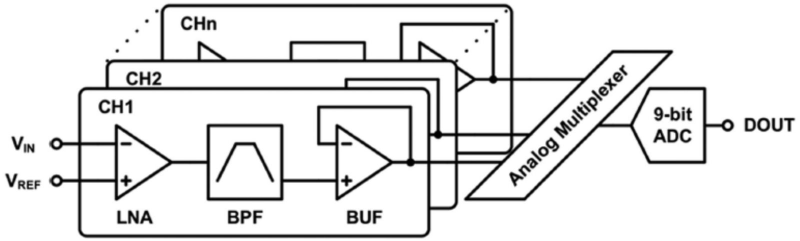
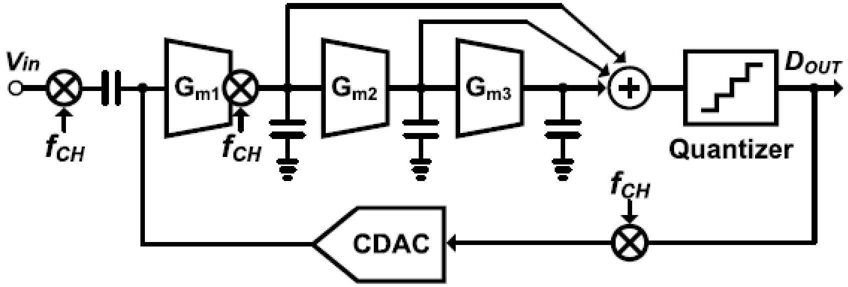
New ADC-focused neural front-end



- Signal conditioning
- Medium resolution ADC

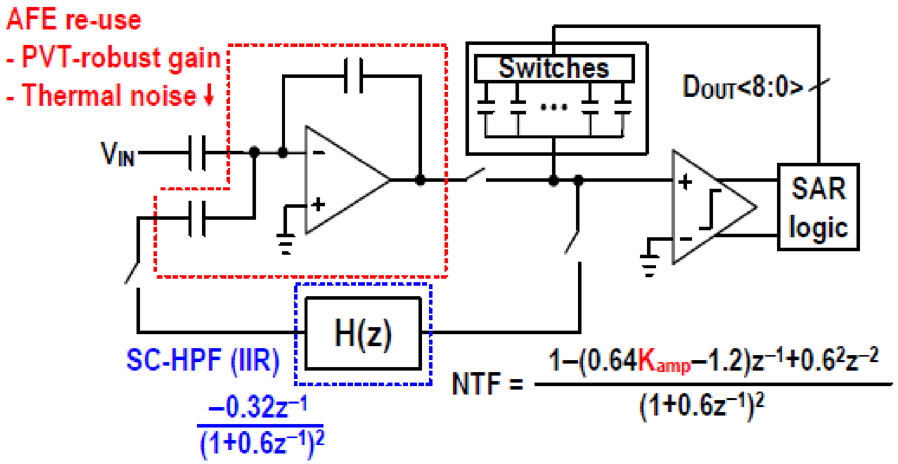
?



- No signal conditioning
- High DR/SNDR ADC

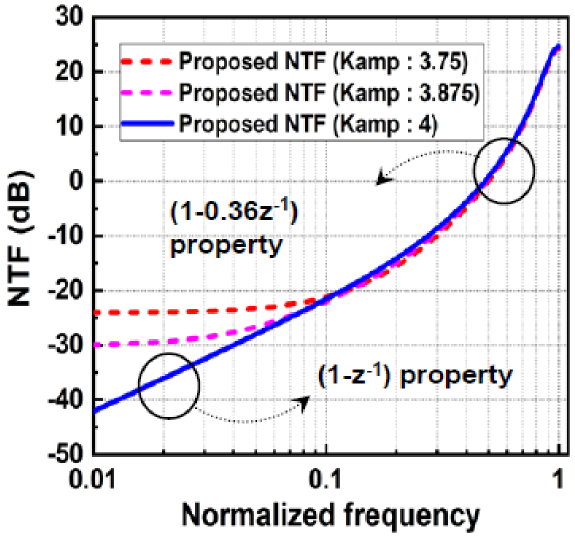
Ref: Dorigo 2018 JSSC, Bang 2018 VLSI

AFE-Embedded NS SAR for Neural Recording



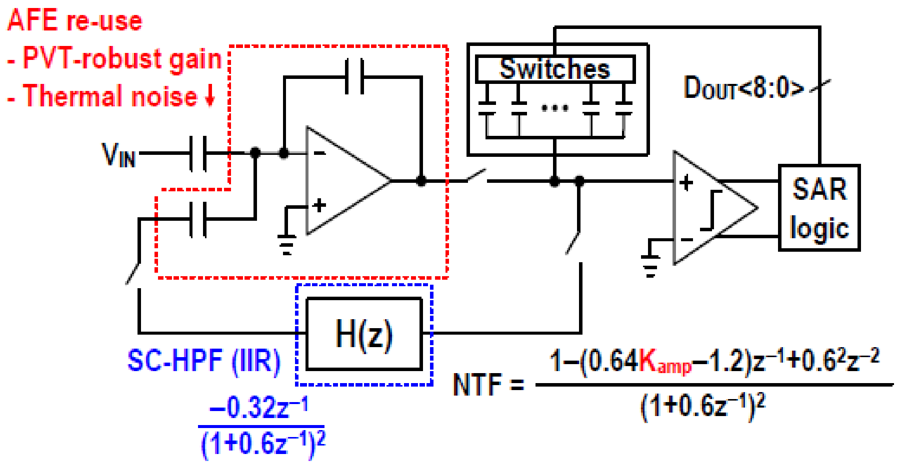
- NS SAR with low OSR
- AFE-embedded architecture

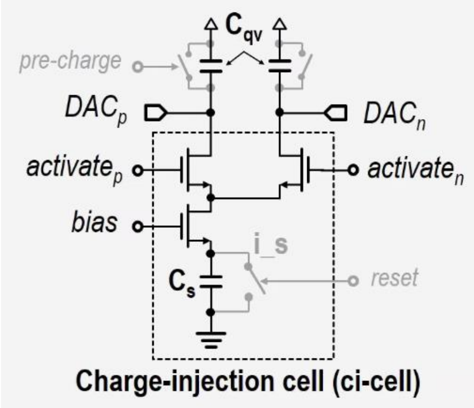
- DAC mismatch and kT/C noise
  - 9 bit (5pF CDAC, 15fF Cu)
  - 15 fF unit capacitor
- Closed-loop opAmp

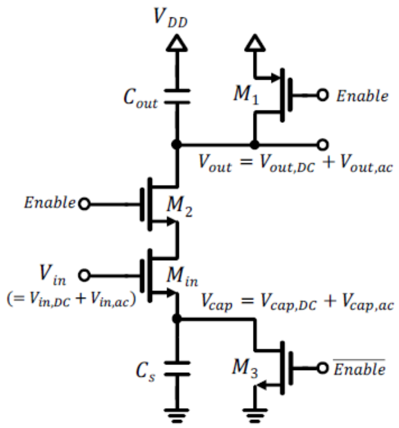


Ref: Jeong TBioCAS 2022

Improvement with ci-cell







- kT/C cancellation
- Amplifier improvement
  - Charge-domain preamplifier
  - PVT-Robust dynamic amplifier
- Mismatch calibration array
  - Calibration the CDAC
  - Calibration the gain
  - Ci-cell

Ref: Li ESSCIRC 2021

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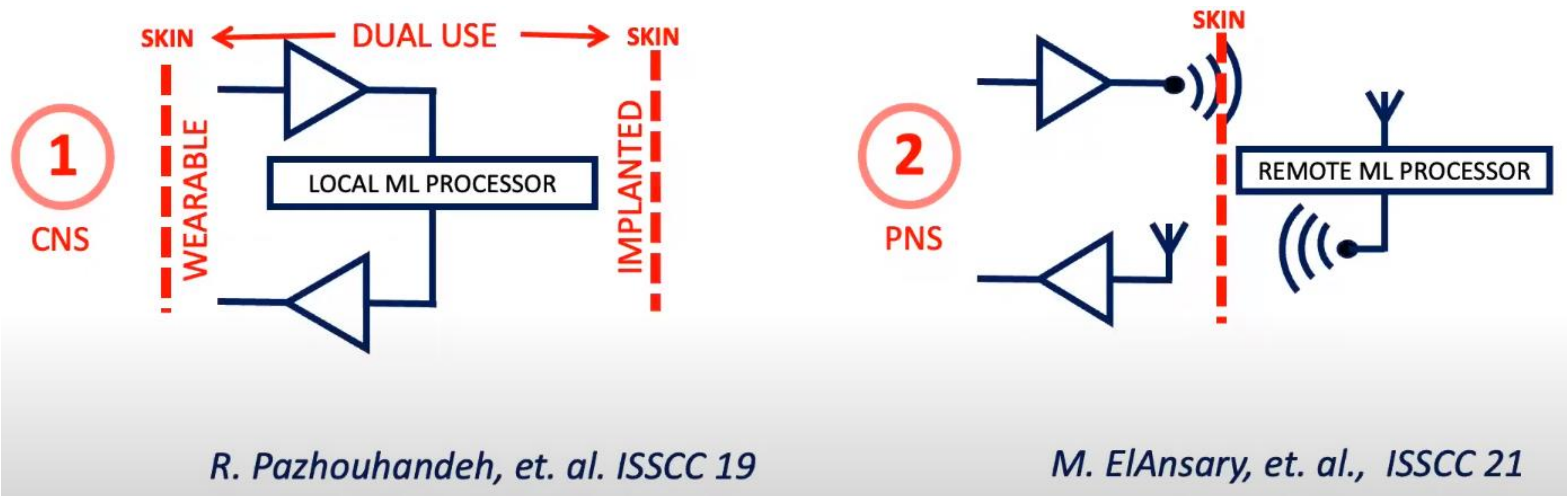
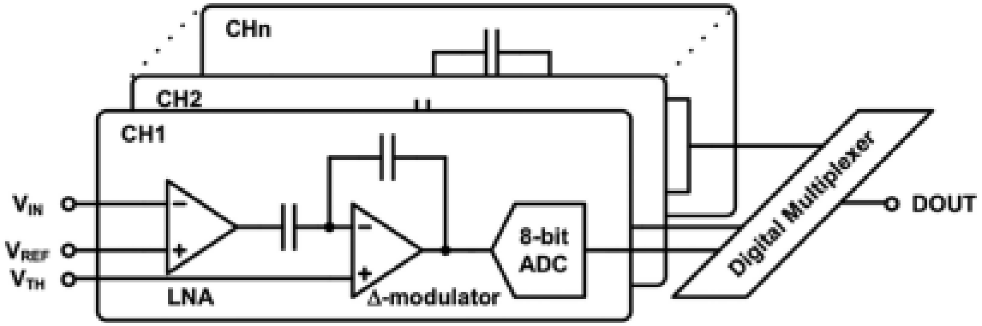
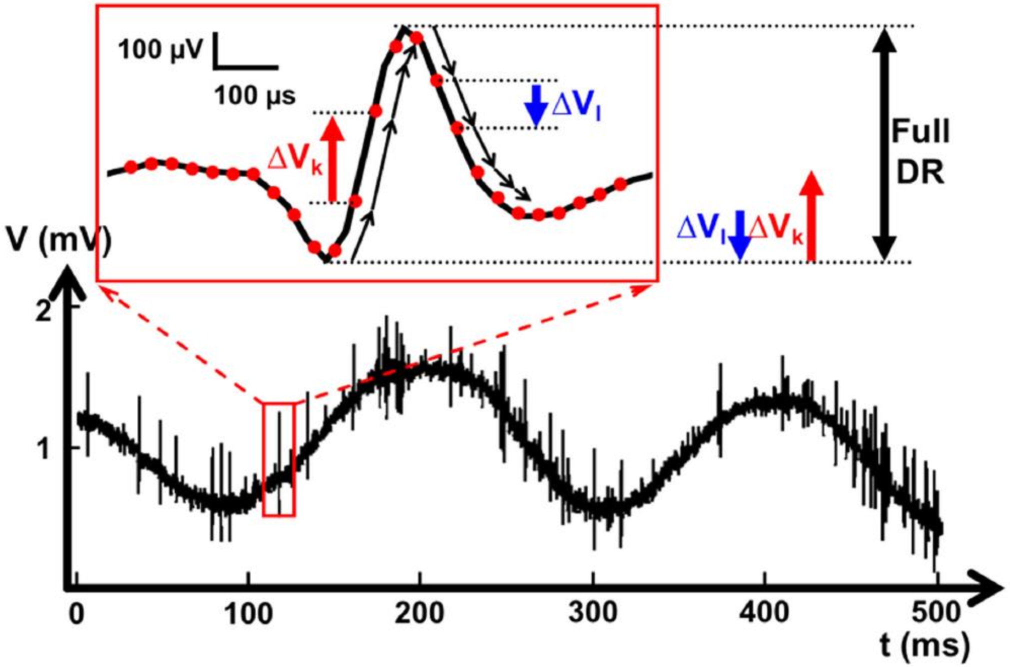
Reduce the data rate to close the loop



- Local ML: Computing resources, e.g. memory
- Remote ML: Communication resources
- Data compression
  - Analog-to-feature converter

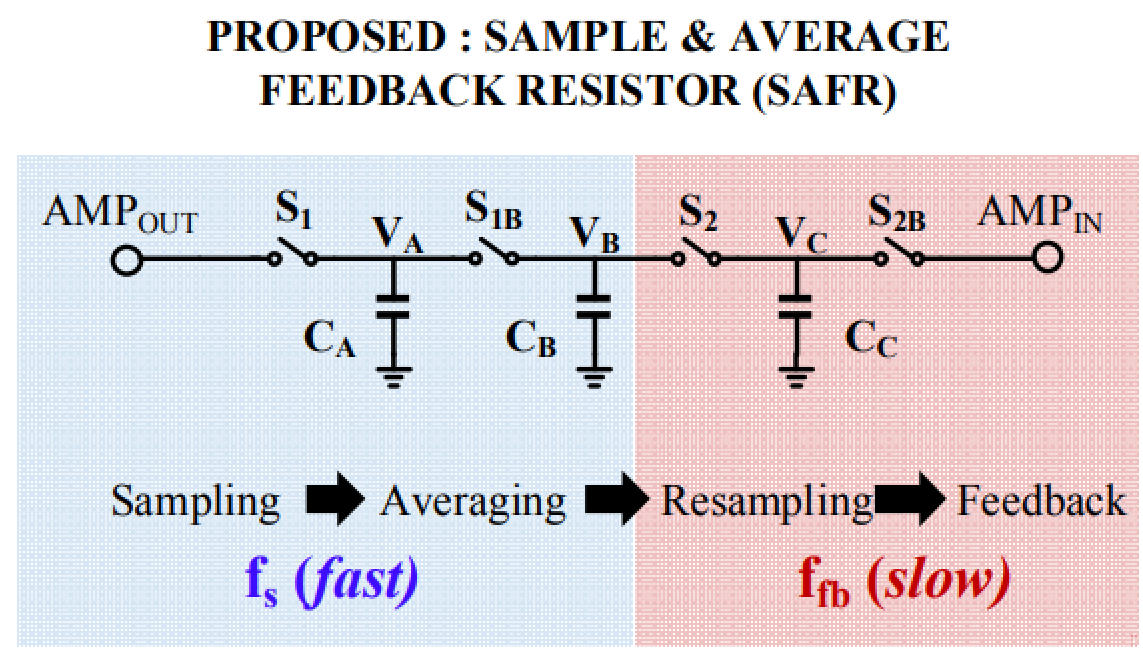
AFE with △-Neural Recording with Data Compression





- AFE with data compression
- Problem
  - LFP information is lost

Solution: Sample and Average Circuits



- LP is sampled and averages
- LP prefiltering + SC resistor
- Digitized as CM artifact through direct sigma delta conversion

Ref: Rothe 2020 VLSI

Outline

- Background
- Proposal 1: improve the artifact tolerance
- Proposal 2: relax the data rate burden
- Conclusion

Conclusion:

- NS SAR for direct neural recording
  - Mismatch, gain calibration
  - Better area and power efficiency
- Analog-to-feature conversion embedded in SoC
  - Before digitalizing, analog to feature conversion can firstly be done to reduce the data rate

Better neural readout

Circuit elements,
e.g. PVT robust amp,
offset-tolerant ci-cell

→

Direct
Conversion ADC

→

SoC solution
e.g. AFC

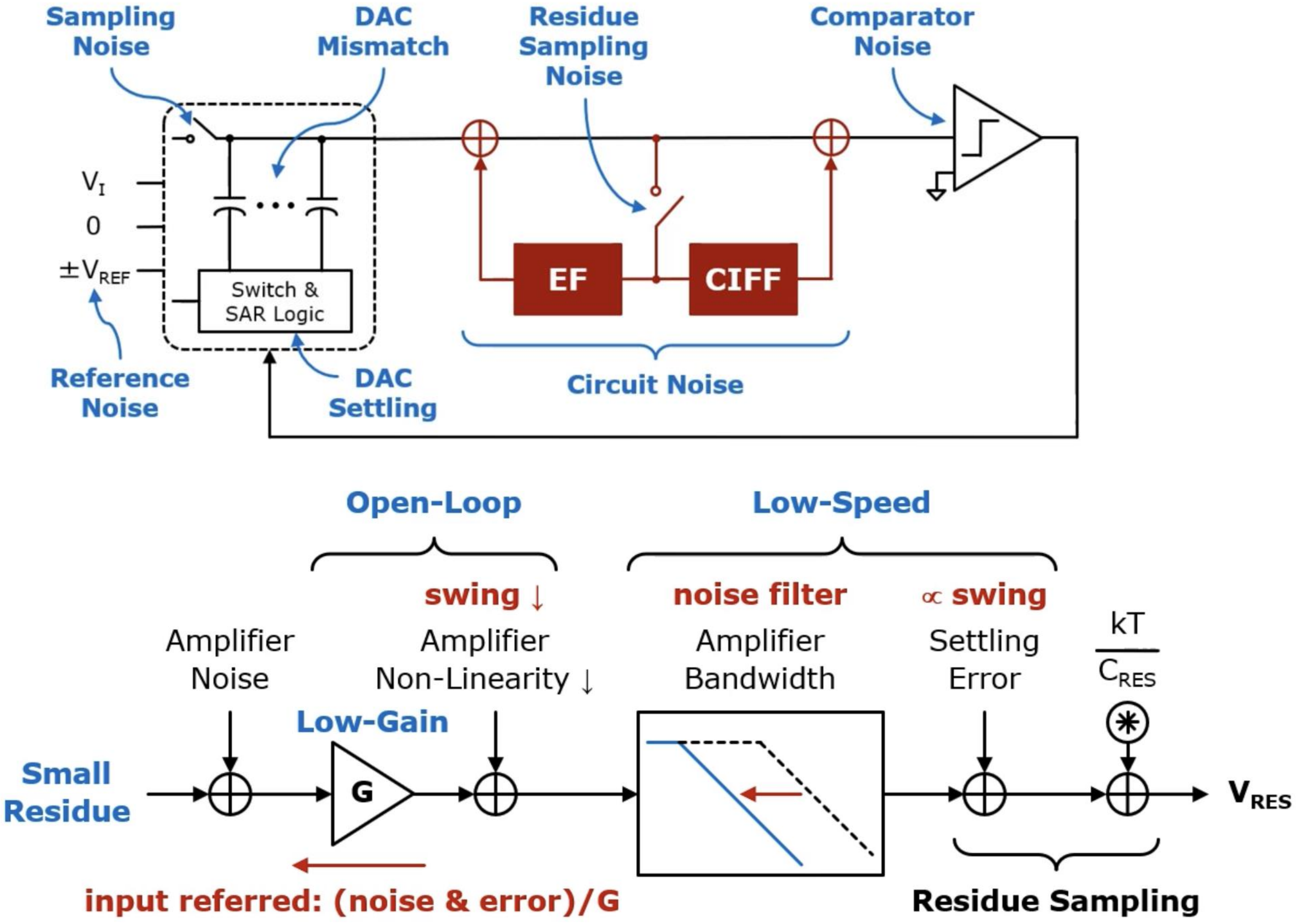
Thanks for your attention!

I am ready for any questions.

AND

Your Suggestions!

Noise-shaping SAR in neural front-end



- Can be noise-shaped
  - Quantization noise
  - Comparator noise
- Can not be noise-shaped
  - Sampling Kt/C noise
  - Loop filter noise
- Additional gain stage is required.
- Reuse the IA!

Cascade of Integrators with feed-forward (CIFF)

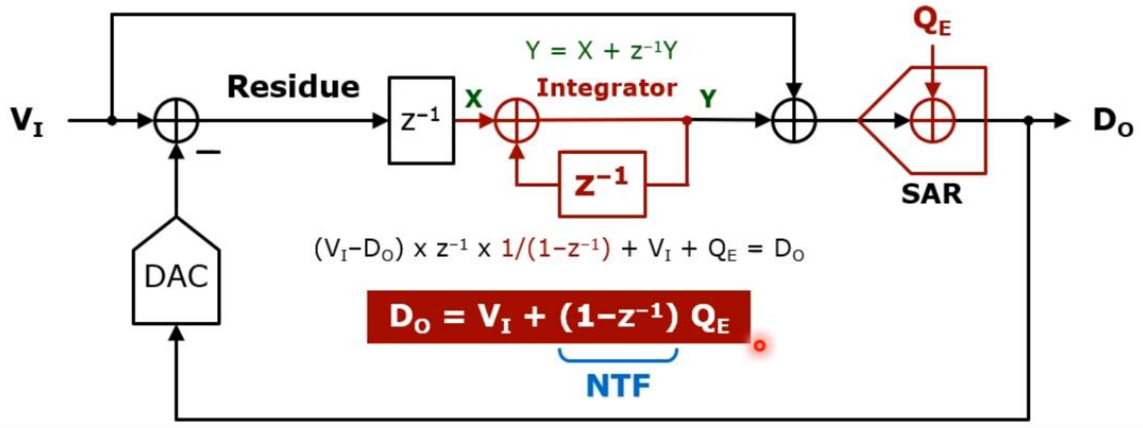
Oversampling + Residue Integration

- D_O = ADC [V_I + Integrated Residue]
- Residue = $V_I - D_O$

Digitize "total remaining signal" along with input signal

Sample	V_I [n]	Integrated Residue	V_I [n] + Inte. Res.	Do [n]	Residue [n]
1	5.2	0	5.2	5	0.2
2	5.2	0.2	5.4	5	0.2
3	5.2	0.4	5.6	6	−0.8
4	5.2	−0.4	4.8	5	0.2
5	5.2	−0.2	5.0	5	0.2
Avg.	5.2			5.2	

Total Residue=0



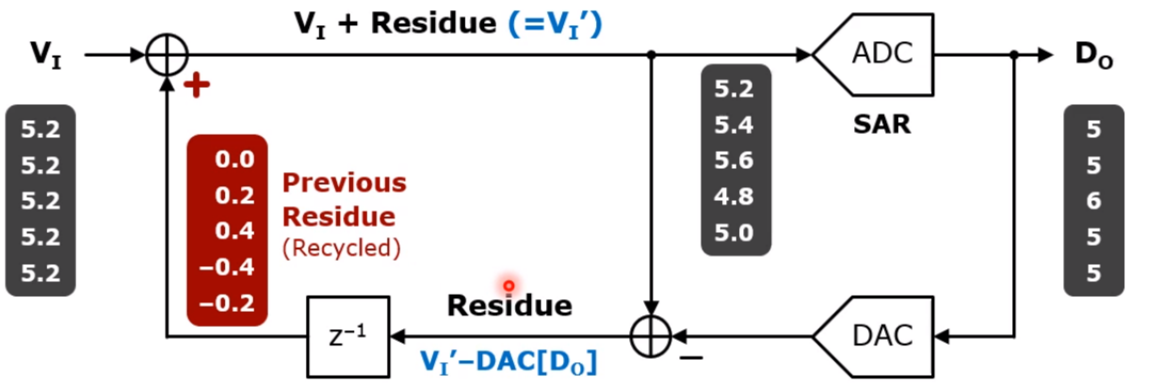
Error feedback (EF)

- ☐ D_O = ADC [V_I' (=V_I + Previous Residue)]
- ☐ Residue = $V_I' - D_O$

Recycle previous "remaining signal" into input signal

Sample	V_I [n]	Residue [n-1]	V_I' = V_I [n] + Residue [n-1]	D_O [n]	Residue [n] (= $V_I' - D_O$)
1	5.2	0	5.2	5	0.2
2	5.2	0.2	5.4	5	0.4
3	5.2	0.4	5.6	6	−0.4
4	5.2	−0.4	4.8	5	−0.2
5	5.2	−0.2	5	5	0
Avg.	5.2			**5.2**	

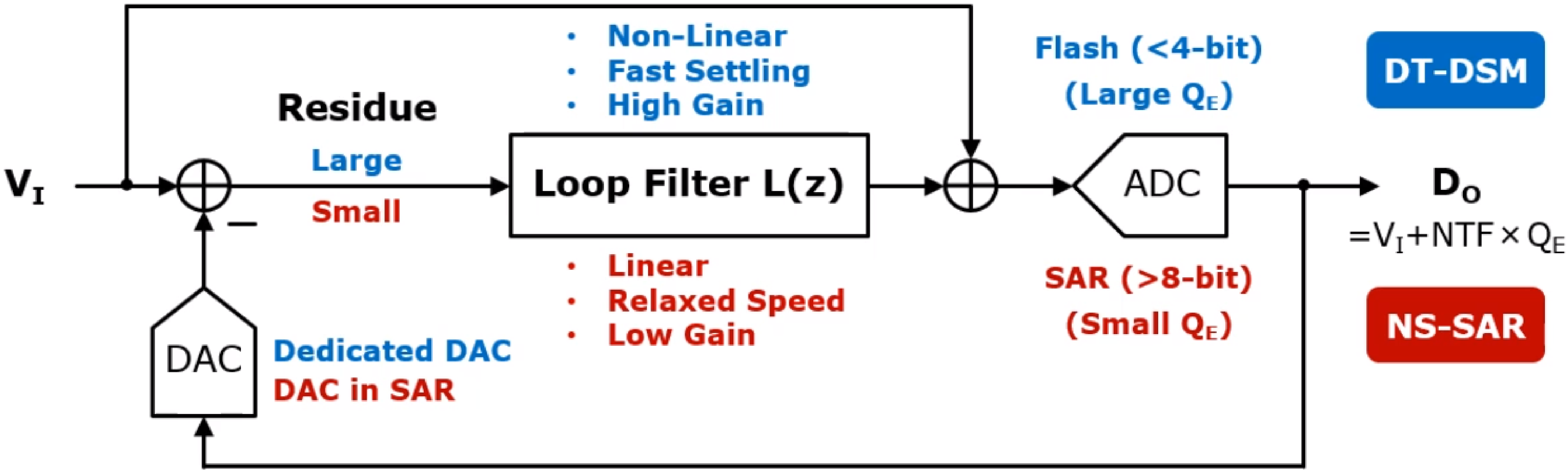
Latest Residue=0



EF CIFF comparsion

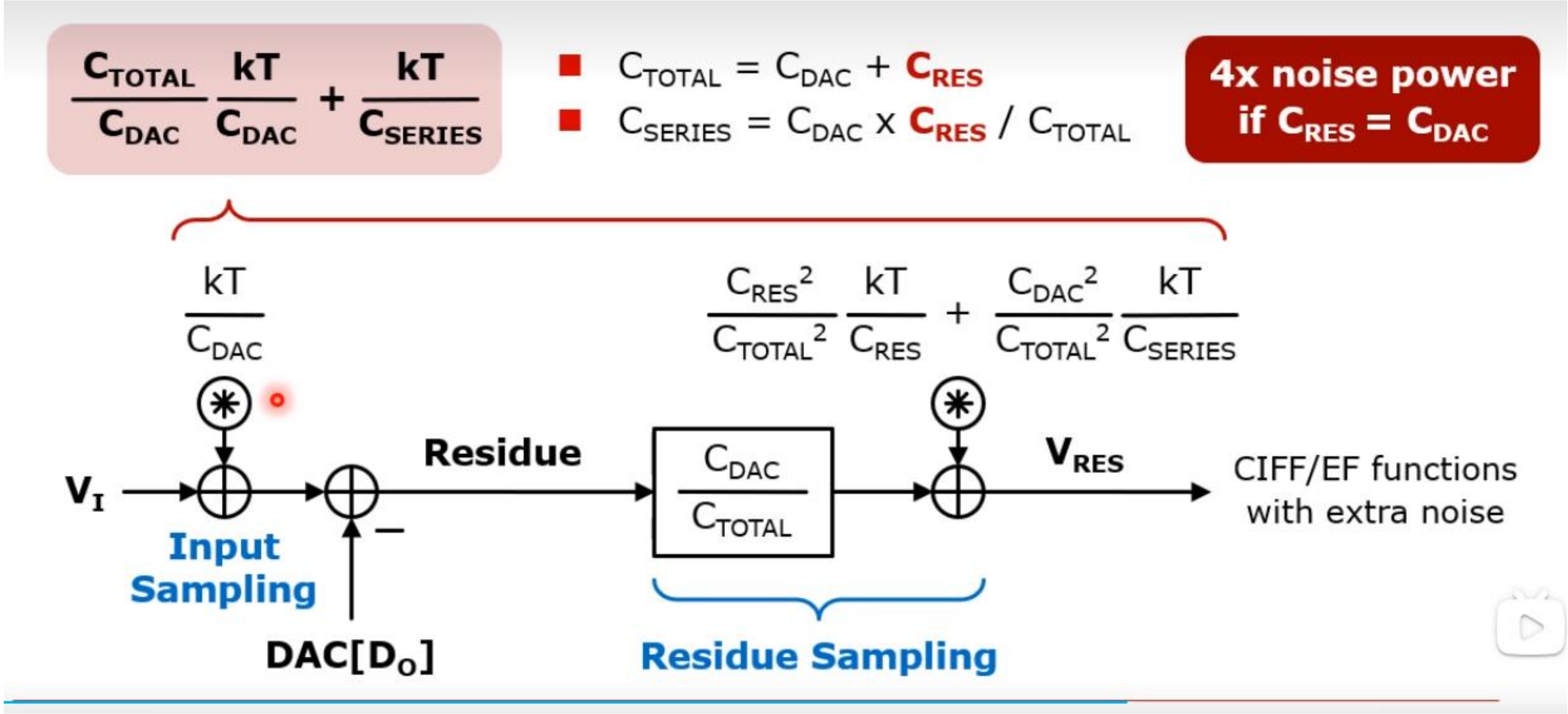
	CIFF	EF
Oversampling with	Residue integration	Residue compensation
Filter	L(z): IIR filter (integrator)	H(z): FIR filter
NTF	1 / (1+L(z))	1 – H(z)
Q_E × NTF → 0	L(z) → ∞	H(z) → 1
Circuit Requirement	Gain stage	Accurate coefficient
PVT Variation	**Less sensitive** (gain variation)	**Sensitive** (coefficient variation)
Design Consideration	Sufficient gain	Coefficient control

DSM vs NS SAR



- However, Noise-Shaping SAR
  - Successive approximation ($F_S \downarrow$) + Noise shaping (OSR $\uparrow$)
  - Effective signal bandwidth = F_S / (2 x OSR) → **VERY SLOW**

Input referred sampling noise



Multi-input comparator