Report (July 26th)

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Summary of previous work (7/8-7/26)

- 7/8-7/11: Configured the working environment on Yangzi and local. Ran through the official tutorial programs on Vitis. Learned the usage of HLS pragmas and tested how they improve performance.
- 7/12-7/15: Learned how to write config files based on available resources and organize host code in OpenCL. Designed several simple functions in HLS and passed all the emulation on Yangzi. Understood how pragmas influence hardware synthesis in these examples.
- 7/16-7/19: Learned the MLP code from Yuan and added several layers to it. Ensured the iteration interval of pipelined loops is 1. Discussed how to optimize the code with Yuan.
- 7/20-7/25: Reconstructed the code structure and arranged new dataflow. Designed structs and interfaces to optimize the performance. The latency has now reduced from 5365 to 2376 cycles on a certain network, as the following pictures show.

Name	Issue Type	Latency (cycles)	Latency (ns)	Iteration Latency	Interval	Trip Count	Pipelined
top		5365	1.788E4		5366		no
dataflow_parent_loop_proc		5095	1.698E4		5095		no
dataflow_in_loop_VITIS_LOOP_121_5		383	1.277E3		314		dataflow

Before optimization

Name	Issue Type	Latency (cycles)	Latency (ns)	Iteration Latency	Interval	Trip Count	Pipelined
top		2376	7.919E3		2377		no
dataflow_parent_loop_proc		2375	7.916E3		2375		no
dataflow_in_loop_VITIS_LOOP_192_5		243	810.000		142		dataflow

After optimization

- 7/26：Discussed with Yuan and came up with a further optimized dataflow balancing the throughput between different layers.

Plans

- Continue implementing the code based on today's discussion.
- Merged the MLP part with the MCTS part ensuring matched throughput.
- Do design space exploration based on the current structure.