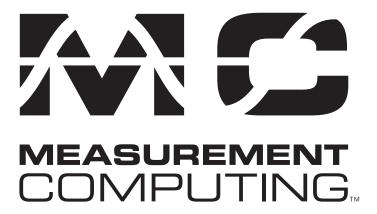
# **SPECIFICATIONS**

# PC104-DAS16JR/12 PC104-DAS16JR/16

Analog Input, Digital I/O, Counters



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### **Power Consumption**

+5VDC quiescent

PC104-DAS16Jr/12 140 mA typical, 230 mA max PC104-DAS16Jr/16 145 mA typical, 205 mA max

+ 5VDC Operating (A/D converting to FIFO)

PC104-DAS16Jr/12 250 mA typical, 375 mA max PC104-DAS16Jr/16 235 mA typical, 350 mA max

#### **Analog Input Section**

A/D converter type

PC104-DAS16Jr/16 AD7805 PC104-DAS16Jr/12 AD7800

Resolution

PC104-DAS16Jr/12 12 bits PC104-DAS16Jr/16 16 bits

Number of channels 8 differential or 16 single-ended, switch-selectable

Input ranges

PC104-DAS16Jr/12  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 2.5V$ ,  $\pm 1.25V$ ,  $\pm 0.625V$ , 0 to 10V, 0 to 5V, 0 to 2.5V,

0 to 1.25V, fully programmable

PC104-DAS16Jr/16  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 2.5V$ ,  $\pm 1.25V$  programmable in Bipolar mode OR 0 to

10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V programmable in Unipolar mode

Polarity Unipolar/Bipolar, switch-selectable

A/D Pacing Programmable: internal counter, external source (Din 0 / Trigger) or

software polled

A/D Trigger sources External polled gate trigger (DIn 0)

A/D Triggering Modes

Digital: Gated pacer, software polled. (Gate must be disabled by software after

trigger event.)

Data transfer From 512 sample FIFO via interrupt, DMA or software polled

DMA Channel 1 or 3, switch-selectable

DMA enable Programmable

A/D conversion time

PC104-DAS16Jr/12 3.3 μs PC104-DAS16Jr/16 10 μs

Throughput

PC104-DAS16Jr/12 150 kHz PC104-DAS16Jr/16 100 kHz

Accuracy

PC104-DAS16Jr/12 0.01% of reading,  $\pm 1LSB$  PC104-DAS16Jr/16 0.003% of reading,  $\pm 1LSB$ 

Integral Linearity error

PC104-DAS16Jr/12  $\pm 1$  LSB

PC104-DAS16Jr/16  $\pm 1.5$  LSB ( $\pm 3$ LSB on 1.25V ranges)

Differential Linearity ±1 LSB

No missing codes guaranteed

PC104-DAS16Jr/12 12 bits PC104-DAS16Jr/16 16 bits

Gain drift (A/D specs)

PC104-DAS16Jr/12 ±6 ppm/°C PC104-DAS16Jr/16 ±7 ppm/°C

Zero drift (A/D specs)

PC104-DAS16Jr/12 ±1 ppm/°C PC104-DAS16Jr/16 ±2 ppm/°C  $\begin{array}{lll} \text{Common Mode Range} & \pm 10 \text{V} \\ \text{CMRR @ 60 Hz} & 70 \text{ dB} \\ \text{Input leakage current (@ 25 deg C)} & \pm 20 \text{ nA} \\ \text{Input impedance} & 10 \text{ Mohms min} \\ \end{array}$ 

Absolute maximum input voltage ±35V

## **Digital I/O Section**

Digital type FPGA

Configuration Two ports, 4 bits each, 4 input and 4 output

Interrupts Programmable: levels 2 to 7

Interrupt enable Programmable

Interrupt sources End-of-conversion, DMA terminal count

#### **Counter Section**

Counter type 82C54

Configuration 3 down-counters, 16 bits each

Counter 0 - Independent user counter

Source: Programmable (external or

100 kHz internal source)

Gate: Available at connector (DIn 2)
Output: Available at connector (Ctr 0 Out)

Counter 1 - ADC Pacer Lower Divider

Source: Jumper-selectable 1/10 MHz

Gate: Tied to Counter 2 gate, can be program-enabled at user

connector (DIn 0 / Trigger).

Output: Chained to Counter 2 Clock. Counter 2 - ADC Pacer Upper Divider

Source: Counter 1 Output.

Gate: Tied to Counter 1 gate, programmable source.

Output: Programmable as ADC Pacer clock, hardwired to user

connector (Ctr 2 Out)

Clock input frequency 10 MHz max High pulse width (clock input) 30 ns min Low pulse width (clock input) 50 ns min Gate width high 50 ns min Gate width low 50 ns min Input low voltage 0.8V max Input high voltage 2.0V min Output low voltage 0.4V max Output high voltage 3.0V min

Crystal oscillator

Frequency 10 MHz Frequency accuracy 100 ppm

#### **Environmental**

Operating temperature range 0 to 50°C Storage temperature range -40 to 100°C

Humidity 0 to 90% non-condensing

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