



# AN10987

## TDF854x and TDF855x automotive amplifiers

Rev. 9 — 20 October 2015

Application note

### Document information

Info	Content
<b>Keywords</b>	TDF8541, TDF8544, TDF8546, TDF8546A, TDF8548A, TDF8554, TDF8555 and TDF8556, 4-channel automotive amplifier, regulator, high efficiency, Class-AB,
<b>Abstract</b>	This application note describes applications for the new NXP Semiconductors class-AB amplifier family, including recommendations, schematics, lay-out, component choices, EMI measurements and heatsink calculation examples.



**Revision history**

Rev	Date	Description
v.9	20150903	Text changes made in relation to heatsink calculation and subwoofer applications
v.8	20131002	minor text corrections made throughout the document
v.7	20130603	<u>Section 3 "Heatsink calculation"</u> has been changed
v.6	20121219	text changes made relating to the addition of TDF8548A
v.5	20120929	text changes made relating to the addition of TDF8546A
v.4	20120815	reworked document
v.3	20111025	reworked text
v.2	20110824	text changes
v.1	20110530	initial version

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## 1. Introduction

### 1.1 General description

The TDF854x and TDF855x family is the new generation of complementary quad BTL audio power amplifiers. The amplifiers have full I<sup>2</sup>C-bus controlled diagnostics (including start-up diagnostics) and they are intended for car radio applications.

These amplifiers operate at a battery voltage as low as 6 V making them suitable for operating in a stop/start car. The amplifier uses a complementary DMOS output stage in a Silicon-On-Insulator (SOI) based BCD process. The DMOS output stage ensures a high-power output signal with perfect sound quality. The SOI-based BCD process ensures a robust amplifier where latch-up cannot occur. There is good separation between the four independent channels (every component is isolated, no substrate currents).

The TDF854x amplifier can be used as a stand-alone amplifier. The TDF8554/55/56 includes a number of linear voltage regulators for use in a typical car radio application. The amplifiers are to a great extent hardware and software compatible with their predecessor amplifiers TDA8594/95 and TDA8588/89.

[Table 1](#) provides a brief overview of the amplifier family.

**Table 1. Brief overview of amplifier family**

Amplifier	Output power (W)	Description	Package
TDF8541	4 × 45	4-channel BTL	DBS27P / DBSMS27P / HSOP36
TDF8544	4 × 50	4-channel BTL	DBS27P / DBSMS27P / HSOP36
TDF8546	4 × 45	4-channel BTL high efficiency	DBS27P / DBSMS27P / HSOP36
TDF8546A	4 × 45	4-channel BTL high efficiency	DBS27P / DBSMS27P / HSOP36
TDF8548A	4 × 48	4-channel BTL high efficiency	DBS27P / DBSMS27P / HSOP36
TDF8554	4 × 45	4-channel BTL + 5 linear regulators	DBS37
TDF8555	4 × 45	4-channel BTL + 6 linear regulators	DBS37
TDF8556	4 × 50	4-channel BTL + 5 linear regulators	DBS37

The TDF8546A and TDF8548A are improved versions of the TDF8546. They have greatly improved EMI immunity, improved quiescent current and can detect 1 kΩ line driver loads.

In this document, all information relating to the TDF8546 is also valid for the TDF8546A and TDF8548A, except for EMI immunity and quiescent current.

The EMI immunity described in [Section 2.2.3.2](#) is not valid for the TDF8546A and TDF8548A. The SMD beads described in [Figure 9](#) are not needed for the TDF8546A and TDF8548A.

## 2. Application circuit

### 2.1 Introduction

The amplifier application circuits are relatively simple with almost no need for a specific layout or for specific components. However, some recommendations are given in the following paragraphs.

### 2.2 Application hints and tips

#### 2.2.1 Basics

The following list comprises the major features:

- **HF decoupling** - To correctly HF decouple the power supply, use capacitors close to the IC supply pins, a typical value of 220 nF is used. When SMD capacitors are used, be aware of differences in behavior regarding the capacitor material. Best results are obtained using NPO capacitors, which have a low Electrical Series Resistance (ESR). Next best are X7R capacitors and finally the Y5V capacitors, which have a considerable ESR.
- **Minimum interference on small input signals** - To achieve minimum interference on small input signals, connect the ground of the input signal to the signal ground of the amplifier. This connection makes the ground track "clean", with no large currents flowing across it, as would be the case with the power ground track.
- **Common-Mode Rejection Ratio (CMRR)** - Keeping the signal ground track close to long input tracks on the application board is beneficial. The amplifier common-mode rejection ratio (CMRR) suppresses any interference that becomes common mode as a result.
- **V<sub>P</sub> and power ground track** - A copper layer of 75 µm (or thicker) and a track-width of at least 5 mm are used for high output power. These tolerances minimize the losses in the tracks for V<sub>P</sub> and power ground.
- **Cross-over** - To prevent cross-over from large output signals to small input signals, avoid placing input tracks close to output tracks.

#### 2.2.2 EMI

To minimize EMI of the amplifier, it may be necessary to place extra components to meet the requirements.

Capacitors can be placed between the amplifier outputs and power ground. These capacitors are used in close range to, or even inside, the connector that is at the edge of the PCB/amplifier box. The capacitor placement is essential to minimize any EMI (immunity) induced by the loudspeaker wires. The value of the capacitors is 100 pF to 22 nF, depending on the application. When larger values are used, it may be necessary to use Boucherot filters across the outputs to prevent instabilities/oscillations.

Fixed values cannot be defined for both countermeasures as they depend on the application, the tracks, the layout, the ground, the shielding, and so on. A start value is chosen that it is sufficient for correct functionality of the application. This start value should be verified by measurement.

### 2.2.3 EMI measurements

#### 2.2.3.1 Radiated EMI

The interference the amplifier application creates in its environment is measured across a large frequency range and contained in the radiated EMI. The frequency range spans from 150 kHz in the AM-band, through the FM-band and up to the 1 GHz GSM-band.

Since the different frequency bands need different antennas, the measurements are split into the following groups:

- **Rod antenna** - 150 kHz to 30 MHz
- **Biconical antenna** - (horizontal and vertical plane) 30 MHz to 300 MHz
- **Log periodic antenna** - (horizontal and vertical plane) 300 MHz to 1 GHz

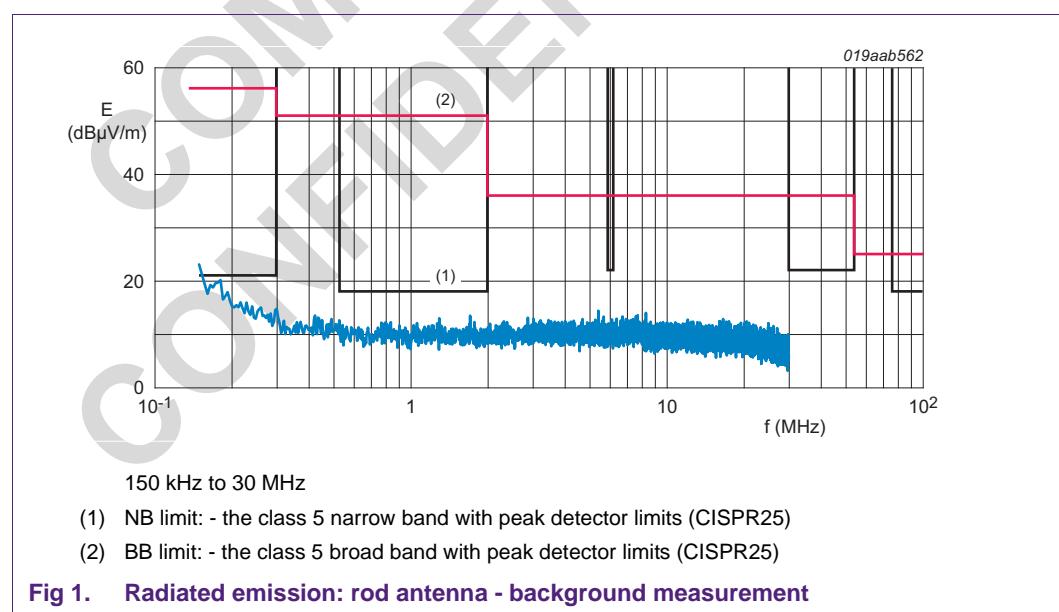
This application note contains measurement data that conforms to "emission EN 55025", with limits of CISPR25 level 5.

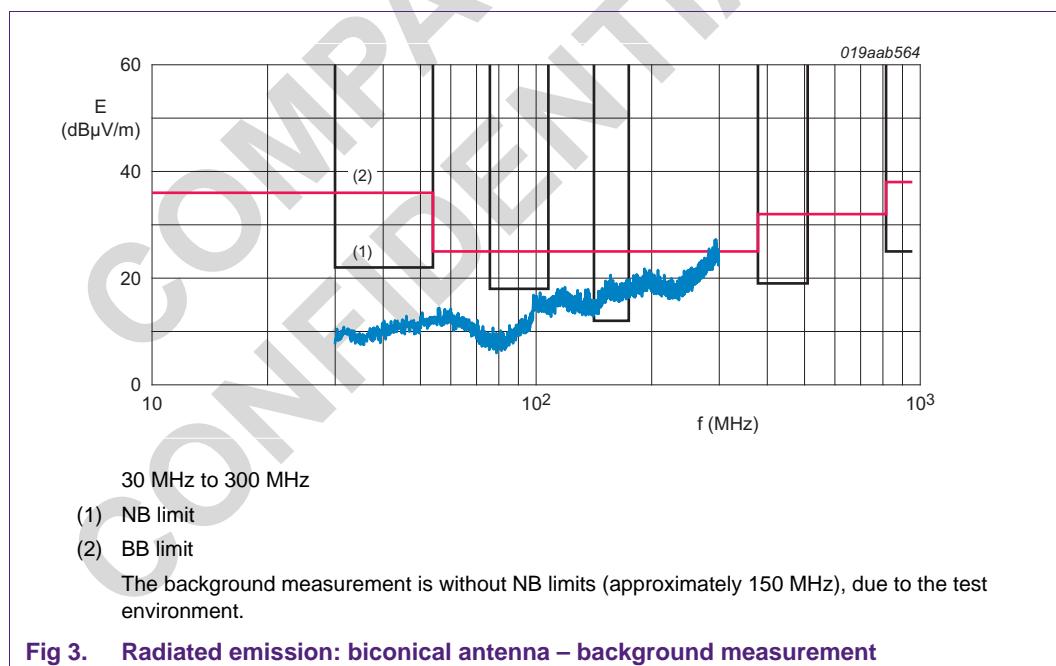
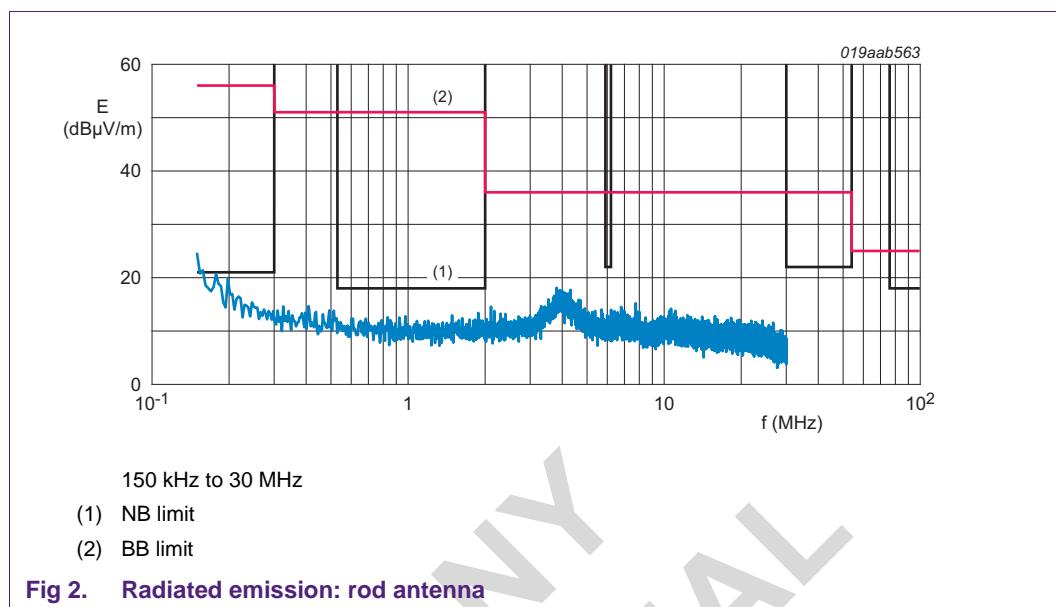
The conditions of the amplifier are as follows:

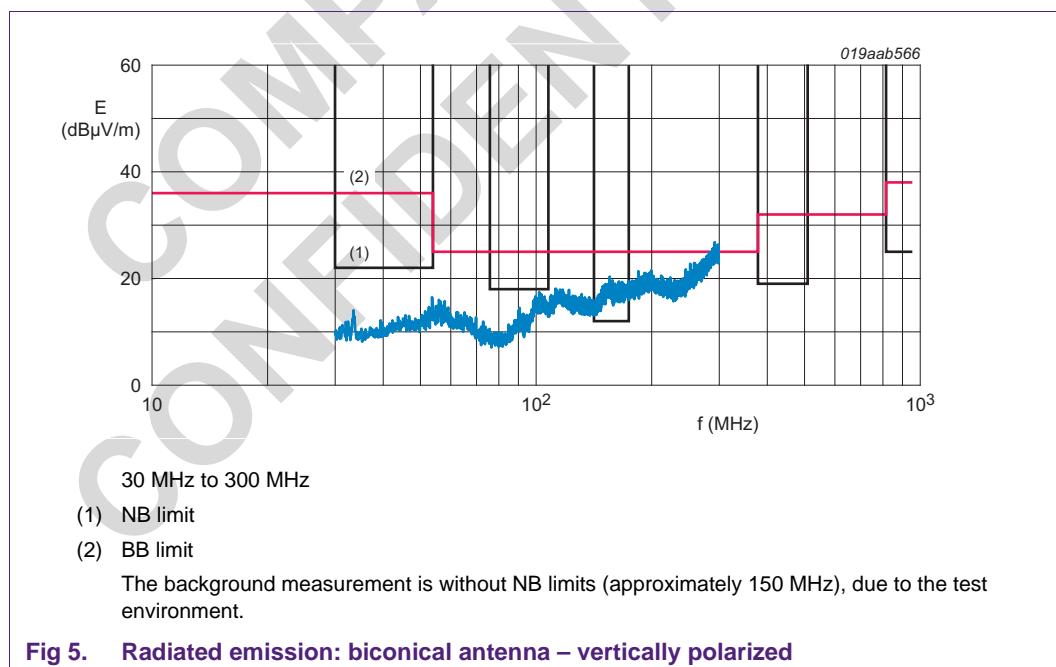
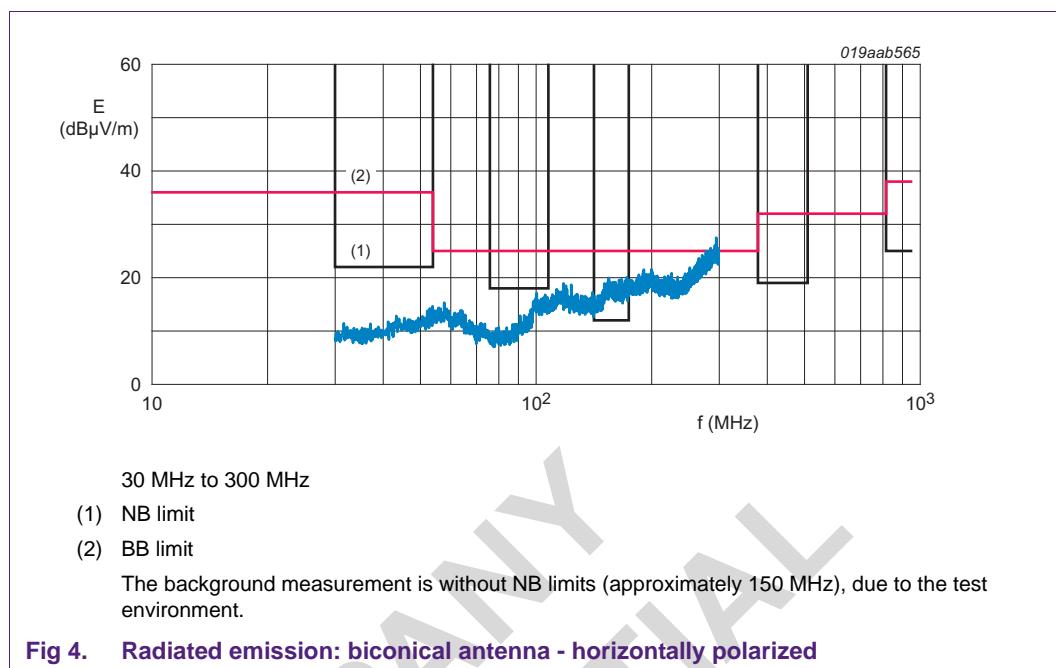
$P_o \sim \frac{1}{4} P_{rated} = 4 \times 6.2 \text{ W RMS}$  into  $4 \Omega$  resistor load, frequency = 1 kHz,  $V_P = 14 \text{ V}$

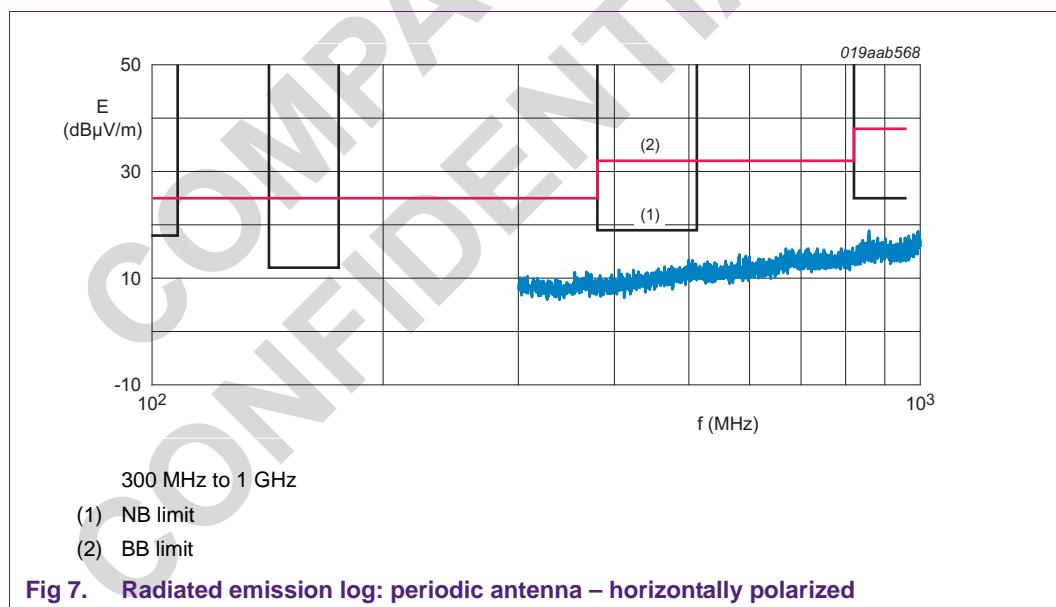
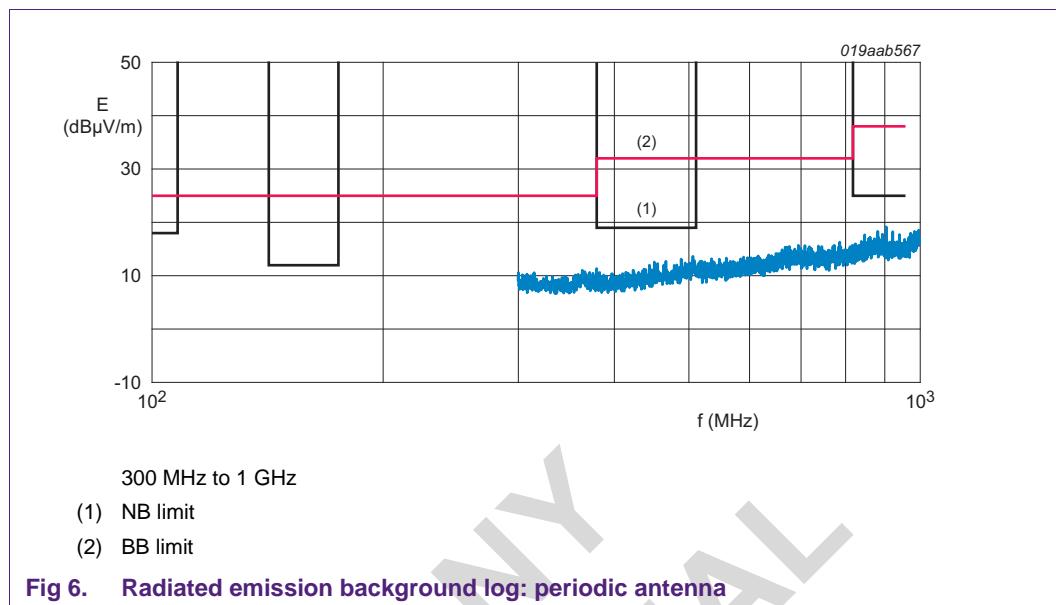
Conclusion:

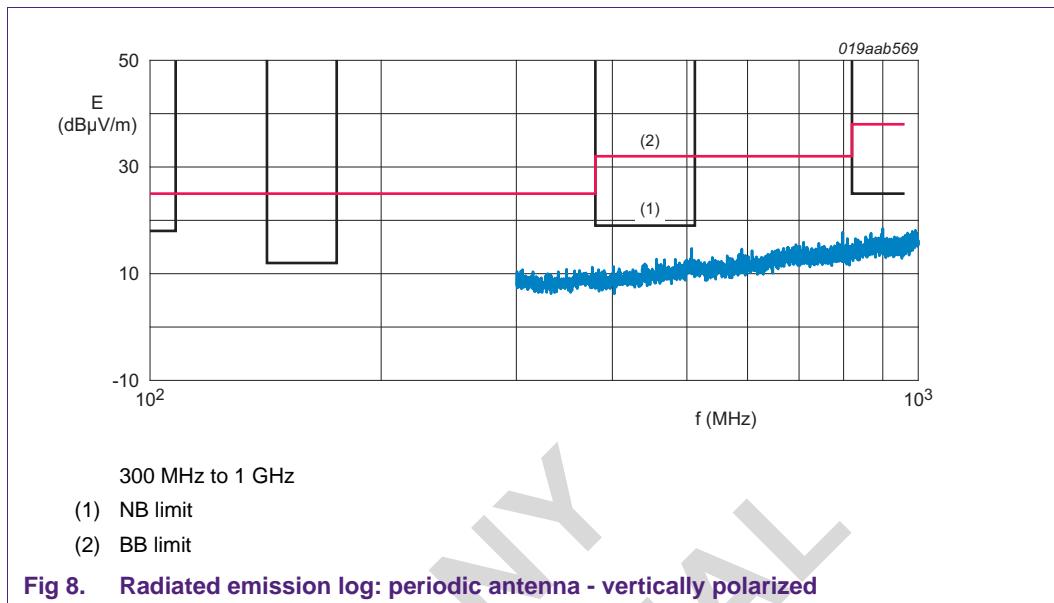
- All radiated EMI measurements are well within the CISPR25 level 5 limits











### 2.2.3.2 EMI immunity

EMI immunity is the sensitivity of the amplifier application against HF interference picked up from the environment. In this case, it is typically the GSM band (phone) or GPRS communication of a navigation device.

An investigation revealed that the influence of a cellular phone (GSM 900 MHz to 1800 MHz) could create disturbance if the PCB is not sufficiently shielded and exposed to the radiation. Similar results are obtained when using a radio which has (sensitive) external unshielded wires. In this case, radiation is picked up more easily resulting in small audible tones from the loudspeakers. The disturbance sounds like a buzzing sound that represents the typical burst frequency of 217 Hz, used in GSM/GPRS communication.

Take extra precautions to keep the disturbance levels acceptable.

Extensive testing revealed that using HF SMD ferrite beads, in series with the 4 inputs and the AC ground pin, suppresses the radiation. The suppression prevents the disturbance from entering the preamplifier stage. The ferrite beads have a very large impedance in the region between 900 MHz and 2 GHz and so block the HF radiation. Place the beads as close as possible to the IC pins (< 1 cm) to be most effective. See [Figure 9](#).

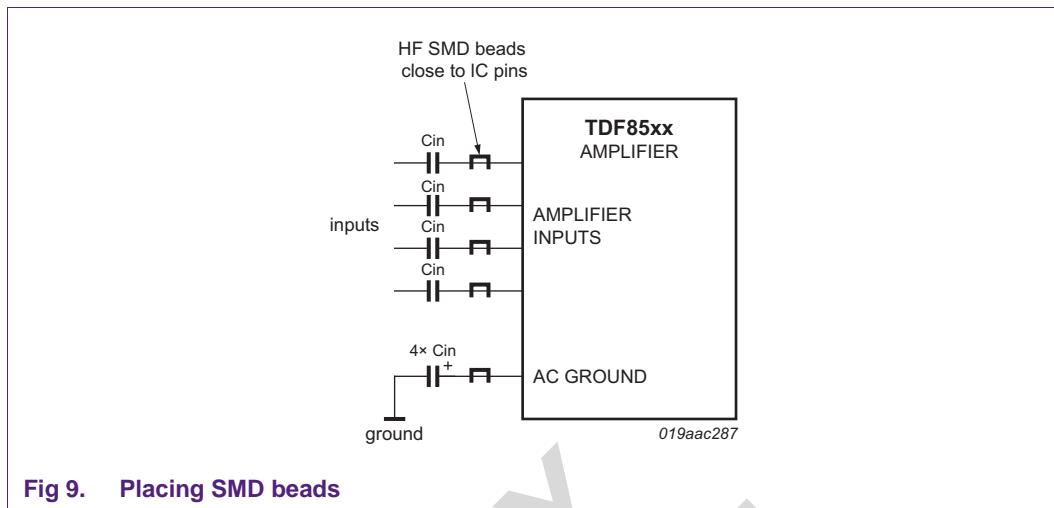


Fig 9. Placing SMD beads

The type of ferrite bead that gave very good results on the demo board is the BLM series of Murata: BLM11HB601SD. This bead is optimal for a frequency range around 1 GHz, where it has an impedance between 1 k $\Omega$  and 2 k $\Omega$  blocking the radiation properly. The measured noise and distortion results did not change when using these beads.

If blocking of even higher frequencies up to 2 GHz is needed, then the Murata BLM18GG471SN1 is the appropriate ferrite bead. The impedance graph is shown in [Figure 10](#).

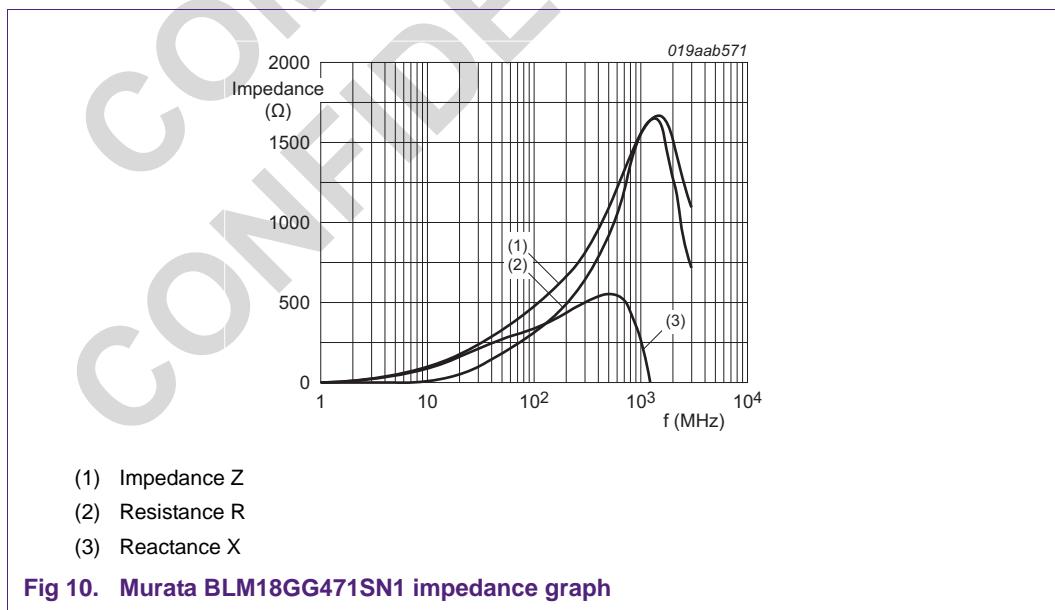


Fig 10. Murata BLM18GG471SN1 impedance graph

Although these types of ferrite beads are a good starting point for GSM/GPRS interference, the correct type for a certain application cannot be determined in advance. Some factors depend on the application itself; shielding, layout, ground planes, ground structure, connectors, cables, and so on. The correct type is determined during correct EMC testing.

With these ferrite beads placed on the demo board, listening tests have been carried out and no negative drawbacks were noticed.

Conclusion:

- The amplifier application can be optimized in such a way that there is no audible tone via a loudspeaker
- To achieve radiated immunity from very high frequencies (1 GHz to 2 GHz), thoroughly shield the application (radio/amplifier box). To prevent HF radiation entering the enclosure, ensure that there are no gaps/cracks.
- If the radio/amplifier box is not/or cannot be properly shielded, the HF radiation can be picked up at the inputs of the amplifier. This results in a weak audible tone via a connected loudspeaker. To prevent the weak tone, place small SMD ferrite beads in series with all the input pins and the AC ground pin. Place the beads as close as possible to the pins of the amplifier IC.

## 2.3 Beep circuit

When an external microcontroller is used to produce a beep, for instance for warnings in a car, use the circuit as depicted in [Figure 11](#). Note that the existing ACGND capacitor is still required.

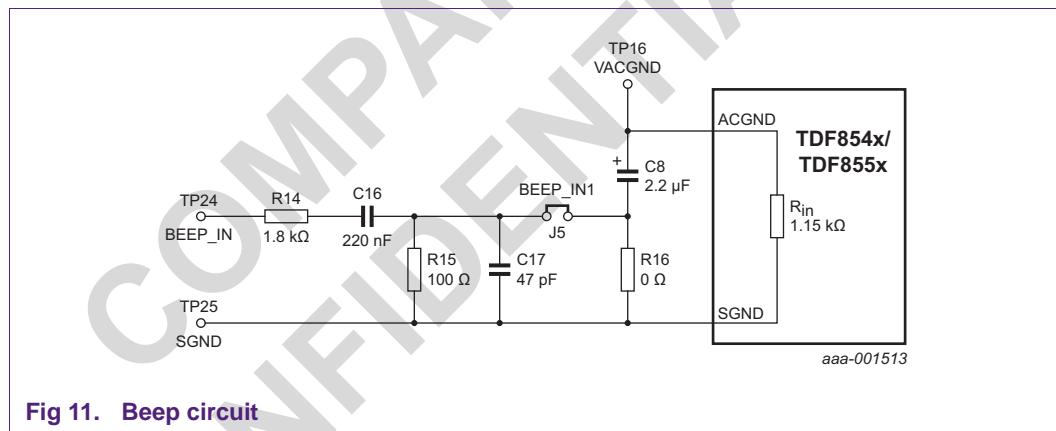


Fig 11. Beep circuit

This circuit feeds the signal directly into the common negative input of the amplifier, the ACGND pin. Although a band-pass-filter is implemented, ensure that the PCB trace, between the external circuit and the ACGND pin, is short. Limiting the length of the PCB trace, prevents it from acting as an antenna and picking up HF noise (noise is amplified directly to the amplifier outputs).

The circuit is designed to provide 1 V RMS on the output when 1 V RMS is applied to the input and the amplifier gain is set to 26 dB.

If other gains are needed, change the value of R14 and C16 in such a way that the band-pass filter characteristic remains the same, by keeping the same time constant of the RC combination. Higher resistor values decrease the output signal and vice versa.

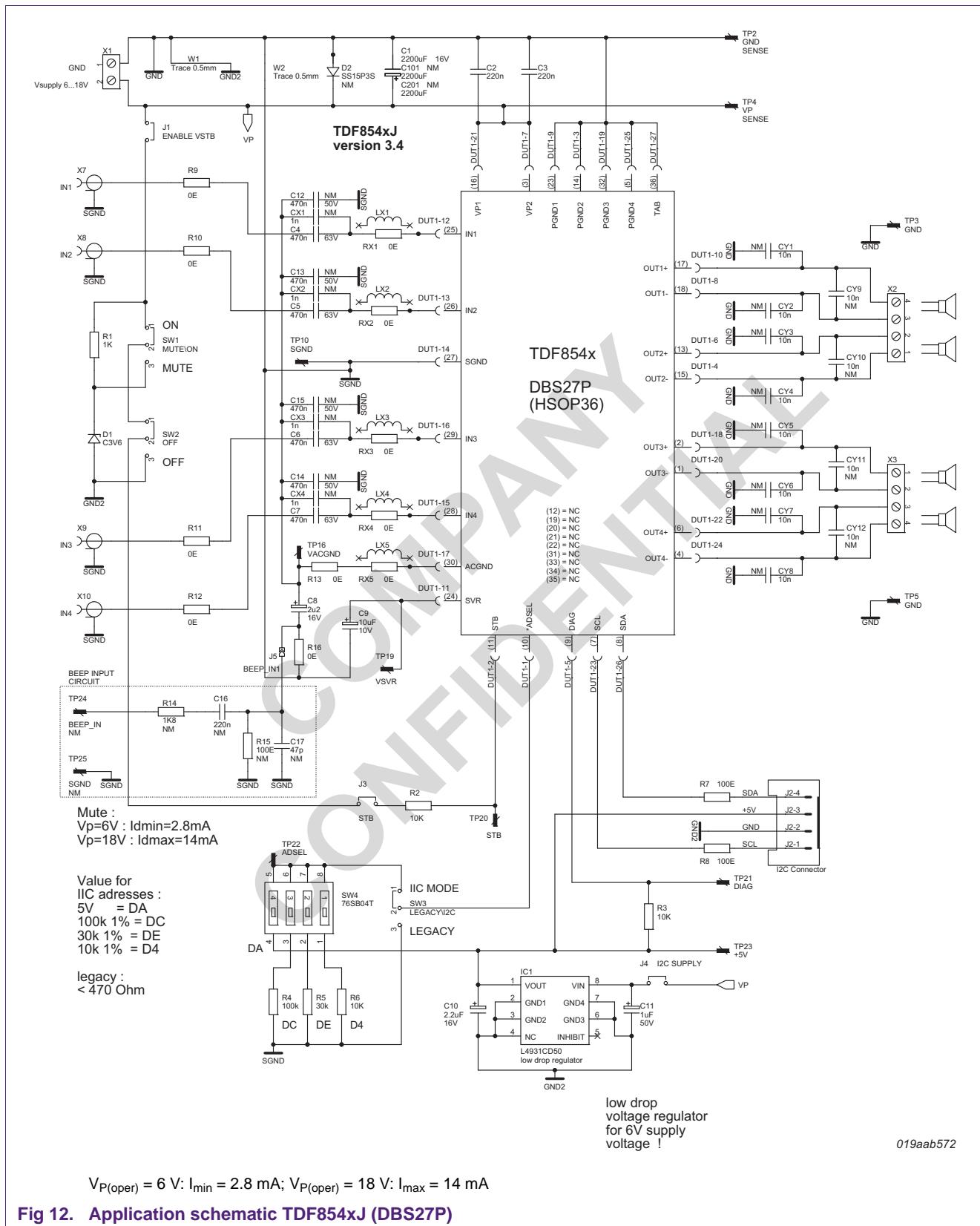
Although this circuit is coupled to the ACGND pin, it is still possible to use the mute functionality in the software.

## 2.4 Application TDF854xJ

### 2.4.1 Schematic application TDF854xJ

[Figure 12](#) is the schematic of the demo board for the DBS27 package. [Figure 15](#) is the schematic for the HSOP36 package (see also [Section 2.5.1](#)).

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### 2.4.2 Application board TDF854xJ BOM

**Table 2.** Components used in the standard application PCB for TDF854xJ

Component	Value	Manufacturer	Part number	Remarks
C1	2200 $\mu$ F/20 %/16 V	Rubycon	electrolytic capacitor, 16YXF2200MEFC12.5X25	supply buffer capacitor
C2, C3	220 nF/10 %/25 V	Kemet	C0805X224K3RACTU	HF decoupling capacitors
C4, C5, C6, C7	470 nF/5 %/63 V	Farnell	1166041 MKT 5 mm pitch	DC decoupling input capacitors
C8	2.2 $\mu$ F/20 %/16 V	Farnell	electrolytic capacitor, 9189297	AC ground capacitors
C9	10 $\mu$ F/50 V		electrolytic capacitor	SVR capacitor
C10	2.2 $\mu$ F/20 %/16 V	Sanyo	electrolytic capacitor, 16SH2.2M	5 V regulator capacitor
C11	1 $\mu$ F/50 V		electrolytic capacitor	
C12, C13, C14, C15	470 nF/5 %/63 V	Farnell	1166041 MKT 5 mm pitch	not mounted
C16	220 nF/10 %/25 V	Kemet	C0805X224K3RACTU	chime circuit capacitor
C17	47 pF/2 %/50 V	Philips	2222 861 74479	chime circuit capacitor
C18	1 $\mu$ F/20 %/50 V	Panasonic	electrolytic capacitor, 16SC3R3M	chime circuit capacitor
C101	2200 $\mu$ F/20 %/35 V	Vishay	electrolytic capacitor	alternative supply buffer capacitor, not mounted
C201	2200 $\mu$ F/20 %/63 V	Panasonic	electrolytic capacitor, ECOS1JA222BA	alternative supply buffer capacitor, not mounted
CX1, CX2, CX3, CX4	1 nF/2 %/50 V	Philips	2222 861 74102	optional input capacitors, not mounted
CY1, CY2, CY3, CY4, CY5, CY6, CY7, CY8, CY9, CY10, CY11, CY12	10 nF/5 %/50 V DC	Kemet	C0805C103J5GAC	optional output capacitors, not mounted
D1	BZX79-C3V6	Philips	9331 176 80113	for mute voltage
D2	SS15P3S	Vishay	SS15P3S-M3/87A	supply protection diode, not mounted
DUT1	socket SOT827-1	Loranger	04556271X217	socket for TDF854xJ
IC1	L4931CD50-TR	STMicroelectronics	SO-8, low drop 5 V regulator	low drop voltage regulator
J1, J3, J4	micro shunt, pitch 2.54 mm, long pin	Molex	90059-0009	Header 2pins off (8322-249-95381)
J2	I <sup>2</sup> C-connector	Stocko	header straight pins 4p	for I <sup>2</sup> C communication cable
J5	SMD jumper		SMD_solder short-open	connect chime circuit
LX1, LX2, LX3, LX4, LX5	SMD0603	Murata	ferrite SMD bead BLM18GG471SN1	improved HF immunity behavior
R1	1 k $\Omega$ /5 %/0.125 W	Yageo	RC0805JR-071KL	for Zener diode
R2	10 k $\Omega$ /5 %/0.125 W	Yageo	RC0805JR-0710KL	for STB pin
R3	10 k $\Omega$ /5 %/0.125 W	Yageo	RC0805JR-0710KL	for diagnostic pin

**Table 2.** Components used in the standard application PCB for TDF854xJ ...continued

Component	Value	Manufacturer	Part number	Remarks
R4	100 kΩ/5 %/0.125 W	Yageo	RC0805JR-0710KL	for I <sup>2</sup> C-address DC
R5	30 kΩ/5 %/0.125 W	Yageo	RC0805JR-0710KL	for I <sup>2</sup> C-address DE
R6	10 kΩ/1 %/0.1 W	Multicomp	MC 0.1 W 0805 1 % 10K	for I <sup>2</sup> C-address D4
R7, R8	100 Ω/5 %/0.125 W			for I <sup>2</sup> C lines
R9, R10, R11, R12, R13	0 Ω	Yageo	RC0805JR-070RL	optional input resistors
R14	1.8 kΩ/1 %/150 V/0.125 W	Yageo	RC0805FR-071K8L	chime circuit resistor
R15	100 E/1 %/0.1 W	Phycomp	2322 734 61001	chime circuit resistor
RX1, RX2, RX3, RX4, RX5	0 Ω	Vishay Dralonic	CRCW06030000Z0EA	optional input resistors beads
SW1, SW2, SW3	Secme PCB jumper switch 3p	EAO Electronics	09-03290-01	for mute on/off, legacy/I <sup>2</sup> C mode
SW4		Grayhill	76SB04T	for I <sup>2</sup> C-address switches
TP2, TP3, TP4, TP5, TP10, TP16, TP19, TP20, TP21, TP22, TP23, TP24, TP25	solder pin 1 mm	JST	RT-01T-1.0B(LF)	test points
X1, X2, X3	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/3-5.08	power connector and speaker connectors
X7, X8, X9, X10	black WBTOR-1	Lumberg	WBTOR 1 BLACK	input connectors

### 2.4.3 Application PCB lay-out TDF854xJ

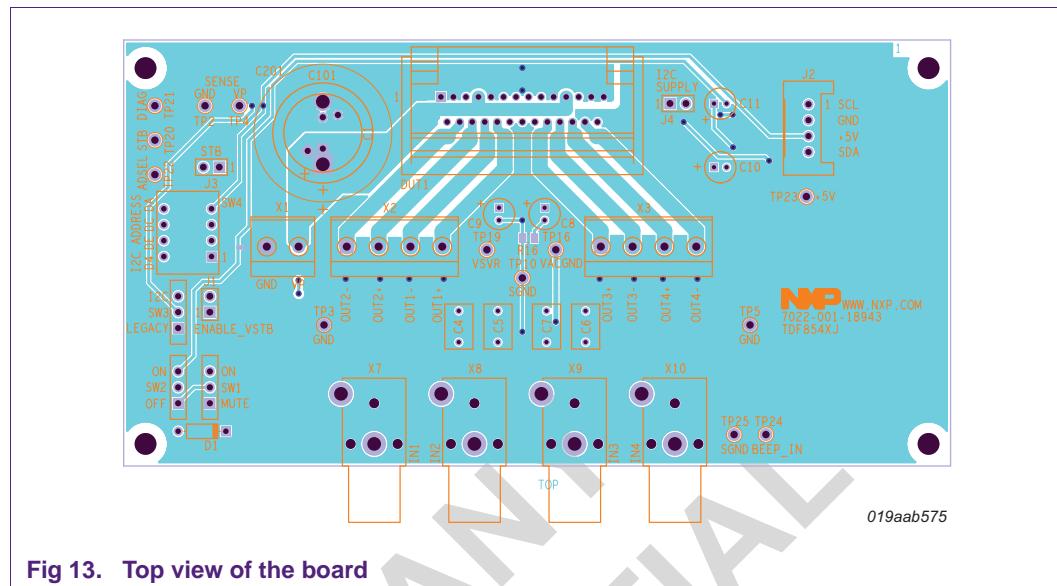


Fig 13. Top view of the board

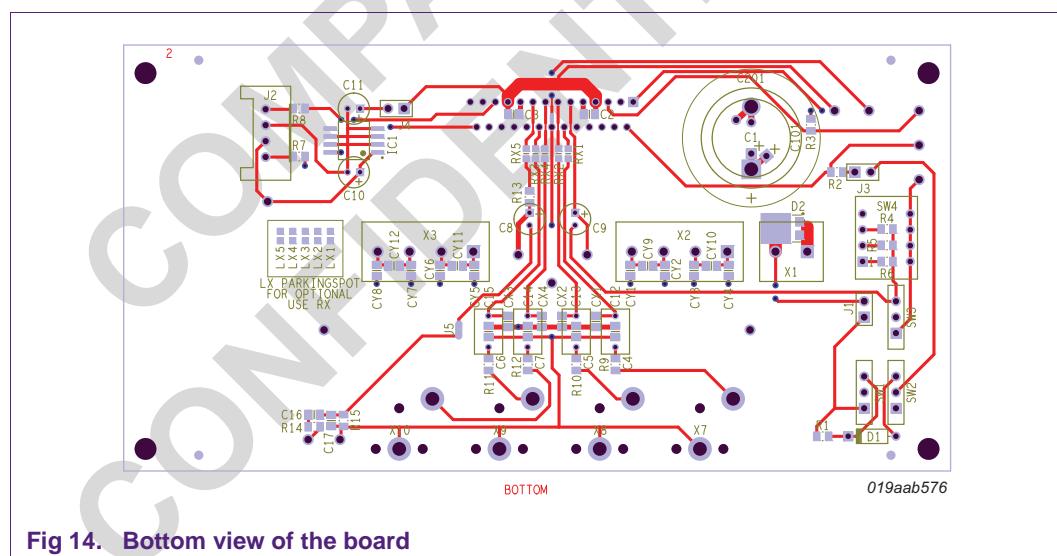
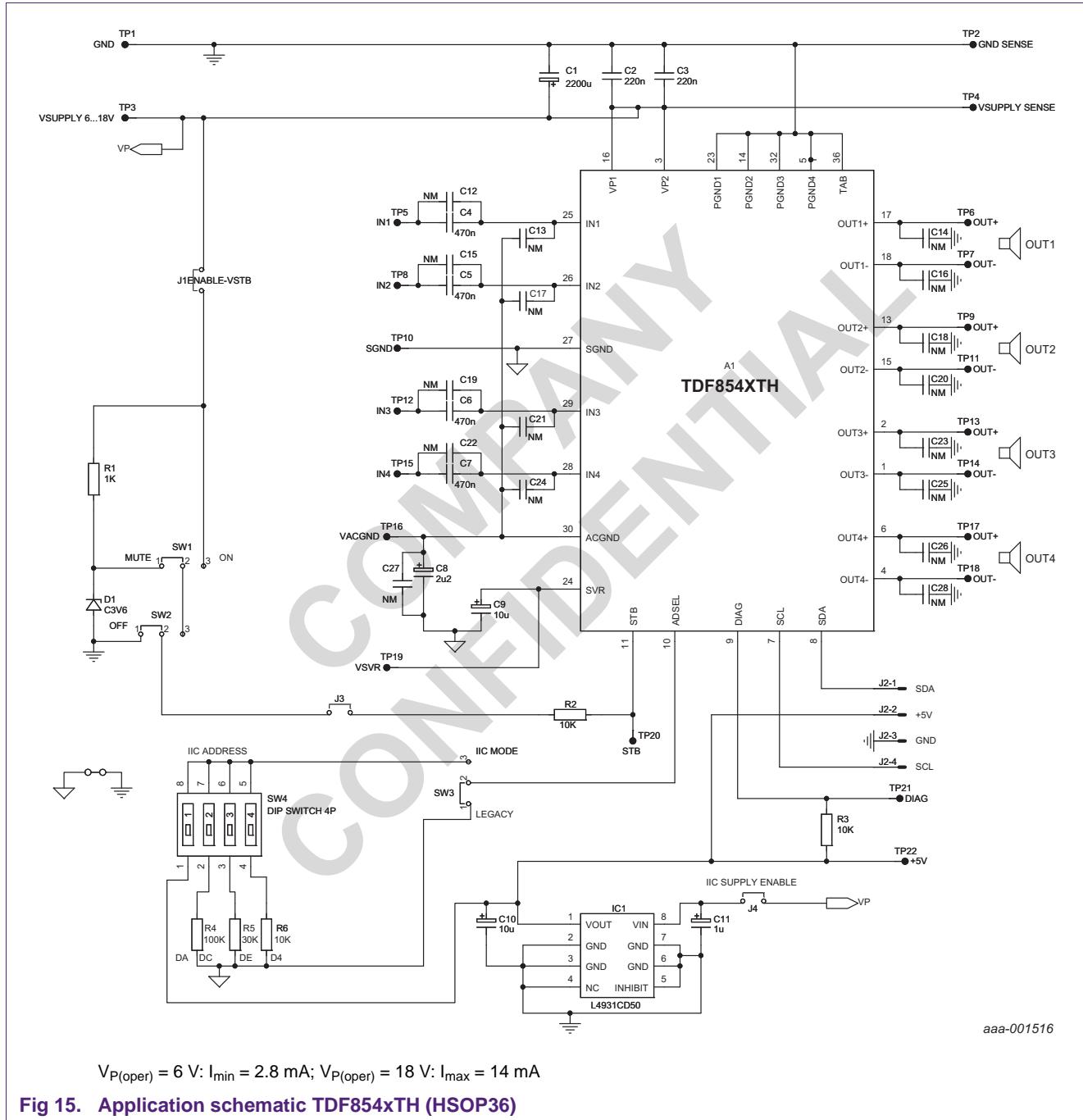


Fig 14. Bottom view of the board

## 2.5 Application TDF854xTH

### 2.5.1 Schematic application TDF854xTH

[Figure 15](#) is the schematic of the demo board for the HSOP36 package.



$$V_{P(\text{oper})} = 6 \text{ V}; I_{\text{min}} = 2.8 \text{ mA}; V_{P(\text{oper})} = 18 \text{ V}; I_{\text{max}} = 14 \text{ mA}$$

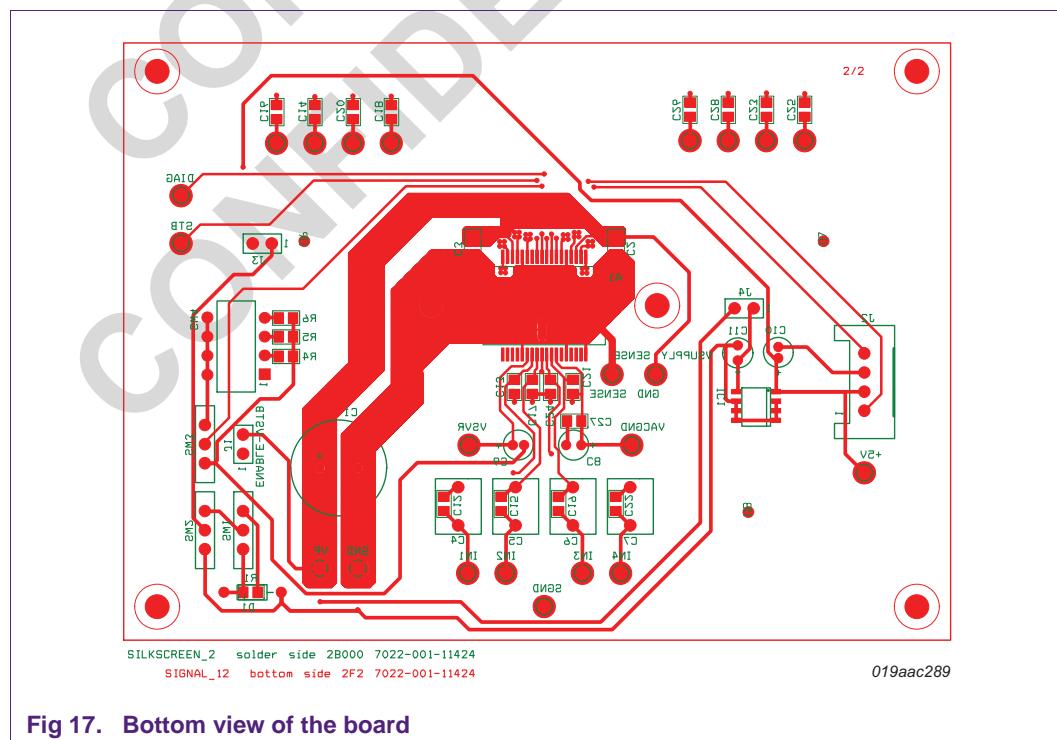
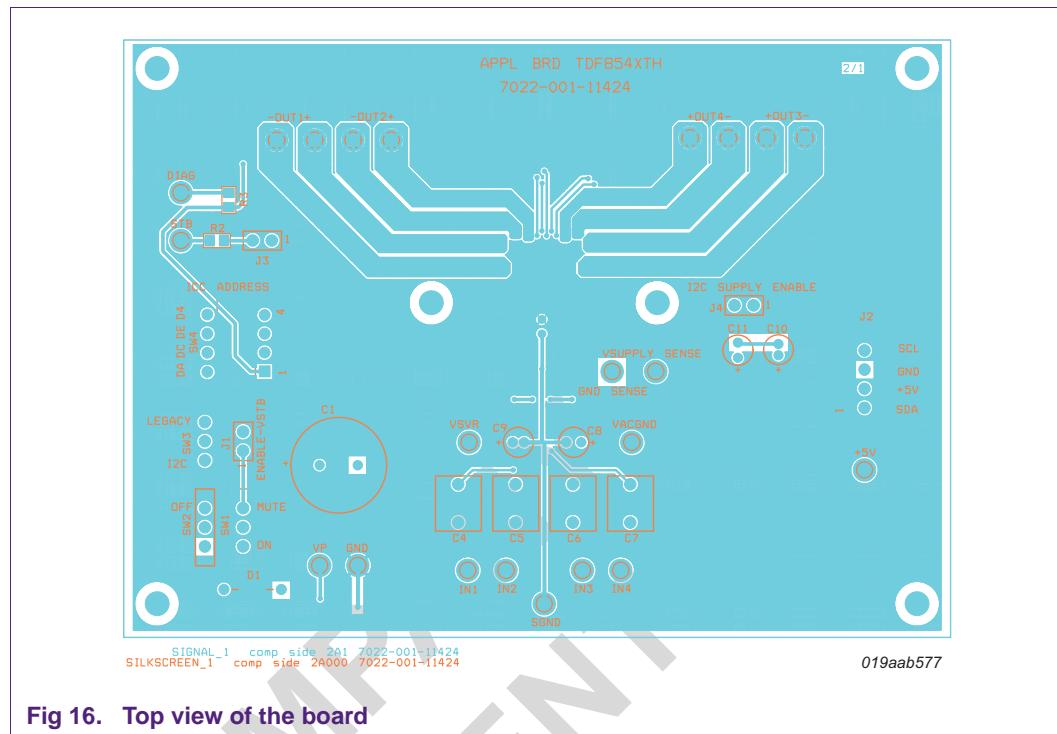
**Fig 15. Application schematic TDF854xTH (HSOP36)**

### 2.5.2 Application board TDF854xTH BOM

**Table 3.** Components used in the standard application PCB for TDF854xTH

Component	Value	Manufacturer	Part number	Remarks
C1	2200 $\mu$ F/20 %/16 V	BC components	2222 037 55222	supply buffer capacitor
C2, C3	220 nF/10 %/100 V DC	Kemet	C1206C224K1RAC	HF decoupling capacitors
C4, C5, C6, C7	470 nF/5 %/100 V	BC components	2222 470 86474	DC decoupling input capacitors
C8	2.2 $\mu$ F/20 %/16 V	Sanyo	16SC2R2M	AC ground capacitors
C9	10 $\mu$ F/20 %/25 V	Panasonic	EEAFC1E100	SVR capacitor
C10	10 $\mu$ F/20 %/25 V	Panasonic	EEAFC1E100	5 V regulator capacitor
C11	1 $\mu$ F/20 %/25 V	Sanyo	255C1M	
C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28	10 nF/10 %/50 V	Philips	2222 580 15636	optional input capacitors, not mounted
D1	BZX79-C3V6	Philips	9331 176 80113	for mute voltage
IC1	L4931CD50	STMicroelectronics		low drop voltage regulator
J1, J3, J4	micro shunt, pitch 2.54 mm, long pin	Molex	90059-0009	Header 2 pins off (8322-249-95381)
J2	I <sup>2</sup> C-connector	Stocko	header straight pins 4p	for I <sup>2</sup> C communication cable
R1	1 k $\Omega$ /1 %/0.1 W	Philips	2322 734 61002	for Zener diode
R2	10 k $\Omega$ /1 %/0.1 W	Philips	2322 734 61003	for STB pin
R3	10 k $\Omega$ /1 %/0.1 W	Philips	2322 734 61003	for diagnostic pin
R4	100 k $\Omega$ /5 %/0.125 $\Omega$			for I <sup>2</sup> C-address DC
R5	30 k $\Omega$ /5 %/0.125 $\Omega$			for I <sup>2</sup> C-address DE
R6	10 k $\Omega$ /1 %/0.1 W	Multicomp	MC 0.1 W 0805 1 % 10K	for I <sup>2</sup> C-address D4
SW1, SW2, SW3	Secme PCB jumper switch 3p	EAO Electronics	09-03290-01	for mute on/off, legacy/I <sup>2</sup> C mode
SW4	DIP switch 4p	Grayhill	76SB04T	for I <sup>2</sup> C-address switches
TP2, TP3, TP4, TP5, TP10, TP16, TP19, TP20, TP21, TP22	solder pin 1.5 mm	JST	RT-01T-1.0B(LF)	test points

### 2.5.3 Application PCB lay-out TDF854xTH



## 2.6 Application TDF8554/56J (with 5 regulators)

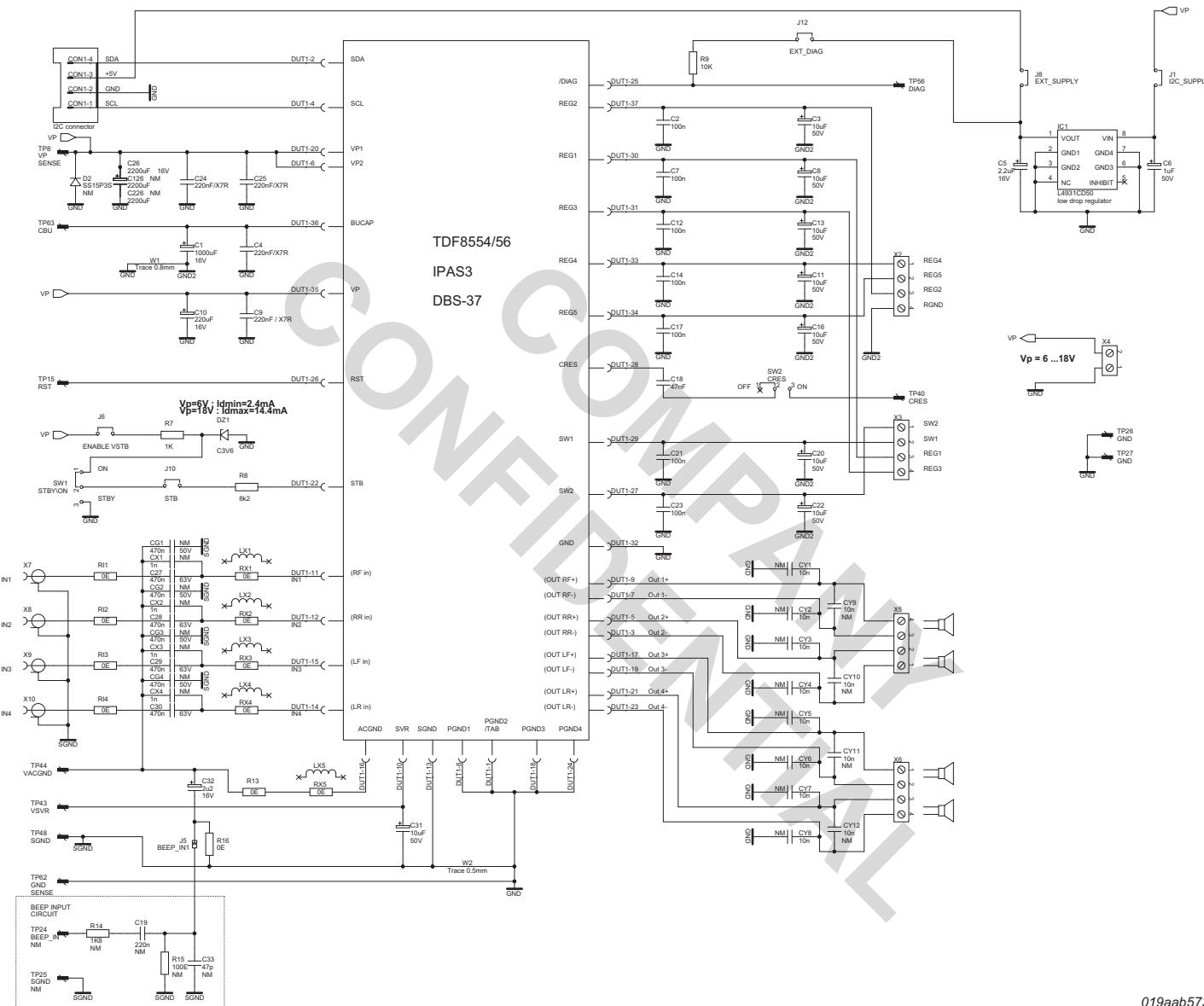
### 2.6.1 Application schematic TDF8554/56J (with 5 regulators)

To improve stability when a regulator is not used, ensure that the pin is not floating and that the regulator contains the same capacitor as the regulators that are in use.

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## TDF854x and TDF855x automotive amplifiers

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$$V_{P(\text{oper})} = 6 \text{ V}: I_{\text{min}} = 2.4 \text{ mA}; V_{P(\text{oper})} = 18 \text{ V}: I_{\text{max}} = 14.4 \text{ mA}$$

Fig 18. Application schematic with 5 regulators TDF8554/56J DBS37

## 2.6.2 Application TDF8554/56J (with 5 regulators) BOM

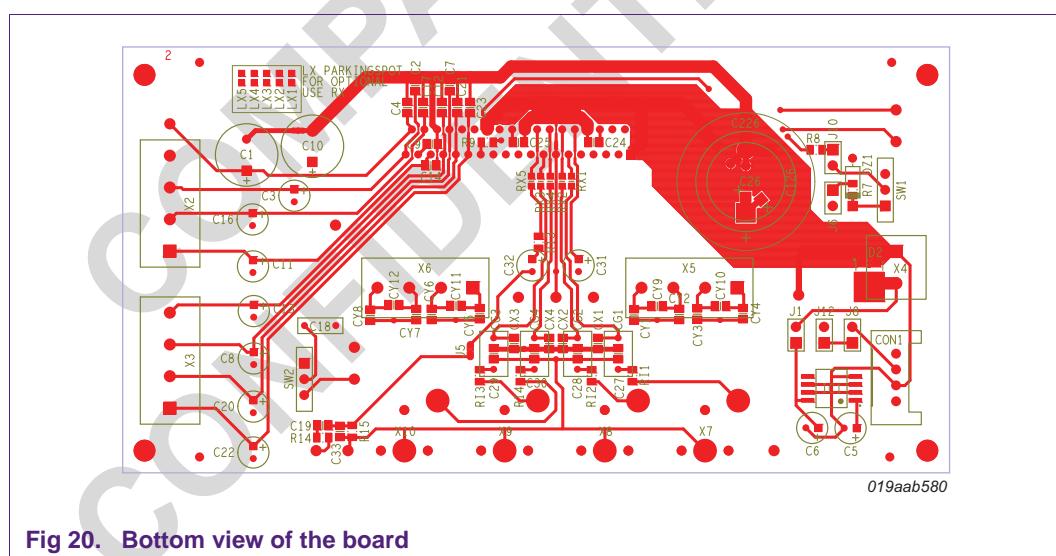
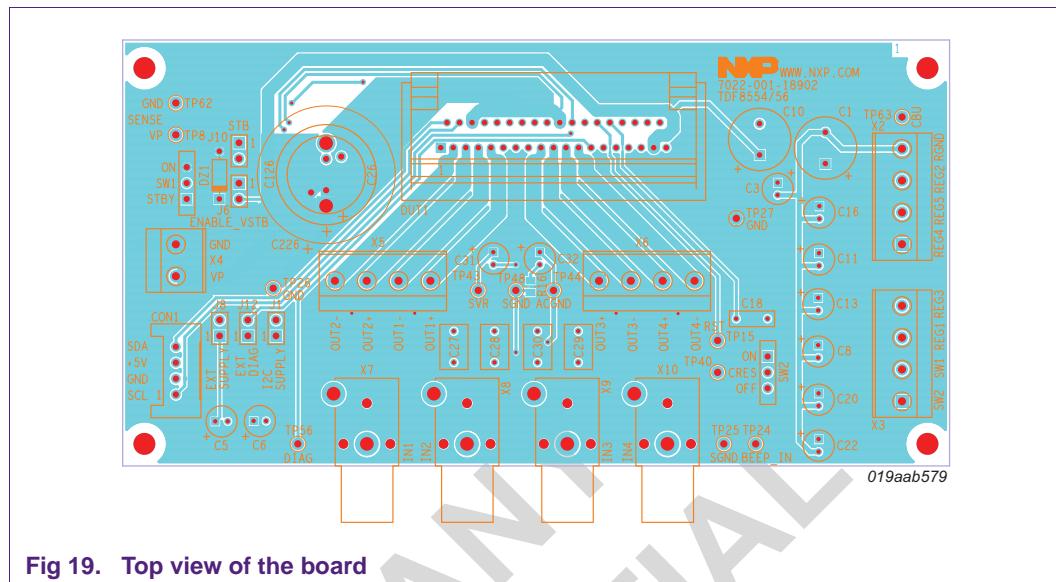
**Table 4.** Components used in the standard application PCB for TDF8554/56J

Component	Value	Manufacturer	Part number	Remarks
C1	1000 $\mu$ F/16 V		electrolytic capacitor, 16YXF2200MEFC12.5X25	back-up capacitor for regulators
C2, C7, C12, C14, C17, C21, C23	100 nF/10 %/50 V	Yageo	CC0805KRX7R9BB104	HF decoupling capacitors
C3, C8, C11, C13, C16, C20, C22	10 $\mu$ F/50 V		electrolytic capacitor	buffer/decoupling capacitors for regulators
C4, C9, C24, C25	220 nF/50 V	Yageo	CC0805KRX7R9BB104	HF decoupling capacitors
C5	2.2 $\mu$ F/20 %/16 V	Sanyo	electrolytic capacitor, 16SC2.2M	buffer/decoupling capacitors for regulators
C6	1 $\mu$ F/50 V		electrolytic capacitor	decoupling capacitor for regulator
C10	220 $\mu$ F/16 V			supply buffer capacitor
C18	47 nF			
C19	220 nF/10 %/25 V	Kemet	C0805X224K3RACTU	chime circuit capacitor
C26	2200 $\mu$ F/20 %/16 V	Rubycon	16YXF2200MEFC12.5X25	supply buffer capacitor
C27, C28, C29, C30	470 nF/5 %/63 V	Farnell	1166041, MKT 5 mm pitch	DC decoupling capacitors
C31	10 $\mu$ F/50 V		electrolytic capacitor	SVR capacitor
C32	2.2 $\mu$ F/20 %/16 V	Farnell	electrolytic capacitor, 9189297	AC ground capacitors
C33	47 pF/2 %/50 V	Philips	2222 861 74479	chime circuit capacitor
C34	1 $\mu$ F/20 %/50 V	Panasonic	EEEHB1H1R0R	chime circuit capacitor
C126	2200 $\mu$ F/20 %/35 V	Vishay	MAL213660222E3	alternative supply buffer capacitor, not mounted
C226	2200 $\mu$ F/20 %/63 V	Panasonic	electrolytic capacitor, ECOS1JA222BA	alternative supply buffer capacitor, not mounted
CG1, CG2, CG3, CG4	470 nF/5 %/63 V	Farnell	1166041, MKT 5 mm pitch	optional input capacitors, not mounted
CON1	header straight pins 4p	Stocko	MKS3734.1.0404	for I <sup>2</sup> C communication cable
CX1, CX2, CX3, C4	1 nF/2 %/50 V	Philips	2222 861 74102	optional input capacitors, not mounted
CY1, CY2, CY3, CY4, CY5, CY6, CY7, CY8, CY9, CY10, CY11, CY12	10 nF/5 %/50 V DC	Kemet	C0805C103J5GAC	optional output capacitors, not mounted
D2	SS15P3S	Vishay	SS15P3S-M3/87A	supply protection diode, not mounted
DUT1	socket SOT827-1	Loranger	04556271X217	socket for TDF8554/56

**Table 4.** Components used in the standard application PCB for TDF8554/56J

Component	Value	Manufacturer	Part number	Remarks
DZ1	BZX79-C3V6	Philips	9331 176 80113	Zener diode for ON voltage
IC1	L4931CD50-TR	STMicroelectronics	SO-8, low drop 5 V regulator	low drop voltage regulator
J1, J6, J8, J10, J12	micro shunt, pitch 2.54 mm, long pin	Molex	90059-0009	Header 2pins off (8322-249-95381) Header Breakaway 36p
J5	SMD jumper		SMD_solder short-open	connect chime circuit
LX1, LX2, LX3, LX4, LX5	SMD0603	Murata	ferrite SMD bead BLM18GG471SN1	improved HF immunity behavior
R7	1 kΩ/5 %/0.125 W	Yageo	RC0805JR-071KL	for Zener diode
R8	8.2 kΩ/5 %/0.125 W	Yageo	RC0805JR-0710KL	for STB pin
R9	10 kΩ/5 %/0.125 Ω	Yageo	RC0805JR-0710KL	for diagnostic pin
R13	0 Ω	Yageo	RC0805JR-070RL	optional ACGND input resistor
R14	1.8 kΩ/1 %/150 V/0.125 W	Yageo	RC0805FR-071K8L	chime circuit resistor
R15	100 E/1 %/0.1 W	Phycomp	2322 734 61001	chime circuit resistor
RI1, RI2, RI3, RI4	0 Ω	Yageo	RC0805JR-070RL	optional signal input resistor
RX1, RX2, RX3, RX4, RX5	0 Ω	Vishay Dralonic	CRCW06030000Z0EA	optional input resistors beads
SW1	Secme PCB jumper switch 3p	EAO Electronics	09-03290-01	for standby/on switch
SW2	Secme PCB jumper switch 3p	EAO Electronics	09-03290-01	for cres switch
TP8, TP15, TP24, TP25, TP26, TP27, TP40, TP43, TP44, TP48, TP56, TP62, TP63	solder pin 1 mm	JST	RT-01T-1.0B(LF)	test points
X2	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/4-5.08	regulator connector
X3	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/4-5.08	regulator and switch connector
X4	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/3-5.08	power connector
X5, X6	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/4-5.08	speaker connector
X7, X8, X9, X10	phone connector black WBTOR-1	Lumberg	WBTOR 1 BLACK	input connectors

### 2.6.3 Application PCB lay-out TDF8554/56J BOM



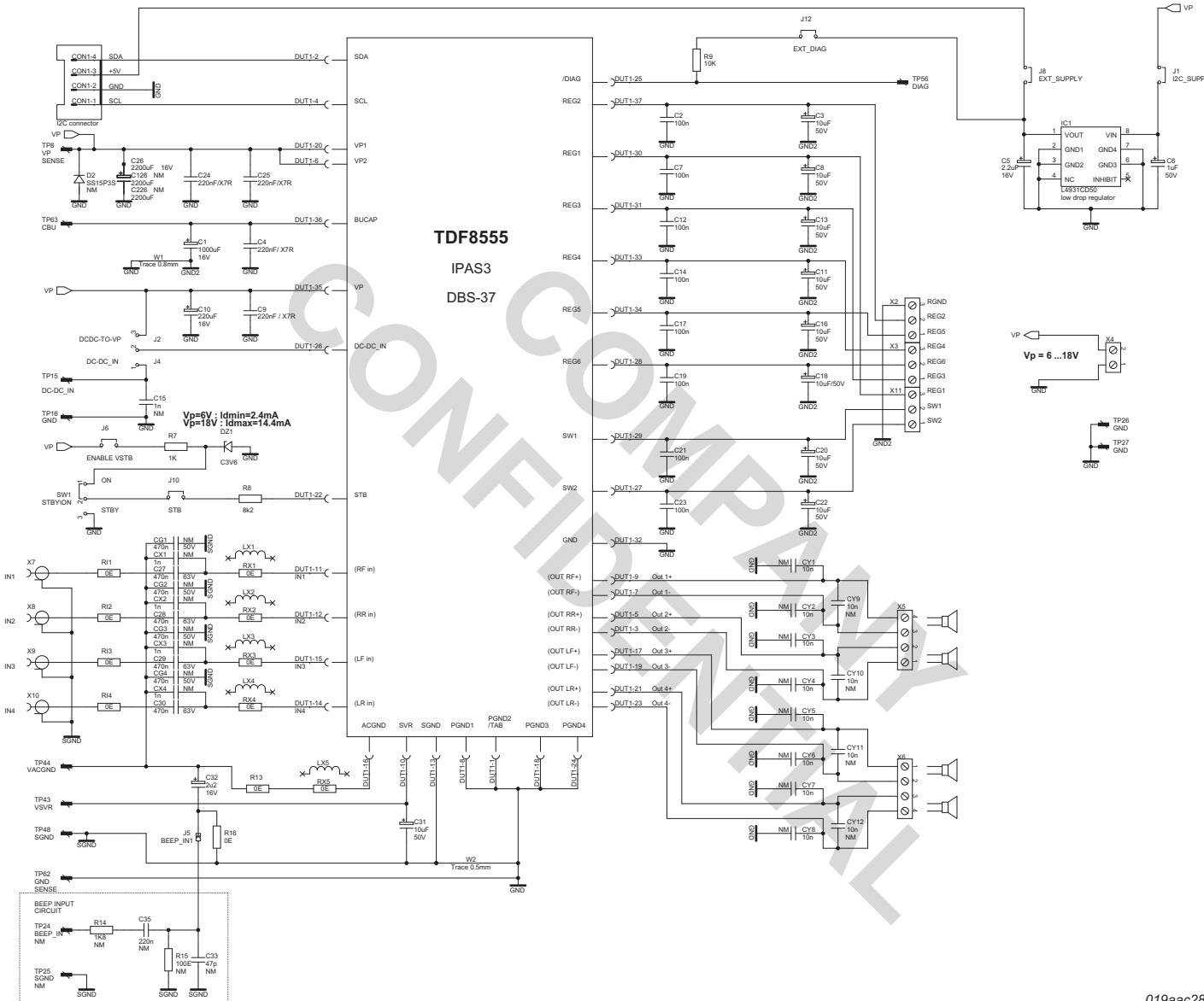
## 2.7 Application TDF8555J (with 6 regulators)

### 2.7.1 Application schematic TDF8555J (with 6 regulators)

To improve stability when a regulator is not used, ensure that the pin is not floating and that the regulator contains the same capacitor as the regulators that are in use.

## TDF854x and TDF855x automotive amplifiers

019aac288



$$V_{P(\text{oper})} = 6 \text{ V}: I_{\text{min}} = 2.4 \text{ mA}; V_{P(\text{oper})} = 18 \text{ V}: I_{\text{max}} = 14.4 \text{ mA}$$

**Fig 21. Application schematic with 6 regulators TDF8555J DBS37**

### 2.7.2 Application TDF8555J (with 6 regulators) BOM

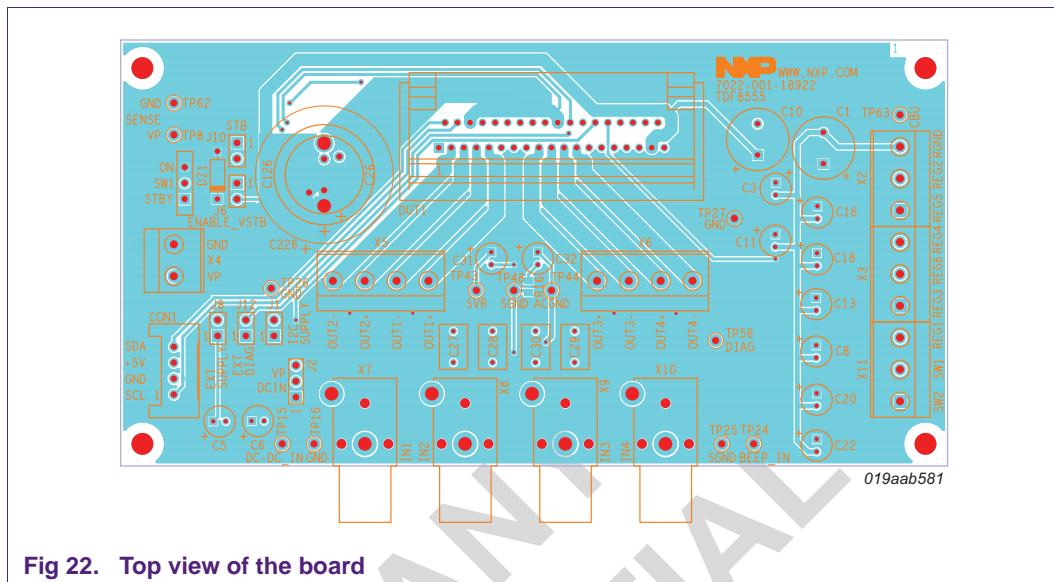
**Table 5.** Components used in the standard application PCB for TDF8555J

Component	Value	Manufacturer	Part number	Remarks
C1	1000 $\mu$ F/16 V			back-up capacitor for regulators
C2, C7, C12, C14, C17, C21, C23	100 nF/10 %/50 V	Yageo	CC0805KRX7R9BB104	HF decoupling capacitors
C3, C8, C11, C13, C16, C20, C22	10 $\mu$ F/50 V		electrolytic capacitor	buffer/decoupling capacitors for regulators
C4, C9, C24, C25	220 nF/50 V	Yageo	CC0805KRX7R9BB104	HF decoupling capacitors
C5	2.2 $\mu$ F/20 %/16 V	Sanyo	electrolytic capacitor, 16SC2.2M	buffer/decoupling capacitors for regulators
C6	1 $\mu$ F/50 V		electrolytic capacitor	decoupling capacitor for regulator
C10	220 $\mu$ F/16 V			supply buffer capacitor
C15	1 nF/2 %/50 V	Philips	2222 861 74102	DC-DC capacitor, not mounted
C26	2200 $\mu$ F/20 %/16 V	Rubycon	16YXF2200MEFC12.5X 25	supply buffer capacitor
C27, C28, C29, C30	470 nF/5 %/63 V	Farnell	1166041, MKT 5 mm pitch	DC decoupling capacitors
C31	10 $\mu$ F/50 V		electrolytic capacitor	SVR capacitor
C32	2.2 $\mu$ F/20 %/16 V	Farnell	electrolytic capacitor, 9189297	AC ground capacitors
C33	47 pF/2 %/50 V	Philips	2222 861 74479	chime circuit capacitor
C34	1 $\mu$ F/20 %/50 V	Panasonic	EEEHB1H1R0R	chime circuit capacitor
C35	220 nF/10 %/25 V	Kemet	C0805X224K3RACTU	chime circuit capacitor
C126	2200 $\mu$ F/20 %/35 V	Vishay	MAL213660222E3	alternative supply buffer capacitor, not mounted
C226	2200 $\mu$ F/20 %/63 V	Panasonic	electrolytic capacitor, ECOS1JA222BA	alternative supply buffer capacitor, not mounted
CG1, CG2, CG3, CG4	470 nF/5 %/63 V	Farnell	MKT, 5 mm pitch 1166041	optional input capacitors, not mounted
CON1	header straight pins 4p	Stocko	MKS3734.1.0404	for I <sup>2</sup> C communication cable
CX1, CX2, CX3, C4	1 nF/2 %/50 V	Philips	2222 861 74102	optional input capacitors, not mounted
CY1, CY2, CY3, CY4, CY5, CY6, CY7, CY8, CY9, CY10, CY11, CY12	10 nF/5 %/50 V DC	Kemet	C0805C103J5GAC	optional output capacitors, not mounted
D2	SS15P3S	Vishay	SS15P3S-M3/87A	supply protection diode, not mounted
DUT1	socket SOT827-1	Loranger	04556271X217	socket for TDF8554/56
DZ1	BZX79-C3V6	Philips	9331 176 80113	Zener diode for ON voltage

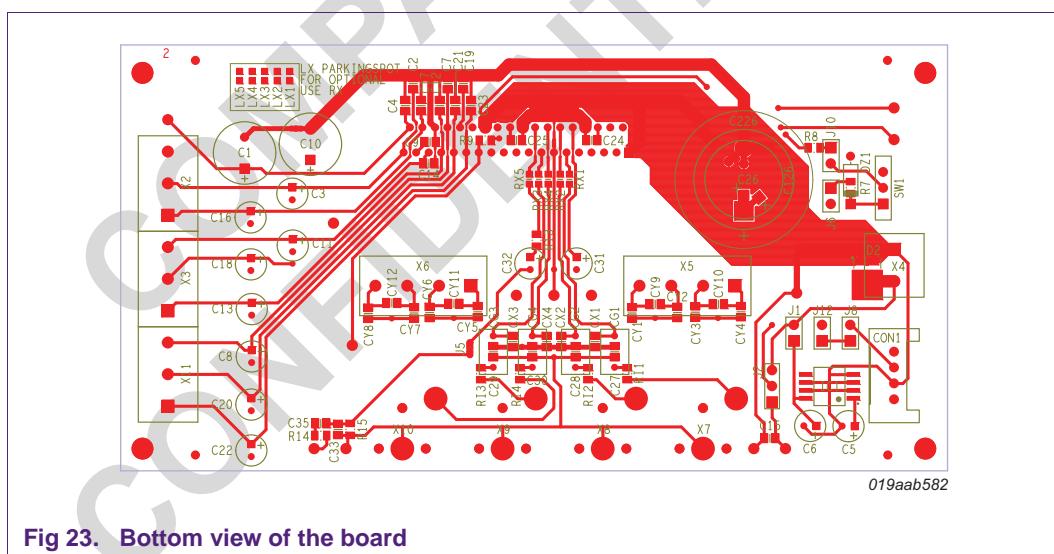
**Table 5.** Components used in the standard application PCB for TDF8555J ...continued

Component	Value	Manufacturer	Part number	Remarks
IC1	L4931CD50-TR	STMicroelectronics	SO-8, low drop 5 V regulator	low drop voltage regulator
J5	SMD jumper		SMD_solder short-open	connect chime circuit
LX1, LX2, LX3, LX4, LX5	SMD0603	Murata	ferrite SMD bead BLM18GG471SN1D	improved HF immunity behavior
R7	1 kΩ/5 %/0.125 W	Yageo	RC0805JR-071KL	for Zener diode
R8	8.2 kΩ/5 %/0.125 W	Yageo	RC0805JR-0710KL	for STB pin
R9	10 kΩ/5 %/0.125 Ω	Yageo	RC0805JR-0710KL	for diagnostic pin
R13	0 Ω	Yageo	RC0805JR-070RL	optional ACGND input resistor
R14	1.8 kΩ/1 %/150 V/0.125 W	Yageo	RC0805FR-071K8L	chime circuit resistor
R15	100 Ω/1 %/0.1 W	Phycomp	2322 734 61001	chime circuit resistor
RI1, RI2, RI3, RI4	0 Ω	Yageo	RC0805JR-070RL	optional signal input resistor
RX1, RX2, RX3, RX4, RX5	0 Ω	Vishay Dralonic	CRCW06030000Z0EA	optional input resistors beads
SW1	Secme PCB jumper switch 3p	EAO Electronics	09-03290-01	for standby/on switch
SW2	Secme PCB jumper switch 3p	EAO Electronics	09-03290-01	for cres switch
TP8, TP15, TP24, TP25, TP26, TP27, TP40, TP43, TP44, TP48, TP56, TP62, TP63	solder pin 1 mm	JST	RT-01T-1.0B(LF)	test points
X2	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/4-5.08	regulator connector
X3	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/4-5.08	regulator and switch connector
X4	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/3-5.08	power connector
X5, X6	PCB mounted screw terminal	Phoenix Contact	MKDSN2,5/4-5.08	speaker connector
X7, X8, X9, X10	phone connector black WBTOR-1	Lumberg	WBTOR 1 BLACK	input connectors

### 2.7.3 Application lay-out for TDF8555J



**Fig 22.** Top view of the board



**Fig 23. Bottom view of the board**

## 2.8 Component choices amplifier part

### 2.8.1 Input capacitors

The values of the input capacitors determine the low frequency roll-off point of the amplifier. With a typical input impedance of  $70\text{ k}\Omega$ , the 1st-order low frequency roll-off point equals approximately 5 Hz ( $-3\text{ dB}$  point). This low frequency roll-off point is sufficient for the audio band. Input capacitors must have a low DC leakage current to avoid DC offset on the outputs.

The input capacitors can change the sound quality of an amplifier. Film capacitors give a very good quality. Ceramic capacitors (NPO/X7R) are also a suitable choice for good sound quality.

### 2.8.2 SVR capacitor

The SVR pin is used to provide a reference voltage for the input biasing set to  $0.23 \times \text{battery voltage} + 2 \times \text{diode voltage } V_{be}$ . It is also used as a reference to generate the filtered half supply voltage at the output. The capacitor on pin SVR provides a better supply voltage ripple rejection and channel separation between the four channels. It also determines the amplifier start-up time. A higher capacitor value, results in a longer start-up time. 10  $\mu\text{F}$  is recommended, which results in a start-up time of approximately 0.6 s (start-up diagnostics disabled).

If a faster start-up time is needed, decrease the SVR capacitor value to 4.7  $\mu\text{F}$ . The SVRR remains almost the same with the exception that for lower frequencies ( $< 100\text{ Hz}$ ) it becomes a little worse. A lower SVR capacitor value causes an increased start-up pop.

### 2.8.3 AC ground capacitor

The AC ground capacitor is connected to the internal (common) AC ground of the four input stages. During amplifier start-up, the input circuit charges the input capacitors and the AC ground capacitor. To get the smallest pop during start-up, choose the same time-constant ( $T$ ) that is seen from the AC ground pin to signal ground. This time-constant should be the same as seen from each input pin to signal ground. The internal resistance observed at the AC ground is a quarter of the internal resistance of the inputs. Consequently, the capacitance at the AC ground pin should be four times the capacitance of the inputs.

If no resistors are used for the inputs or AC ground pin, the value for the AC ground capacitor must be four times the input capacitor. The increase in value is to get the lowest amount of unmuted pop at the outputs during start-up.

For example: if the input capacitor = 470 nF, the AC ground capacitor =  $4 \times 470\text{ nF}$ , which results in a practical value of 2.2  $\mu\text{F}$ .

### 2.8.4 Supply decoupling capacitor

The value of the supply decoupling capacitor is approximately 2200  $\mu\text{F}$ . If a long track/wire exists between the amplifier (box) and the battery, it may be necessary to increase the value.

The voltage rating of the capacitor is normally 16 V because of the typical voltage-clamp function of an electrolytic capacitor. The voltage clamp function provides the amplifier with extra protection against high-voltage spikes, for example load dump.

Low ESR capacitors are not needed. However, they can improve sound quality during dynamic music or low frequencies.

#### 2.8.5 Diagnostic pin

In order to detect a failure in the amplifier/regulator, a pull-up resistor can be connected between pin DIAG and a voltage. Pin DIAG is an open drain. When a failure occurs, the voltage on this pin is pulled LOW.

#### 2.8.6 STB pin

The STB pin has 2 functions; the first function is to switch the amplifier on/off or to mute (in legacy mode). The second function is to read clipping output signals (determined by I<sup>2</sup>C-bus), by using a series resistor on this pin.

#### 2.8.7 ADSEL pin

The resistance between pin ADSEL and the signal ground, determines the I<sup>2</sup>C-address of the amplifier. Four hexadecimal addresses can be chosen: DAh, DCh, DEh, D4h. When pin ADSEL is connected to signal ground (or resistance < 470 Ω, typical) the amplifier automatically operates in Legacy mode (see [Table 8](#)).

#### 2.8.8 TAB pin

Pin TAB is internally connected to the metal underside of the amplifier and to the power ground in the application.

## 2.9 Component choices regulator part

### 2.9.1 Capacitors on voltage regulator outputs and switches

To operate correctly, all switches and linear voltage regulators need a small, low ESR, buffer capacitor of 10 µF and an HF decoupling capacitor of 100 nF. It is preferential to position the capacitors close to the IC pins.

### 2.9.2 Supply buffer capacitor

The voltage regulator part has a separate supply connection pin. When it is connected to the same supply as the amplifier part (battery), a capacitor of approximately 220 µF is used. An extra 220 nF HF-decoupling capacitor is used in parallel.

When it is connected to an external DC-DC converter for higher efficiency, only a small HF decoupling capacitor is needed. The DC-DC supply is regulated and has its own buffer capacitor.

### 2.9.3 Backup capacitor

A buffer capacitor can be connected to pin BUCAP to help prevent voltage reductions at the output of regulator 2 during brief interruptions of the supply voltage. When the supply voltage is present at pin  $V_P$ , the capacitor charges to  $V_P - 0.3$  V and is used to supply regulator 2 during brief interruptions of the supply voltage.

The delay time is calculated using the formula:

$$t_{\text{backup}} = C_{\text{backup}} \times R_L \times \left( \frac{V_P - (V_{\text{REG2}} - 0.5)}{V_{\text{REG2}}} \right) \quad (1)$$

Example: For a  $V_P = 14.4$  V,  $V_{\text{REG2}} = 3.3$  V,  $R_L = 1 \text{ k}\Omega$  and  $C_{\text{backup}} = 100 \mu\text{F}$ , the delay time is 321 ms.

When an overvoltage condition occurs, the voltage on pin BUCAP is limited to approximately 24 V.

### 3. Heatsink calculation

#### 3.1 Introduction

The use of a proper heatsink is recommended in the amplifier application in order to guarantee its lifetime.

As defined in the Generic Mission Profile that was used for the reliability qualification of the TDF854x family, the average die temperature must not exceed 105 °C (see document GQS NX1-00023).

This device was qualified as a broadband audio amplifier at a test frequency of 1 kHz. It must be taken into account that subwoofer applications may need thermal compensation.

With a proper heatsink design and temperature pre-warning settings, the amplifier operates normally. It does not enter 'reduced gain' or switch off mode, unless there are severe problems e.g. a bad mechanical contact between the device and the heatsink. In these incidental cases, the maximum temperature protection becomes active and the gain will be reduced rapidly.

The maximum temperature protection is intended in these incidental cases to prevent the amplifier from continuously operating under too high die temperatures.

#### 3.2 Example 1, TDF8546/48 Best efficiency quad

To determine a suitable heatsink for the TDF8546, perform the following steps:

1. Determine power dissipation for a chosen output power with help of a dissipation graph (see [Figure 24](#))
2. Create a thermal model
3. Determine the values for the thermal model and calculate the heatsink

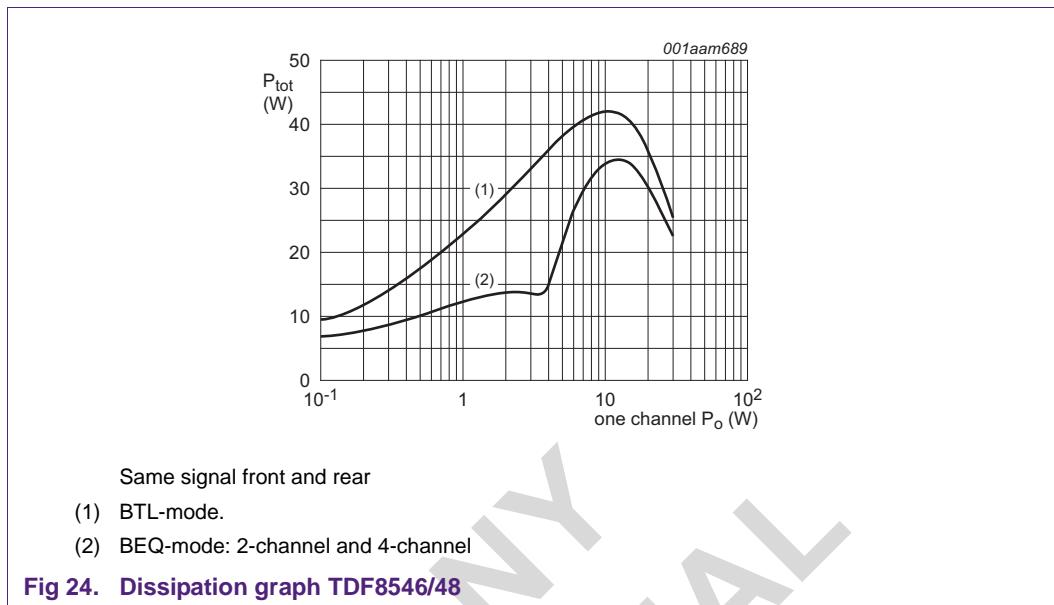
##### 3.2.1 Determine power dissipation

When designing a heatsink, the amount of dissipated power is determined first with the help of the dissipation graph [Figure 24](#). When all 4 channels are driven, the dissipation graph displays the total dissipated power of the amplifier IC as a function of output power (per channel). In this case, curve 2 in [Figure 24](#).

The total power dissipation (vertical axis) is read from the graph of the amplifier, at a chosen output power per channel (horizontal axis  $P_o$ ).

The amplifier output power of a typical used case equals about 4 W (sine wave) per channel (depending on music style). With that output power, it can be seen that the total power dissipation equals 15 W in best efficiency mode.

[Figure 24](#) represents the total power dissipation when all 4 channels are driven (y-axis) compared with the output power of one channel (x-axis).



### 3.2.2 Thermal model

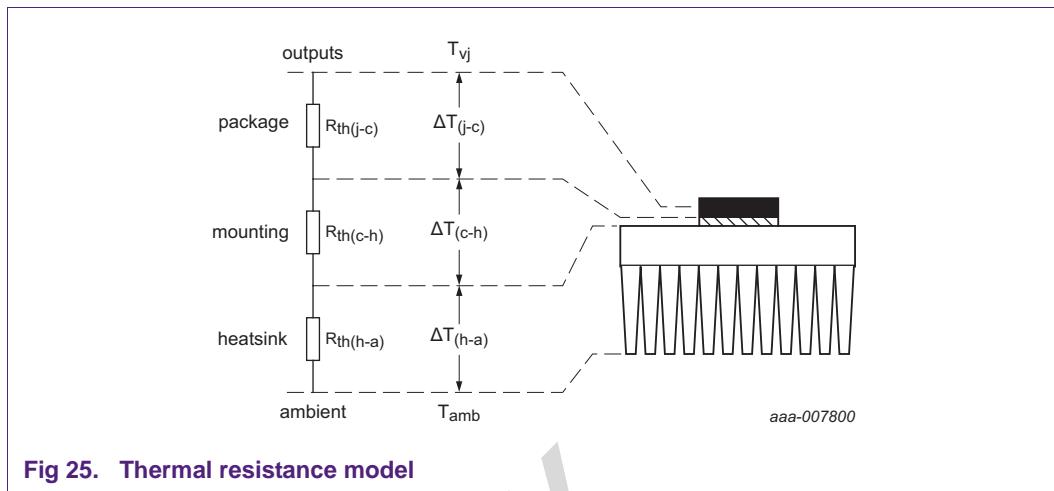
The equation for the thermal resistance [ $R_{th}$ ] equals Ohms law, when temperature [ $T$ ] is substituted for voltage and power [ $P$ ] is substituted for current.

$$R_{th} = \frac{T}{P} \quad (2)$$

In fact,  $\Delta T$  is the temperature difference across the thermal resistance while  $P_{tot}$  is the dissipated power of the amplifier, so:

$$R_{th} = \frac{\Delta T}{P_{tot}} \quad (3)$$

Figure 25 shows that the total thermal resistance is the sum of the thermal resistances from the junction (outputs) of the amplifier to the ambient. The temperature difference is the difference between the junction temperature of the amplifier and the ambient temperature.

**Fig 25. Thermal resistance model**

This means that the calculation can be extended to [Equation 4](#).

$$R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} = \frac{T_{vj} - T_{amb}}{P} \quad (4)$$

The equation for the thermal resistance then leads to [Equation 5](#).

$$R_{th(h-a)} = \frac{T_{vj} - T_{amb}}{P} - R_{th(j-c)} - R_{th(c-h)} \quad (5)$$

### 3.2.3 Determine values for thermal model and calculate heatsink

Find all values for the equations. First choose the maximum virtual junction temperature  $T_{vj}$ . This value must not exceed the value of 105 °C to guarantee the life time.

The ambient heat sink temperature of a head unit mounted in the dashboard of a car can easily reach  $T_{amb} = 60$  °C.

The total power dissipation of the amplifier can be found in the dissipation graph (see [Figure 24](#)) and is  $P = 15$  W.

The thermal resistance from the junction of the amplifier to the case (package) for this amplifier is  $R_{th(j-c)} = 1$  K/W.

The thermal resistance from case to heatsink when using thermal paste is  $R_{th(c-h)} = 0.1$  K/W. Thermal pads have a higher thermal resistance and can go up to approximately 1 K/W, depending on the material used.

The thermal resistance of the required heatsink can be calculated using [Equation 5](#)

$$R_{th(h-a)} = \frac{105 - 60}{15} - 1 - 0.1 = 1.9 \text{ K/W} \quad (6)$$

### 3.3 Example 2, TDF8541/44 Super best quad

The calculations used for example 1 can be applied to the TDF8541/44, which is a standard 4-channel BTL amplifier. The TDF8541/44 has a different dissipation graph to the TDF8546/48 in example 1. [Figure 24](#), curve (1) shows that when the output power equals 4 W, the dissipated power equals  $P = 36$  W (instead of 15 W).

Using the same conditions, the thermal resistance for the required heatsink is shown in [Equation 7](#).

$$R_{th(h-a)} = \frac{105 - 60}{36} - 1 - 0.1 = 0.15 \text{ K/W} \quad (7)$$

### 3.4 Example 3, TDF8556 IPAS3

For this typical type, determine the power dissipation in the amplifier and also the power dissipation in the linear regulators. Then the total power dissipation equals the sum of both  $P_{tot} = P_{amp} + P_{reg}$ .

The amplifier part is the same as for example 2.

For the regulator part, the power dissipation equals  $P_{reg}$ :

$$P_{reg} = (V_p - V_{out1}) \times I_{out1} + (V_p - V_{out2}) \times I_{out2} + \text{etc.} \quad (8)$$

where:

- $V_p$  = supply voltage
- $V_{out}$  = regulator output voltage
- $I_{out}$  = regulator load current

The values shown in [Table 6](#) represent values for a car radio with a Dirana2 DSP + Leaf Dice tuner.

**Table 6. Dirana2 DSP + Leaf Dice tuner**

Purpose	Regulator	Regulator voltage (V)	Regulator load current (mA) typical
Tuner TEF67xx	1	8.5	100
Microcontroller	2	3.3	100
DSP SAF77xx	3	3.3	330
CD/laser mechanism	4	8.6	200
Radio display	5	8.2	200

When these values are used in [Equation 8](#), the dissipation in the regulator equals:

$$P_{reg} = (14.4 - 8.5) \times 0.1 + (14.4 - 3.3) \times 0.1 + (14.4 - 3.3) \times 0.33 + (14.4 - 8.6) \times 0.2 + (14.4 - 8.2) \times 0.2 = 7.8 \text{ W.}$$

If regulator 6 of TDF8555 is also used, enter it into the equation and then the total power dissipation equals:

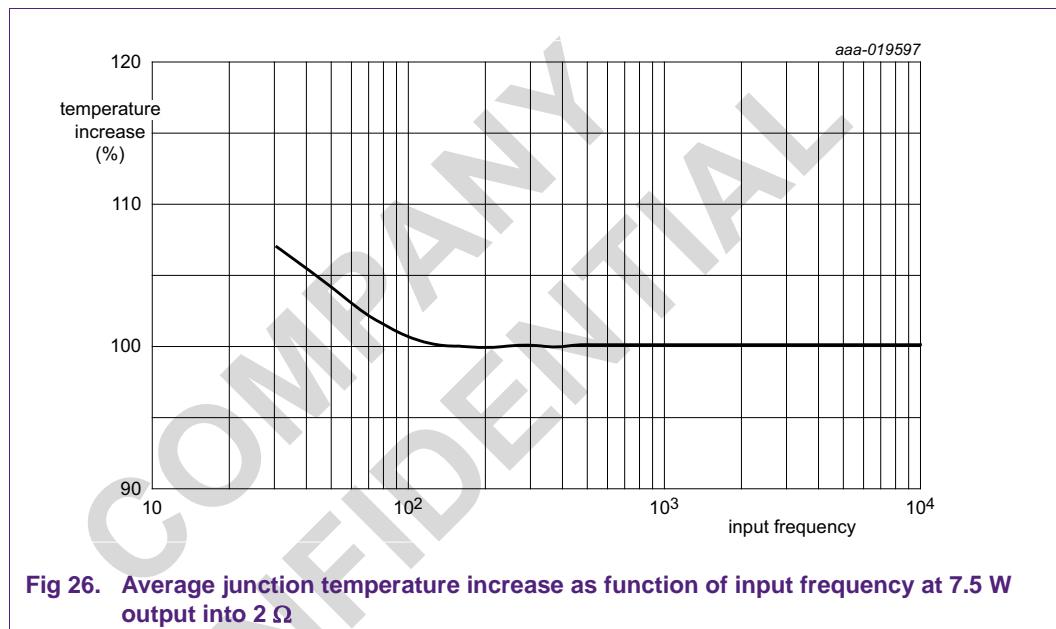
$$P_{tot} = P_{amp} + P_{reg} = 36 + 7.8 = 43.8 \text{ W} \quad (9)$$

The thermal resistance of the heatsink is shown in [Equation 10](#).

$$R_{th(h-a)} = \frac{105 - 60}{43.8} - 0.75 - 0.1 = 0.2 \text{ K/W} \quad (10)$$

### 3.5 TDF8546/48 and subwoofer applications

A subwoofer design targets a limited low frequency range of the audio frequency spectrum which causes the die to heat up more than in a full frequency range application. This can be the case with a  $2 \times 2 \Omega$  subwoofer application, due to the inherent thermal properties of silicon. The die heat is further influenced by the high power output. [Figure 26](#) shows the relationship between input frequency and temperature increase.



As the thermal warnings of the TDF8546/48 are based on full range audio application, the heatsink must be designed with an  $R_{th}$  value that is approximately 40 % smaller for subwoofer applications.

Besides the increased heatsink design, it is advised to reduce the risk for a high die temperature by programming an I<sup>2</sup>C software routine in the application. It uses the pre warning level of 135 °C. Based on the pre warning temperature information it reduces the subwoofer volume and switches the TDF8546 from best efficiency to BTL mode.

[Figure 27](#) shows a possible implementation for TDF8546/48.

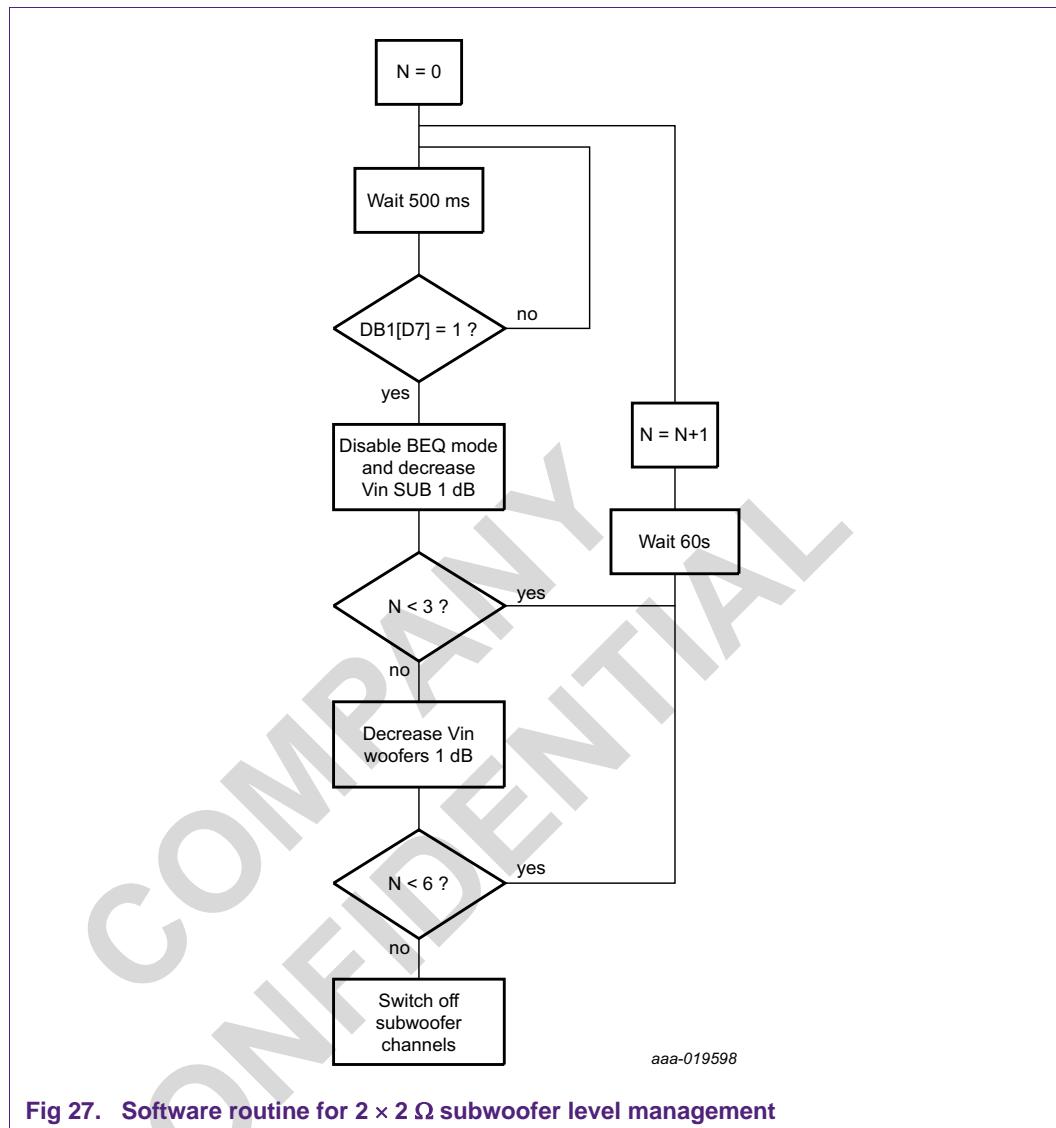


Fig 27. Software routine for  $2 \times 2 \Omega$  subwoofer level management

### 3.6 Heatsink graph

To select the length of heatsink required for the calculated value of thermal resistance, use the graph depicted in [Figure 28](#).

The thermal resistance of a heatsink as a function of its length is not linear, see [Figure 28](#).

For example:

- 50 mm = 6 K/W
- 100 mm equals 4.1 K/W (and not 3 K/W)

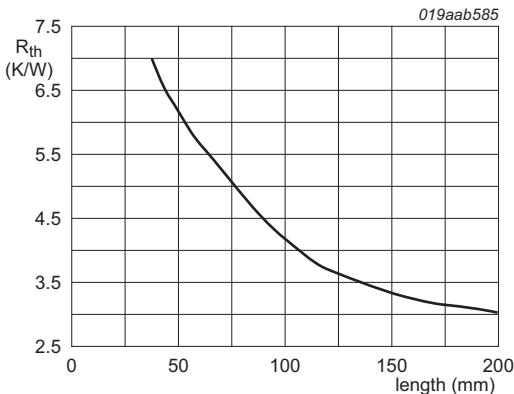


Fig 28. Heatsink thermal resistance as a function of its length

### 3.7 Dissipation reduction of TDF8555J

The TDF8555J has an optional V<sub>DCDC</sub> input which supplies regulator 3 only and produces a dissipation reduction of regulator 3. The dissipation reduction translates to a temperature reduction inside the application (when using the same heatsink).

The dissipation reduction depends on the chosen input voltage and the drive current of regulator 3.

The following two examples include the reductions calculated for dissipation and temperature.

To obtain values which take the ambient conditions (temperature) into account, perform actual temperature measurements in the final application.

- **Example 1**

Conditions:

- V<sub>DCDC</sub> = 14.4 V (connected to battery)
- V<sub>out</sub> = 3.3 V
- I<sub>out</sub> = 1 A

The dissipation is calculated as:

$$P_{\text{diss}} = (V_{\text{DCDC}} - V_{\text{out}}) \times I_{\text{out}} = (14.4 - 3.3) \times 1 = 11.1 \text{ W}$$

If V<sub>DCDC</sub> is changed from 14.4 V to 5 V, the dissipation is calculated as:

$$P_{\text{diss}} = (5 - 3.3) \times 1 = 1.7 \text{ W}$$

**Dissipation improvement = 9.4 W**

Temperature decreases (dT) with dissipation improvement.

Conditions:

- dissipation improvement  $\Delta P_{\text{diss}} = 9.4 \text{ W}$

- thermal resistance of junction to case of voltage regulator  $R_{th(j-c)} = 1.2 \text{ K/W}$
- thermal resistance of thermal paste between casing and heatsink  $R_{th(c-h)} = 0.1 \text{ K/W}$
- thermal resistance of heatsink to ambient  $R_{th\_h-a} = 2.8 \text{ K/W}$

$$dT = (R_{th(j-c)} + R_{th(c-h)} + R_{th\_h-a}) \times \Delta P_{diss} = (1.2 + 0.1 + 2.8) \times 9.4 = 39 \text{ }^{\circ}\text{C}$$

Based on this calculation, the heatsink temperature is approximately 39 °C lower.

- **Example 2**

Conditions:

- $V_{DCDC} = 14.4 \text{ V}$  (connected to battery)
- $V_{out} = 3.3 \text{ V}$
- $I_{out} = 500 \text{ mA}$

The dissipation is calculated as:

$$P_{diss} = (V_{DCDC} - V_{out}) \times I_{out} = (14.4 - 3.3) \times 0.5 = 5.55 \text{ W}$$

If  $V_{DCDC}$  is changed from 14.4 V to 5 V, the dissipation is calculated as:

$$P_{diss} = (5 - 3.3) \times 0.5 = 0.85 \text{ W}$$

**Dissipation improvement = 4.7 W**

Temperature decreases ( $dT$ ) with dissipation improvement.

Conditions:

- dissipation improvement  $\Delta P_{diss} = 4.7 \text{ W}$
- thermal resistance of junction to case of voltage regulator  $R_{th\_j-c} = 1.2 \text{ K/W}$
- thermal resistance of thermal paste between casing and heatsink  $R_{th\_c-h} = 0.1 \text{ K/W}$
- thermal resistance of heatsink to ambient  $R_{th\_h-a} = 2.8 \text{ K/W}$

$$dT = (R_{th\_j-c} + R_{th\_c-h} + R_{th\_h-a}) \times \Delta P_{diss} = (1.2 + 0.1 + 2.8) \times 4.7 = 19.5 \text{ }^{\circ}\text{C}$$

Based on this calculation, the heatsink temperature is approximately 20 °C lower.

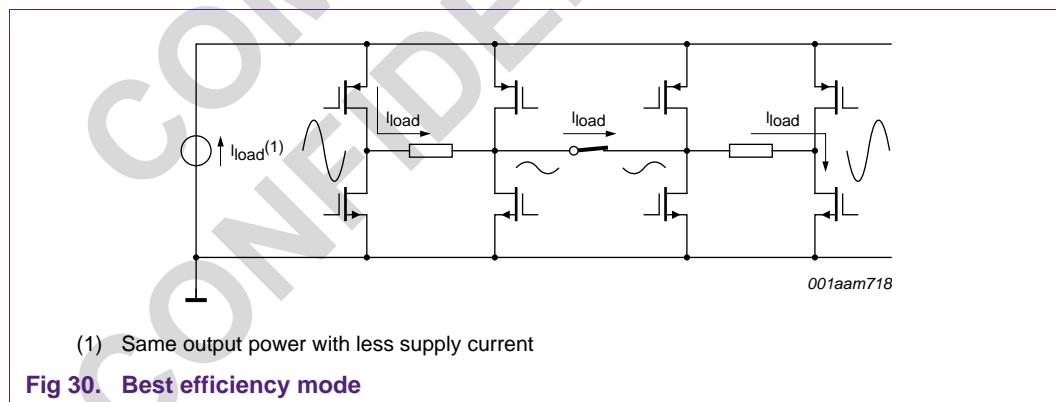
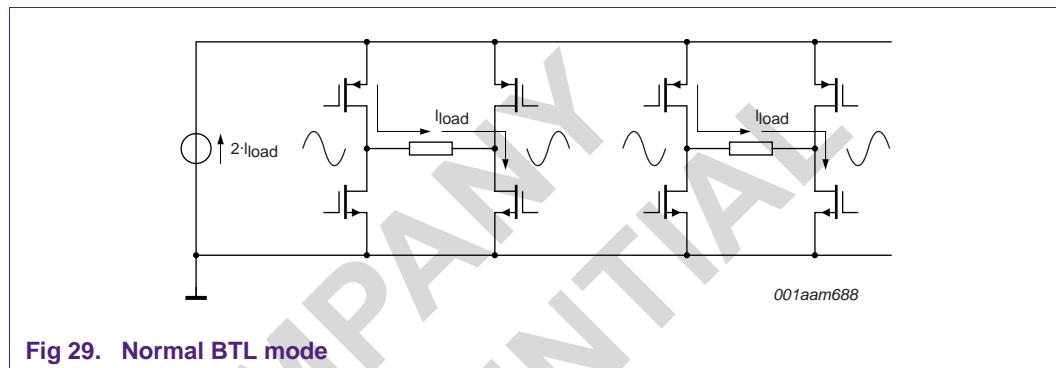
The calculations in example 1 and example 2, demonstrate how to achieve lower dissipation and heatsink temperatures. They are achieved by choosing a lower voltage on the  $V_{DCDC}$  input of the TDF8555J when the output current is high.

Practical assumptions are made during the calculations. Always use actual values determined during the practical setup.

## 4. Operating modes

### 4.1 TDF8546 Best efficiency amplifier, principle of operation

The TDF8546 is a new generation of complementary quad Bridge-Tied Load (BTL) audio power which has a built-in best efficiency mode. In this best efficiency mode, the loads of different channels can be dynamically placed in series to enable current sharing through these loads. This current sharing significantly reduces the amplifier dissipation. If enabled, the best efficiency mode is used for output signals of amplitudes less than half the supply voltage. It reuses the current between two channels by adding a switch (see best efficiency mode in [Figure 30](#)).



If the two channels depicted in [Figure 29](#) and [Figure 30](#) have the same signal, the current from the supply in normal BTL mode, is twice  $I_{load}$ . In the best efficiency mode, the current from the supply is only  $I_{load}$ . For the same output power, the best efficiency mode requires less power from the supply, resulting in less power dissipation.

The amplitude of the voltage at the output terminal which is internally connected to the switch is almost zero. It only contains the voltage drop across the internal switch.

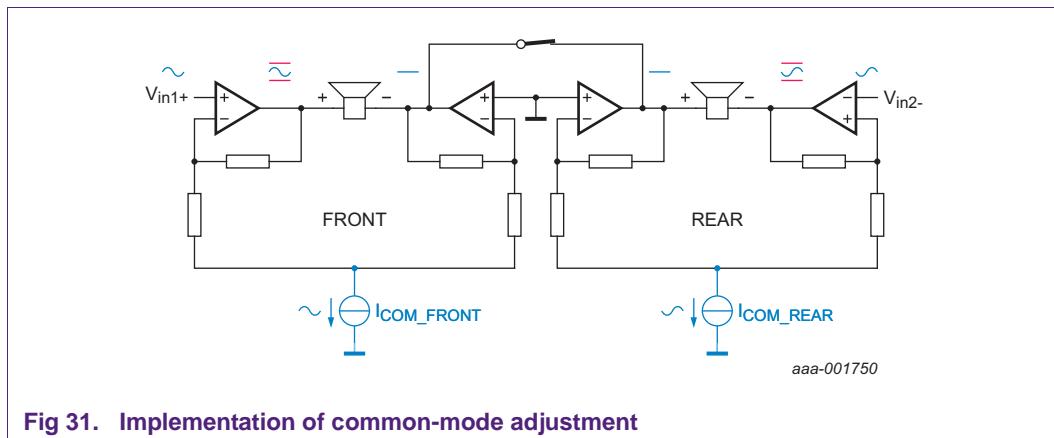


Fig 31. Implementation of common-mode adjustment

In the best efficiency mode both, the amplifiers for the positive and the negative BTL pair are supplied with an additional signal-dependent feed-forward common-mode current  $I_{\text{com}}$ . As a result, one of the BTL output signals is doubled and the other is almost constant, as can be seen in [Figure 31](#). The positive output of the front channel is doubled and the negative output is almost zero.

The TDF8546 has a best efficiency mode that has two modes of operation referred to as the 2×2-channel mode and the 4-channel mode.

#### 4.1.1 2×2-channel best efficiency mode

In the 2×2-channel best efficiency mode each front channel can share current with its corresponding rear channel, as can be seen in [Figure 32](#).

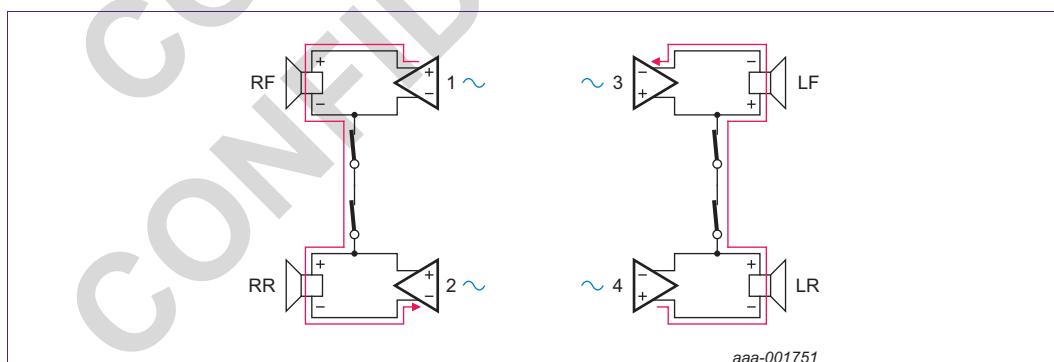


Fig 32. Best efficiency mode: 2x2-channel mode

The red arrows show how the front and the rear loads share the current. The internal connection of the switches is not symmetrical regarding the polarity of the channels. The left switch is connected to the minus output of the front channel. The right switch is connected to the plus output of the front channel. This results in inverse polarity of the currents between the left and the right part of the figure. The inverse polarity enables the 4-channel best efficiency mode.

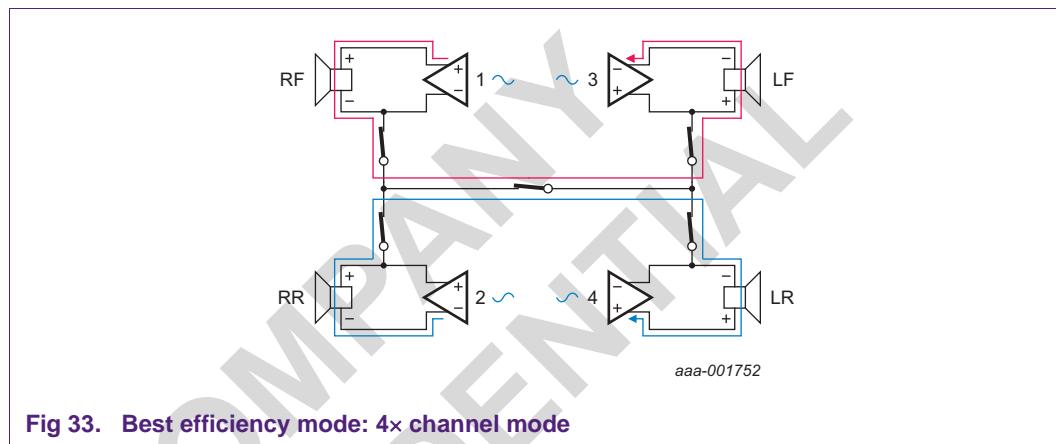
If the front channels cannot share current with the rear channels, there is no current sharing in the 2×2-channel best efficiency mode. This can occur when there is no correlation between front and rear or when the fader is turned completely to the front channels. When current sharing is required, use the 4-channel mode.

#### 4.1.2 4-channel best efficiency mode

In the 4-channel best efficiency mode the front and rear channels can share load current with each other. The left and right channels can also share current in this mode.

In the 4-channel best efficiency mode, the front and rear channels can share load current with each other. Similarly, the left and right channels can also share load current with each other in the 4-channel best efficiency mode.

If the rear channels have no correlation with the front channels, the current of the left and right channels can be shared, see [Figure 33](#). In this example, the signal of the rear channels is inverted with respect to the signal of the front channels. The two front channels have the same signal and also the two rear channels have the same signal.



**Fig 33. Best efficiency mode: 4x channel mode**

The red arrow shows how the front right and left loads share the current. The blue arrow shows how the rear right and left loads share the current.

#### 4.1.3 How to connect the amplifier to the speakers

To gain the most in efficiency, it is important to map each amplifier channel to the correct speaker channel

In 2x2-channel best efficiency mode, Channel 1 can share current with channel 2 and channel 3 can share current with channel 4.

In principle, all channels can share with all other channels in the 4-channel best efficiency mode. As an example: if channel 1 cannot share current with channel 2, if these signals are correlated, it shares current with channel 3.

The most efficient configurations are provided in [Table 7](#):

**Table 7. Overview of the most efficient configurations**

Configuration	RF	RR	LF	LR
1 (default)	channel 1	channel 2	channel 3	channel 4
2	channel 2	channel 1	channel 4	channel 3
3	channel 3	channel 4	channel 1	channel 2
4	channel 4	channel 3	channel 2	channel 1

Other configurations are possible but they result in less optimum efficiency.

## 4.2 Legacy mode and I<sup>2</sup>C mode

The TDF854x can operate in legacy mode, which does not require a microcontroller/PC/laptop. When pin ADSEL is shorted to ground, the amplifier operates in legacy mode.

## 4.3 I<sup>2</sup>C address selection

The TDF854x operates in I<sup>2</sup>C mode by applying the appropriate resistor value on pin ADSEL to signal ground. The value of the resistor determines the I<sup>2</sup>C address.

The number of I<sup>2</sup>C-addresses, instruction bytes and data bytes depends on the amplifier type. [Table 8](#) gives an overview.

**Table 8. Overview of instruction bytes and data bytes**

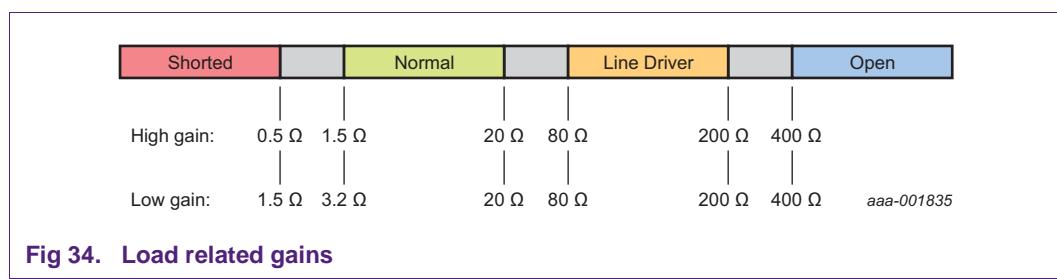
Device	Instruction bytes	Data bytes	Legacy mode	I <sup>2</sup> C-address (hex)	ADSEL pin connected to
TDF8541/44	4	5	yes	D4	10 kΩ/1 %
				DA	5 V
				DC	100 kΩ/1 %
				DE	30 kΩ/1 %
TDF8546	5	5	yes	D4	10 kΩ/1 %
				DA	5 V
				DC	100 kΩ/1 %
				DE	30 kΩ/1 %
TDF8554/55/56	4	4	no	D8	n.a.

## 4.4 Start-up diagnostics

The start-up diagnostics consists of two stages. Perform the first stage **before** enabling the amplifier. During this stage, the type of load that is connected to the outputs of the amplifier is determined:

- No load
- Normal load
- Line driver load
- Short circuit

[Figure 34](#) shows the values for the different loads, with high gain = 26 dB and low gain = 16 dB.



The second stage is carried out **during start-up** of the amplifier. During this stage, the following protections are checked:

- output short-circuited to ground
- output short-circuited to  $V_p$
- loudspeaker fault - one wire of the speaker is connected to the amplifier output and the other wire is connected to ground or  $V_p$

If there is a fault (e.g. a short circuit to ground on an output) the load type is "not valid". The second stage diagnoses the actual fault.

#### 4.4.1 Diagnostics start-up time

The total start-up time from start-up command ( $stbpin = \text{high}$ ,  $IB1D1=1$ ) until amplifier on (90 % of output signal available), including start-up diagnostics stage 1 and stage 2 equals:

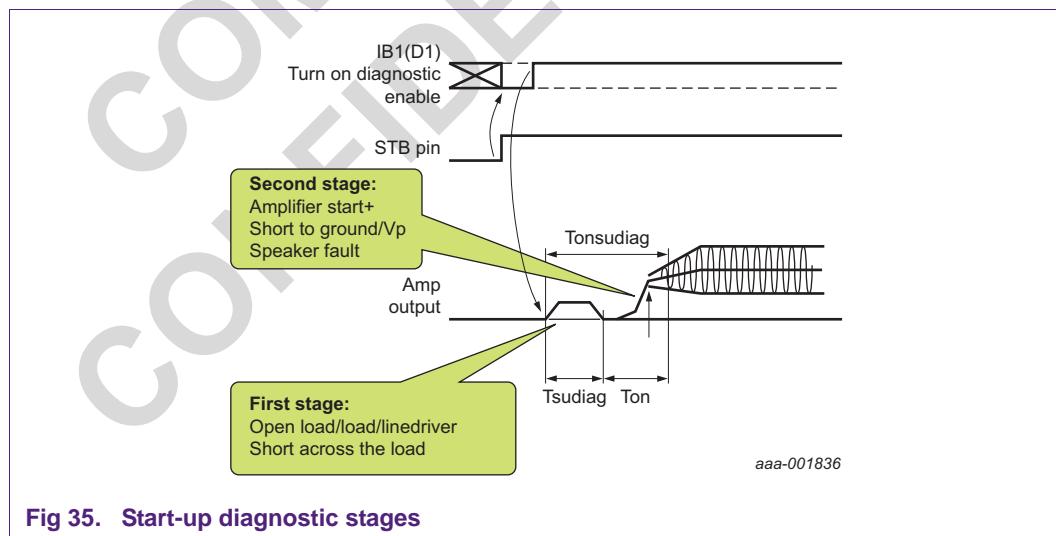
$$T_{\text{total startup}} = T_{\text{wake}} + T_{\text{onsudiag}} = T_{\text{wake}} + T_{\text{sudiag}} + T_{\text{on}}$$

If only start-up diagnostics stage 2 is carried out, then the total start-up time equals:

$$T_{\text{total startup}} = T_{\text{wake}} + T_{\text{on}}$$

#### 4.4.2 Start-up diagnostics procedure

To ensure success, perform the start-up diagnostics in accordance with a set procedure.



#### Example 1: TDF854x, starting up the amplifier performing start-up diagnostics

This example shows the procedure for the start-up diagnostics for sending the proper I<sup>2</sup>C commands to the amplifier under the following conditions:

- best efficiency mode enabled
- 4 ohm load connected to the outputs of the amplifier
- supply voltage = 14.4 V

Table 9. Start-up with start-up diagnostics<sup>[1]</sup>

Step	Duration	Action	I <sup>2</sup> C bits	Write/ Read	I <sup>2</sup> C command (hex)				
					IB1/ DB1	IB2/ DB2	IB3/ DB3	IB4/ DB4	IB5/ DB5
1	-	• set STB pin = low	none	-	-	-	-	-	-
2	-	• set STB pin = high, via microcontroller	none	-	-	-	-	-	-
3	T <sub>wake</sub>	• amplifier start not enabled	IB1, D0=0	W	00	06	00	00	90
		• all channels in soft mute	IB2, D1, D2 = 1.1						
		• set gain set to 26 dB	IB3, D5, D6 = 0.0						
		• enable all the channels	IB3, D0...D3 = 0						
		• put DC load info on DBx, D5, D4	IB4, D4 = 0						
		• set high efficiency mode active	IB5, D7 = 1						
		• set high efficiency mod to all 4 channels	IB5, D6 = 0						
		• set best efficiency switch level set to 4 Ω	IB5, D4 = 1						
4	-	• keep reading data until "start-up diag busy bit" DB5, D5 = 0 • if DB5, D5 = 0 then next instruction byte can be written; this read clears results from previous diagnostics	DB5, D5	R	xx	xx	xx	xx	x0
5	T <sub>su_diag</sub>	• start-up amplifier	IB1, D0 = 1	W	03	06	00	00	90
	T <sub>onsu_diag</sub>	• enable start-up diagnostic	IB1, D1 = 1						
6	T <sub>amp_on</sub>	wait at least until T <sub>amp_on</sub> is MAX • read back the result of: – shorted load detection – short to V <sub>p</sub> – short to ground – load detection	DBx, D3 DBx, D1 DBx, D0 DBx, D5, D4	R	00	00	00	00	xx
7		• unmute amplifier channels	IB2, D2, D1 = 0,0	W	03	00	00	00	90
8		• amplifier is now on and ready to play audio							

## [1] Key:

IB = instruction byte =&gt; write data

DB = data byte =&gt; read data

W = write instruction byte

R = read data byte

x = do not care

**Note:**

The shorted load, short to V<sub>p</sub> and ground information from the start-up diagnostic, is cleared after one I<sup>2</sup>C read and shows the actual situation. When the short has been removed, the bits are also cleared. The DBxD5 and DBxD4 information, generated at start-up, will be refreshed after a new start-up diagnostic cycle.

**Example 2: TDF854x, starting up the amplifier performing repeated start-up diagnostics**

In order to increase the reliability of the start-up diagnostics, the first stage is carried out more than once:

- best efficiency mode enabled
- 4 ohm load connected to the outputs of the amplifier
- supply voltage = 14.4 V

[Table 10](#) contains the steps of the I<sup>2</sup>C command that must be performed.

**Table 10. Start-up with repeated diagnostic procedure<sup>[1]</sup>**

Step	Duration	Action	I <sup>2</sup> C bits	Write/ Read	I <sup>2</sup> C command (hex)				
					IB1/ DB1	IB2/ DB2	IB3/ DB3	IB4/ DB4	IB5/ DB5
1	-	• set STB pin = low	none	-	-	-	-	-	-
2	-	• set STB pin = high, via microcontroller	none	-	-	-	-	-	-
3	T <sub>wake</sub>	• amplifier start not enabled	IB1, D0=0	W	00	06	00	00	90
		• all channels in soft mute	IB2, D1, D2 = 1.1						
		• set gain set to 26 dB	IB3, D5, D6 = 0.0						
		• enable all the channels	IB3, D0...D3 = 0						
		• put DC load info on DBx, D5, D4	IB4, D4 = 0						
		• set high efficiency mode active	IB5, D7 = 1						
		• set high efficiency mod to all 4 channels	IB5, D6 = 0						
		• set best efficiency switch level set to 4 Ω	IB5, D4 = 1						
4	-	• keep reading data until "start-up diag busy bit" DB5, D5 = 0 • if DB5, D5 = 0 then next instruction byte can be written; this read clears results from previous diagnostics	DB5, D5	R	xx	xx	xx	xx	x0
5	T <sub>su_diag</sub>	• start-up amplifier	IB1, D0 = 1	W	03	06	00	00	90
	T <sub>onsu_diag</sub>	• enable start-up diagnostic	IB1, D1 = 1						
6	T <sub>amp_on</sub>	wait at least until T <sub>amp_on</sub> is MAX • read back the result of: – shorted load detection – short to V <sub>p</sub> – short to ground – load detection	DBx, D3 DBx, D1 DBx, D0 DBx, D5, D4	R	00	00	00	00	xx
7	-	• start-up diagnostic disabled	IB1, D1 = 0	W	01	06	00	00	90
8	-	• go to step 3 (repeat twice then proceed to step 9)	-	-	-	-	-	-	-
9		• unmute amplifier channels	IB2, D2, D1 = 0,0	W	01	00	00	00	90
10		• amplifier is now on and ready to play audio							

[1] **Key:**

IB = instruction byte =&gt; write data

DB= data byte =&gt; read data

W = write instruction byte

R = read data byte

x = do not care

**Note:**

The shorted load, short to  $V_p$  and ground information from the start-up diagnostic, is cleared after one I<sup>2</sup>C read and shows the actual situation. When the short has been removed, the bits are also cleared. The DBxD5 and DBxD4 information, generated at start-up, will be refreshed after a new start-up diagnostic cycle.

**Example 3: Shutting down the amplifier**

[Table 11](#) contains the steps of the I<sup>2</sup>C command that must be performed.

**Table 11. Amplifier shut-down procedure<sup>[1]</sup>**

Step	Duration	Action	I <sup>2</sup> C bits	Write/ Read	I <sup>2</sup> C command (hex)				
					IB1/ DB1	IB2/ DB2	IB3/ DB3	IB4/ DB4	IB5/ DB5
<b>Amplifier is on and playing</b>									
1	-	<ul style="list-style-type: none"> <li>• set all channels to soft mute,</li> <li>• disable fast mute</li> <li>• disable amplifier</li> </ul>	IB2, D1, D2 = 1.1 IB2, D0 = 0 IB1, D0 = 0	W	x0	x6	xx	xx	xx
2	-	• set STB pin = high, via microcontroller	none	-	-	-	-	-	-
<b>Amplifier is off</b>									

[1] **Key:**

IB = instruction byte (write data)

DB= data byte (read data)

W = write instruction byte

x = do not care

**Note:**

The shorted load, short to  $V_p$  and ground information from the start-up diagnostic, is cleared after one I<sup>2</sup>C read and shows the actual situation. When the short has been removed, the bits are also cleared. The DBxD5 and DBxD4 information, generated at start-up, will be refreshed after a new start-up diagnostic cycle.

The start-up diagnostic busy bit DB5D5 is only valid for the first stage on the start-up, refer to [Figure 35](#).

## 4.5 Operation of I<sup>2</sup>C clear after a read command

After every I<sup>2</sup>C command, all data bytes (4 or 5, depending on amplifier type) can be read.

After the last data byte is read, all protection data bits are reset to logic 0.

If a short to ground is still present, the short to ground bit DB[1:4]D0 is immediately set to logic 1 again. If the short to ground is removed before the next I<sup>2</sup>C read, the short to ground bit remains set. In the next I<sup>2</sup>C read-out, the short to ground bits resets to logic 0. The most complete information is gathered after 2 read commands.

During offset detection, output offset bits DB[1:4]D2 are set to logic 1 when the output voltage rises above the 1.5 V offset threshold. If the output voltage falls below 1.5 V, it resets to logic 0.

If the output voltage rises above 1.5 V again, within a 1 s read interval, the offset bit remains at logic 0.

If, after the output voltage is less than 1.5 V, an I<sup>2</sup>C-read command occurs, first the logic 0 will be read. After the last data-byte has been read, the offset bit is set to logic 1. When the output voltage now goes below 1.5 V, the latch is reset again.

For the following conditions, the bits are cleared after reading the last data byte. If the error condition is still active, the bits are set immediately and are indicated at the next read. No waiting time needed:

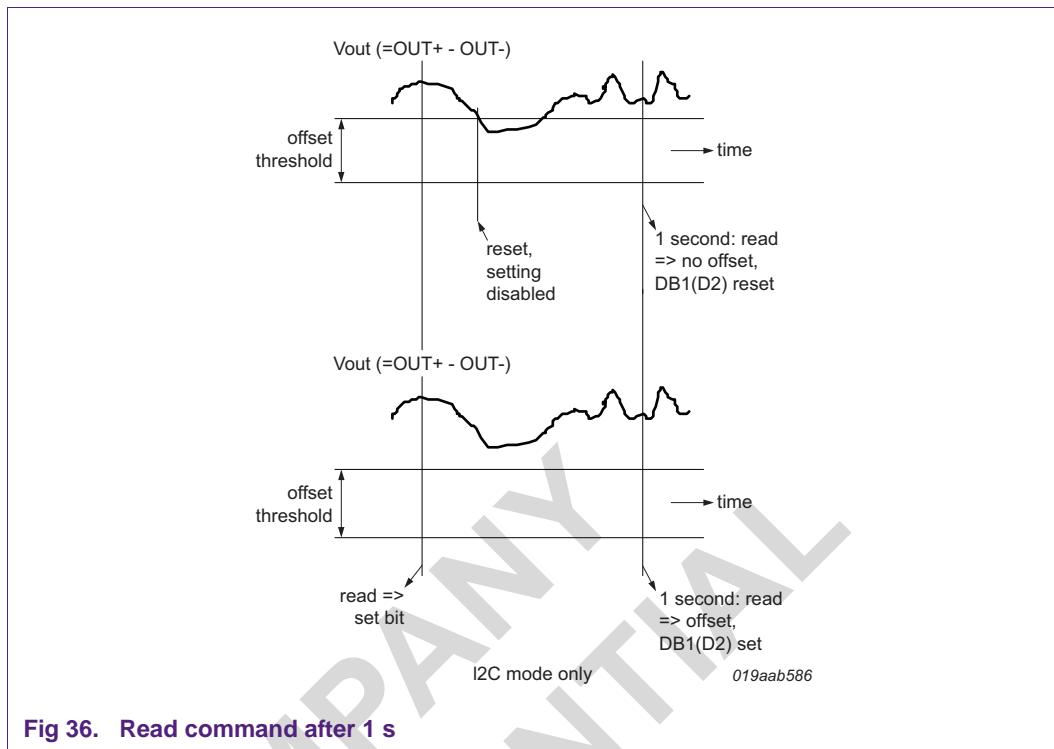
- short to V<sub>P</sub>
- short to GND
- shorted load
- overvoltage
- undervoltage
- temperature pre-warning
- maximum temperature protection

Offset detection requires a waiting time for the "software filtering". The waiting time is preferably more than 1 s, for example 3 s, and it is only needed when there is an audio input signal. Waiting time is not needed when there is no audio input signal (ASP/DSP in mute, amplifier not in mute) because there is no audio to filter.

A more detailed explanation is provided in [Section 4.5.1](#), [Section 4.5.2](#) and [Section 4.5.3](#).

### 4.5.1 Offset detection after 1 s read command

After each I<sup>2</sup>C read command, the offset information is read first. Then, when the last data byte is read, the offset bit is set to logic 1, see [Figure 36](#).



**Fig 36. Read command after 1 s**

When, after 1 s, all data bytes are read and the offset bit is still logic 0:

- the output voltage has been (once) below the offset threshold of 1.5 V, after the last I<sup>2</sup>C read command (1 s ago)

When, after 1 s, all data bytes are read, and the offset bit is still logic 1:

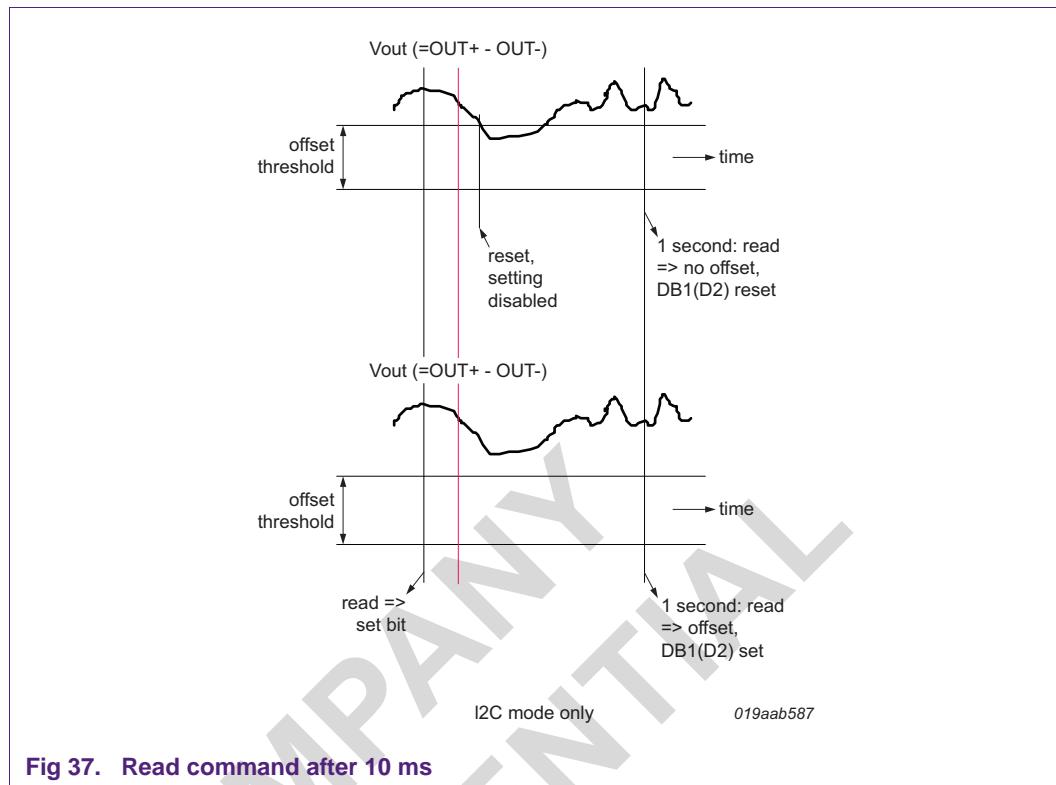
- the output signal remains above 1.5 V after the last I<sup>2</sup>C-read command (1 s ago). Possible causes are:
  - a very low frequency with half of a period of 1 s is present:  $f = 1/T = 1/(2 \times 1) = 0.5$  Hz (software filtering)
  - an offset on the outputs preventing the output signal from reaching the 1.5 V threshold window

After all data bytes are read, the offset bit is reset to logic 1.

#### 4.5.2 Offset detection after a 10 ms read command

When, after 10 ms, all data bytes are read (see [Figure 37](#)) and the offset bit is still logic 1:

- The output level has not been lower than 1.5 V, after the last I<sup>2</sup>C-read (10 ms ago). Possible causes are:
  - A frequency with half a period of more than 10 ms is present:  $f = 1/T = 1/(2 \times 0.01) = 50$  Hz. These signals can occur in the audio signal which means incorrect software filtering
  - An offset which prevents the output level from reaching the 1.5 V threshold window

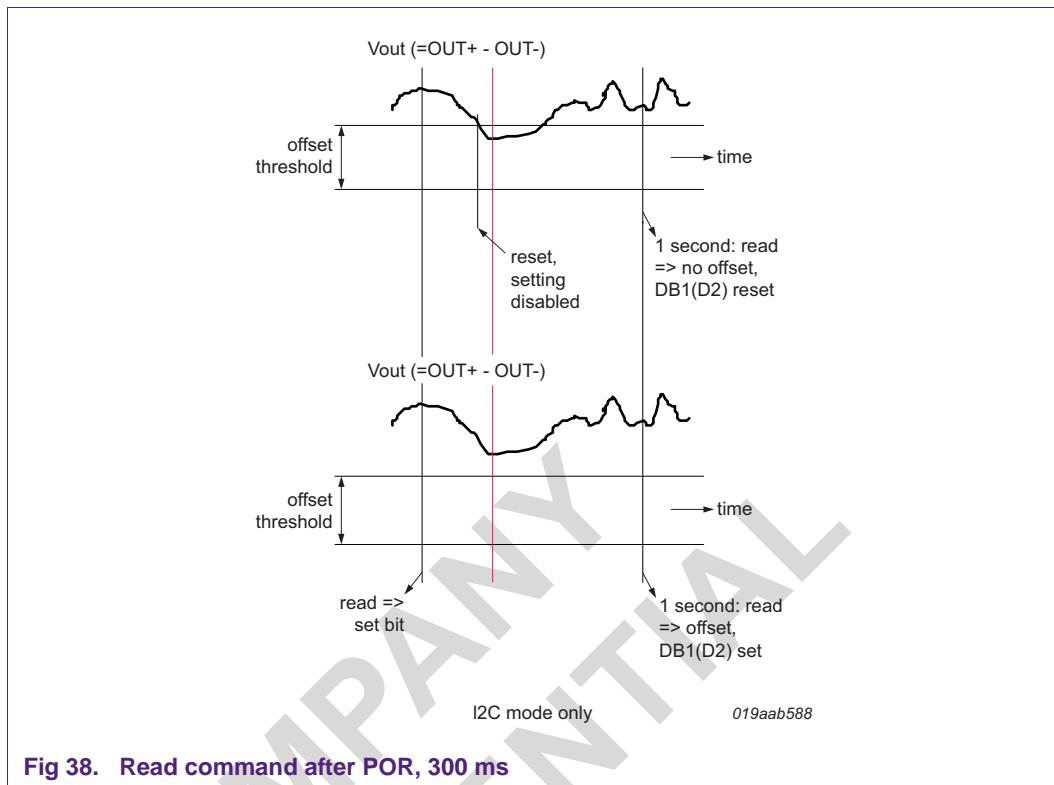


#### 4.5.3 Offset detection after power-on reset

After a power-on reset, the offset bit is set to logic 1. When the amplifier is started, the amplifier starts up in mute. This means that the output voltage is zero, and the offset bit is immediately set to logic 0 (see [Figure 38](#)).

When the start-up mute is released (after approximately 300 ms), and if there is a leakage at the input, an output voltage offset of more than 1.5 V is generated and:

- The first I<sup>2</sup>C-read of the data bytes does not indicate an offset because the offset bit is reset. The reset is the result of the amplifier mute during start-up
- The second I<sup>2</sup>C-read command indicates an offset if, during the first I<sup>2</sup>C read command (sets the offset bit) and the second I<sup>2</sup>C-read command, the output voltage is more than 1.5 V (offset threshold).



#### 4.6 Shorted load detection in TDF8541/44

This section gives a more detailed explanation about the short-circuit detection across the load.

A short-circuit across the load is detected in the following situations:

1. During start-up, with the built-in start-up diagnostics enabled
  - High gain mode,  $R_{load} < 0.5 \Omega$
  - Low gain mode,  $R_{load} < 1.5 \Omega$
2. After start-up if the maximum current protection is activated
  - Inside the safe operating area (SOAR) of output power transistors window,  $I_{max} > 4 \text{ A}$  for  $V_{oM} < 1.3 \text{ V}$
  - Outside SOAR window,  $I_{max} > 8 \text{ A}$  for  $V_{oM} > 1.3 \text{ V}$

A short across the load cannot be detected if there is no output signal present after start-up.

##### Example 1: $R_{load} 250 \text{ m}\Omega$ - detect short circuit across the load:

- during start-up
- After start-up
  - inside the SOAR window for  $V_{oM} > 1 \text{ V}$  ( $4 \text{ A} \times 250 \text{ m}\Omega$ )
  - outside the SOAR window for  $V_{oM} > 2 \text{ V}$  ( $8 \text{ A} \times 250 \text{ m}\Omega$ )
- For  $V_{oM} < 1 \text{ V}$  and  $1.3 \text{ V} < V_{oM} < 2 \text{ V}$  short across the load is **not detected** because  $I_{max}$  protection level is not activated

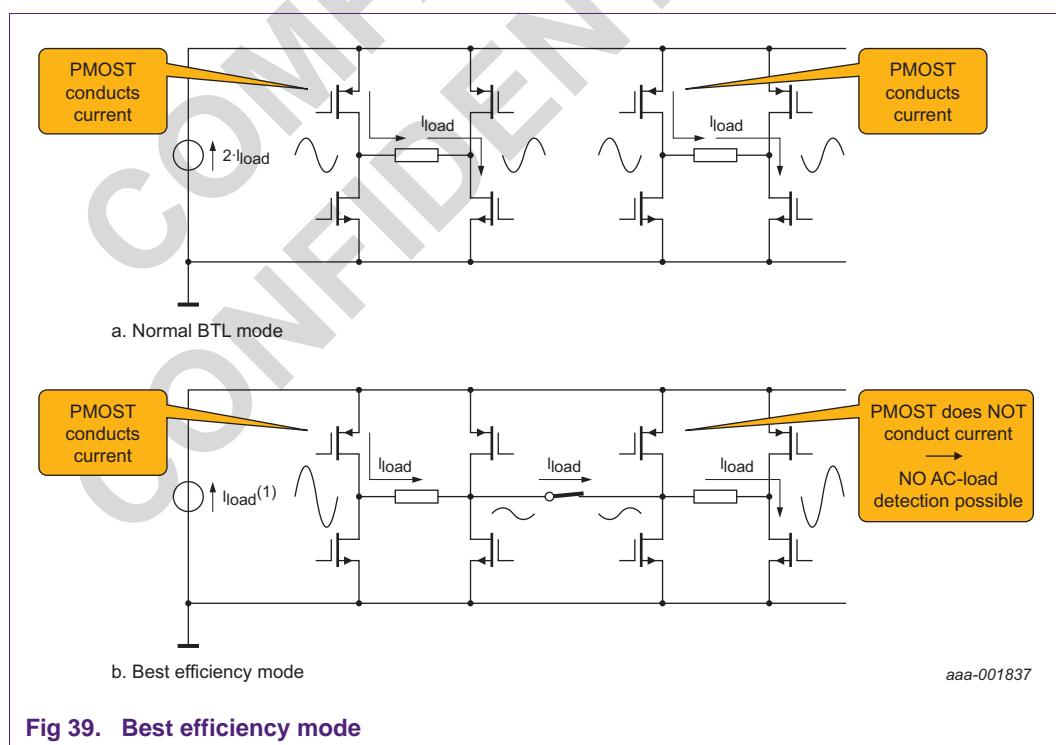
**Example 2:  $R_{load}$  150 mΩ - detect short circuit across the load:**

- during start-up
- After start-up
  - inside the SOAR window for  $V_{oM} > 0.6$  V ( $4\text{ A} \times 150\text{ m}\Omega$ )
  - outside the SOAR window for  $V_{oM} > 1.2$  V ( $8\text{ A} \times 150\text{ m}\Omega$ )
- For  $V_{oM} < 0.6$  V short across the load is **not detected** because  $I_{max}$  protection level is not activated

**4.7 AC load detection functionality in best efficiency mode TDF8546**

When using TDF8546J in best efficiency mode, AC load detection is not functional for channels 2 and 3, due to the principle of best efficiency:

- in best efficiency mode, current is shared among channels (current is reused)
- AC load detection sensor only measures current in PMOST of the positive outputs (+) of the BTL stages
- When the amplifier operates in best efficiency mode, the positive outputs (+) of channels 2 and 3 are at the midtap voltage (~½ V<sub>p</sub>). The channels do not carry current and consequently, no current is measured or detected for them.

**Fig 39. Best efficiency mode**

If it is still required to carry out AC load detection, switch to normal BTL mode, by setting instruction bit IB5D7 = 0.

#### 4.8 STB pin as second clip detect\connect to a 3.3 V microcontroller

The STB pin can be used as second clip detect pin. I<sup>2</sup>C selects which channel provides the clip information on the clip pin or the STB pin. The selection is made using instruction bits: IB1[D3] up to IB1[D6].

If the STB pin voltage drops below 2.5 V, the IC switches to standby. To prevent this from happening, when the clip detect pin is activated, the voltage drops to 6 V. Functionally, the clip detect pin looks like an open-drain with a Zener voltage of 5.5 V in series.

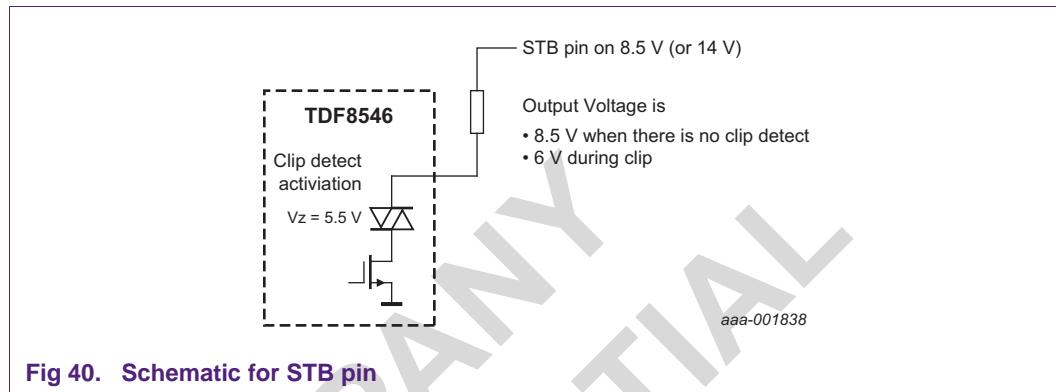


Fig 40. Schematic for STB pin

An interface circuit (level shift) is required to convert the clip detect information from the STB pin to the microcontroller. The interface circuit depicted in [Figure 41](#) is based on a recommended reference voltage of 8.5 V.

If the amplifier is switched off, the 8.5 V reference voltage must be disabled to prevent draining the car battery by leakage current. For example, when the ignition key is turned off - V<sub>acc</sub>.

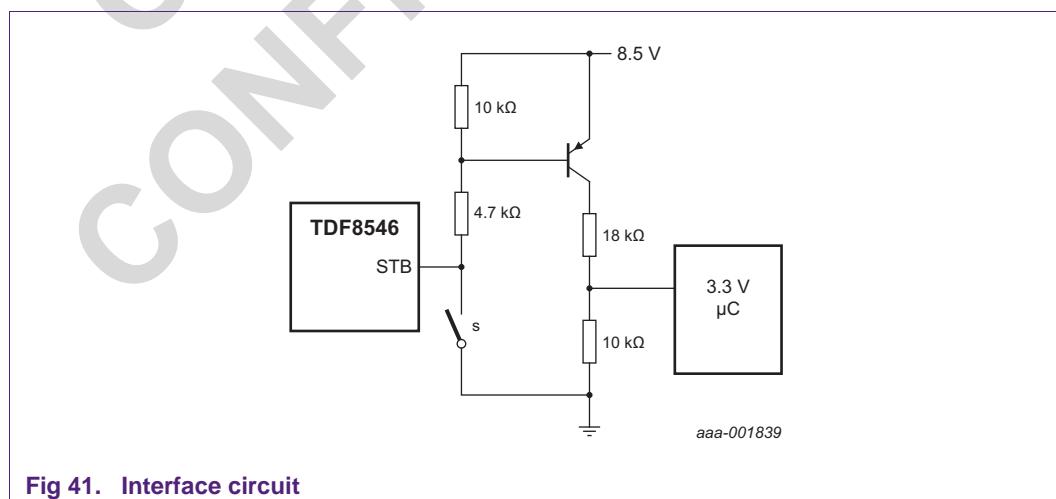


Fig 41. Interface circuit

#### 4.9 Thermal foldback handling

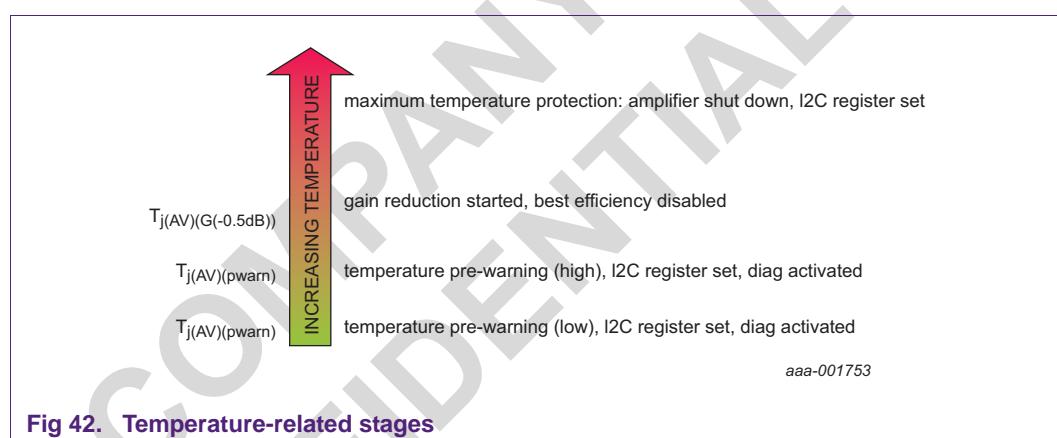
When the average junction temperature of the amplifier rises, each type of amplifier described in this application note has multiple temperature levels to which it reacts.

When it reaches the pre-warning level ( $T_{j(AV)(pwarn)}$ ), the amplifier sets a bit in the I2C register (IB3[D4]). The absolute temperature level of this pre-warning level can be set to two different levels using the associated I2C bit.

If the temperature increases further and approaches  $T_{j(AV)(G(-0.5dB))}$ , the temperature-controlled gain reduction is activated and, if activated, the best efficiency mode is turned off.

If the temperature still increases despite the gain reduction, the amplifier is shut down completely. The associated I2C bit for the maximum temperature protection is activated.

If the output level of an amplifier is not contained, the amplifier can reach a temperature where it starts to reduce its gain (see [Figure 42](#)). This pre-warning register can be used to provide an indication that the output level must be reduced to prevent it. One method is to adjust the low frequency content smoothly to lower the total output power with a relatively small subjective reduction.



The gain reduction feature of the amplifier is regarded as protection and, as such, it is not advised to employ this feature during normal usage. The harmonic distortion increases during gain reduction.

Amplifiers with regulators are switched off when the regulator junction temperature becomes too high. The switch-off prevents undefined audio signals when the regulators are switched off while the amplifier is still on.

Occasionally a false temperature pre-warning can be given. The false warning is the result of an internal glitch. It occurs when a short between any output to GND or to V<sub>p</sub> is generated during operation of the amplifier. To prevent pre-warning, read the I2C register twice to be sure that the latest status is read (see [Section 4.5](#)).

## 5. Control software

### 5.1 Windows 7 32-bit and 64-bit I<sup>2</sup>C driver

In order to install the I<sup>2</sup>C driver for Windows 7, the next steps are performed before I<sup>2</sup>C communication is possible.

- Remove the previous (32-bit) driver before installing the updated drivers as follows:
  - press START
  - select Control Panel and then Add/Remove programs
  - locate the I<sup>2</sup>C entry and remove it
  - reboot the PC
  - install the new driver

**Failing to uninstall the previous driver leads to a non-functional PC with respect to the USB to I<sup>2</sup>C communication.**

- Run the I2C\_Setup\_V700.exe utility, which now (V7xx and higher) installs the driver in 32-bit and 64-bit environments.
- The new driver files are installed in the folder C:\USB-I2C.

The 32-bit installation is described in [Section 5.2](#). The remainder of this section is dedicated to the 64-bit installation. The 64-bit driver only supports USB-I2C interfaces.

When the setup utility has finished, attach a USB-I2C interface to the PC. Windows 7 does not recognize the adapter, so manual intervention with administrator privileges is now required.

- Press START.
- Proceed to Control Panel and select the Device Manager (see [Figure 43](#)).

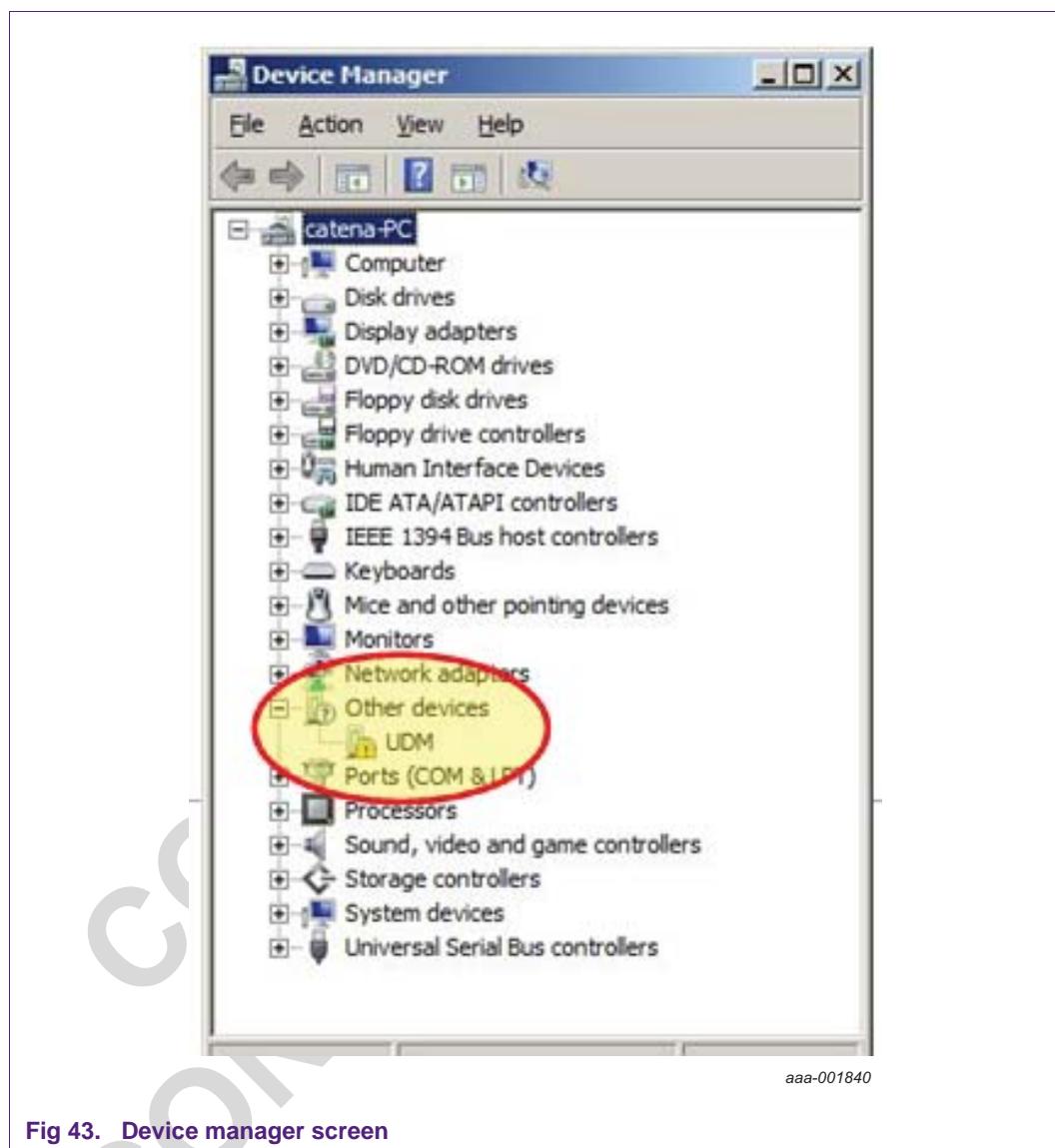


Fig 43. Device manager screen

- Double-click the UDM link (see [Figure 43](#)) to enter the UDM properties page (see [Figure 44](#)).

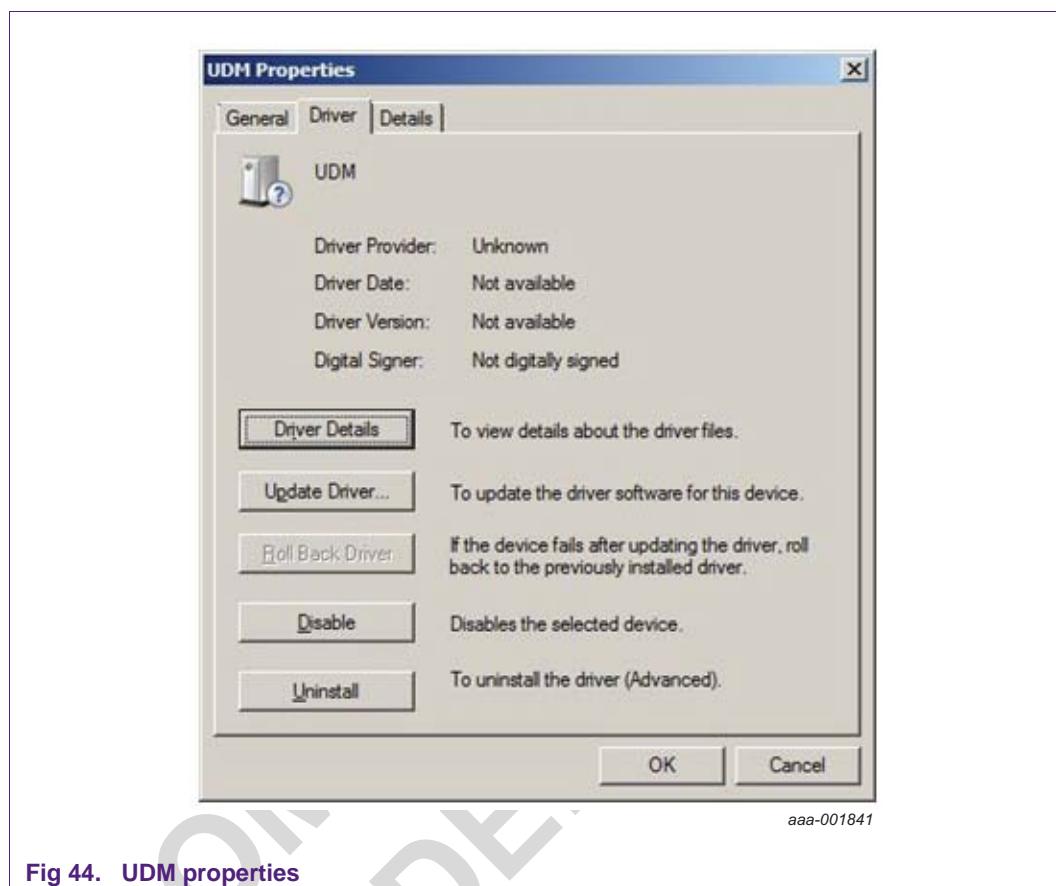


Fig 44. UDM properties

- Click the “Update Driver” button to gain access the “Update Driver Software - UDM” screen (see [Figure 45](#)).

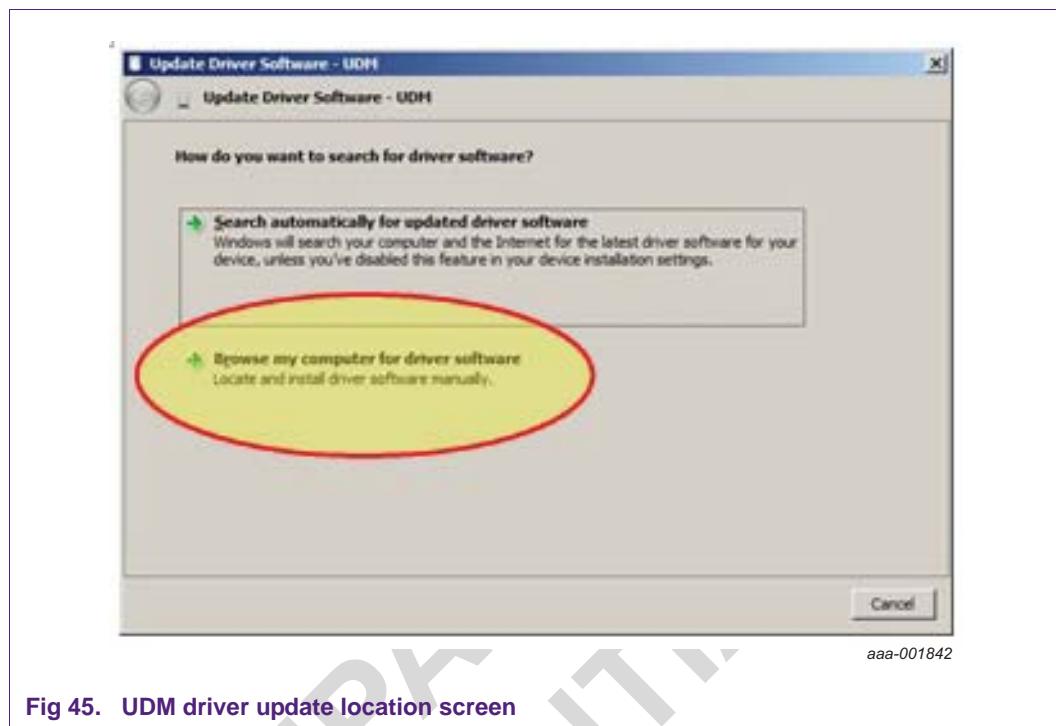


Fig 45. UDM driver update location screen

- Select "Browse my computer for driver software" (see [Figure 45](#)) to open the Windows driver location screen (see [Figure 46](#)).

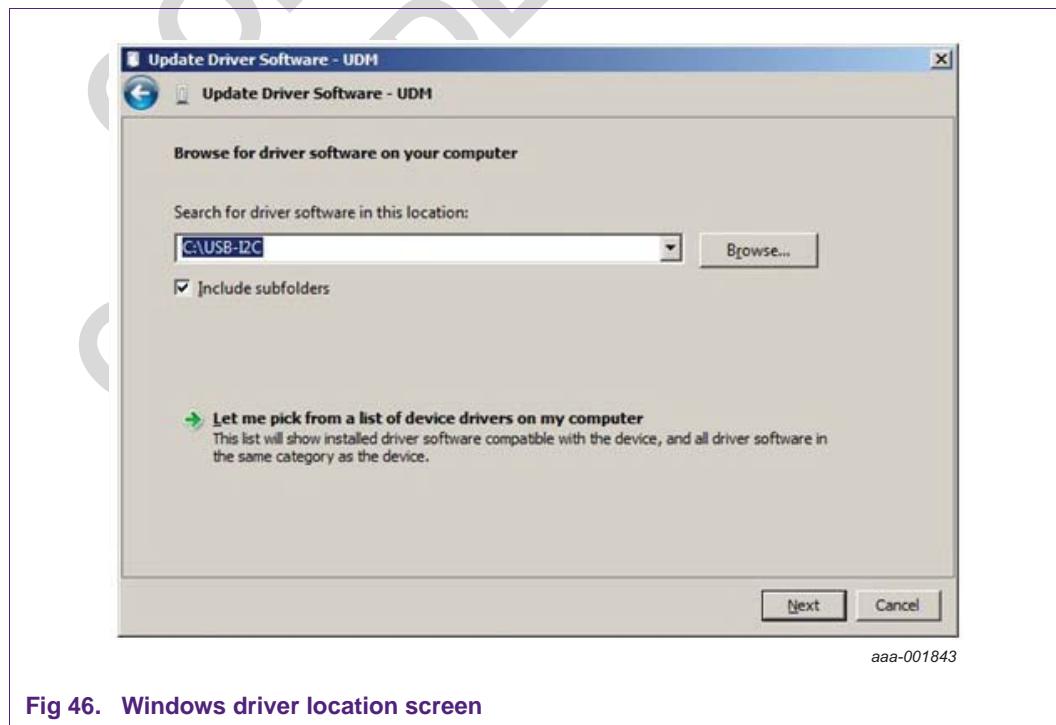


Fig 46. Windows driver location screen

- Enter the driver location in the "Browse" entry field (see [Figure 46](#)) and select "Next" to instigate the driver installation.

- If a warning screen appears (see [Figure 47](#)), ignore the warning and select the lower option “Install this driver software anyway”.

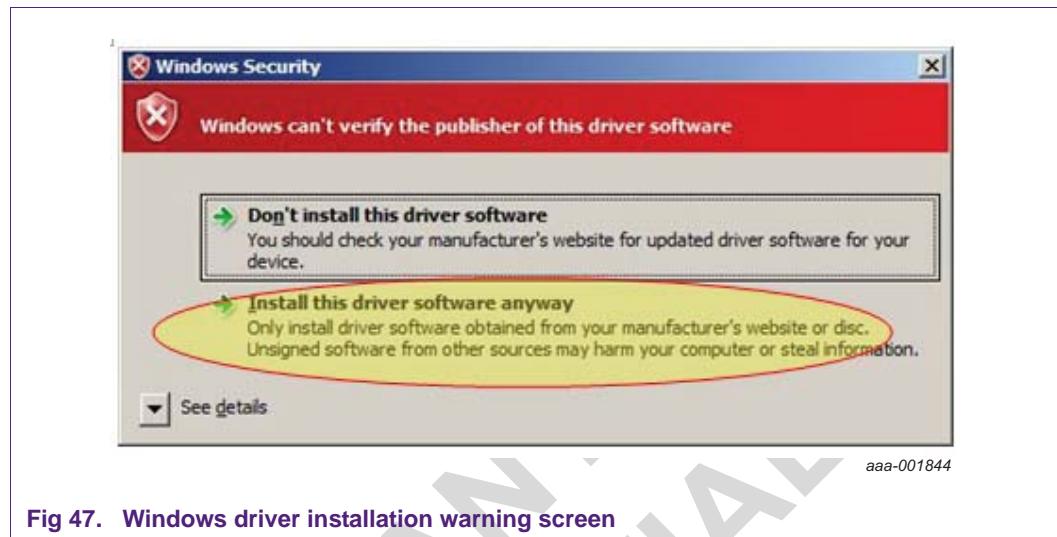


Fig 47. Windows driver installation warning screen

- The driver installation progresses and when fully installed, it opens the screen depicted by [Figure 47](#). Select “Close” to complete the process.

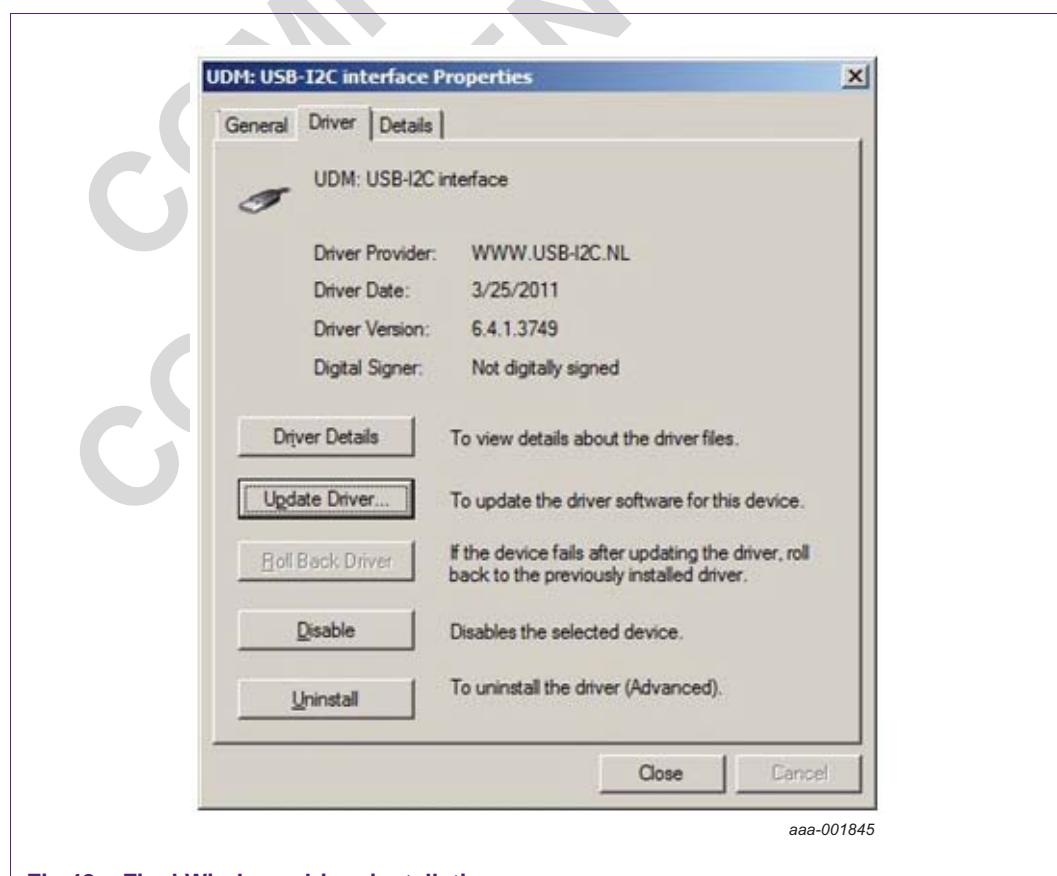


Fig 48. Final Windows driver installation screen

The I<sup>2</sup>C driver is now installed and ready to use. All current applications are written for 32-bit operating systems as is the I<sup>2</sup>C library. All 32-bit programs run under 64-bit operating systems.

## 5.2 I<sup>2</sup>C-bus control software, GUI

NXP Semiconductors provides customers with I<sup>2</sup>C-bus control software that enables amplifier control through I<sup>2</sup>C.

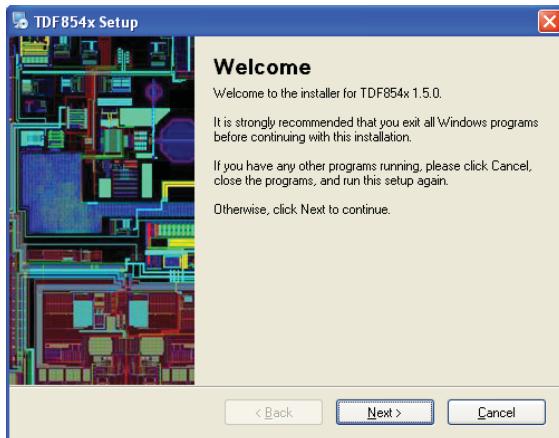
Install the software on a PC or laptop running Windows. The computer and amplifier are interfaced using an I<sup>2</sup>C-bus interface (USM or UDM) that is connected to one of the USB outputs of the computer.

### 5.2.1 Installation

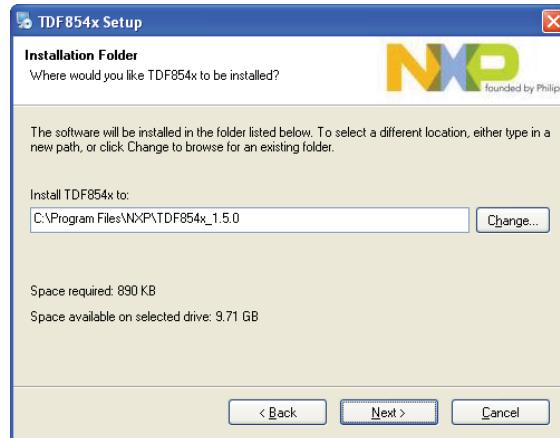
**Remark:** Do not insert a USB-connector before the installation is completed. If a 64-bit driver is already installed, steps g - j are not required.

This section describes the procedure for installing the user interface on a computer.

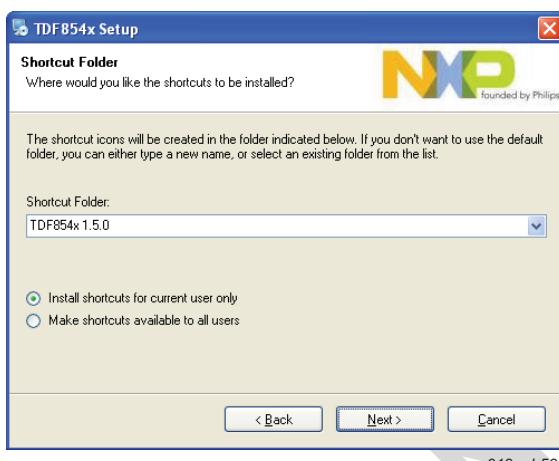
The TDF854x and TDF855x use the same procedure, so only the TDF854x is shown in this example. First, double-click the file TDF854xSetup.zip to unpack the files. After unpacking the file, double-click the TDF854xSetup.exe file, after which the screens depicted in [Figure 49](#) appear:



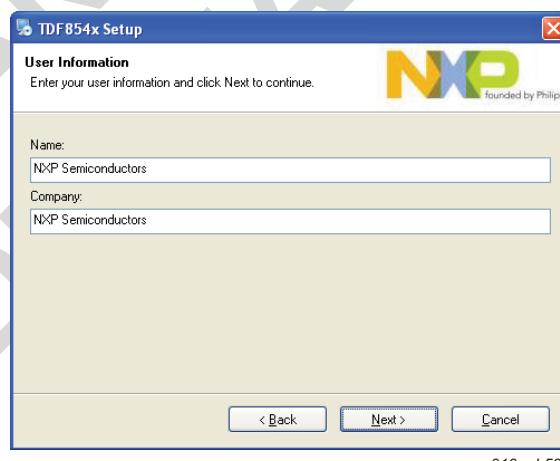
a. Click "Next>"



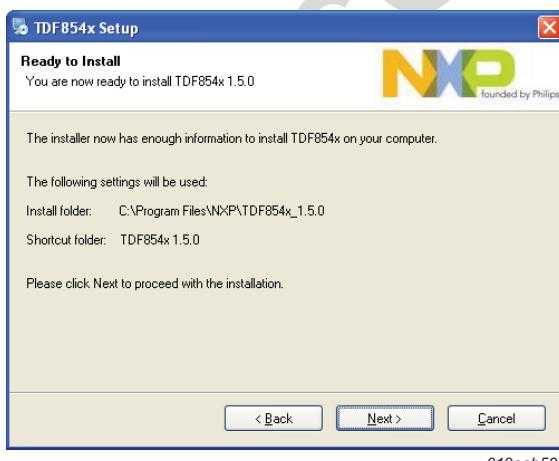
b. Select target folder and click "Next>"



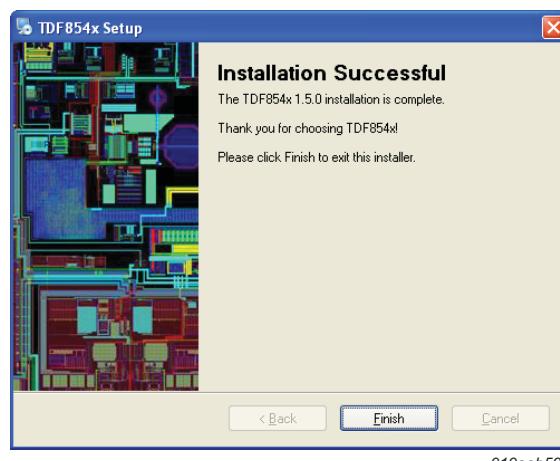
c. Click "Next>"



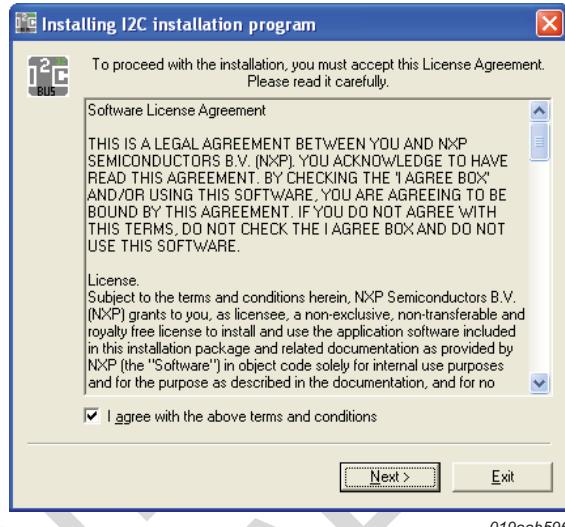
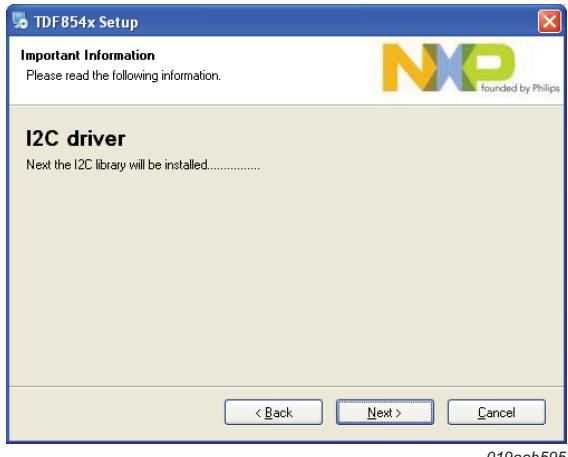
d. Click "Next>"



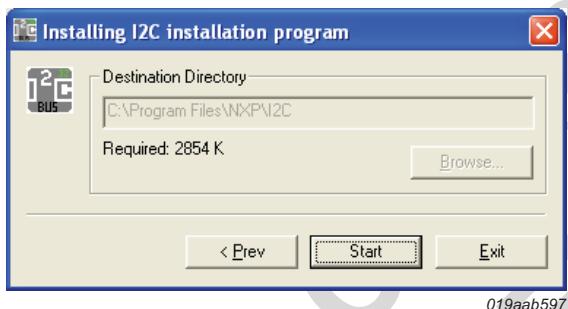
e. Click "Next>"



f. Software installed, click "Finish"



g. The driver is now installed, click "Next>"



i. Click "Start"

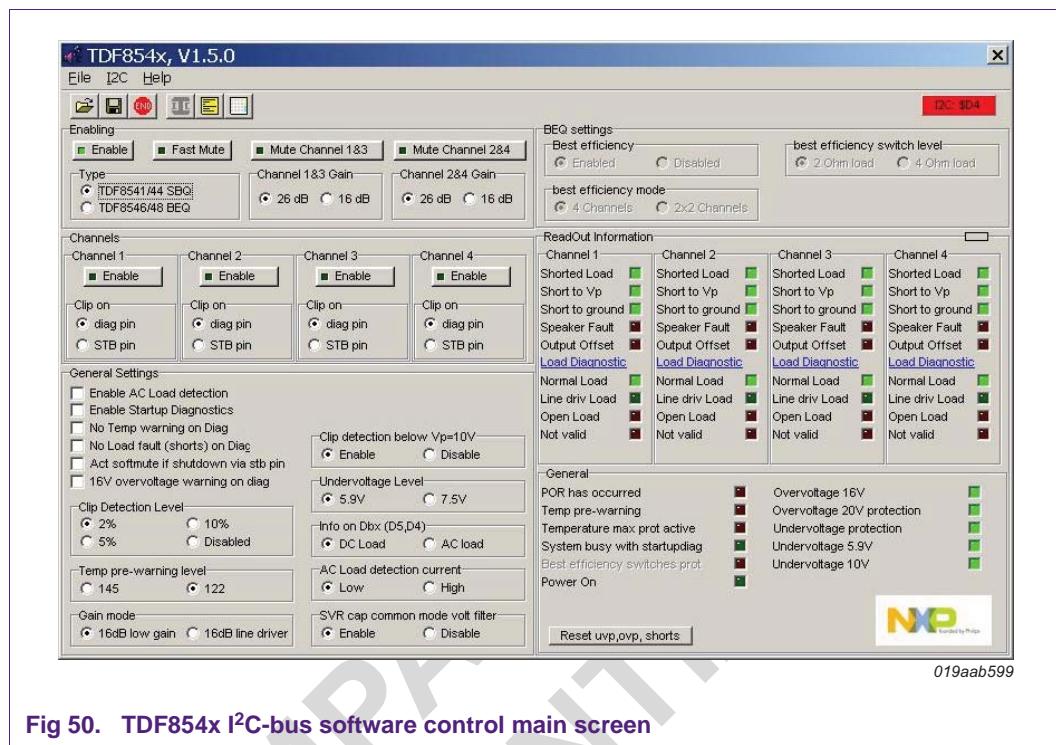


j. Driver installed successfully, click "OK" to load the interface, see [Section 5.2.2](#)

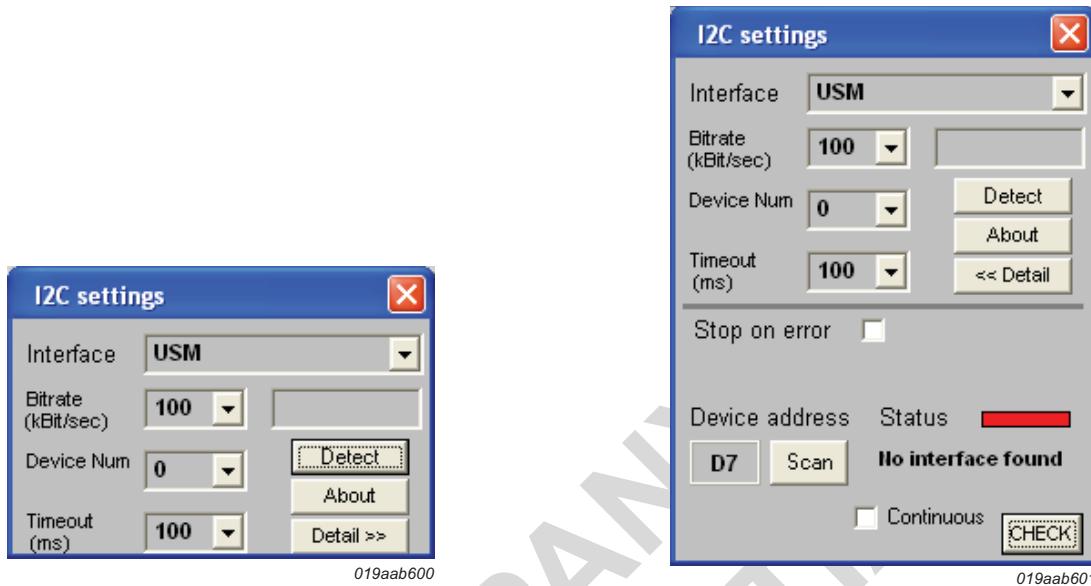
**Fig 49. User interface installation**

### 5.2.2 GUI operation

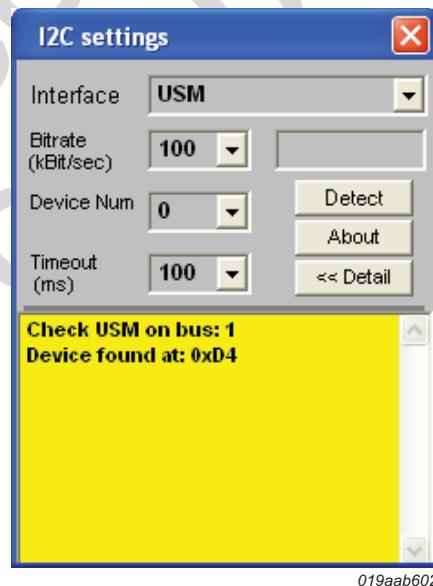
After the software has been installed, the interface is connected to a free USB connector on the computer. The 4-wired cable is connected between the interface and the application board.

Fig 50. TDF854x I<sup>2</sup>C-bus software control main screen

Choose the appropriate I<sup>2</sup>C-address as follows:



- Click "I2C", then "configuration" and then on button "Detect". It searches for a connected USB interface, depending on the connection, "USM" or "UDM" appears in the Interface field. Click the button "Detail" and a new screen appears.
- Click the button "Scan" to display the selected (hardware) address of the connected amplifier in the left box, while the Status bar turns green.



- Close the window by clicking the "x" in the top right corner.

**Fig 51. I<sup>2</sup>C-address selection**

The main screen reappears and the I<sup>2</sup>C-address is inserted in the top right box, by clicking it with the right-hand mouse button.

When the box turns green, communication with the amplifier has succeeded.

If it remains red, something is incorrect, for example:

- The connected amplifier has no supply voltage
- 4-wired I<sup>2</sup>C-cable is not properly connected
- There is no 5 V present on the I<sup>2</sup>C-connector

[Figure 52](#) provides a representation of the GUI for the TDF855x.

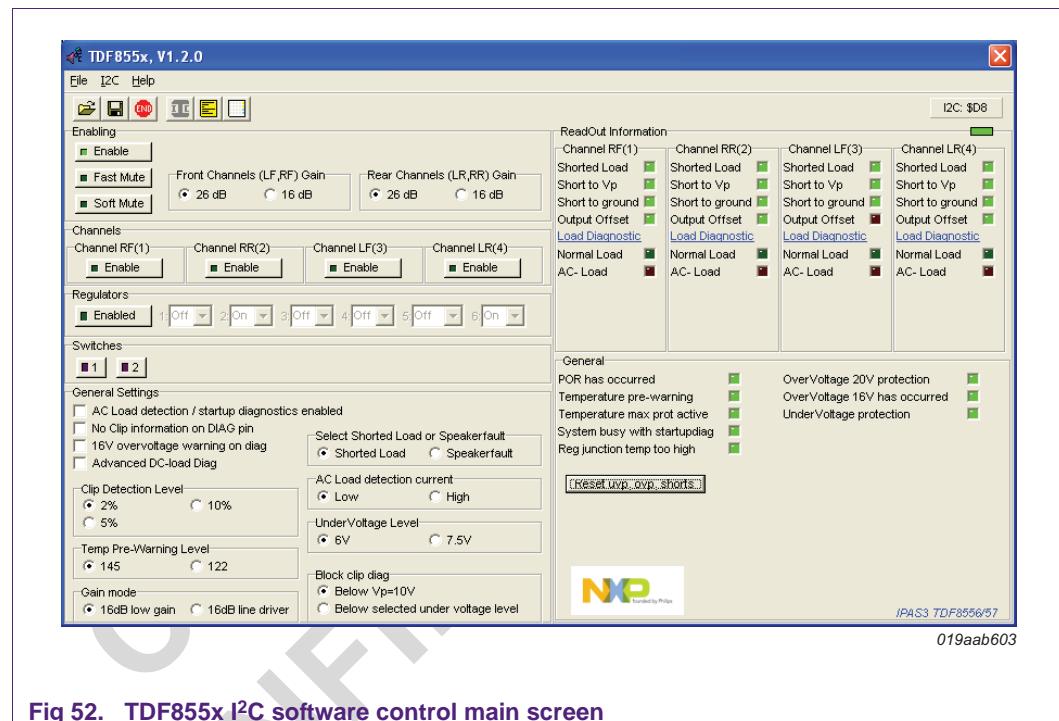


Fig 52. TDF855x I<sup>2</sup>C software control main screen

## 6. Abbreviations

**Table 12. Abbreviations**

Acronym	Description
AM/FM	Amplitude Modulation/Frequency Modulation
BB	Broad Band
BOM	Bill Of Material
BTL	Bridge-Tied Load
CMRR	Common-Mode Rejection Ratio
DMOS	Diffusion Metal-Oxide Semiconductor
DSP	Digital Signal Processor
EMI	ElectroMagnetic Interference
EMC	ElectroMagnetic Compatibility
GUI	Graphical User Interface
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
HF	High Frequency
NB	Narrow Band
PCB	Printed-Circuit Board
POR	Power-On Reset
RMS	Root Mean Square
SMD	Surface Mounted Device
SOAR	Safe Operating ARea
SOI BCD	Silicon On Isolator Bipolar Complementary Diffused
SPDT	Single Pole Double Throw
SVRR	Supply Voltage Ripple Rejection
UDM	USB Dual Master
USB	Universal Serial Bus
USM	USB Single Master

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