GOC-Q71007W

Bluetooth Module Specification

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Be careful:

1. The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.

2. Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.

Release Record

Version Number	Release Date	Comments
V1.0	2019/08/21	Initial draft

Contents

1. Introduction

The GOC-Q71007W is a single-chip flash programmable dual mode Bluetooth v5.0 device with integrated application processor, low-power audio DSP, on-chip ROM and RAM, stereo codec, battery charger, switch-mode and linearregulators, and LED drivers.

The GOC-Q71007W on-chip ROM includes Bluetooth HCI lower and upper stack, and the audio DSP application withthe end product application and user interface in external flash programmable memory.

The GOC-Q71007W device, the 1-mic hands-free stereo speaker application (binary image and source code), IDE,and configuration tools provide a flexible and powerful platform for developing Bluetooth audio products with fasttime to market.

GOC-Q71007W can be the same with instructions of A2DP V1.3.1 AVRCP V1.6 HFP V1.7 HSP V1.2 SPP V1.2 DIDV1.3 HOGP V1.0 PXP V1.0.1 FMP V1.0 BAS V1.0 and so on, and is easy to apply the module into your own product design.

In addition,GOC-Q71007W can help users to customize soft well based on abundance in extra soft well design.

1.1 Module Block Diagram

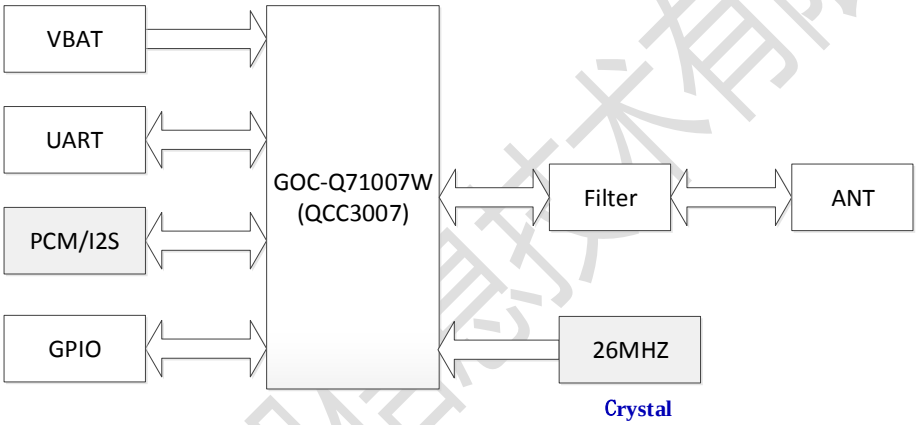

Figure 1: Module Block Diagram

1.2 Features

- Bluetooth v5.0 specification compliant
- Dual Mode Bluetooth
- Dual Mode Topoloy
- Link Layer Topoloy
- Supports Multiple BR/EDR and Bluetooth Low Energy connection scenarios
- 9 dBm (typ) RF transmit power
- -92 dBm (typ) π/4 DQPSK receiver sensitivity and -82.0 dBm(typ) 8DPSK receiver sensitivity
- Bluetooth Radio
  Dual Mode(BR/EDR/LE) internal Balun
  RF Tx:+9dBm
  RF Rx:-91dBm
- Qualcomm® Bluetooth® Low Energy secure connection
- Qualcomm®cVc™ noise reduction technology Mic/ Generation
- Qualcomm®aptX™ audio/aptX Low Latency
- Bluetooth Profiles
  A2DP V1.3.1
  AVRCP V1.6

HFP V1.7
HSP V1.2
SPP V1.2
DIDV1.3
HOGP V1.0
PXP V1.0.1
FMP V1.0
BAS V1.0

- Stereo audio of SBC and AAC audio codecs
- Decoders
- Qualcomm TrueWireless™ Stereo
- Use Cases
  Concurrent A2DP and Android/iOS L APP LE connections
  Background over-the-air software uodate

- Over the air Update
- Voice Prompt Updates
- LE Secure Connections
- Dual I^2S outputs
- I^2S input, SPDIF input (uncompressed PCM only)
- Fully configurable EQ: 6 banks for music enhancement; 1 bank for speaker
- Serial interfaces: UART
- USB 2.0 (full-speed) interface
- Operating Voltage : VBAT : 3.13 to 3.46V
- GPIO Voltage:3.30V
- Dimension 19.80mm *14.80mm * 2.38mm(H)
- Stamp-51 package module suitable for Surface Mounted Technology (SMT)
- Green (RoHS compliant and noantinomy or halogenated flame retardants)

1. 3 Application

- Stereo speakers
- Speakerphones
- TVs
- Smart remote controllers
- Wired or wireless soundbars
- Wired or wireless speakers and headphones
- Wearable audio with sensors (health and well-being applications)
- Wired or wireless speakers
- Wired or wireless speakerphones

- Mono headsets for voice
- Stereo headsets
- Wired stereo headsets and headphones

2. Main Specification Instruction

Production	Bluetooth Module
Type	GOC-Q71007W
Standard	Bluetooth V5.0
IC	QCC3007
Frequency Range	2402~2480MHz
Modulation Method	GFSK, π/4-DQPSK,8DPSK
Max Speed For Transfer	Asynchronous: 723.2Kbps/57.6Kbps Synchronous: 433.9Kbps/433.9Kbps
Hop	1600hops/sec, 1MHz Channel Space
Output Impedance	50 Ohms
Crystal Frequency	26MHz
Outer Interface	UART, PIO, SPI,PCM,USB,I2S Speaker, Microphone
Apply To Bluetooth Instructions	A2DP V1.3.1 AVRCP V1.6 HFP V1.7 HSP V1.2 SPP V1.2 DIDV1.3 HOGP V1.0 PXP V1.0.1 FMP V1.0 BAS V1.0
Range For Working Distance	10 meters
Receiving Sensitivity	-92dBm π/4 DQPSK -82dBm 8DPSK
Transmit Power	9dBm
Size	19.80mm *14.80mm * 2.38mm
Power Voltage	3.30 V Supply Voltage Typically
Working Current	<25mA
Standby Current	<63uA
Storage Temperature	-40℃ to +105℃
Temperature Range	-40℃ to +85℃
Humidity Range	10%~90% Non-Condensing

Table 1: Main Specifications

3. Pin Diagram And Description

3.1 Pin Diagram

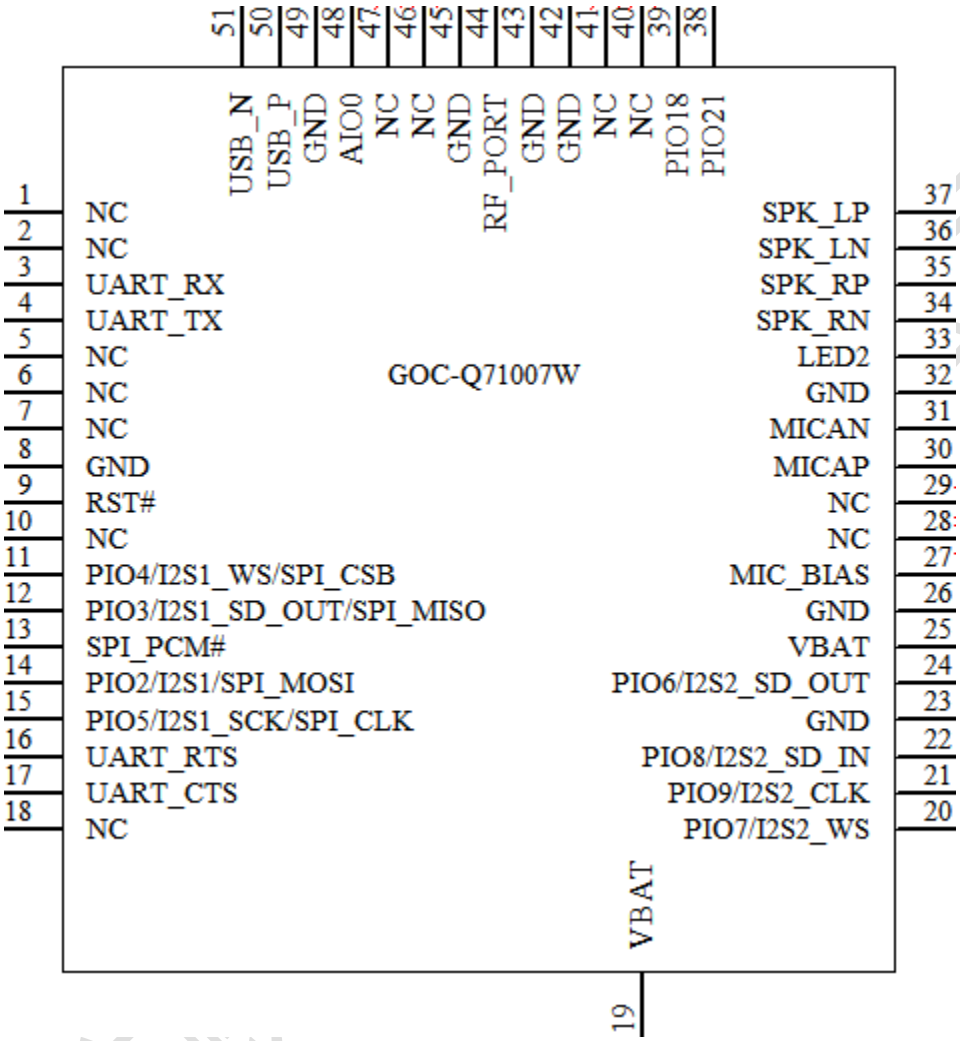

Figure2: Pin Diagram

3.2 Pin Definition

Pin	Pin Name	Pad Type	Description
1	NC	NC	NOT CONNECTED
2	NC	NC	NOT CONNECTED
3	UART_RX	Bidirectional with strong pull-up	UART data input
4	UART_TX	Bidirectional with strong pull-up	UART data output
5	NC	NC	NOT CONNECTED
6	NC	NC	NOT CONNECTED
7	NC	NC	NOT CONNECTED

8	GND	GND	Ground connections
9	RST#	input / output	Reset if low, Pull low for minimum 5ms to cause a reset
10	NC	NC	NOT CONNECTED
11	PIO4/I2S1_WS/SPI_CSB	input / output	SPI_CSB: chip select for SPI I2S1_WS: I2S synchronous data sync PIO4:Programmable input / output line 4
12	PIO3/I2S1_SD_OUT/SPI_MISO	input / output	SPI_MISO: SPI data output I2S1_SD_OUT: I2S synchronous data output PIO3:Programmable input / output line 3
13	SPI_PCM#	input / output	0 = PCM1/PIO interface 1 = SPI
14	PIO2/I2S1_IN/ SPI_MOSI	input / output	SPI_MOSI: SPI data input I2S1: I2S synchronous data input PIO2:Programmable input / output line 2
15	PIO5/I2S1_SCK/ SPI_CLK	input / output	SPI_CLK: SPI clock I2S1_SCK: I2S synchronous data clock PIO5:Programmable input / output line 5
16	UART_RTS	Bidirectional with strong pull-up	UART request to send, active low
17	UART_CTS	Bidirectional with strong pull-down	UART clear to send, active low
18	NC	NC	NOT CONNECTED
19	VBAT	POWER	3.3V Supply voltage
20	PIO7/I2S2_WS	input / output	PIO7:Programmable input / output line 7 I2S2_WS: I2S2 synchronous data sync
21	PIO9/I2S2_CLK	input / output	PIO9:Programmable input / output line 9 I2S2_SCLK:I2S2 synchronous data clock
22	PIO8/I2S2_SD_IN	input / output	PIO8:Programmable input / output line 8 I2S2_SD_IN: I2S2 synchronous data input
23	GND	GND	Ground connections
24	PIO6/I2S2_SD_OUT	input / output	PIO6:Programmable input / output line 6 I2S2_SD_OUT: I2S2 synchronous data output
25	VBAT	POWER	3.3V Supply voltage
26	GND	GND	Ground connections
27	MIC_BAIS	Analogue out	Microphone bias
28	NC	NC	NOT CONNECTED
29	NC	NC	NOT CONNECTED
30	MICAP	Analog in	Microphone input positive,channel A
31	MICAN	Analog in	Microphone input negative,channel A

32	GND	GND	Ground connections
33	LED2	Bidirectional	Open-drain output
34	SPK_RN	Analog out	Speaker output negative, right
35	SPK_RP	Analog out	Speaker output positive, right
36	SPK_LN	Analog out	Speaker output negative, left
37	SPK_LP	Analog out	Speaker output positive, left
38	PIO21	Bidirectional with strong pull-down	Programmable input/output line
39	PIO18	Bidirectional with strong pull-down	Programmable input/output line
40	NC	NC	NOT CONNECTED
41	NC	NC	NOT CONNECTED
42	GND	GND	Ground connections
43	GND	GND	Ground connections
44	RF_PORT	RF	Connect an external antenna
45	GND	GND	Ground connections
46	NC	NC	NOT CONNECTED
47	NC	NC	NOT CONNECTED
48	AIO0	Bidirectional	Analog programmable input
49	GND	GND	Ground connections
50	USB_P	Bidirectional	USB data plus with selectable internal 1.5 kΩ pull-up resistor
51	USB_N	Bidirectional	USB data minus

Table2:Pin Description

3.3 PCB Layout Footprint

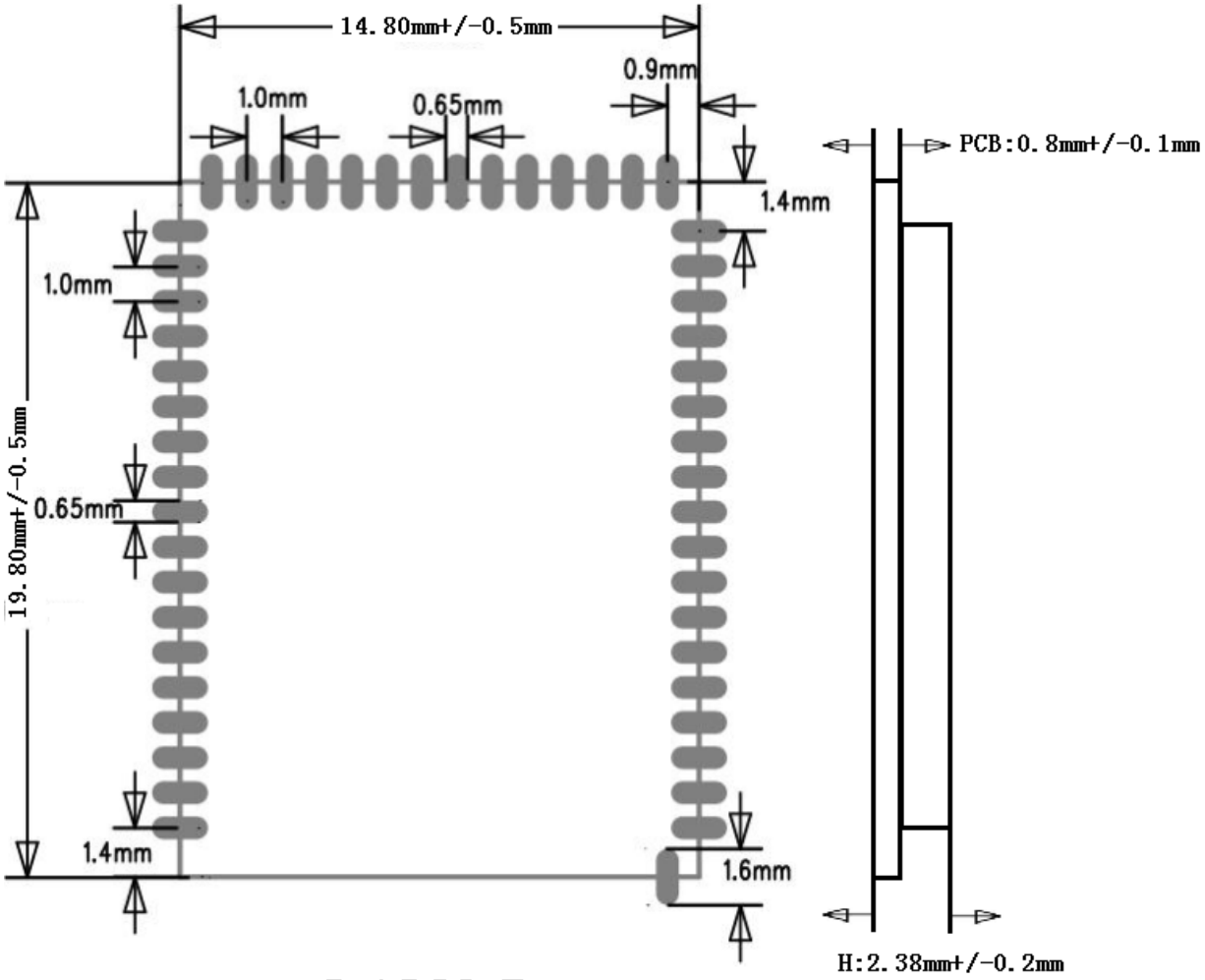

Figure 3: GOC-Q71007W PCB Layout Footprint

4. UART Interface

GOC-Q71007W has a UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug. The UART interface is multiplexed with PIOs and other functions, and hardware flow control is optional.

PS Keys for UART/PIO multiplexing

PS Key	PIO location
UART_RX	PIO[0]
UART_TX	PIO[1]
UART_RTS	PIO[8] or PIO[16]
UART_CTS	PIO[9] or PIO[17]

shows the 4 signals that implement the UART function

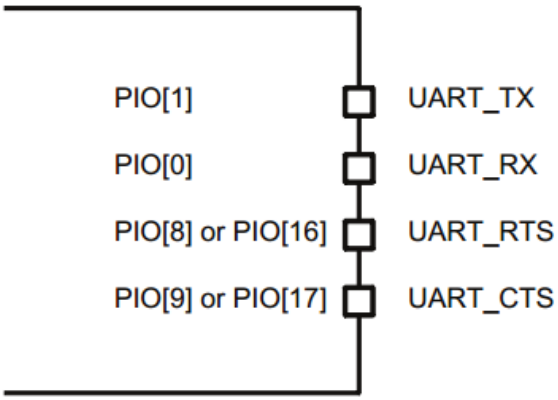

Figure 4:Universal asynchronous receiver

When GOC-Q71007W is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using the GOC-Q71007W firmware.

Possible UART settings

Parameter		**Possible values**
Baud rate	Minimum	1200 baud (≤ 2% Error)
		9600 baud (≤ 1% Error)
	Maximum	4 M baud (≤ 1% Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table3:Possible UART settings

Standard baud rates

Baud rate	**Error**
1200	1.73%
2400	1.73%
4800	1.73%
9600	-0.82%
19200	0.45%
38400	-0.18%
57600	0.03%
76800	0.14%
115200	0.03%
230400	0.03%
460800	-0.02%
921600	0.00%
1382400	-0.01%
1843200	0.00%
2764800	0.00%
3686400	0.00%

Table4:Standard baud rates

5. PCM Imterface

The PCM Interface on the GOC-Q71007W can connect to linear PCM Codec devices in master or slave mode. In master mode,the GOC-Q71007W generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the GOC-Q71007W.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The GOC-Q71007W supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The GOC-Q71007W supports both short- and long-frame synchronization in both master and slave modes. In shortframe synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The GOC-Q71007W may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the GOC-Q71007W uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

PCM Interface Timing

Short Frame Sync, Master Mode

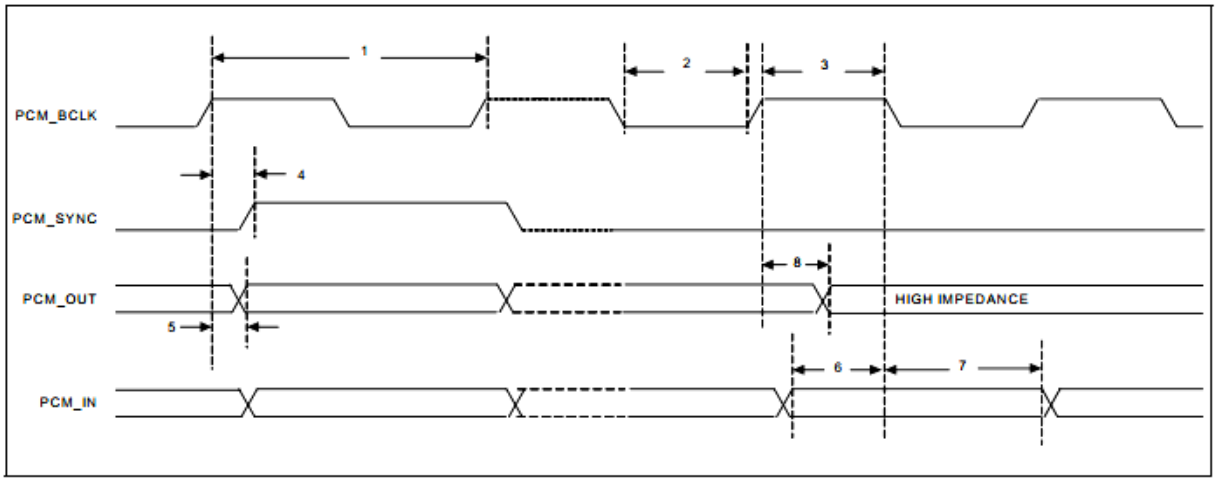

Figure 5:PCM Timing Diagram (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	**12**	MHz
2	PCM bit clock LOW	**41**	-	-	ns
3	PCM bit clock HIGH	**41**	-	-	ns
4	PCM_SYNC delay	**0**	-	**25**	ns
5	PCM_OUT delay	**0**	-	**25**	ns
6	PCM_IN setup	**8**	-	-	ns
7	PCM_IN hold	**8**	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	**0**	-	**25**	ns

Table5:PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Short Frame Sync, Slave Mode

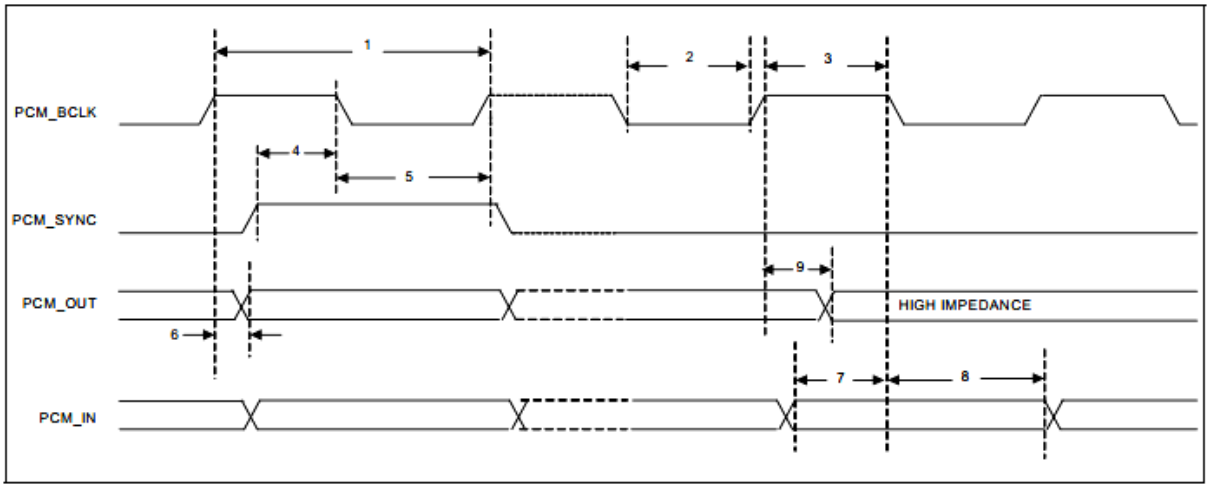

Figure6:PCM Timing Diagram (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	**12**	MHz
2	PCM bit clock LOW	**41**	-	-	ns
3	PCM bit clock HIGH	**41**	-	-	ns
4	PCM_SYNC setup	**8**	-	-	ns
5	PCM_SYNC hold	**8**	-	-	ns
6	PCM_OUT delay	**0**	-	**25**	ns
7	PCM_IN setup	**8**	-	-	ns
8	PCM_IN hold	**8**	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	**0**	-	**25**	ns

Table 6: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Long Frame Sync, Master Mode

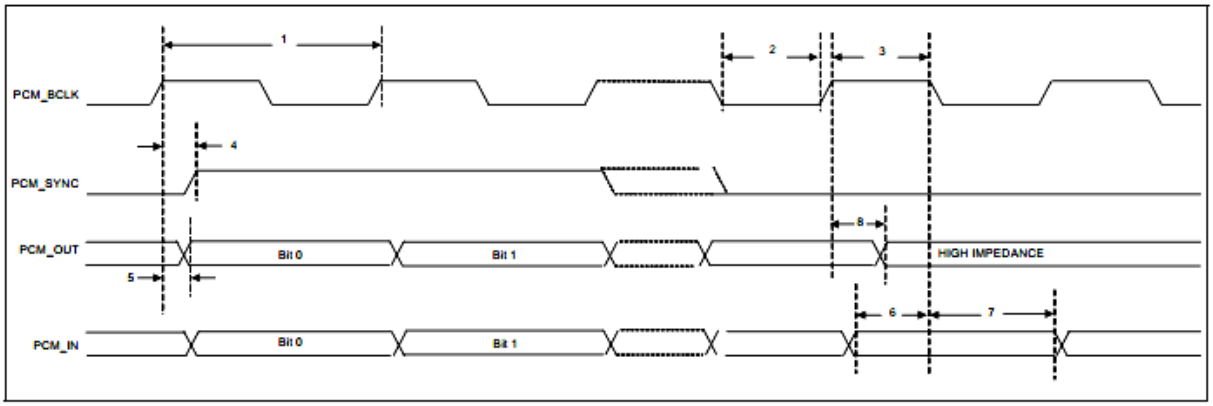

Figure 7: PCM Timing Diagram (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	**12**	MHz
2	PCM bit clock LOW	**41**	-	-	ns
3	PCM bit clock HIGH	**41**	-	-	ns
4	PCM_SYNC delay	**0**	-	**25**	ns
5	PCM_OUT delay	**0**	-	**25**	ns
6	PCM_IN setup	**8**	-	-	ns
7	PCM_IN hold	**8**	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	**0**	-	**25**	ns

Table 7: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Long Frame Sync, Slave Mode

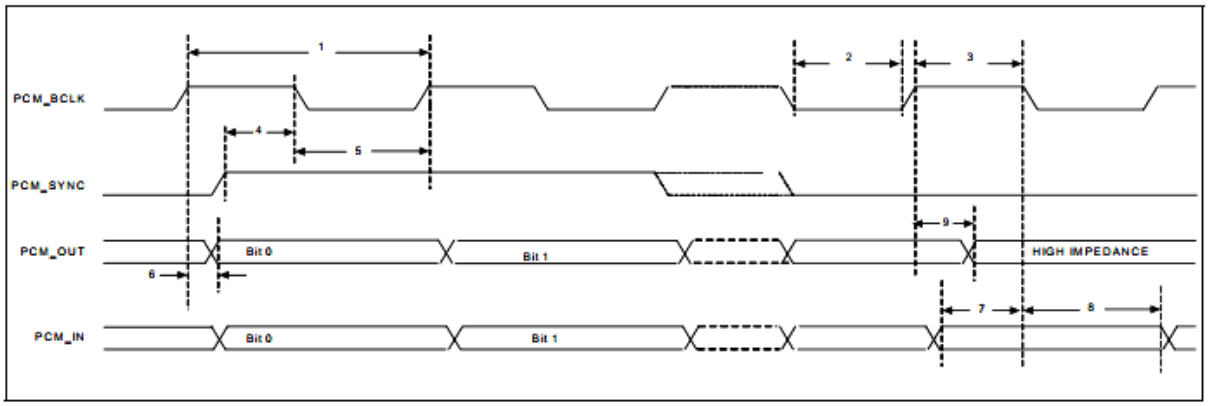

Figure 8: PCM Timing Diagram (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	**12**	MHz
2	PCM bit clock LOW	**41**	-	-	ns
3	PCM bit clock HIGH	**41**	-	-	ns

4	PCM_SYNC setup	**8**	-	-	ns
5	PCM_SYNC hold	**8**	-	-	ns
6	PCM_OUT delay	**0**	-	**25**	ns
7	PCM_IN setup	**8**	-	-	ns
8	PCM_IN hold	**8**	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	**0**	-	**25**	ns

Table 8: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Short Frame Sync, Burst Mode

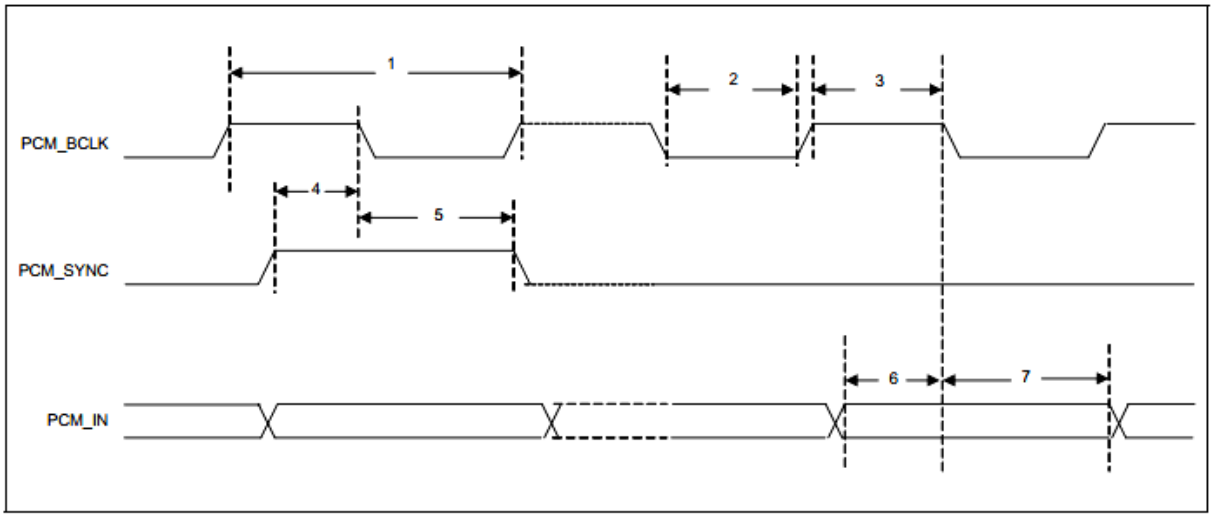

Figure 9: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	**24**	MHz
2	PCM bit clock LOW	**20.8**	-	-	ns
3	PCM bit clock HIGH	**20.8**	-	-	ns
4	PCM_SYNC setup	**8**	-	-	ns
5	PCM_SYNC hold	**8**	-	-	ns
6	PCM_OUT delay	**8**	-	-	ns
7	PCM_IN setup	**8**	-	-	ns
8	PCM_IN hold	**8**	-	-	ns

Table 9: PCM Burst Mode (Receive Only, Short Frame Sync)

Long Frame Sync, Burst Mode

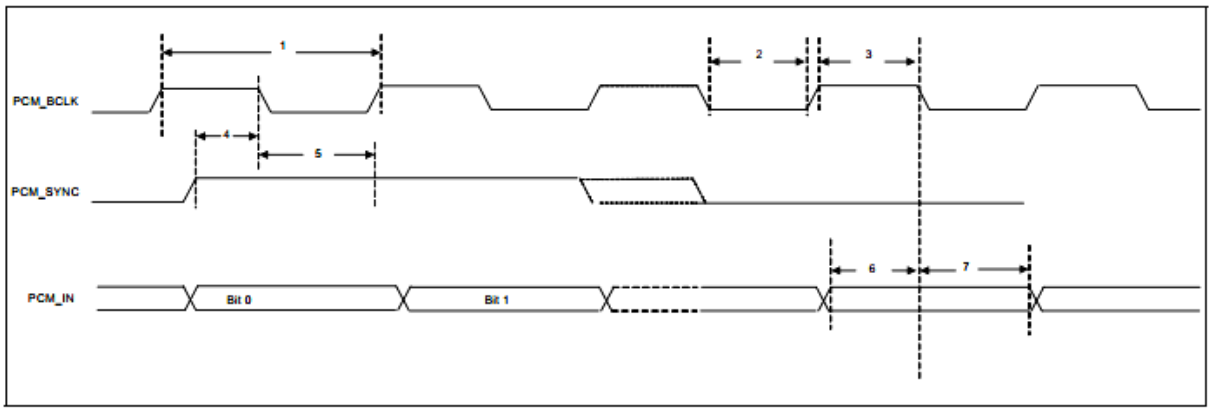

Figure 10: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	8	-	-	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns

Table 10: PCM Burst Mode (Receive Only, Long Frame Sync)

6.USB Interface

GOC-Q71007W has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on GOC-Q71007W acts as a USB peripheral, responding to requests from a master host controller.

GOC-Q71007W contains internal USB termination resistors and requires no external resistors.

GOC-Q71007W supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification), supports USB standard charger detection, and fully supports the USB Battery Charging Specification v1.2. For more information on how to integrate the USB interface on GOC-Q71007W, see the Bluetooth and USB Design Considerations Application Note.

As well as describing USB basics and architecture, the application note describes:

- USB Audio
- DFU

7. I2S Interface

GOC-Q71007W supports I2S input and output via the industry-standard I2S digital audio interface, left-justified or right-justified.

In this section, terms are defined as follows:

I2S_SDI I2S_SDO I2S_WS I2S_SCK

GOC-Q71007W also supports several alternative PCM data formats. For further details, contact Goodocom. When in PCM mode, the following pin name to function mappings apply.

I2S pin	PCM function
I2S_SDI	PCM_IN
I2S_SDO	PCM_OUT
I2S_WS	PCM_SYNC
I2S_SCK	PCM_CLK

Shows the timing diagram for the I²S interface

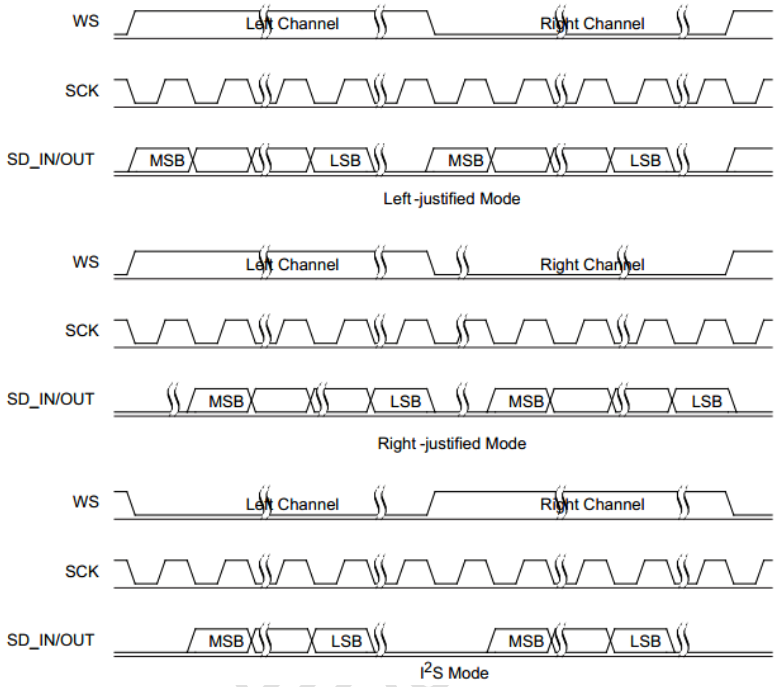

Figure 11: Shows the timing diagram for the I² S interface

The internal representation of audio samples within the GOC-Q71007W is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
–	SCK Frequency	–	–	6.2	MHz
–	WS Frequency	–	–	96	kHz
t_{ch}	SCK high time	80	–	–	ns
t_{cl}	SCK low time	80	–	–	ns

Table 11: Digital audio interface slave timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	–	–	ns
t_{sh}	SCK high to WS invalid hold time	2.5	–	–	ns
t_{opd}	SCK low to SD_OUT valid delay time	–	–	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	–	–	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	–	–	ns

Table 12: I²S slave mode timing

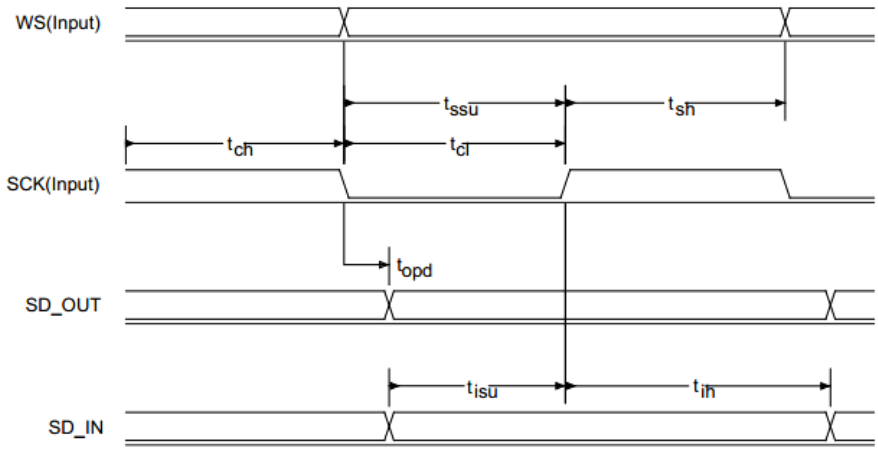

Figure12:Digital audio interface slave timing

Symbol	Parameter	Min	Typ	Max	Unit
–	SCK Frequency	–	–	6.2	MHz
–	WS Frequency	–	–	96	kHz

Table 13 Digital audio interface master timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	–	–	39.27	ns
t_{opd}	SCK low to WS valid delay time	–	–	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	–	–	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	–	–	ns

Table 14 I²S master mode timing parameters, WS and SCK as outputs

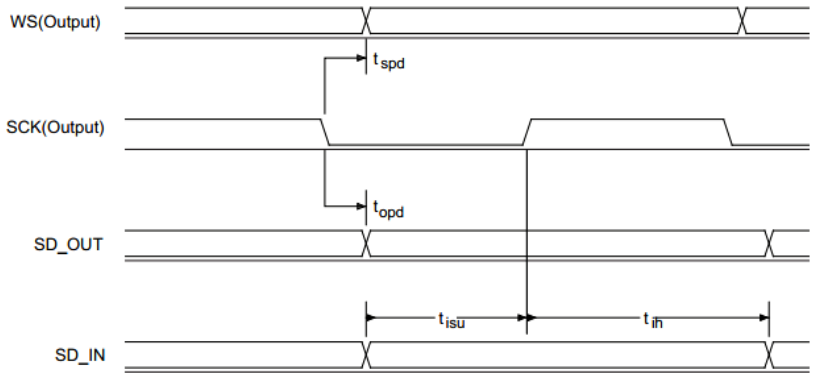

Figure13: Digital audio interface master timing

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Rating	Min	Typical	Max
VBAT	3.10V	3.30V	3.60V

Table 15: Absolute Maximum Ratings

8.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max
Storage Temperature	-40℃	/	+105℃
OperatingTemperature	-40℃	20℃	+85℃
VBAT	3.14V	3.30V	3.46V

Table 16: Recommended Operating Conditions

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ≦260℃

Number of Times : 2 times

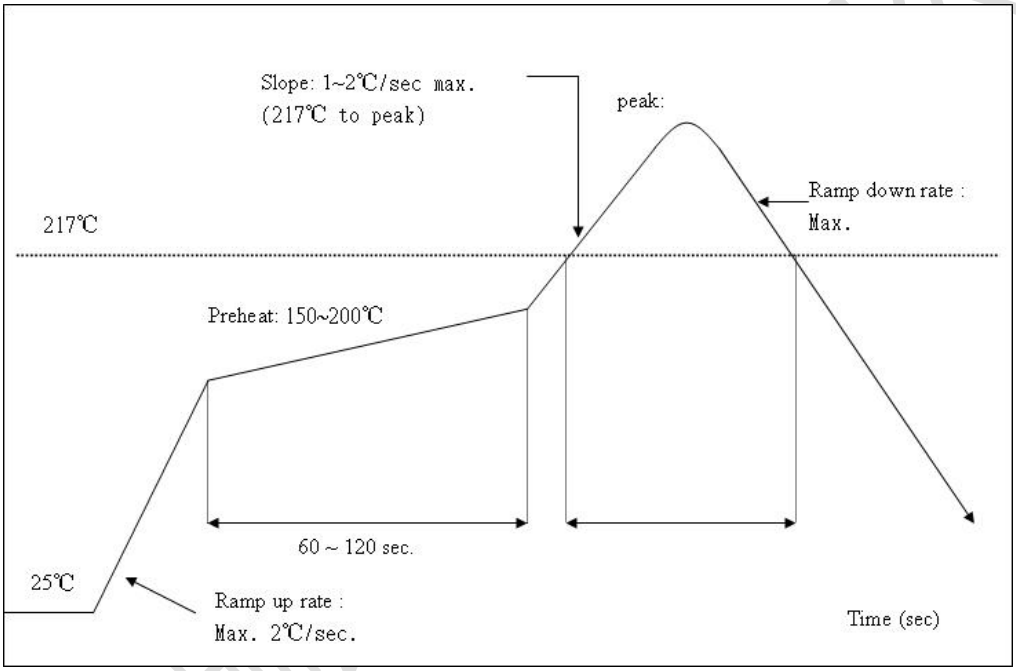

Figure14:Solder Reflow Profile

10. PCB Layout Recommendation

10.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above(or under)the RF antenna trace should be free from other traces.

10.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX UART_TX UART_CTS UART_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

10.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA

PCM_SYNC PCM_CLK PCM_OUT PCM_IN
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

10.4 Power Trace Lines Layout Guideline

- VBAT Trace Width: 20mil

10.5 Ground Lines Layout Guideline

- A Complete Ground in Ground Layer.
- Add Ground Through Holes to GOC-Q71007W Module Ground Pads
- Decoupling Capacitors close to GOC-Q71007W Module Power and Ground Pads

11. Module Part Number Description

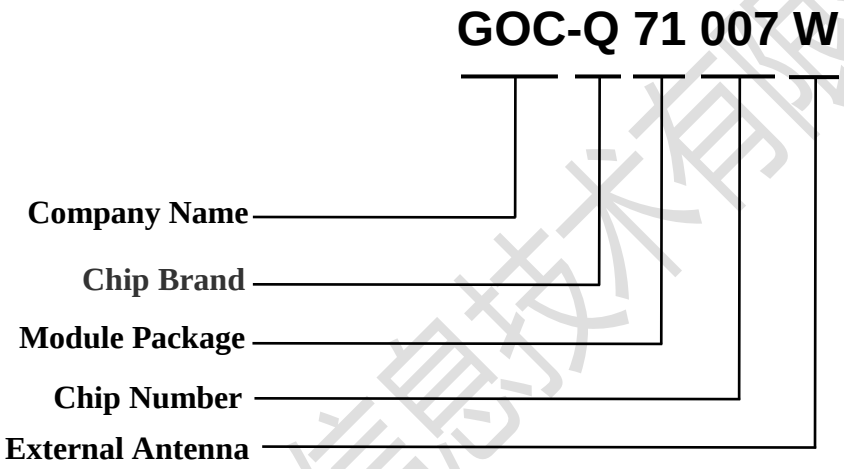

Figure15: Ordering information

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to *www.goodocom.com* or contact the GOODOCOM Sales Office nearest to you.

12. Ordering Information

Part Number	Description	Remark
GOC-Q71007W V1.0	Bluetooth Module	

Table 13: Ordering information

13. Packaging Information

13.1 Net Weight

The module net weight: TBD

13.2 Package

TBD

13.3 Storage Requirements

1）Temperature: 22~28℃;

2 ）Humidity: <70%（ RH）;

Vacuum packed and sealed in good condition to ensure 12 months of welding.

13.4 Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).

3） Handling, storage, and processing should follow JEDEC J-STD-020