i1107e Datasheet

May 03, 2018

Version 1.0

VERSION HISTORY

REVISION	AMENDMENT	DATE	AUTHOR
1.0	Initial version	2018-05-03	wuting

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i1107e *Bluetooth* module

Introduction

IVT has announced the latest *Bluetooth* HCI high-end HCI automotive solution.

i1107e is one of i-series products . i1107e is compatible with *Bluetooth* specification version 5.0 dual mode. It integrates hardware echo cancellation (latest CVC), stereo decoder, *Bluetooth* controller, etc., a completed *Bluetooth* subsystem for Car Kit. i1107e product supports HS/HF, A2DP, AVRCP, PBAP, SPP Profiles,MAP,GATT. It provides UART interface, stereo speaker outputs, microphone inputs and power.

i1107e can be programming through AUDSDK or AT CMD interface for Car Kit application.

Compatible phones

i1107e supports the mainly phones. Such as iPhone, Android, Nokia, Sony Ericsson, Samsung, Motorola, LG, Blackberry, Oppo, K-touch,MTK, Mstar and Spreadtrum.

MSL grade:

MSL 3

ESD grade:

Human Body Model： H1C

Charged Device Model： C3

Key Features

- Compatible with *Bluetooth* v 5.0 dual mode, class2
- Stereo/Dual-mono codec with 1 microphone inputs and stereo audio output
- CSR's latest 1-mic cVc ® Hands-free algorithm for narrowband and **wideband in-car voice** connections, including wind noise reduction
- Embedded SBC and aptX codec for A2DP
- Analog/Digital audio interfaces , PCM or I2S
- **HID, MFi iAP2 for mirror-link**
- FTP/OPP/SPP, upload and download file with mobile phone
- Support Windows CE 4.2/5.0/6.X, Android 1.5/1.6/2.0/2.1/2.2/3.X/4.X and None-OS

APPLICATIONS

- Automotive
- PDA, PMP, PND,SPEAKER

1. Block Diagram and Descriptions

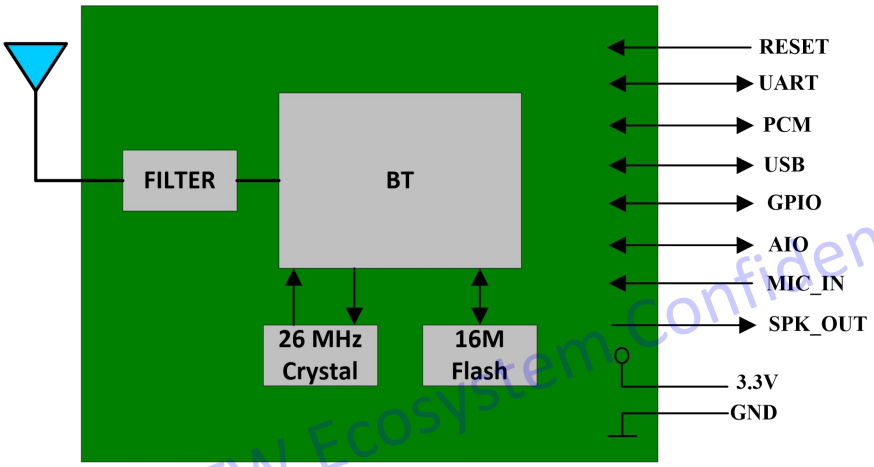


Figure 1 Block Diagram of i1107e

BT

This BT is a highly integrated and sophisticated *Bluetooth*® chip, containing a *Bluetooth* radio, baseband, DAC/ADC, DSP Codec (voice and stereo) and power management in a compact QFN package.

Bluetooth controller implements v5.0 dual mode complaint, *Bluetooth* smart ready.

Crystal

The crystal oscillates at 26MHz.

Balun /filter

Combined balun and filter changes the balanced input/output signal of the module to unbalanced signal of the monopole antenna. The filter is a band pass filter (ISM band).

UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

Antenna

The size of i1107e module is little. So it has no antenna, customer should design an external antenna based on the requirement.

USB

i1107e has a full-speed (12Mbps) USB interface for communicating with other

compatible digital devices. The USB interface on i1107e acts as a USB peripheral, responding to requests from a master host controller.

PCM

There are 2 digital audio interfaces. Each is independently configurable as an I²S or PCM port. The PCM interface also shares the same physical set of pins with the SPI interface.

SPK

The speaker is single output stereo.

MIC

i1107e supports 1 MIC input. External MIC can work.

1-mic cVc hands-free includes a tuning tool enabling the developer to easily adapt cVc with different audio configurations and tuning parameters. The tool provides real-time system statistics with immediate feedback enabling designers to quickly investigate the effect of changes.

RESET

This can be used to reset i1107e.i1107e is equipped with circuitry for generating Power ON Reset form the internal core voltage. A reset is generated when the core voltage falls bellow typically 1.8V and is released when it rises above typically 1.98V.

2.General Characteristics

Table 1 General Characteristics

Product	**BlueLet i-series *Bluetooth* Module**
model	i1107e
***Bluetooth* Specification**	***Bluetooth* v5.0 dual mode, Class II**
Frequency Band	2.4~2.48GHz
Modulation Method	π/4DQPSK,8DPSK
Maximum Data Rate	4Mbps
RF Input Impedance	50 ohms
Crystal OSC	26MHz
Interface	UART, Speaker, Microphone, USB,PCM,GPIO,AIO
Profiles	HS/HF, A2DP, AVRCP, PBAP, SPP Profiles,MAP,GATT
Operation Range	≥10 meters
Sensitivity	87dBm@0.1%BER
Transmit power	7dBm Typ
Connectivity	Point to Multi-Point
Audio Specification	
16-bit DSP w/ Hardware Accelerator	80 MIPs Kalimba DSP coprocessor
Dimension	
Dimension	19.8mm×14.8mm×2.3mm
Shielding case	Yes (The module reserved position of shielded)
Antenna	No
Power	
Supply Voltage	3.0V~3.6V
Consumption power	20mA（A2DP）
Operation Environment	
Temperature	-40ºC to +85ºC
Certifications	
Firmware option	SOC
Application	Automotive

3. PIN diagram and Description

3.1PIN diagram

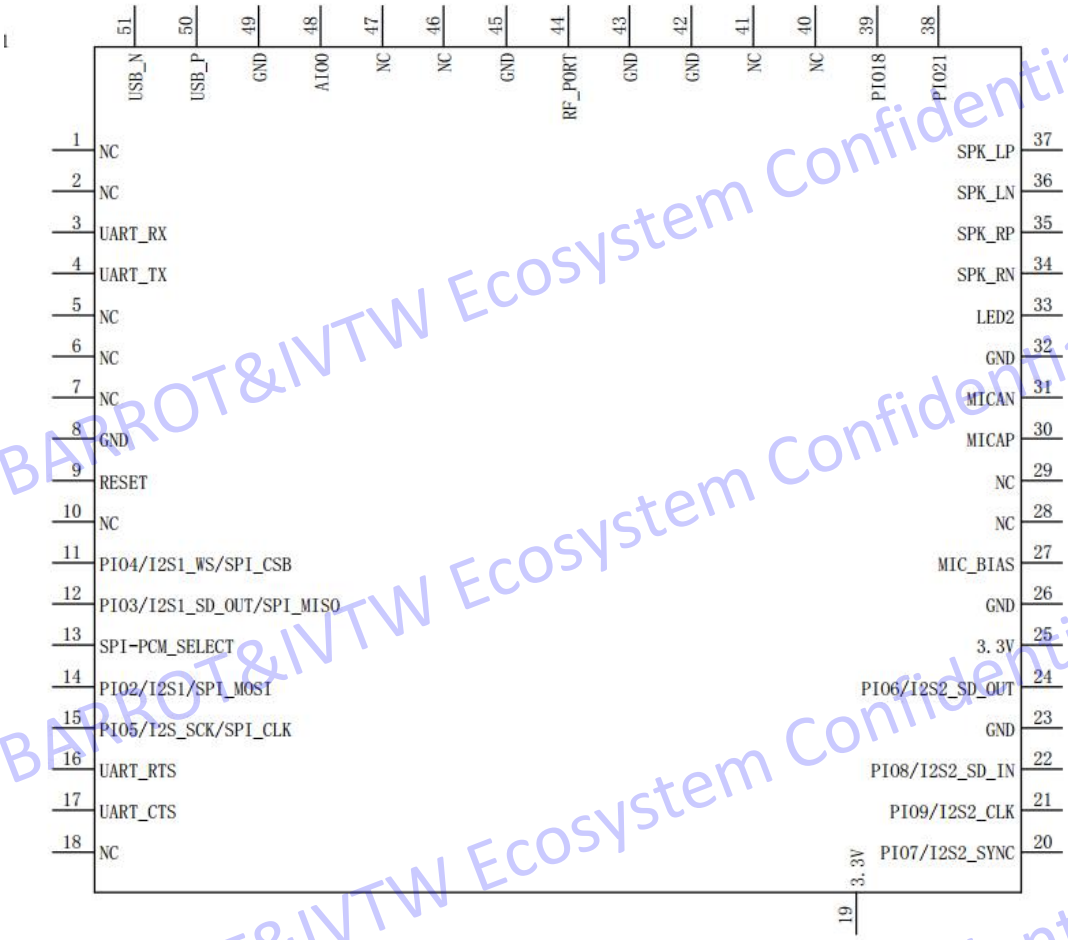


Figure 2 i1107e pin diagram

3.2 PIN Description

i1107e's PIN definition refers to Table 2 below.

Table 2 PIN Description

PIN NO	Pin Name	Descriptions
1	NC	NOT CONNECTED
2	NC	NOT CONNECTED
3	UART_RX	UART DATA INPUT

4	UART_TX	UART DATA OUTPUT
5	NC	NOT CONNECTED
6	NC	NOT CONNECTED PIO12:Programmable input / output line 12
7	NC	NOT CONNECTED
8	GND	Ground
9	RESET	Reset if low, Pull low for minimum 5ms to cause a reset
10	NC	NOT CONNECTED
11	PIO4/PCM1SYNC/SPI_CSB	SPI_CSB: chip select for SPI PCM1SYNC: PCM1 synchronous data sync PIO4:Programmable input / output line 4
12	PIO3/PCM1OUT/SPI_MISO	SPI_MISO: SPI data output PCM1OUT: PCM1 synchronous data output PIO3:Programmable input / output line 3
13	SPI-PCM_SELECT	0 = PCM1/PIO interface 1 = SPI
14	PIO2/PCM1IN/ SPI_MOSI	SPI_MOSI: SPI data input PCM1IN: PCM1 synchronous data input PIO2:Programmable input / output line 2
15	PIO5/PCM1CLK/ SPI_CLK	SPI_CLK: SPI clock PCM1CLK: PCM1 synchronous data clock PIO5:Programmable input / output line 5
16	UART_RTS	UART request to send,
17	UART_CTS	UART clear to send
18	NC	NOT CONNECTED
19	3.3V	3.3V input
20	PIO7/PCM2_SYNC	PIO7:Programmable input / output line 7 PCM2_SYNC: PCM2 synchronous data sync
21	PIO9/PCM2_CLK	PIO9:Programmable input / output line 9 PCM2_CLK: PCM2 synchronous data clock
22	PIO8/PCM2_IN	PIO8:Programmable input / output line 8 PCM2_IN: PCM2 synchronous data input
23	GND	Ground
24	PIO6/PCM2_OUT	PIO6:Programmable input / output line 6 PCM2_OUT: PCM2 synchronous data output
25	3.3V	3.3V input
26	GND	Ground
27	MIC_BIAS	Microphone bias
28	NC	NOT CONNECTED
29	NC	NOT CONNECTED
30	MICAP	Microphone input positive, channel A
31	MICAN	Microphone input negative, channel A

32	GND	Ground
33	LED2	Open-drain output
34	SPK_RN	Speaker output negative, right
35	SPK_RP	Speaker output positive, right
36	SPK_LN	Speaker output negative, left
37	SPK_LP	Speaker output positive, left
38	PIO21	Programmable input / output line 21.
39	PIO18	Programmable input / output line 18.
40	NC	NOT CONNECTED
41	NC	NOT CONNECTED
42	GND	Ground
43	GND	Ground
44	RF_PORT	Connect an external antenna
45	GND	Ground
46	NC	NOT CONNECTED
47	NC	NOT CONNECTED
48	AIO0	Analogue programmable input / output line 0.
49	GND	Ground
50	USB_P	USB data plus with selectable internal 1.5kΩ pull-up resistor
51	USB_N	USB data minus

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Max Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	℃
Supply Voltage	VBAT	-	3.6	V
Microphone Bias Supply Voltage	MIC_BIAS	-	VBAT	V
IO Supply voltage	VDD_IO	-0.4	3.6	V

4.2 Recommended Operating Conditions

Recommended Operating Conditions refers to Table 4 below.

Table 4 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range		-40	20	85	°C
VDDIO	IO Supply voltage RF supply voltage	3.0	3.3	3.6	V
MIC_BIAS	Microphone bias Output voltage	1.8	-	2.6	V
Digital Terminals		**Min**	**Typ.**	**Max**	**Unit**
Input Voltage					
VIL input logic level low		-0.4	-	0.4	V
VIH input logic level high		0.7*VDD	-	VDD+0.4	V
Tr/Tf		-	-	25	ns
Output Voltage					
VOL output logic level low, lOL = 4.0mA		-	-	0.4	V
VOH output logic level high, lOH = -4.0m		0.75*VDD	-	-	V
Tr/Tf		-	-	5	ns

4.3Current Consumption

Supply voltage range: Lowest 3.0v, Highest 3.6v, Typical 3.3v. Working voltage: 3.3V, Temperature: Room temperature around 20°C.

Table 5 Current Consumption

Test case Working voltage: 3.3V Temperature: Room temperature around 20°C	Min	Tye	Max	Unit
No connection(Discoverable)	-	4	-	mA
Searching nearby *Bluetooth* devices	-	16	-	mA
Connected standby（No UART data transfer after connected）	-	12	-	mA
The instantaneous maximum current during the connection establishment.	-	16	-	mA
HFP calling	-	20	-	mA
A2DP steaming calling	-	20	-	mA

4.4*Bluetooth* Startup Signaling Sequence

As shown in the power-up sequence diagram of i1107e.

As shown in the figure 3 ,the module is in the reset state in the power pin pulled at least 5ms,T_{rst}>5ms.

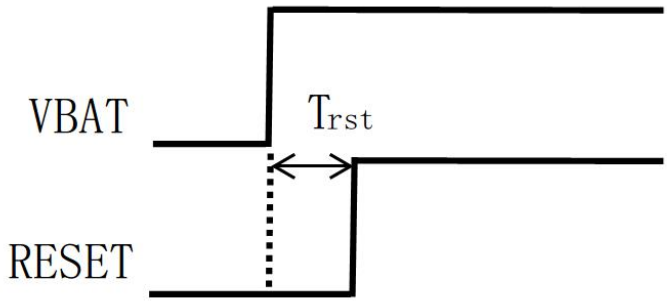


Figure 3 Reset sequence diagram

4.5RF Characteristic

Table 6 RF Characteristic for *Bluetooth*

Items	Contents			
Bluetooth specification	Version 5.0 dual mode			
Channel frequency（spacing）	2402 to 2480 MHz（1MHz）			
Transmitter	Min.	Typ.	Max.	Unit
Output Power	-	7	7.5	dBm
Frequency range	2400	-	2483.5	MHz
Receiver	Min.	Typ.	Max.	Unit
Sensitivity(BER<0.1%)	-	-87	-	dBm

4.6Audio codec

4.6.1 Audio codec: ADC

ADC performance refers to Table 7 below.

Table 7 ADC performance

Analogue to Digital Converter					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	-	16	Bits
Input Sample Rate,Fsample	-	8	-	48	kHz
Maximum ADC Input Signal Amplitude	0dB=1600mVpk-pk	13	-	2260	mVpk-pk

SNR	fln=1kHz B/W=20Hz→Fsample/2 (20kHz max)A-Weighted THD+N<0.1% 1.6Vpk-pk input	**Fsample**				
		8kHz	-	94.40	-	dB
		16kHz	-	92.40	-	dB
		32kHz	-	92.5	-	dB
		44.1kHz	-	93.2	-	dB
		48kHz	-	91.9	-	dB
THD+N	fln=1kHz B/W=20Hz→Fsample/2 (20kHz max) 1.6Vpk-pk input	**Fsample**				
		8kHz	-	0.004	-	%
		48kHz	-	0.016	-	%
Digital gain	Digital gain resolution=1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting=0dB,9dB, 21dB or 30dB Analogue setting=-20dB to 12dB in 3dB steps		-3	-	42	dB
Stereo separation(crosstalk)			-	-89.9	-	dB

4.6.2 Audio codec: DAC

DAC performance refers to Table 8 below.

Table 8 DAC performance

Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Output Sample Rate,Fsample	-		8	-	48	kHz
SNR	fln=1kHz B/W=20Hz→20kHz A-Weighted THD+N<0.1% 0dBFS input	**Fsample** / **Load**				
		48kHz / 100kΩ	-	95.4	-	dB
		48kHz / 32Ω	-	96.5	-	dB
		48kHz / 16Ω	-	95.8	-	dB
THD+N	fln=1kHz B/W=20Hz→Fsample/2(20kHz max) 1.6Vpk-pk input	**Fsample** / **Load**				
		8kHz / 100kΩ	-	0.0021	-	%
		8kHz / 32Ω	-	0.0031	-	%

		8kHz	16Ω	-	0.0034	-	%
		48kHz	100kΩ	-	0.0037	-	%
		48kHz	32Ω	-	0.0029	-	%
		48kHz	16Ω	-	0.0042	-	%
Digital gain	Digital gain resolution=1/32			-24	-	21.5	dB
Analogue gain	Analogue gain Resolution=3dB			-21	-	0	dB
Output voltage	Full-scale swing(differential)			-	-	778	mV rms
Stereo separation(crosstalk)				-	-90.5	-	dB

4.7Clock

Clock performance refers to Table 9 below.

Table 9 Clock performance

Operating Condition	Test Condition	MIN	TYP	MAX	Unit
Crystal Frequency	-	16	26	32	MHZ
Frequency Tolerance	-	-	±20	-	ppm
Operating Temperature	-	-40	-	85	℃
Trimming Capacitance	-	-	9	-	pF
Trimming Step Size	-	-	0.2	-	pF

5.Physical Interfaces

5.1UART Interface

An embedded HCI UART (Universal Asynchronous Receiver Transmitter) with programmable data rate up to 4Mbps is included in this design. The HCI UART supports the following functions:

- Full-Duplex operation

- 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module

5.2USB Interface

i1107e has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on i1107e acts as a USB peripheral, responding to requests from a master host controller.

i1107e contains internal USB termination resistors and requires no external resistor matching.

i1107e supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification).

6.Audio Interface

The audio interface circuit consists of:

- Dual analogue audio inputs
- Dual analogue audio outputs
- 1 digital microphone inputs
- 2 configurable I2S interfaces
- Configurable SPDIF input interface

6.1 Audio Input and Output

The audio input circuitry consists of:

- 2 independent 16-bit high-quality ADC channels:
- Programmable as either stereo or dual-mono inputs
- 1 input programmable as either microphone or line input, the other as line input only.
- Each channel can be connected as either single-ended or fully differential

- Each channel has an analog and digital programmable gain stage
- 1 digital microphone inputs (MEMS)

The audio output circuitry consists of a dual differential class A-B output stage.

6.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

6.3 Microphone Input

i1107e contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones. A biasing circuit for microphones with a sensitivity between about - 40 to - 60dB (0dB = 1V/Pa).

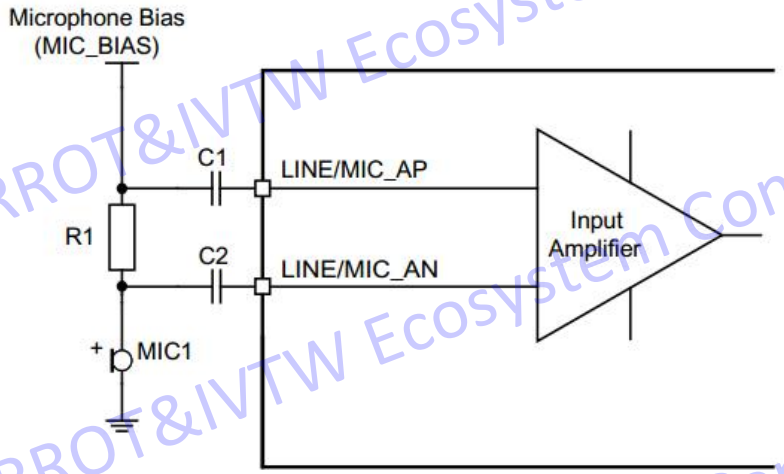


Figure 4: Microphone Biasing

The microphone bias characteristics include:

- Power supply:
- i1107e microphone supply is VBAT or VOUT_3V3
- Minimum input voltage = Output voltage+drop out voltage
- Maximum input voltage is 4.3V
- Drop-out voltage:
- 300mV maximum
- Output voltage:
- 1.8V or 2.6V

- Tolerance 90% to 110%
- Output current:
- 70μA to 2.8mA
- No load capacitor required

6.4 PCM Interface

There are 2 digital audio interfaces. Each is independently configurable as an I²S or PCM port. The PCM interface also shares the same physical set of pins with the SPI interface,The audio PCM interface on the i1107e supports:

- Continuous transmission and reception of PCM encoded audio data over *Bluetooth*.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on i1107e for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
- Long Frame Sync
- Short Frame Sync
- GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32 and using audio API commands.

6.4.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, i1107e generates PCM_CLK and PCM_SYNC.

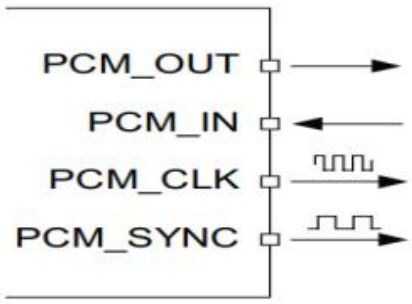


Figure 5 PCM Interface Master

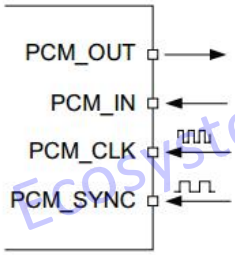


Figure 6 PCM Interface Slave

6.4.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When i1107e is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When i1107e is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

i1107e samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

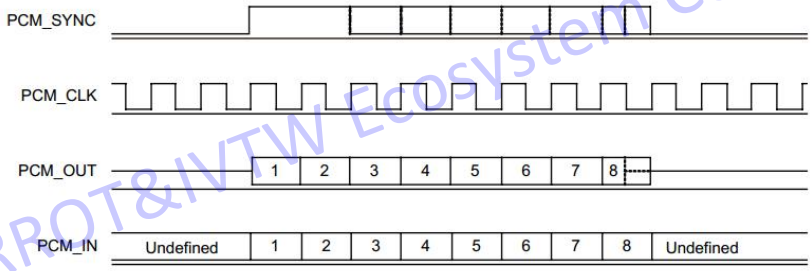


Figure7 Long Frame Sync (shown with 8-bit Companded Sample)

6.4.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

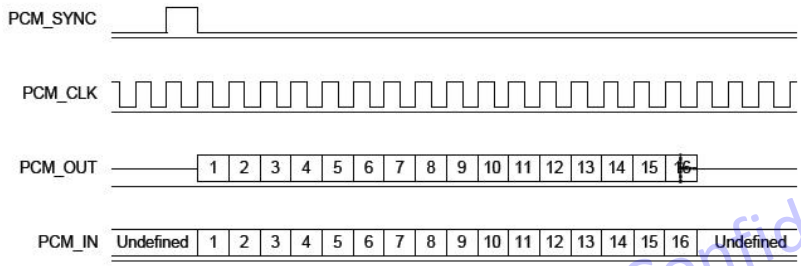


Figure 8 Short Frame Sync (shown with 16-bit Companded Sample)

As with Long Frame Sync, i1107e samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

6.5 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

7.Layout guidelines

Antenna out of the local alignment to do 50 ohm impedance, to ban all layers of the shop. As shown in the red box in the figure below.

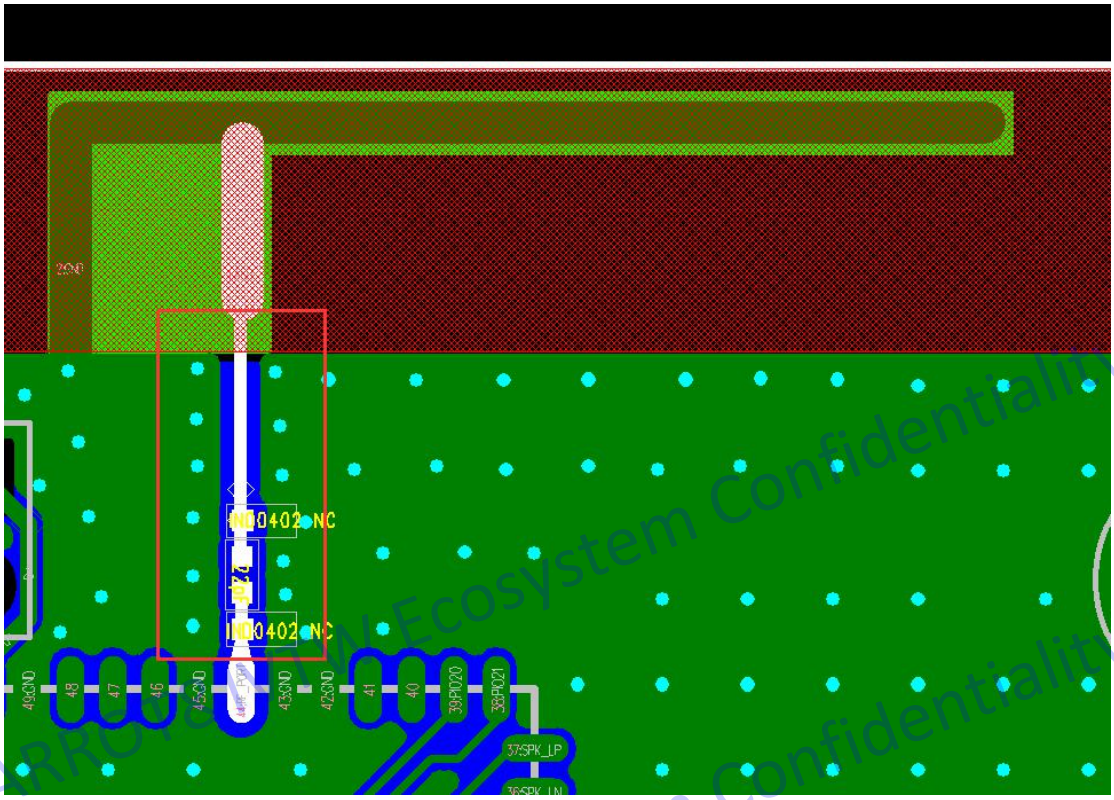
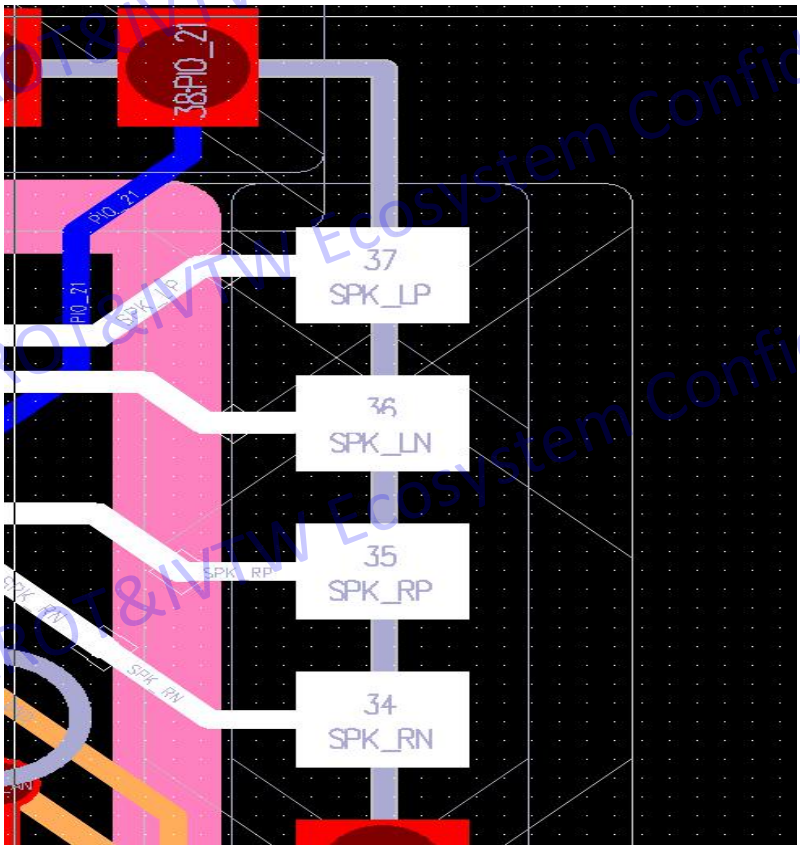


Figure 9 PCB Layout guide

MIC Single line and SPK differential line alignment to do packet processing. If the external op amp needs to be divided.



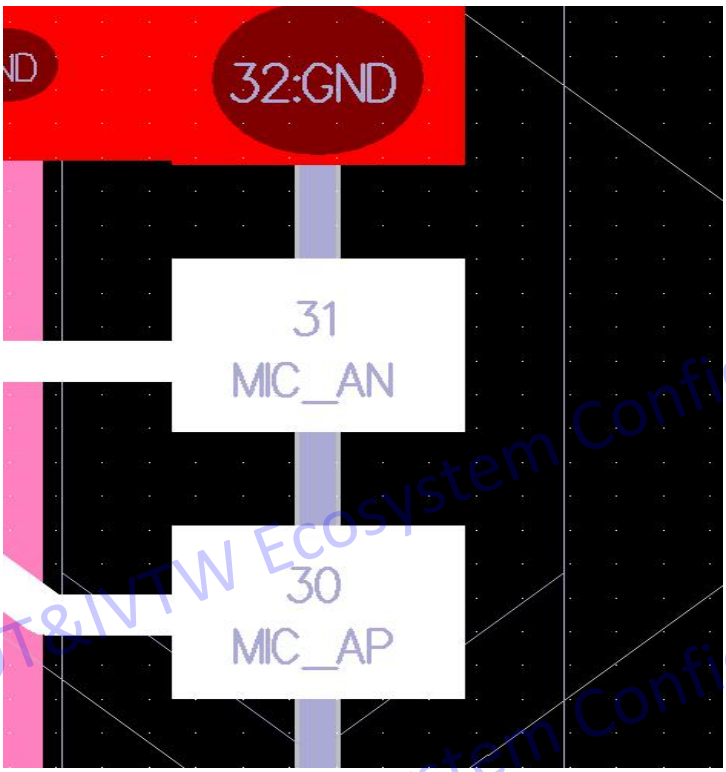


Figure 10 PCB Layout guide

7.1Soldering recommendations

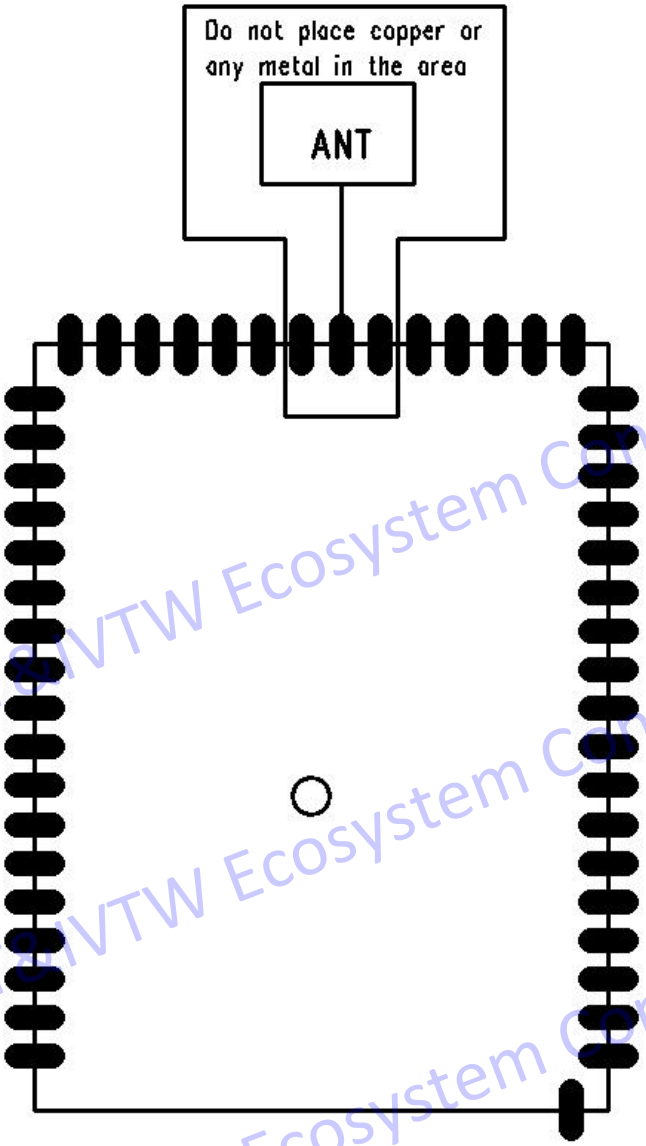


Figure 11 i1107e Restricted Area

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground via around it. Locate them tightly and symmetrically around the signal via. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

Audio Layout

Route audio lines as differential pairs. The positive and negative signals should run parallel and close to each other until they are converted to single-ended signals. Use dedicated audio ground plane for entire audio section.

8.Module Package Information

8.1 Package dimensions （Top view）

Module	PCB package	Mechanical size	Process type	Remarks
i1107e	Stamp holes	19.8mm*14.8mm*2.3mm	SMD	-

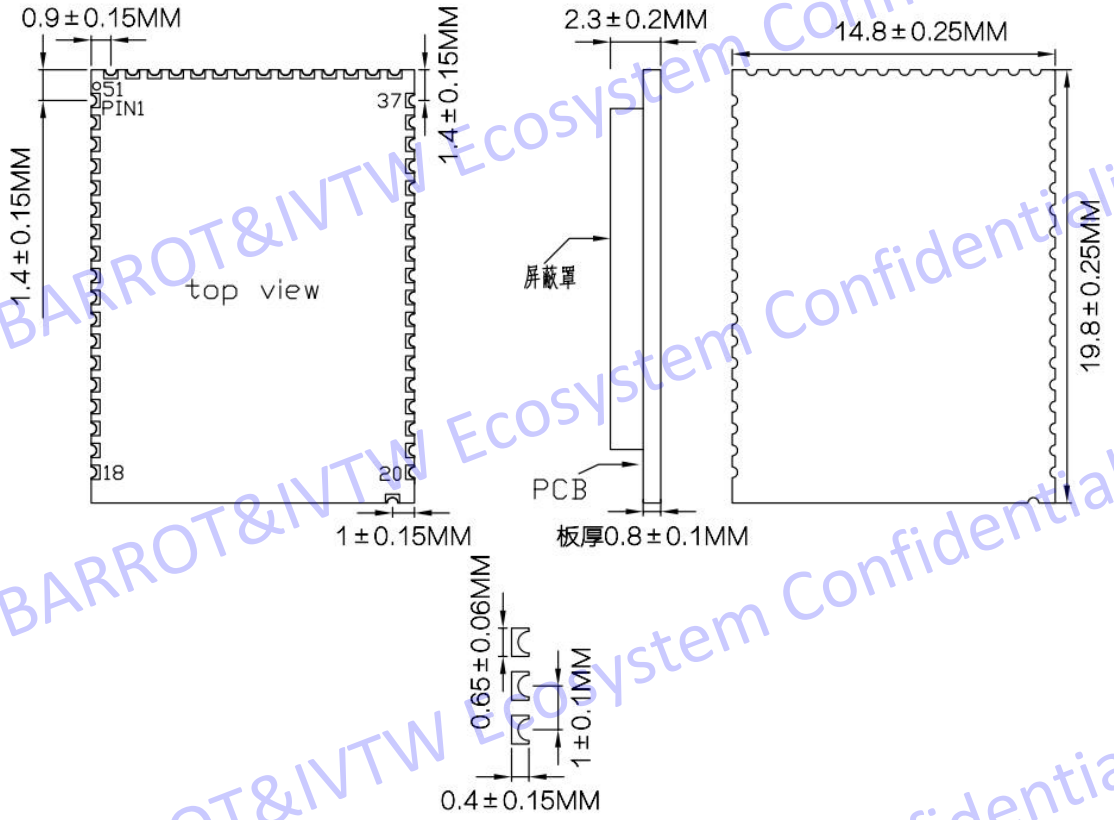


Figure 12 Package dimensions（Top view）

8.2Recommended PCB layout footprint

Pad size:1.6mmX0.65mm

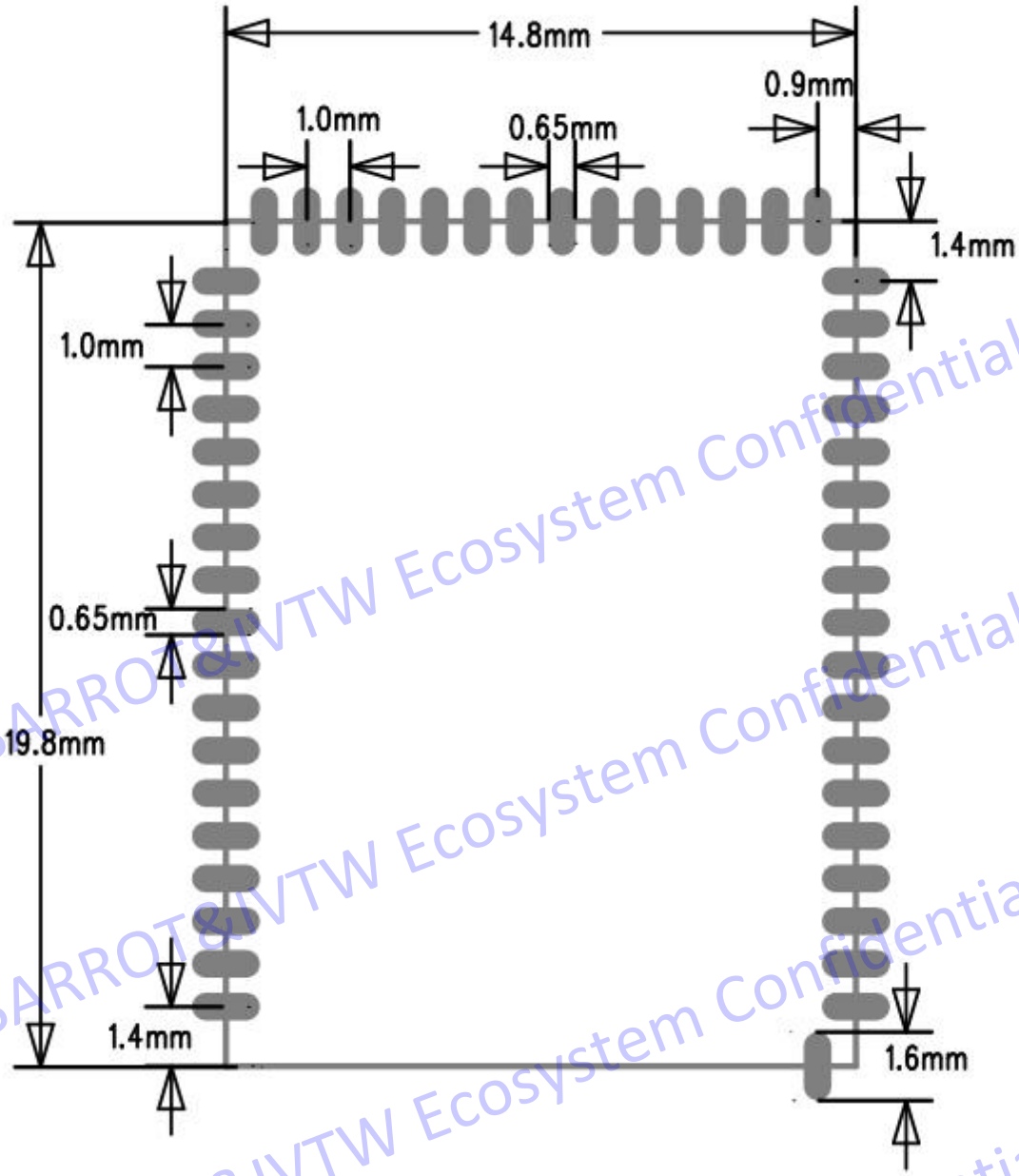


Figure 13 BlueSoleil i1107e Dimension

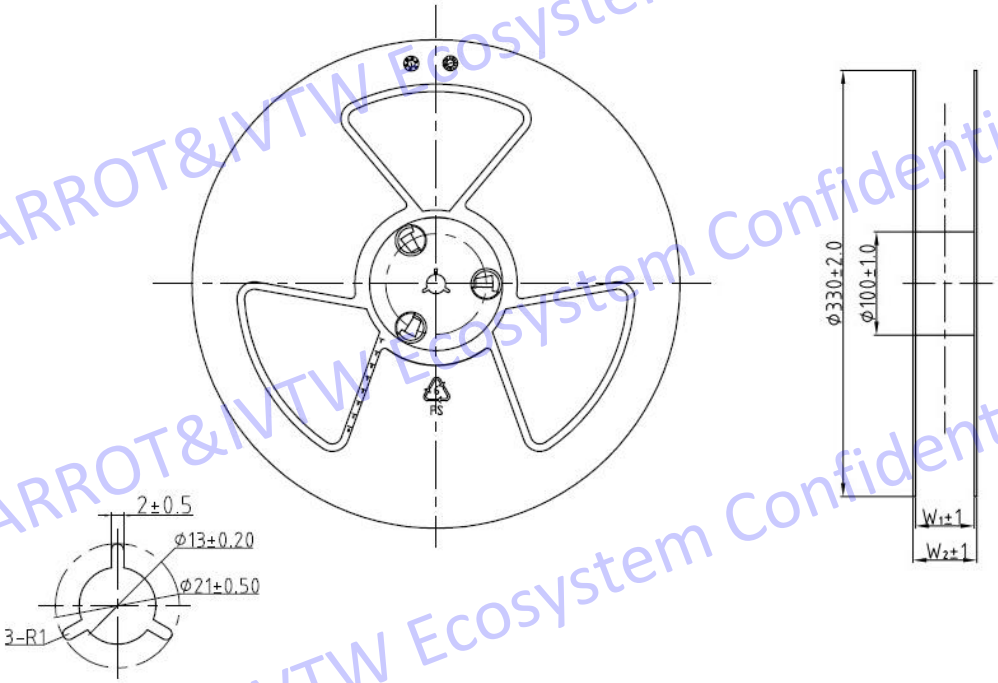
9. Package information

9.1 Net weight

The module net weight : 0.95g ±0.02g

9.2 Package

IVT Wireless i1107e package information is summarized in below figure.



MATERIAL ; PS COLOR : BLUE

Width	12mm	16mm	24mm	32mm	44mm	56mm	72mm	88mm
W1	13.5	17.5	25.5	33.5	45.5	57.5	74.0	90
W2	17.5	21.5	29.5	37.5	49.5	61.5	78.0	94

Figure 14 Reel Information

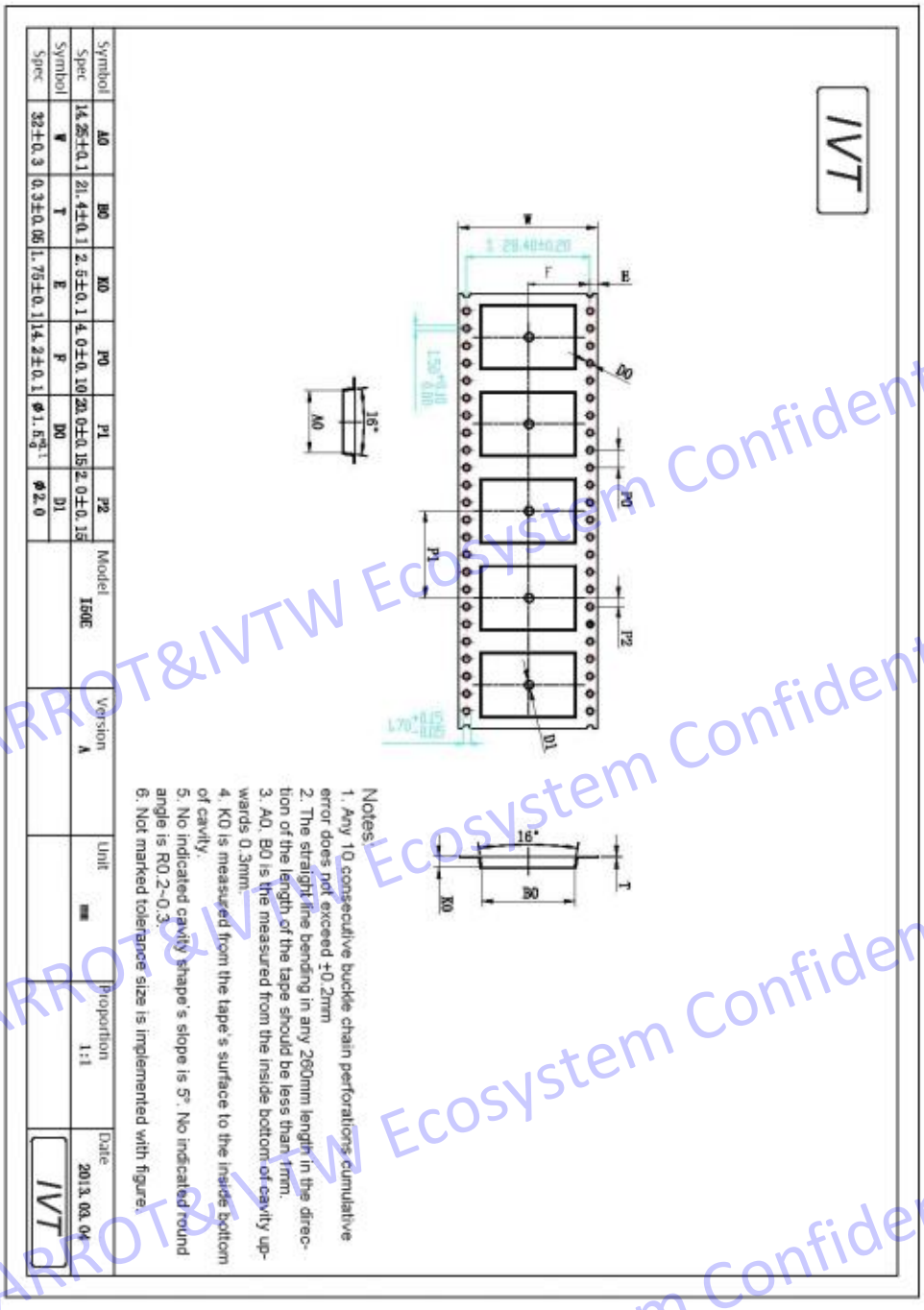


Figure 15 Tape Information

Tray package: 80pcs (10 column x8 row) per tray.

Tray package size: 29.3cm(L)x21.8cm(W)

Each cell size: 3cm(L)x1.6 cm(W)

Tray texture: Transparent A-PET-A anti-static

Tray antistatic dosage forms: KJD-12

Measuring apparatus: surface resistance meter (8-9 power)

10.Bluetooth Technology Best Developed Together

IVT Wireless Limited is one of Bluetooth® technology BEST developed together which is authenticated by The Bluetooth SIG. See Figure below. IVT Wireless ecosystem is one completed Bluetooth productions including Bluetooth software, modules and end productions.

Figure 16 IVTW is One of Bluetooth Technology BEST Developed Together

11.Contact Information

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12.Copyright

Appendix

1. Storage Requirements

1.1 Temperature: 22~28°C;

1.2 Humidity: <70%（RH）;

Vacuum packed and sealed in good condition to ensure 12 months of welding.

2. Humidity Sensitive Characteristic

2.1 MSL: 3 level

2.2 Once opened, SMT within 168 hours in the condition of temperature: 22~28°C and humidity<60%（RH）. Once production line stops, modules should either be stored in the drying box or be vacuum packed. If it fails to meet above storage conditions, *Bluetooth* modules need drying. Drying parameters refer to Table 2-1.

2.3 Handling, storage, and processing should follow IPC/JEDECJ-STD-033

Table 2-1： Mounted or un-mounted SMD package drying reference condition
（User drying：Shop life starts after drying， Time=0）

Drying under 125°C		Drying under 90°C，≤5%RH		Drying under 40°C，≤5%RH	
Over floor life >72 hours	Over floor life≤72 hours	Over floor life >72 hours	Over floor life≤72 hours	Over floor life >72 hours	Over floor life≤72 hours
9 hours	7 hours	33 hours	23 hours	13 days	9 days

3.PCB Design Instruction

3.1 PCB Pad Surface Treatment

ENIG（Chemistry Ni/Au）、OSP are recommended for PCB surface treatment. ENIG（Chemistry Ni/Au）is preferred.

3.2 PCB Pad Design

3.2.1 In order to ensure high production efficiency and high reliability of solder joints, PCB pad design refers to recommended PCB pad size in the corresponding product specification.

3.2.2 Even only part of PINs are used, it is recommended to do full pad design, symmetric pad design, or asymmetric pad design(refer to Figure 3-1). During reflow, if the pad paste melts, the module is vulnerable to non-balanced force pull. It may lead to PIN short circuit if the module deflects under the action of torque.

Figure 3-1 :Asymmetric Pad Design

3.3.3 Layout Requirements

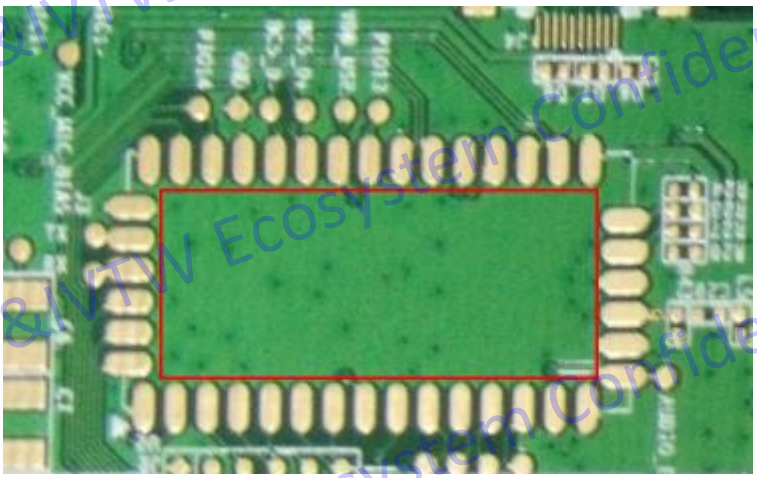
a. For PCB double sided layout, it is recommended to process on 2nd side.

b. The layout of other elements should be avoided on the outermost end 1mm area of module pad. In order to increase repair space, other elements layouts should be as far away from the module as possible. The minimum distance between the module pad and PCB board edge is 1.5mm.

3.3.4 Compatible Design Considerations

To prevent any hidden risks, module placement area（See the red rectangle in Figure 3-2 below） shouldn't include any pad design which intends to be compatible with other elements.

Figure 3-2 :Module Placement Area Example



4. SMT Notes

4.1 All *Bluetooth* modules of our company are lead free. It is suggested to use lead free process technique when SMT processing to prevent the reduction of the reliability of module welding technique which may be caused by the usage of lead production process technique.

Note：the lead BGA solder ball has low melting point（183°C），the lead-free BGA solder ball has high melting point（217°C -221°C）。When the temperature rises to 183°C, the solder paste is melting; when the temperature rises to 220°C, lead free

BGA solder ball starts to melt, and it is in the state of coexistence of solid and liquid. If lead technology is used and the furnace starts cooling, the original welding surface structure of BGA elements is damaged, and a new alloyed layer of the welding surface cannot be formed. This may lead to lead free BGA solder joint failure during reflow, which results in pseudo solder joints and other reliability issues in further.

4.2 SMT stencil Design

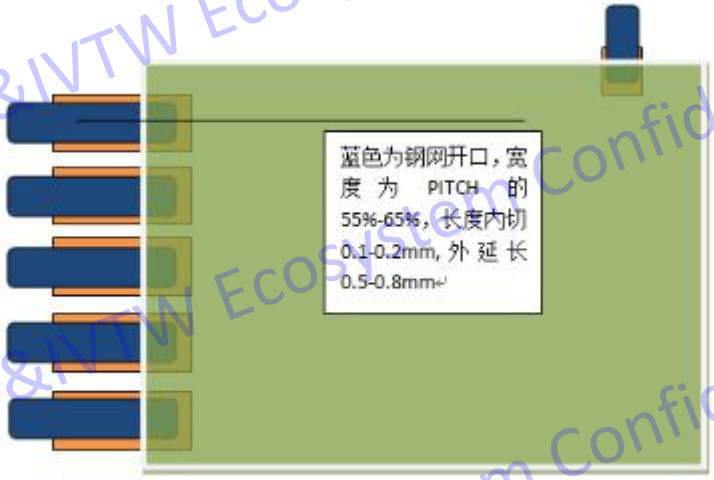
Ladder stencil is recommended. Stencil opening design requirements are as follows:

4.2.1 The module PIN foot area is suggested to be thickened to 0.18-0.25mm; this thickened area should be kept at least 1mm spacing with other elements;

4.2.2 Opening width: 55%-65% of PCB PIN foot pad Pitch (centre-to-centre spacing)

(Since the actual width of the motherboard pad is not ensured, the opening width is determined by pitch.)

4.2.3 Opening length: based on PCB PIN foot, cutting 0.1-0.2mm towards inside, and extending 0.5-0.8mm towards outside. Outer extension pads maintain at least 0.25mm safety spacing with other elements. Cutting module pad opening if not enough space is left. Opening should be round corners.



4.3 Reflow Profile

4.3.1When the temperature curve， it should add temperature measuring circuit under *Bluetooth* module's BGA to measure its real time temperature.

Recommended temperature parameters：

Increasing slope（°C /SEC）： 1~2

Descending slope（°C /SEC）： -4~-1

Reflow time（S）： 40~70

Peak temperature（°C）： 240-248

The actual furnace temperature curve for *Bluetooth* modules production:

4.4 Reflow Soldering

4.4.1 When PCBA which is mounted with *Bluetooth* module and it enters reflow, please strictly ensure PCBA boards to pass through furnace via track path. Passing through furnace via the net cover of reflow oven is prohibited.

Since *Bluetooth* contains BGA elements, the net cover vibration may lead to high rates of BGA solder welding defects.

4.4.2 During reflow, if it is not double-side board, it shouldn't place the side which is mounted *Bluetooth* as the first side to proceed. Mounting *Bluetooth* on the second sid is suggested. Note: During reflow, since BGA type components are downwards, BGA solder joints are stretched. This may lead to the vulnerability of solder joints. It may eventually result in the brokenness of solder joints and other hidden dangers under the influence of external forces.

4.4.3 Interference Design which may lead to offset of module's elements should be avoided during reflow soldering technique design (i.e. designing furnace jig).

4.4.4 No need to add red glue or other adhesive on the lower part of module. Module recommended pad design can ensure the good solder ability of module PIN foot. Even for any special reason, modules are designed on the first side and need to

be reflowed.

4.5 Wave soldering of PCBA after module is mounted

4.5.1 If process requirements require PCBA which is mounted with modules do wave soldering, please ensure special protection to the module in order to prevent its elements from soldering shortcut or other unpredictable hidden risks which may be caused by splash or other abnormity during wave soldering.

4.5.2 Wave soldering on PCBA which is mounted with module is not recommended. Pls wave soldering PCBA at the first and then manually soldering module on it.

4.6 Manual welding of other elements after module is mounted on PCBA

4.6.1 If some elements needs to be manually soldered onto PCBA after PCBA is mounted with module, such as welding wires, please protect the module with the cover during manual welding process, especially when the manual welding area is close to the module.

4.6.2 PCBA should be placed in the upper part of the manual welding bench, or quickly flows to the next bench. It is not suggested to place it in the lower part of welding bench, such as under welding bench.

5. Repair Instructions

5.1 Repair the situation to decide according to the process of repair

The recommended repair method in this document is not the only method. The selection of repair operations depends on the actual hardware, and it should follow the basic technique requirements during repair.

5.2 Repair Technique Instruction

5.2.1 No matter it is disassembly or welding, repairing requires for the condition of the temperature ascension requirement ≤3°C /sec， highest temperature ≤260°C

5.2.2 If repair elements exceed the storage period, it needs drying (refers to Table 2-1) before repairing

5.3 Module Disassembly

5.3.1 When disassembly, melting and reflowing soldering flux by proving fast, controllable and even heating. It ensures all solder joints melt at the same time. When disassemble, it should avoid any thermal or mechanical damage to modules, PCB, adjacent elements, and their solder joints.

5.3.2 It is recommended to adopt infrared heating or hot air heating method; It is recommended to design & use special jig for module disassembly or pickup

5.4 Module Welding/Replacement

5.4.1 Preparation Before Welding：

5.4.1.1 Using irons and woven materials which are able to moisten soldering flux to remove the old soldering flux on soldering pad.

5.4.1.2 Cleaning pad & remove flux residues

5.4.1.3 Soldering flux pre-fill：Before module is installed into the board, using the appropriate way to add soldering tin on solder pads, it ensures the closeness of the height of solder paste after it melts and re-solidifies.

5.4.1.4 It is suggested to make jig or small printed tin steel mesh to repair solder paste printing

5.4.2 Installing modules into solder pads and ensure the correction of its direction. In order to ensure the temperature of each assembly element stays same during reflow, it is suggested to preheat modules. After heating soldering flux, it reflows to ensure reliable connection. When the solder joint maintains the appropriate reflow time at a predetermined temperature, it forms better IMC.

5.4.3 When the module is installed into the pad after printing, it is suggested to use special jig to pick it up.

5.4.4 Special repair equipment is recommended to be either selected or designed for repairing.