EE/CS 120A: Logic Design

Spring 2019
Syllabus

Overview
EE/CS120A introduces you to the exciting world of digital design. Digital circuits not only form the foundation of computers, but make possible many of the advances around us, like cell phones, video games, medical instruments, automotive systems, satellites, music equipment, military equipment, store automation. You name it -- if it runs on electricity, it's probably got digital circuits (known as embedded systems) inside! 120A gets you up to speed on the basics; the follow-up course, 120B, teaches you to build a computer, and to build complete working embedded computing systems. Finally, you can put your knowledge of digital design to use in EE/CS 168 where you learn the design process of creating Integrated Circuits from a digital design.

Catalog description:
EE/CS 120A. Logic Design (5) Lecture, 3 hours; laboratory, 3 hours. Prerequisite(s): CS 061. Covers design of digital systems. Includes Boolean algebra; combinational and sequential logic design; design and use of arithmetic logic units, carry-lookahead adders, multiplexors, decoders, comparators, multipliers, flip-flops, registers, and simple memories; state-machine design; and basic register-transfer level design. Uses hardware description languages, synthesis tools, programmable logic, and significant hardware prototyping. Cross-listed with EE 120A.

General Information:

Instructor: Chase Cook (ccook009@ucr.edu).
Office hours: Tuesday 2:30 PM – 3:30 PM, Office location: WCH361
Prerequisites: CS061 "C- or better"
Course website: ilearn.ucr.edu
Other: Cross-listed with CS/EE 120A

Teaching Assistants:
Section 022: Ishmam Zabir (izabi001@ucr.edu),
Section 021: Fangfang Yang (fangfang.yang@email.ucr.edu)

Lecture:

Time: T/Th, 12:40 PM – 2:00 PM

Location: MSE 103

Lab:

Section 021: Wed 12:10 PM – 3:00 PM, WCH 125
Section 022: Wed 6:10 PM 9:0 PM, WCH 125

Textbook (**Required**):

Digital Design with RTL Design, VHDL, and Verilog, 2nd Edition by Prof. Frank Vahid Please buy the book at UCR book store (ISBN 978-0-470-53108-2) The discounted version is also available directly from the publisher Digital Design 2nd Edition Binder Ready Version.

Reference books:

Logic and Computer Design Fundamentals and Xilinx Student Edition 4.2 Packge, 3/E, by Mano and Kime, 3rd edition

Course Grading:

The course consists of 100 points (subject to modification)

- Lecture Component (60 points)
  - 20pts: Midterm(s)
  - 24pts: Final
  - 16 pts (8x2pts): Homework
- Lab Component (40 points)
  - 30pts (6x5pts): Lab assignments
  - 10pts: Mini project

Grades will be assigned using a conventional grading scale: 100-90 A, 89-80 B, 79-70 C, 69-60 D, 59-0 F. +/- grades will be given. Students are NOT competing against one another, but rather against the scale -- all students can get good grades if all do well. We may adjust ("curve") an individual assessment item if such adjusting HELPS the class, i.e., changes to the course grading structure will only be made if it beneficial to students.

Minimum competency requirement: We want students to master both the conceptual as well as the hands-on aspects of the course. Thus, students must

receive a passing grade (60% or better) in each of the lecture component and lab component, in order to receive a passing course grade (D- or better).

Study Groups: It is highly encouraged that you find and meet with other students as necessary.

Lecture Schedule:

Subject to change as the quarter progresses.

Read the book before lecture! Reading ahead is one of the most effective ways of doing better in class -
- you'll be amazed how much more useful the lectures will be. We'll follow the book closely.

Also for students who can't access ilearn, please let me know so that I can enroll you into ilearn for this
course

- Week 1:
  - Ch1 -- Introduction: digital systems, number systems, microprocessors versus custom designs.
  - Ch2 -- Combinational logic design: gates, Boolean algebra.
  - Homework 1
- Week 2:
  - Ch2: Combinational logic design: combinational design process, more gates, mux, decoders.
  - Verilog introduction: combinational logic
  - Homework 2
- Week 3:
  - Ch6: Combinational logic optimization: K-maps.
  - Ch3: Sequential logic design: latch, flip-flop.
  - Homework 3;
- Week 4:
  - Ch3: Sequential logic design: finite stat machines, controller design.
  - Verilog introduction: sequential logic
  - Midterm 1 (in Friday lecture time)
- Week 5:
  - Ch6: Sequential logic optimization: state reduction, state encoding.
  - Ch4: Datapath components: registers.

    - Homework 4
- Week 6:
    - Ch4: Datapath components: adders, comparators.
    - Verilog introduction: datapath
    - Homework 5
- Week 7:
    - Ch4: Datapath components: multipliers, subtractors, ALU, counters, timers, shifters, register files.
    - Homework 6; midterm 2 (tentative)
- Week 8:
    - Ch5: High-level state machines, RTL design process.
    - Verilog introduction: RTL
    - Homework 7
- Week 9:
    - Ch5: More RTL design, memory components.
    - Ch5: Queue, design hierarchy
    - Homework 8
- Week 10:
    - Ch7: Programming IC technologies.
    - Review
- FINAL:
    - Scheduled for June 14, 8:00 AM – 11:00 AM (We may move up depending on how much content we cover during lectures.)

Lab Schedule

Subject to change
Refer to the lab overview and report format on the main course ilearn page

Week 1: Lab 1 – Xilinx Environment and Verilog introduction
Week 2: Lab 2 – Decoders and Multiplexers
Week 3: Lab 3 – Programming Combinational Logic on Basys FPGA Board
Week 4: Lab 4 – Sequential Logic Design
Week 5: Lab 4 continued
Week 6: Lab 5 – Datapath Components – adders
Week 7: Lab 6 – Timer Design
Week 8: Mini Project
Week 9: Mini Project continued
Week 10: TBD.

Course Policies and Advice:

- **Material Covered:** You'll be responsible for learning material covered in lecture, in the textbook, and in lab. We expect you to read the textbook; lecture only emphasizes key material, but does not cover all required material alone.
- **Collaboration policy (modifiable at instructor/TA discretion):**
    - Midterm, Final, and any quizzes – Obviously no collaboration
    - In-lecture exercises – Allowed if applicable.
    - Homework – Allowed and **encouraged**. Study groups are a great help and I strongly recommend you find someone, or some group of people, to study with at the beginning of the quarter. However, do not turn in identical solutions. In the end, the best way to learn the material and prepare for the exams is to thoroughly understand and work through the homework assignments. In my experience, the vast majority of students do about the same amount of work no matter what. What really differentiates the A student and the C student is when they do their homework, e.g., the night after the assignment is given or the night before the assignment is due. Either way, you spend about the same amount of time doing the assignments, although one obviously allows for a bit of leeway.
    - Lab assignments – Labs will be done in groups of 2 (or 3 where required). Lab reports are to be completed and submitted individually. Even when completed as a team, each member should write their own code.
- **Academic Dishonesty:** Cheating is not tolerated and will be reported when observed. You are all adults, you will be treated as such, and will be expected to take responsibility for your actions. Copied answers are OBVIOUS and inevitably five people will turn in solutions that are the equivalent of "2+2 = cat." Furthermore, during exams, cellphones are strictly prohibited. If you are seen with such a device, your exam will be disqualified and you will be unable to make this up (no you can't check the time, no you can't use the calculator function).
- **Regrade policy:** You deserve credit where credit is due! Always check the status of your grades to ensure accuracy. Requests for updated, fixed, or corrected grades should be made no later than 1 week after the grade is entered. Any requests should be done in writing to ensure we all have a record.
- **Communication with course staff:** When contacting course staff, please include your name, SSID, course, and lab section. Many students have the

same names and course staff often have multiple courses. Please use your ucr email.

- **Cell Phones:** Cell phones are huge distraction to both the teaching staff and your fellow students. Please be courteous to your colleagues, silence and refrain from using these devices during lecture. Refer to academic dishonesty for exam policy on cell phones.
- **Lab attendance:** You are **required** to attend lab unless otherwise stated. This ensures that all students in a group are indeed carrying out the work that is needed for each project. If you miss lab or come late to lab, your TA reserves the right to penalize your lab score.
- **Lab enrollment:** You are required to attend the lab section that you are enrolled in. This helps ensure the instructional load for TAs is balanced and that equipment/lab space is sufficient for the class size.
- **Homework:** In general, homework is due before the start of the class, one week after the assignment was posted. Homework should be completed using a word processor and submitted to ilearn. Late assignments will be heavily penalized, up to 50% of the score achieved.
- **Lab work:** Each lab contains two components (where applicable), the demonstration and the report, each worth 50% of the lab score. Labs should be finished and demonstrated during the lab session that it was initially assigned. In the event that a lab is not finished during the established lab time, it will be the student's responsibility to complete the lab on their own time and demonstrate the project's functionality to the TA prior to the start of the next lab. Lab reports will be due prior to the start of the next lab. Late labs will be penalized 10% for each day the report and demonstration are not completed. A "day" is 24 hours after the time the lab was due.
- **Time Requirements:** This is a five-unit engineering course. As such, you should expect to spend 3 hours/week in lecture, 3 hours/week in lab, and 6-10 hours/week doing individual study (reading, homework, programming, lab preparation, etc)
- **Final Grades:** Per university policy, changes to your final grade will be made ONLY in the event of a clerical error.