CS 161

HW2

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1. a. This instruction can reference to blocks about:

① I - cache / RegDst

② Register File

③ ALUSrc

④ MEM Read

⑤ write data to registers

b. add a mux for Rt(20-16) for second source

C. we need to add a signal, to control MUX.

2. (a). Because latency for I-mem is greater than Add, so the clock is 200 ps.

(b) 200ps + 15ps + 10ps + 70 = 295 ps

(c) 200ps + 90ps + 20ps + 90ps = 400 ps.

3. a. by combine the Lw and Sw instructions

25% + 10% = 35%

b. the instruction needs

Addit beq + lw + sw

= 20% + 25% + 25% + 10% = 80%

4. a. sign-extend for output:

0000 0000 0000 0000 0000 0000 0001 0100

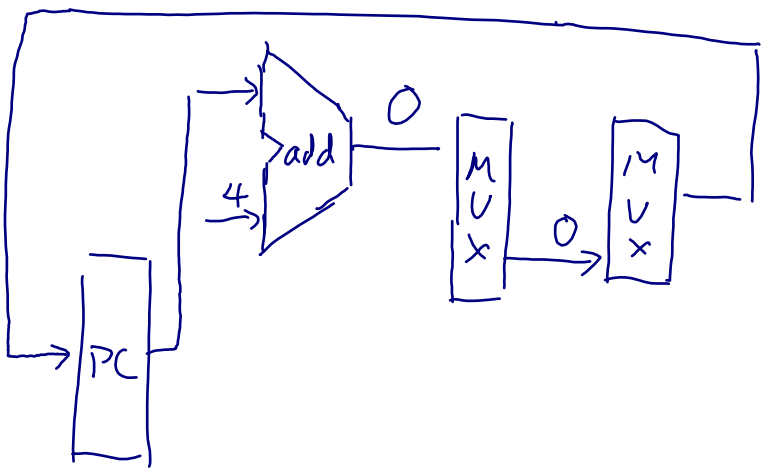
shift-left-2 for output:

0001 1000 1000 0000 0008 0101 0000

b. ALUOp[1-0]: 00

Instruction [5-0]: 0001 0100 (20)

c. the new PC address is (PC+4)



d. WrReg MUX: 2 or 0 (RegDst: X)

ALU MUX: 0001 0100 (20)

MEM ALU MUX: X

BRANCH MUX: PC+4

JUMP MUX: PC+4

e. ALU: −3, 0100 | 0100 (20)

Add (PC+4): PC, 4

Add (Branch): PC+4, 0101 0000 (80)

f: Read Reg1: 00011 (3)

Read Reg2: 00010 (2)

Write Register: x/?

Write Data: x/?

RegWrite: 0

5. We need to modify for the state machine in the picture.: the instruction fetch & instruction decode keeps the same

In the execution process:

Execution.

ALUSrcA = 1

ALUSrcB = 10

ALUOp = 00

In the Write-back:

Write-back step:

RegDst = 0

RegWrite

MemtoReg = 1