Summer CS 161 – Design and Arch. of Computer Systems 2019 - Homework 3

NAME (FIRST LAST) **ID#:**

WRITE THE ANSWERS IN THE TABLE

1. (14 points) A cache has 32 KB, each cache block is 16 B. The address is 44 bits.
   1.a. (12 points) Indicate the size in bits of each of the fields for the four cache architectures listed (in the table).
   1.b. (1 points) Which of these cache architectures would have the lowest miss rate?
   1.c. (1 points) Which will have the lowest hit time?

CACHE ARCHITECTURE		tag	index	byte offset	lowest miss rate	lowest hit time
A	direct mapped					
B	2-way set associative					
C	4-way set associative					
D	fully associative					

CS 161 - HW 3 - Summer 2019

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2. (10 points) A CPU has an instruction and a data cache. The I$ miss rate is 4% and the D$ miss is 12%. The miss penalty for both is 80 cycles.
   a. (6 points) Compute the miss cycles due to the I$ and D$ respectively
   b. (4 points) How does the CPI with the caches compare to the ideal CPI (assuming perfect caches)

miss cycles due to I$	
miss cycles due to D$	
ideal CPI	
actual CPI	

Instruction class	Instruction frequentcy	Cycles/ inst
ALU	28%	2
Load	25%	4
Store	11%	2
Cond. Branch	34%	4
Jump	2%	2

CS 161 - HW 3 - Summer 2019

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3. (6 points) Since the CPU need not wait for the result of a store instruction, we change the design of the cache to use a store buffer. The data is written by the CPU in a store buffer and then moved to the cache and/or main memory by the memory system. What is the speedup of this new design?

miss cycles due to D$	
new actual CPI	
speedup	