

FOSS FPGA

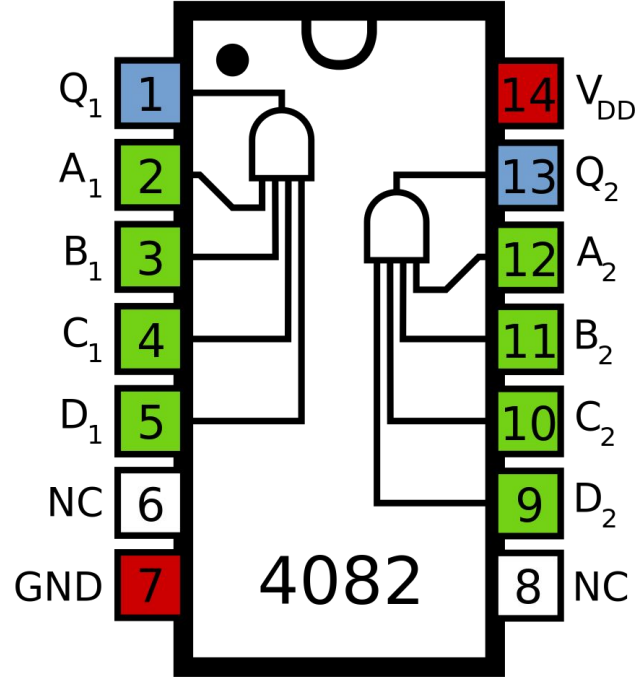
Martin Hubáček

@hubmartin 

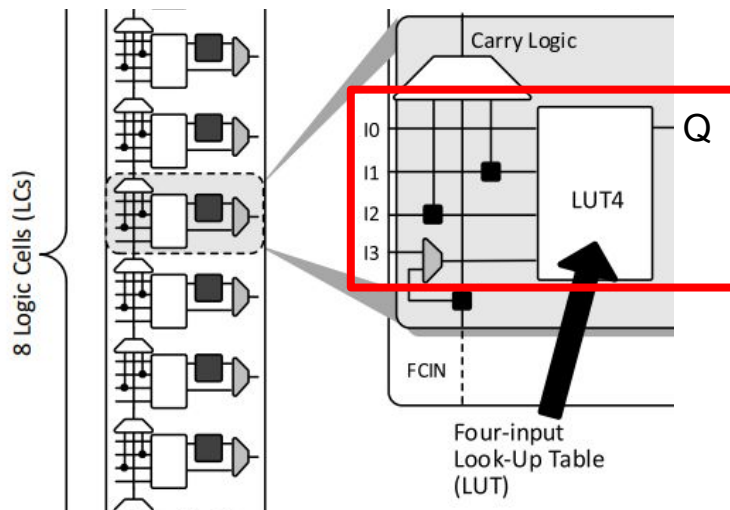
martinhubacek.cz

youtube.com/hubmartin 

$$Q = I_0 \ \& \ I_1 \ \& \ I_2 \ \& \ I_3$$



Combinatorial logic



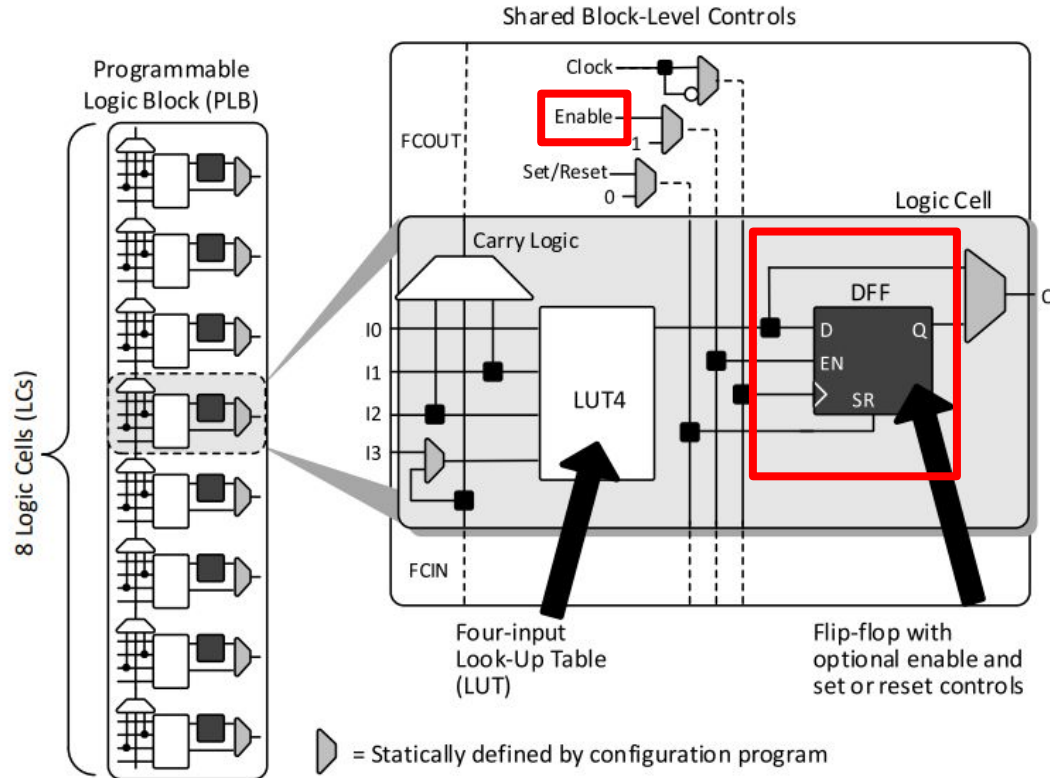
I0 - I3	Q
0000	0
0001	0
0010	0
0011	0
0100	0
0101	0
0110	0
0111	0
1000	0
1001	0
1010	0
1011	0
1100	0
1101	0
1110	0
1111	1

$Q = I_0 \ \& \ I_1 \ \& \ I_2 \ \& \ I_3$

```
if(Q != Q_previous)
{ ... }
```

$Q_previous = Q$

Sequential logic



Register

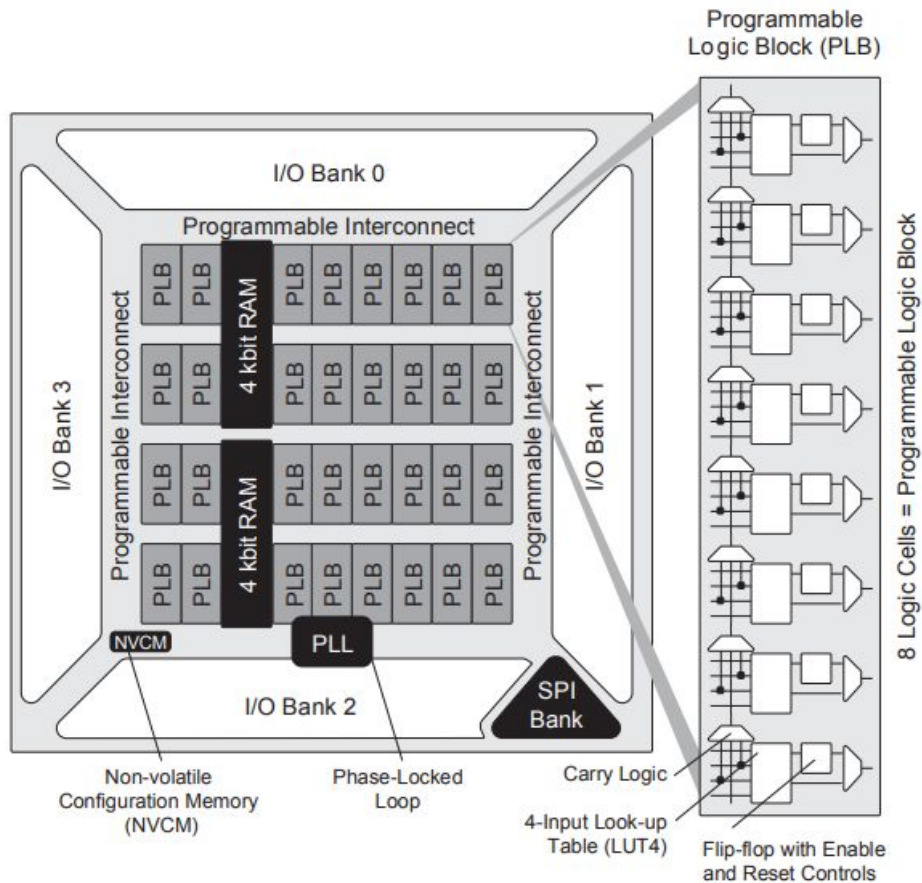
Memory

Counter

FPGA fabric

IO, BRAM, PLL, DSP

Hard-core/Soft-core
peripherals or CPUs



Official tools

Xilinx Vivado (ISE WebPACK)

Intel Quartus (Altera)

Lattice Diamond

Quartus Prime Lite Edition - /home/hub/Desktop/dev/fpga-Cyclone/blinky_archive/blinky - blinky

File Edit View Project Assignments Processing Tools Window Help

Search altera.co...

Project Navigator Hierarchy

- Cyclone 10 LP: 10CL025YU256C8G
 - blinky
 - pll:myPLL
 - lvds:my_lvds
 - uart:my_uart
 - ram:ram_inst
 - rom:rom_inst

Tasks Compilation

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate program...
Timing Analysis
EDA Netlist Writer

blinky.v

```
70
71
72 wire sdram_ctrl_busy;
73
74 assign MEM_CLK = clk_mem_100;
75
76 sdram_controller sdram_controller1 (
77 // HOST INTERFACE
78 .wr_addr      (sdram_wr_addr),
79 .wr_data      (sdram_wr_data),
80 .wr_enable    (sdram_ctrl_wr_enable),
81 .rd_addr      (sdram_rd_addr),
82 .rd_data      (sdram_rd_data),
83 .rd_ready     (sdram_ctrl_rd_ready),
84 .rd_enable    (sdram_ctrl_rd_enable),
85
86 .busy         (sdram_ctrl_busy),
87 .rst_n        (button),
88 .clk          (clk_mem_100),
89
90 // SDRAM SIDE
91 .addr         (A),
92 .bank_addr    (BA),
93
```

Compilation Report - blinky

267
268

IP Catalog

- Installed IP
 - Project Directory
 - System
 - Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and C
 - Processors and Periphera
 - University Program

Search for Partner IP

+ Add...

All Find... Find Next

Type ID Message

- Running Quartus Prime EDA Netlist Writer
- Command: quartus_eda --read_settings_files=off --write_settings_files=off blinky -c blinky
- 204019 Generated file blinky.vo in folder "/home/hub/Desktop/dev/fpga-Cyclone/blinky_archive/simulation/modelsim/" for EDA simulation tool
- Quartus Prime EDA Netlist Writer was successful. 0 errors, 0 warnings
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 102 warnings

System Processing (198)

Ln 25 Col 1 Verilog HDL File 100% 00:00:30

Pin Planner - /home/hub/Desktop/dev/fpga-Cyclone/blinky_archive/blinky - blinky

FileEditViewProcessingToolsWindowHelp

Search altera.co...

Report

Pin Resource Reports

I/O Banks

1

2

3

4

5

6

7

8

VREF Groups

GroupsReport

Tasks

Early Pin Planning

Early Pin Planning...

Run I/O Assignment Analysis

Export Pin Assignments...

Pin Finder...

Highlight Pins

I/O Banks

VREF Groups

Edges

Top View - Wire Bond

Cyclone 10 LP - 10CL025YU256C8G

Pin Legend

SymbolPin Type

User I/O

User assigned...

Fitter assigne...

Unbonded pad

Reserved pin

Other configu...

DIFF_n

DIFF_p

DIFF_n output

DIFF_p output

CLK_n

CLK_p

Other dual pu...

MSEL0

MSEL1

MSEL2

CONF_DONE

nCE

nCONFIG

TDI

TCK

TMS

TDO

Named: *Edit: X

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	trict Pr
led[3]	Output	PIN_R3	3	B3_N0	PIN_R3	2.5 V		8mA (default)	2 (default)		
led[2]	Output	PIN_T3	3	B3_N0	PIN_T3	2.5 V		8mA (default)	2 (default)		
led[1]	Output	PIN_T4	3	B3_N0	PIN_T4	2.5 V		8mA (default)	2 (default)		
led[0]	Output	PIN_M6	3	B3_N0	PIN_M6	2.5 V		8mA (default)	2 (default)		
lvds_clk	Output	PIN_N2	2	B2_N0	PIN_N2	LVDS_E_3R		Maximu...fault	2 (default)	lvds_clk(n)	
lvds_even_rx[2]	Output	PIN_T14	4	B4_N0	PIN_T14	LVDS_E_3R		Maximu...fault	2 (default)	lvds_ev...x[2](n)	
lvds_even_rx[1]	Output	PIN_R12	4	B4_N0	PIN_R12	LVDS_E_3R		Maximu...fault	2 (default)	lvds_ev...x[1](n)	

0%00:00:00

Chip Planner - /home/hub/Desktop/dev/fpga-Cyclone/blinky_archive/blinky - blinky

File Edit View Tools Window Help

Search altera.co...

Report

Report not available

Coordinate: Editing Mode: ECO - 10CL025YU256C8G

Layers Settings

Basic

- ☒ Background
 - ☐ None
 - ☒ Block Utilization
 - ☐ Design Partition Planner
- ☒ Logic Lock Regions
 - ☒ User-assigned Logic Lock Re...

Layers Settings Color Legend

Device Properties

Selected elements:

General

Device	1
Family	C
Device Extents	5
LEs	2
Total I/Os	1
GPIOs	1
Memory Bits	6
Embedded multiplier 9-bit elements	1
DSP Blocks	6
PLLs	4
Global Clocks	2

Tasks

- Generate Clock Data
- Toggle Background
- Report Resources...
- Report Compilation
- Mark Selection
- Core Reports
 - Report High-Spe
 - Report Routing U
- Rapid Recompile Rep
 - Show Changed P
 - Show Changed P
 - Show Changed R
- Clock Reports
 - Report Used Clo
 - Report Spine Clo
 - Report Clock Det

Console

tcl>

Timing Located Objects

Locate ...

Chip Planner - /home/hub/Desktop/dev/fpga-Cyclone/blinky_archive/blinky - blinky

File Edit View Tools Window Help

Search altera.co...

Report

Tasks

Coordinate: (26, 16)

Editing Mode: ECO - 10CL025YU256C8G

Node Properties

Selected elements: ~4

Properties/Modes

Full Name |blinky|rom_address[3]

Coordinate (25, 16)

Register Combinational

Properties Fan-In Fan-out

Console

tcl>

History

Timing

Located Objects

Locate ...

Layers Settings

Color Legend

Official tools negatives

Complex many gigabyte tools

License installations

Non-effective IPs

Highest FPGA lines needs licenses

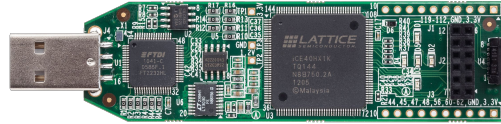


*\$\$\$

Generic low-cost FPGA boards

Altera MAX2 + JTAG \$10

Altera Cyclone II + \$15



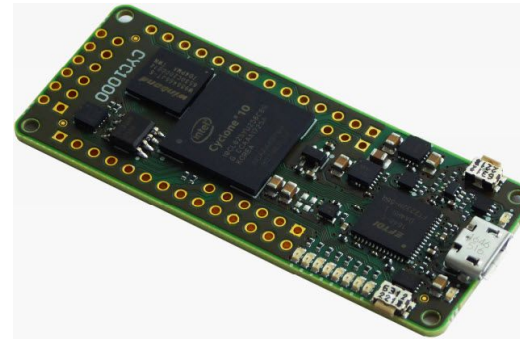
Lattice IceStick \$25



Lattice MachXO2 (FLASH) \$30



Cyclone III / IV / V



Intel (Altera) CYC1000 / MAX \$40

<https://joelw.id.au/FPGA/CheapFPGADevelopmentBoards>

How to reverse engineer an FPGA?

No details of programming internal logic and bitstream

Compare small gradual code changes (change > synthesize > compare bitstream)

Fuzzing

FOSS FPGA chips/boards

IceStorm - iCE40 (ICE40, 8k, 128kb, PLL)

- [TinyFPGA BX](#) \$38
- [iCEBreaker](#)
- [Glasgow](#)
- Olimex iCE40HX8K-EVB
- ICObboard (Rpi HAT) [OpenTechLab YouTube](#)
- [Alhambra](#) (Arduino footprint)

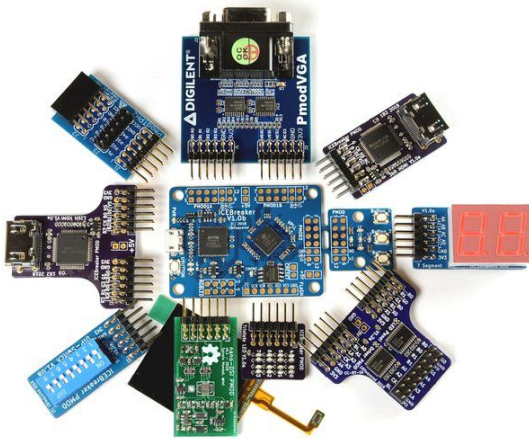


Trellis - ECP5

(85k, 3.7Mb BRAM, 156 18x18 DSPs, 5Gbps SERDES)

- TinyFPGA EX
- ULX3S

X-Ray - Xilinx 7-series

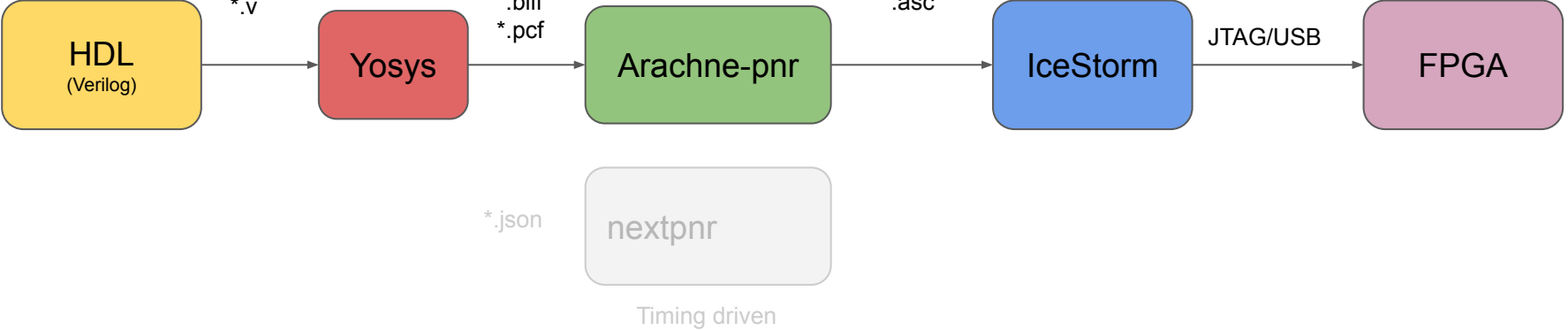


Source code

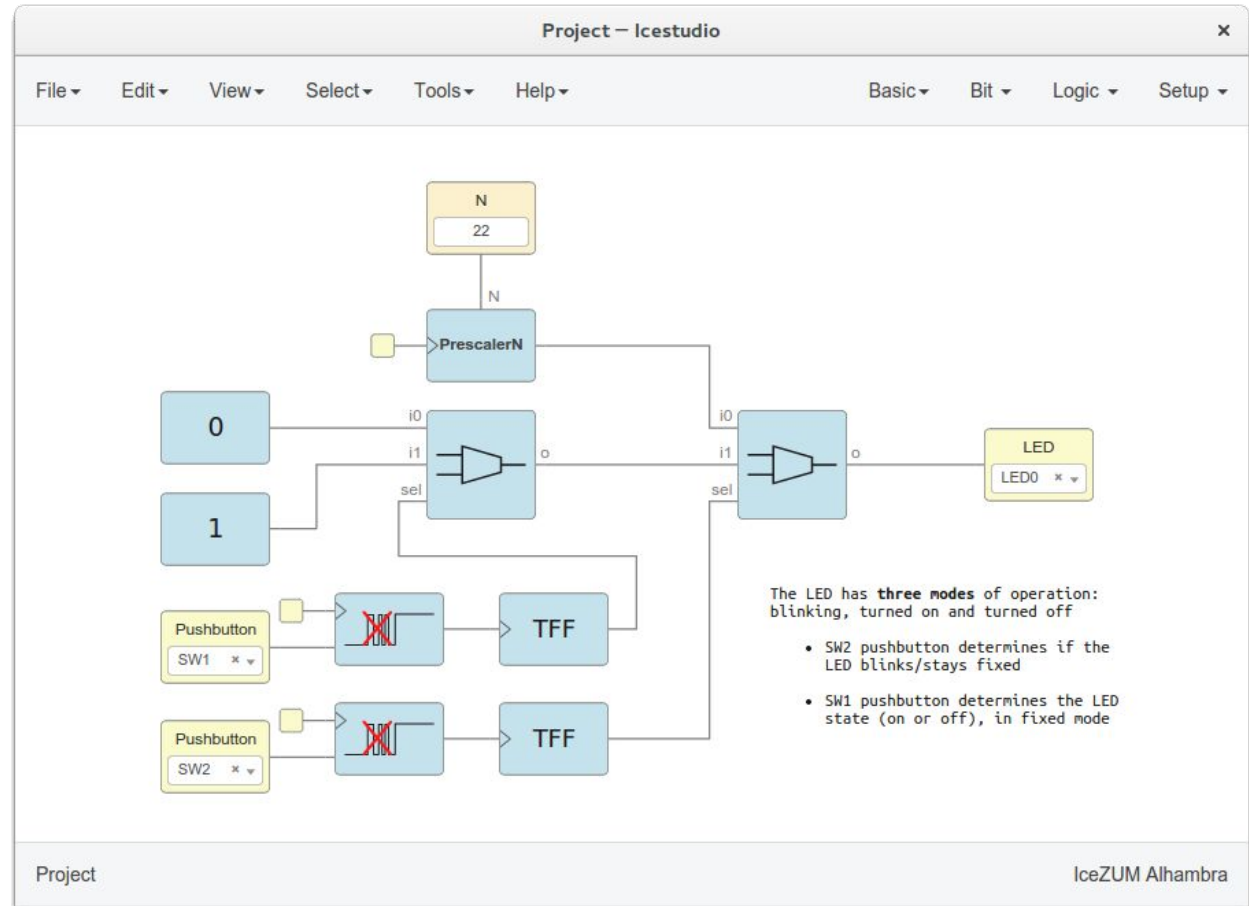
Synthesis

Place&Route

Bitstream gen.



Icestudio



APIO

Makefile / ATOM

Dropbox/ws2812b_apio

Litex , Vivado non efficient <https://www.bunniestudios.com/blog/?p=5018>

<https://www.youtube.com/watch?v=v7WrTmexod0> Tim has too many projects

<https://fupy.github.io> upython on litex fpga

Verilog compiled simulator - Verilator <https://www.veripool.org/projects/verilator/wiki/Documentation>

Přednáška ORconf19 <https://ds0.me/orconf19.pdf>

Simulace

iverilog

Gtkview

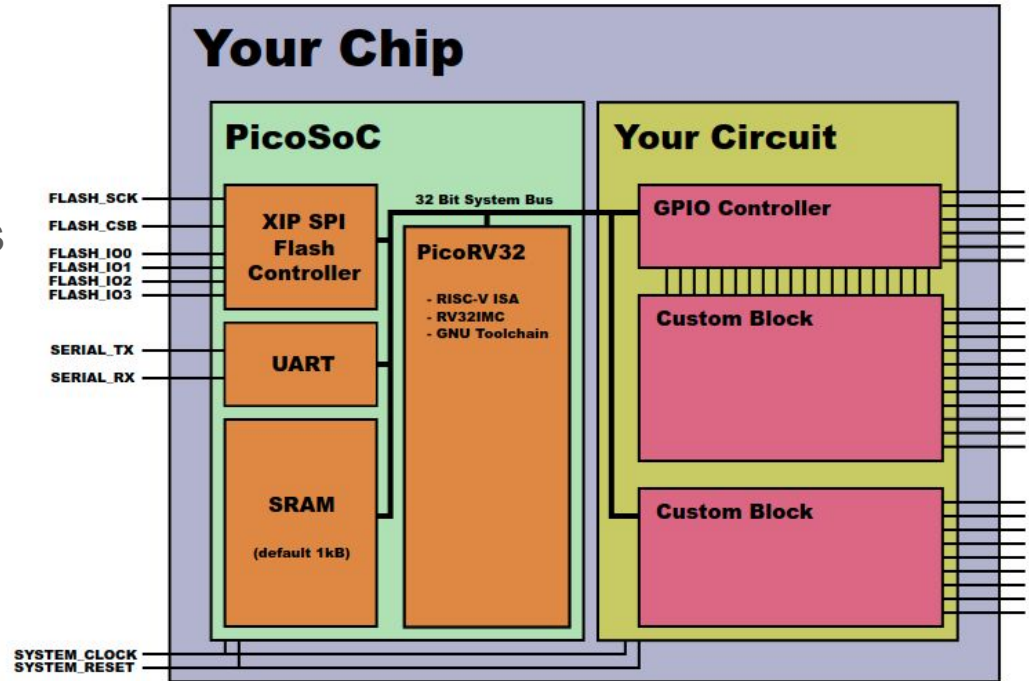
Verilator

<https://www.edaplayground.com/>

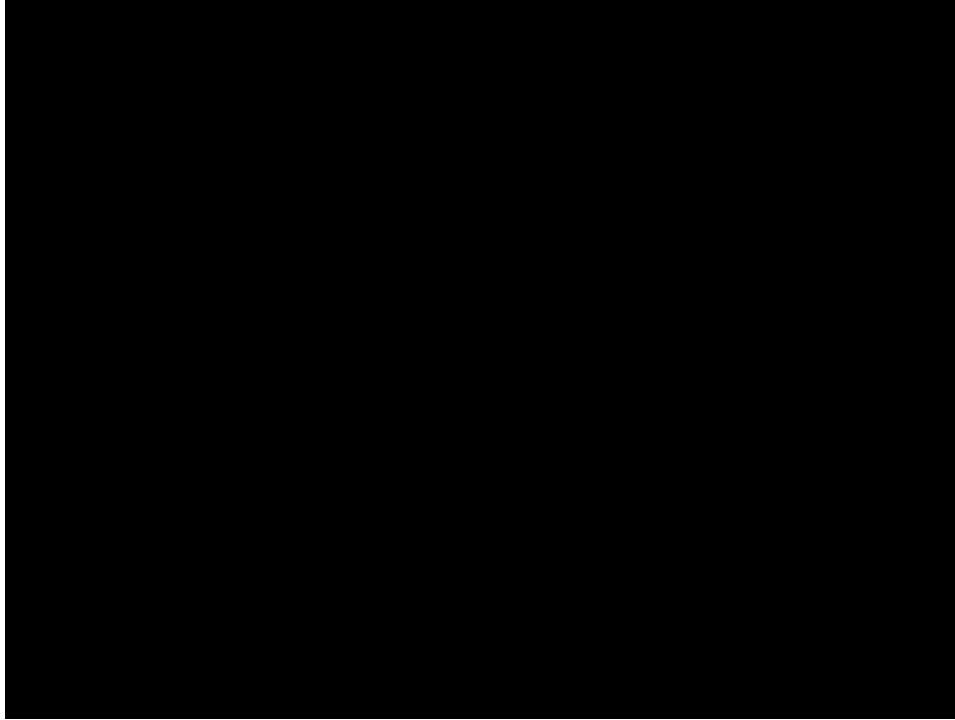
PicoSOC

Soft-core RISC-V

Compilation is faster than synthetis



Two PicoSOCs place&route



<https://twitter.com/q3k/status/1024623710165237760>

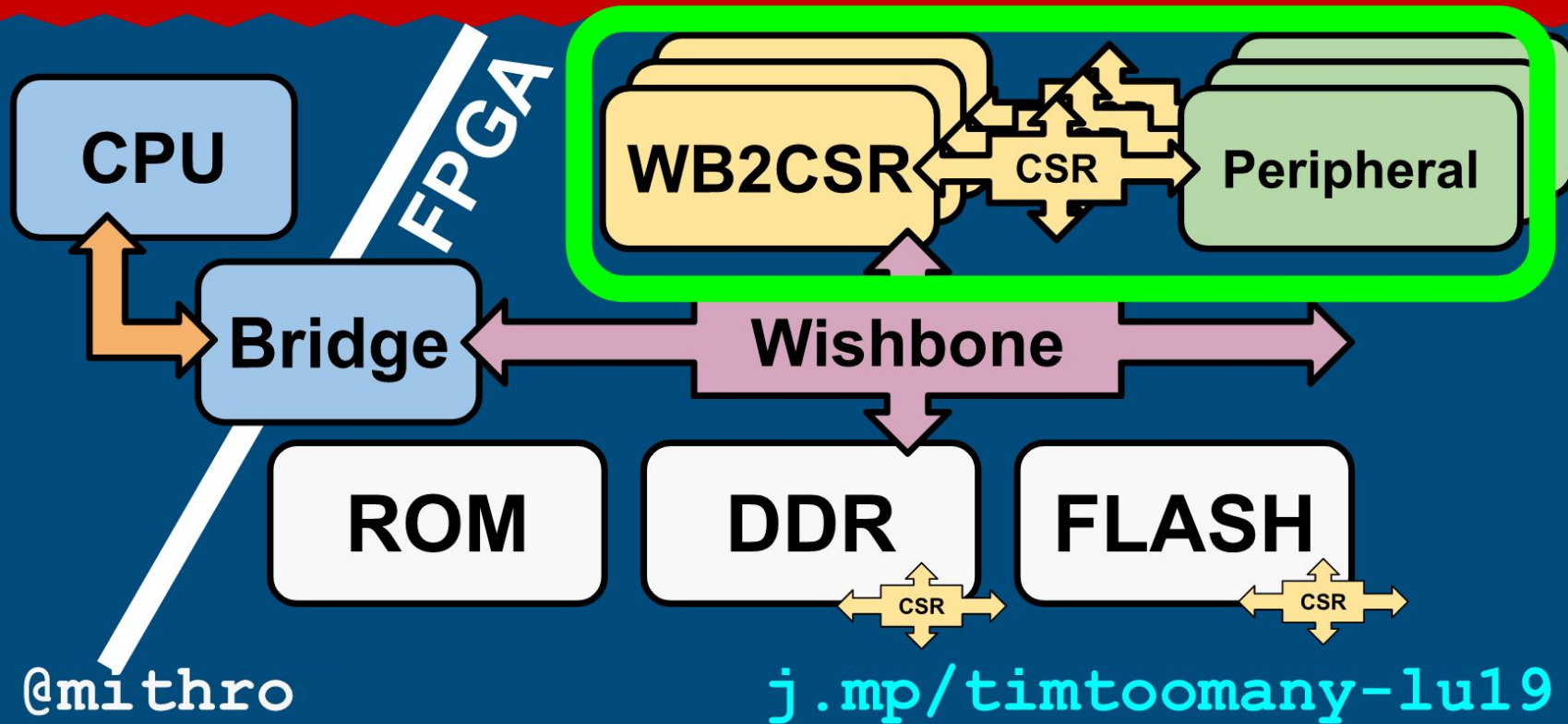
Migen, Litex

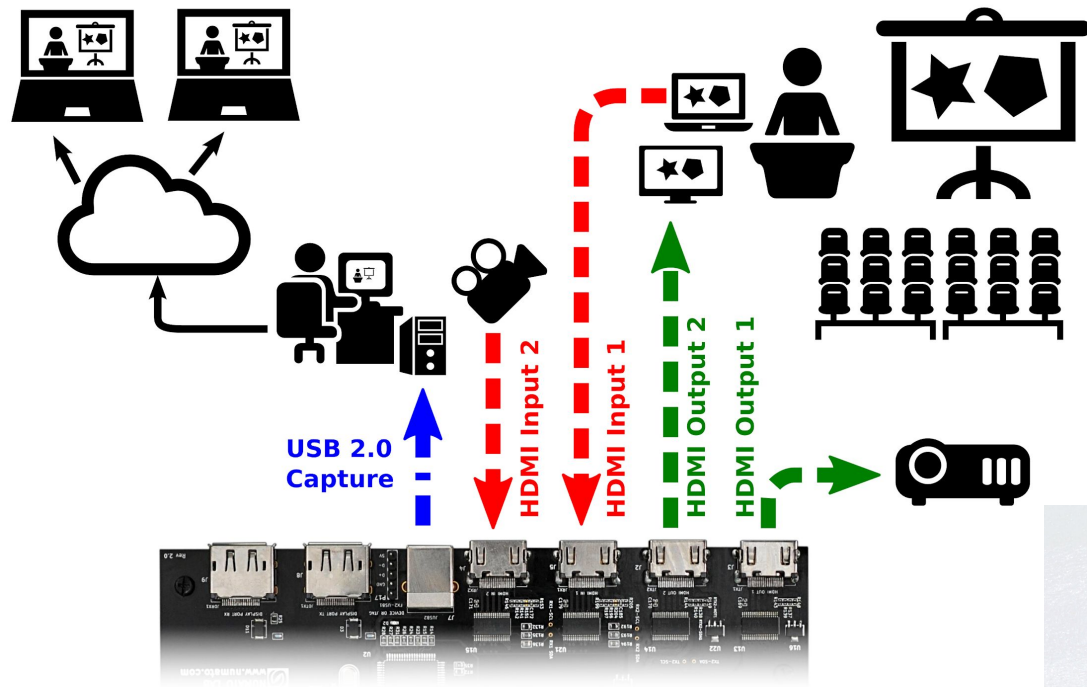
Migen, nMigen - python nástroj pro generování komplexního hardware

Nekompiluje python, pomáhá tvořit HDL kód

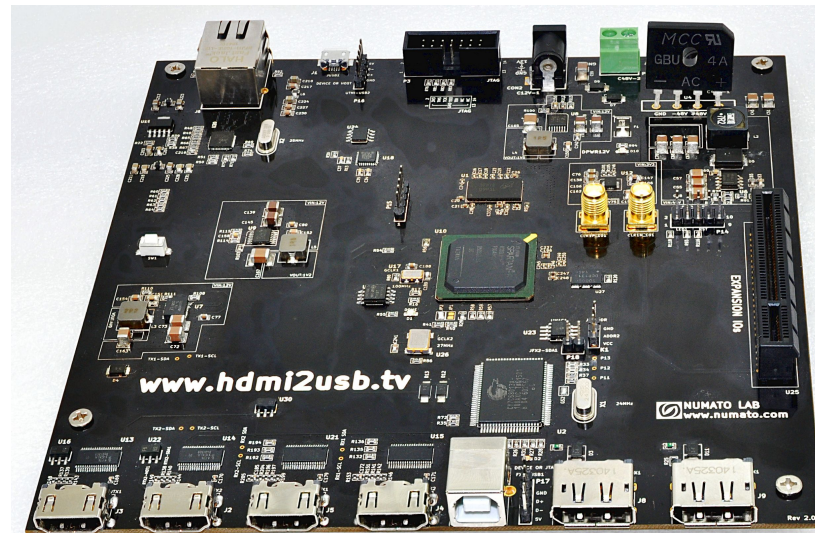
LiteX - LiteX is a MiSoC-based SoC builder using Migen as Python DSL that can be used to create SoCs and full FPGA designs.

Inside the FPGA...





HDMI2USB.tv



Future

Partial reconfiguration

Glasgow

...



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22.-23.11.2019

TECHNOLOGIES FOR THE FUTURE

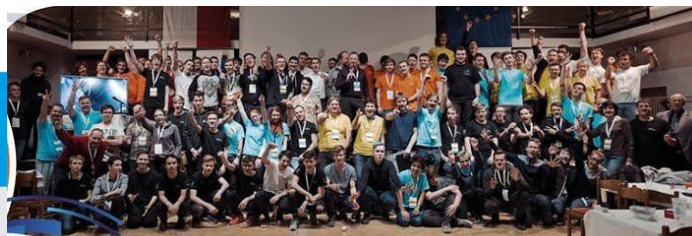
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- Smart Factory
- Smart Office
- Device, Grid & Infrastructure security

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<https://www.hackathons.cz/>



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HARDWARIO

FAB] BRNO

cz.nic











HWDEV Podcast

Hardware Development Podcast se zaměřuje na zajímavá témata z oblasti vývoje, výroby a ožiování elektroniky.

<https://soundcloud.com/hwdevpodcast>

Top played tracks

All time

1		#1 Vývoj hardware není nákup rohlíku	1,763
2		#6 IoT sítě Sigfox, LoRa a NB-IoT	1,576
3		#3 Žádné kecy, dnes pájíme v peci!	960
4		#2 Bez měření není vědění	952
5		#4 Low Power	799
6		#9 Digitrony	781
7		#7 RTOSy, plánovače, tasky	779
8		#8 Elektronická odysea	700
9		#5 Distribuce křemíku	697



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