Digital Logic Design Lab

Spring 2019

FAST-NU Peshawar

Campus

Lab Report # 6-14: Weightage: 8

Due Date: 11 May2019

A note of warning: Start work on assignments as soon as they are given. Do not underestimate the demanding nature of this course. Expect the system to crash the night before your program is due. Aim to have it done the day before.

Submit the assignment on **slate**. Do not email me assignments after due date. It will not be accepted in any case. Students are required to submit actual content written in MS word or Pdf. Hand written/ Scanned assignments will not be accepted.

Use Logic.ly to design circuit diagrams.

Lab: 6-8

1. Design Half Adder and Full Adder along with truth tables.
2. Design Half Subtractor and Full Subtractor along with truth tables.
3. Design BCD to Excess-3 Code Converter with truth table.
4. Design Excess to BCD Code Converter with truth table.
5. Design BCD to Gray-code Code Converter with truth table.
6. Design Gray-code to BCD Code Converter truth table.
7. Design 16:1 mux using basic gates
8. Design 16:4 encoder using basic gates
9. Design 4:16 decoder using basic gates

Lab: 9-10

1. Design a combinational circuit that generates the 9's complement of a BCD digit.
2. A combinational circuit is defined by the following functions, Design the circuit with the decoder and external gates.
3. A combinational circuit is defined by the following functions, Design the circuit with the multiplexers and external gates.
    - F1 = A'B'+AB'C+A'BC+AB'+C+AB'+C'+AB
    - F2 = AB'C'D+AC'D+C'D+C'D+A'B+AD
    - F3=AB+A'C'D+A'BD+AB'C'

Lab: 9-13

1. Design all possible latches and flip-flops using basic gates (RS flip flop/latch, T type flip flop, D type flip flop/latch, JK flip flop and JK master slave flip flop)