MICHAEL R. SPICA

Eagle, ID 83616 | (503) 730 7751 | mrspica@gmail.com

PRODUCT ENGINEERING/ARCHITECTURE

Dynamic and strategic leader with experience providing hands-on technology leadership and guidance to Agile teams. Experience with Semiconductor, PCB, and contract manufacturing, Test, Product, Design and Architecture. Works in fast-paced environments to develop and implement solutions aligned with client's specific technology needs. Leads projects and teams providing career coaching and support for team members to develop their technical, business and interpersonal professional skills. Ability to build and maintain strong collaborative relationships, earning and maintaining confidence with both customers, business leaders, and team members.

CORE COMPETENCIES

✓ Test Engineering	✓ Firmware Architecture	✓ Program Management
✓ Business Transformation	✓ Risk Management	✓ Test Development
✓ Cross Functional Collaboration	✓ Agile Project Management	✓ Leadership/Training
✓ System Design/Testing/Implementation	✓ System security	✓ Data Analysis
✓ Architecture/Security Focus	✓ Rapid Prototyping	✓ Technical leader

PROFESSIONAL EXPERIENCE

LinkedIn: https://www.linkedin.com/in/michael-spica-57b4881/

MICRON TECHNOLOGY INC. | Boise, ID, 80% remote pre-Covid 2013 - Present

Senior Test Engineer/Product Engineering Manager/Principal SSD Product Engineer

Test Process Development SSD PE NVE– Present

Team Size: 7 with cross functional of 4 other indirect reports (10 of 11 reports were at remote sites)

Work collaboratively across a geographically dispersed team to lead Test Process Development SSD PE NVE. Function as patent review committee member for Micron Technology. Operating as scrum master and agile project management for projects. Aligned the agile operations to flow into the classical waterfall project space for executive observation. Utilized both JIRA/Confluence and MS Project to manage programs. Executed projects while working in "flexible work arrangement" FWA, or remote.

- Products SATA client drives (M510/550/600/700/1100/MX300/5100/5210/5200+), PCIe/NVMe drive (9200/8200/7450/7400+)
- Products NVMe 1 and 2 Enterprise Drives (7400, 7450, 6400)
- OCP alignment and requirements
- The PE expert on SERDES PHY items up through current Gen6 operation, defining re-driver/re-timer implementations
- Lead change from UART to SMBus (3.1) for sideband communications.
- Define and drive the SiP (System in a Package) SSD drives for full chip SSD and MCP (Multi-chip package) testing.
- Leverage nascent ASIC (NVMe Controller) DFT features to support system level testing and reduce cost.
- Drive new SSD ATE tester architecture/tooling to reduce MFG costs by $1/10^{th}$
- Specified all SSD ATE manufacturing testers, sideband, in-band, and chamber.
- Evaluate compliance to ISO 26262 as well as SPICE on the firmware aspects of the drives and coordinate with firmware teams for new tests and apply structured test evaluations and solutions
- Executed initial characterization for system/subsystem requirements, most successful release on M600, and continue to identify HW design marginalities.
- PHY layer evaluation of DDR, ONFI, I2C, I3C and primary (SATA/PCIe) drive interfaces. Implemented high speed SERDES PHY loopback for structural testing on SATA and PCIe products. Continue to upgrade the ASIC/System in a package (SiP) to better support full testing.
- Deliver new test methods for NAND working on floating gate and replacement gate technologies. Aided Media Access Group (MAG) with data pull, analysis, and test organization and integration into the manufacturing flows, both internally and at subcon.
- Drive UART operation on proprietary and XMODEM variant platforms (e.g. XModem 1k).
- Developed Virtual Interface Testing (VIT) to further cost reduce the manufacturing by CAPEX avoidance for high speed functional test solutions. This is a firmware emulation of the host on the drive.
- Developed the requirements specification for equipment definition for new ATE architecture including defining requirements and focus on capability requirements to support current/future drive technologies. Developed vendor qualification requirements including SI evaluation, s-parameter evaluation/requirement from vendor, and high speed (64 GBs) channel evaluations.
- Established standards for firmware and ATE code bases to limit process errors due to code incompatibilities.
- Created a new FW architecture for manufacturing code bases to ease MFG interlock (DUT response vs. ATE code host acquisition).
- Detailed data analysis on parametric variations (e.g. power, performance).
- Developed and deployed Electrical "out of box" step that drove process PPM from 5.5k to 100.

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- Developed firmware tests for DRAM to mitigate DDR fallout and find an additional 400 ppm of potential DMC items.
- Developed and deployed standard code for processing drive response information (VU/VS parsing) based on open standards technology (Java/Python utilizing JSON for transport).
- Created Java/Python server to allow for well managed rules/processing distribution from packed binary to JSON.
- Highlighted items necessary to close TS 16949, AEC Q100, Q101, Q104 and ISO 26262 automotive quality requirements.
- Focus on TAA/FIPS compliance and certifications as well as coordination with security architecture team to align on manufacturing vs. security requirements to meet each one.
- Defined ASIC/processor requirements and coordination with ROM content for manufacturing/security capabilities.
- Work with data systems for optimization of TAD (Test Analysis Database) generating custom SQL schema and recommendations for DB modifications as well as mentoring SQL query/function development.
- Coordinated with sub-contractor and requirements to maximize effectiveness in outsourced operations, including data transfer, HW design support and fixturing, ATE design recommendations, etc.
- Examined the FW (both production and manufacturing) for coverage and downstream support.
- Constructed the documentation system and automation based on the documentation to have a 'live specification' via Confluence and JIRA systems. Created the spaces and content to manage coordination with cross functional teams.
- Collaborated with QRA for excursion management and closure.
- Produced 14 patent submissions and received 3 technical innovation awards.
- Leverage use of machine learning in some data analysis operations (data science).

HUGINN AND MUNINN TECHNOLOGIES, INC., | Sisters, OR : http://huginnandmuninntech.com/ 2020 - Present

Founder and CEO

- Developer and owner for the company. Creating web presence as well as items for consumer market. Currently in development and product prototyping phase.
- Have created a mockup prototype,
- Schematic capture, PCB preliminary layout and contract manufacturing of the prototype.
- Global supply chain shortage has delayed launch and have done multiple BOM evaluations/modifications to find parts that are available.
- Contract consulting on manufacturing and test development

MGP PRODUCTS, INC., | Mead, CO, 100% remote 2016 - 2019

Vice President/Founder

- Owned end-to-end process including design, development, manufacturing, and marketing and sales of a consumer product on Amazon with fulfillment by Amazon. Generated physical designs in Fusion 360 (Autodesk), rendered for marketing material and website display for online sales
- Managed operational functions including trademark filings, development of website for the corporation, solicitation/coordination of fabricators/suppliers in China, quality control as well as full contract manufacturing and facilitating shipping to the U.S. with freight forwarding operations and management of inventory.
- Established seller's operation and delivery of products for Amazon, generated marketing materials and sales and ensured compliance to corporate accounting.
- Developed other projects using Eagle CAD leveraging experience in Fusion 360, as well as prototype development with 3D models.
- 3D Printing of models for prototyping and evaluation of business opportunities within the 3D printing space.
- Constructed documentation system (Confluence) to record/keep minutes and shared all corporate files with geographically dispersed co-founders.

CYPRESS SEMICONDUCTORS INC. | Lynnwood, WA, 90% remote 2007 - 2013

Electrical Design Engineer Member of Technical Staff/Director of DFT and New Products Business Development

Test Methods Development – New Products Division January 2012 – August 2013

Team Size: 1 (Building team to a size of 3 total) with cross functional reports of 14 indirect reports

Products: TrueTouch. PSoC 3,4a, 4b, 4c, 5, C28 (28 nm NVSRAM).

Key Accomplishments:

- HOBTO (Hang on Bus to Tape Out) Architecture Definition for PSoC4* family. DFx ownership and test flow.
- ATE modeling for interface optimization with tester parallelism.
- I/O ring standardization and cost modeling for loadboard/probe card cost and package alignment evaluations.

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- Analog test features for full internal system test. Using/creating on-die resources for self-test of digital and mixed signal components.
- Drove new development process flow to achieve entitlement production faster.
- Engineered solutions with verification and validation, with validation board definition and requirements for early ATE vector qualification on Pre-Silicon Validation Platform. Used OVM outputs where fungible. FPGA test system architecture interaction. Created cost estimator.
- C28 (NVSRAM) DFT definition and evaluation of items and provided feedback to JEDEC representative.
- Drove changes to test methods and criteria to encompass automotive/medical requirements.
- TSG4 (Released 1/2012) Shortest Cycle time from 1st Silicon to Production of any PSoC based chip at Cypress.
- Defined the test strategy for high speed NVSRAMs and when to employ ECC vs. redundancy in the memory subsystem. Data Path testing architecture and requirements defined.
- Fault model evaluation and RCCA work for Denso (automotive) response on CAR.
- Drove systems to achieve automotive quality and compliance to work with Denso and Continental distribution.
- Utilized LEAN principles to shorten SoC Development time from 3 years to 47 days with a guarantee of 100% of final test patterns available on first silicon.

DFT Center of Excellence Lead – CCD Products May 2007 – January 2012

Team Size: 3 in US Indirect team of 20.

Products: PSOC3/PSoC5 8051/ARM7 based SoC with 32 bit DMA/EEPROM/Flash/SRAM, fully configurable/Route-able Analog: SC/CT block; General Purpose OP Amp/Digital Filter Block; VIDAC, Comparators; 20bit 180ksps Sigma Delta ADC; 12-bit SAR 1Msps; Low Pass Filter, Temp Sensor, Capsense support, Configurable Digital via PLD, Fixed function digital peripherals: I2C, CAN, USB + 56GPIOs and 16 SIOs

- Responsible for Manufacturing Testability, Test Vector Development, Hardware Support/Training of Software Test division (2 Direct Reports 20 Engineers in multiple divisions).

Key Accomplishments:

- Re-organized the vector development process and fault grading operations. Consistent First Pass Yield on new products.
- Significant architecture modifications to DFX to support the fastest 1st Si bring up as well as well as the shortest test time for TrueTouch products.
- New test coverage methodology developed for analog/mixed signal design evaluations. Automation work with verification teams.
- Generated and owned the DFT Test Methodology for the company.
- Generated and supported the quality prediction tool (PPM Calculator) for the company (statistical modeling).
- Performed functional vector and characterization work on PSoC5 to drive up coverage limited by previous ATPG scan implementation. Defining vectors and operations that are required.
- Developed internal memory tests using the ARM processor code relocation for SRAM test.
- Owned the DFT Architecture definition for three PSoC platforms.
- Developed internal concurrent tests and self "trimming" operations and algorithms.
- Firmware developed and executed on 8051 and ARM CM0 and CM3 processor SoCs.

INTEL CORPORATION | Hillsboro, OR, 100% Remote 1998 - 2007

Senior Product Design Engineer

Test Technology Development: -Sept 2005 – April 2007 **(1 Direct report in US)**

- Owned Memory Test Methodology (ITMH Ch 9 author) and evaluation for concurrent internal memory test methods for multicore devices.
- Developed and owned the redundancy estimator and yield recovery model for the corporation.
- Developed the methods to evaluate aliasing and associated risks with internal memory test compression methods.
- Developed novel BIST methods to provide statistically high coverage with a minimal set of algorithmic operations.
    - Drove definition and Defined Requirements and feasibility for all SRAM testing
    - Performed cost analysis of adding physical redundancy vs ECC to support DFT.
    - Performance analysis showed that there was a performance trade off in adding equivalent space in the correction arrays relative to physical repair.

Strategic Test Methods Development: February 1998 – Sept 2005 **(4 Direct Reports in US)**

- Used Inductive Fault Analysis (IFA) and Empirical data to determine if current test methodologies are sufficient to capture new failure mechanisms due to process changes and new device architectures.
- Used Inductive Fault Analysis to assess impact to LYA (Low Yield Analysis) test mode signatures for P1262.
- Owned Intel Defect Density Model used in fault grading and critical area layout analysis.

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- Correlated KLA-Tencor defect data to Fmax on X1S to determine if Open defects due to Copper Dual Damascene required any new test screens.
- Evaluated yield and repair impacts of Through Silicon Via (3D wafer stacking) technology.
- Developed new TTR (Test Time Reduction) algorithms and new programmable BIST solutions for the microprocessor families as well as chipsets and communications products.
- Developed Burn in Modeling methods and strategies that were employed on all microprocessors.
- Worked on FLASH testing and evaluated new test methodologies to determine need for optimization or effectiveness.
- Electrical defect characterization/density and modeling.
- Develop tools to assist in predictive yield analysis, and developed and implemented multiple BIST solutions, coordinated technology development research down to 28 nm node and evaluation of SOI, and various new process technologies.

Previous Work Experience

CYPRESS SEMICONDUCTOR INC., Senior Yield Engineer – Physical FA/FI and parametric test + statistical data analysis

MICRON SEMICONDUCTOR, Test Sustaining Engineer – Test development on ATE (Teradyne J994)

AMERICAN LENDER SERVICES, INC., System Administrator – SCO Unix sysadmin + document programming

ZENITH DATA SYSTEMS, Test Engineer – Creation of custom test fixtures and manufacturing line disposition

Education/Coursework

Masters Coursework Device Physics, Utah State University, Boise, ID

Masters Coursework on Process Technology, University of Minnesota

Bachelor of Science, Electrical Engineering, Biomedical Engineering

Completed Managing at Intel (MAI) and Micron Leadership in Action (MLA) courses.

Professional Development/Training

PrimeTime PX, Tetramax, DFTCompiler, DFT Max, IC Compiler, DVE, LabView, PYVisa
Mentor Graphics:
FastScan, TestKompress
System Verilog, OVM/UVM, Assertions, ICManage
Managing at Intel, SPC and DOE, 8-D process and RCCA, Antitrust, Harassment Avoidance I II, FCPA, Principles of Program Management
Guest Lecturer at University of Bologna (June 2011, May 2012) on DFT Methods for PhD survey course

Publications/Patents

Co-Author on several papers related to ECC and redundancy/repair
Internal panelist at Intel Corporation on memory test challenges at future technology nodes
Sponsored research with several universities (University of Maryland, Purdue, University of Bologna, Stanford, UCal Berkely)
Author of 4 patents with Intel Corporation
14 patents in submission with Micron

Technical Skills

Operating Systems: MS-DOS, All Microsoft Windows environment, HP/UX 9.10 and HP/U.X. 10.2, Sun/Sparc/Solaris, Linux/Unix, MAC OS. Visio, MS Project,

Languages: Python, including Pandas, C, C++, Assembly, ARM Thumb, JAVA, Perl, Tcl/Tk, Pascal. DOS Batch files, C and Bourne shell scripts, sql, MySQL database, Microsoft Office, JMP, Compiler construction, Go

Design software packages: HSPICE, PSPICE, Verilog, Verilog AMS, System Verilog, OVM/UVM, Cadence, Lynx, Cougar, Eldo, Modelsim, Opus, PSoC Creator, RealView. Fusion 360, Eagle CAD, Arduino AVR and Sketch IDE, MSP430 toolchain, Green River tools, various IDEs (Netbeans, Eclipse, Pycharm, Anaconda, etc.)

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Equipment: HP4145 Bench Parametric Tester, HP4062UX ATE Parametric Test System, Logic Analyzers, Protocol Analyzers, Inovys, Oscilloscopes, Advantest CMT, Mixed Signal Oscilloscope, Teradyne J994, NexTest Magnum I, II,V, Advantest MPT3000HVM, Neosem IBIR.

- Agile and waterfall (e.g. MS Project) project management methods, JIRA, Confluence, Trello
- Familiar with ONFI DDR, DRAM DDDR, PCIe, SATA, UFS, CAN, I2C, UART, Bluetooth BLE (4 and 5), JTAG, BSDL, STIL, ATPG, SWD, and various other protocols.
- In depth knowledge of automotive requirements in documentation and specification compliance (TS 16949, AEC Q101, Q102, Q104)
- Very strong knowledge of statistical methods for both prediction evaluation as well as empirical studies
- In depth knowledge of SERDES PHY IP from GUC, Broadcom, Cadence, Synopsys