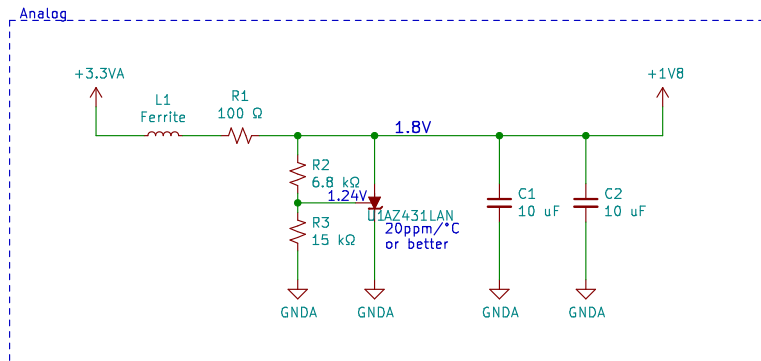
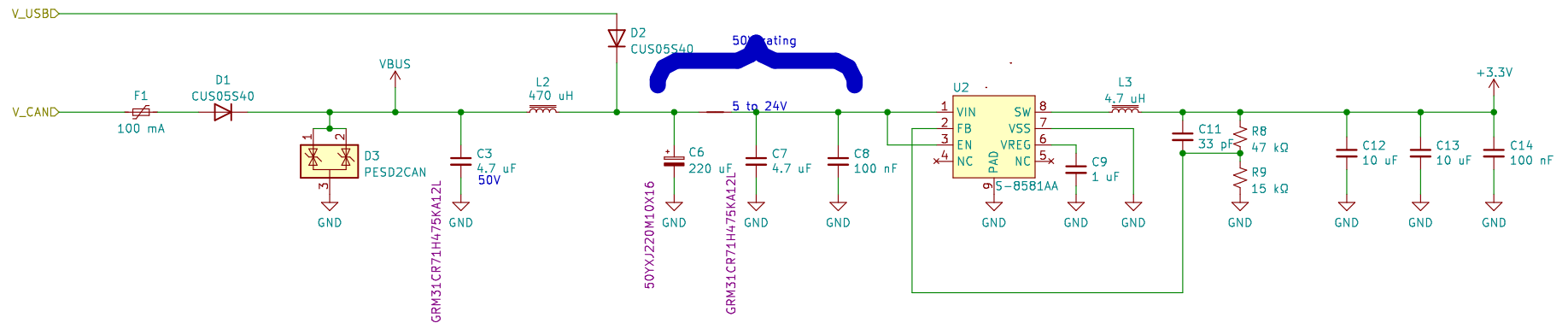
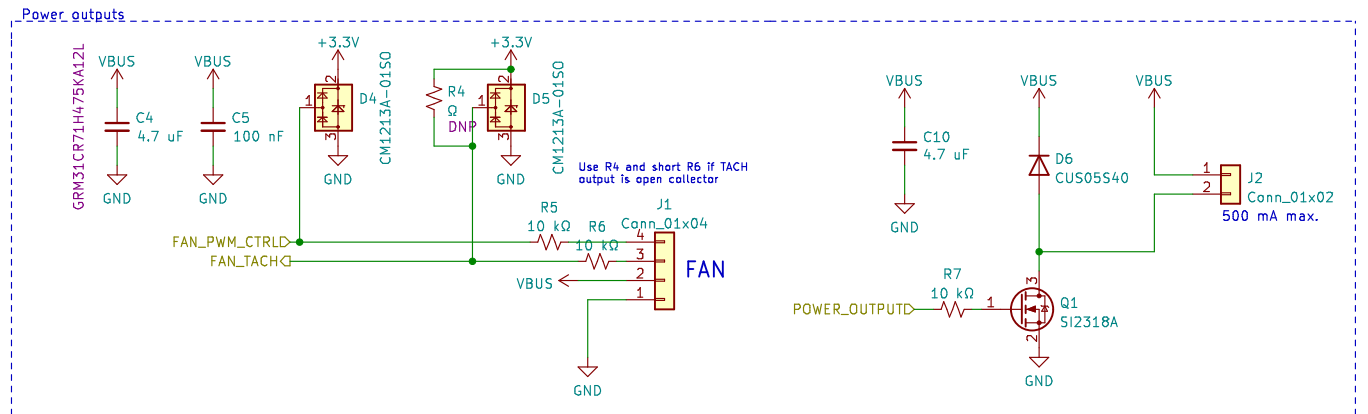


--- Revision History ---

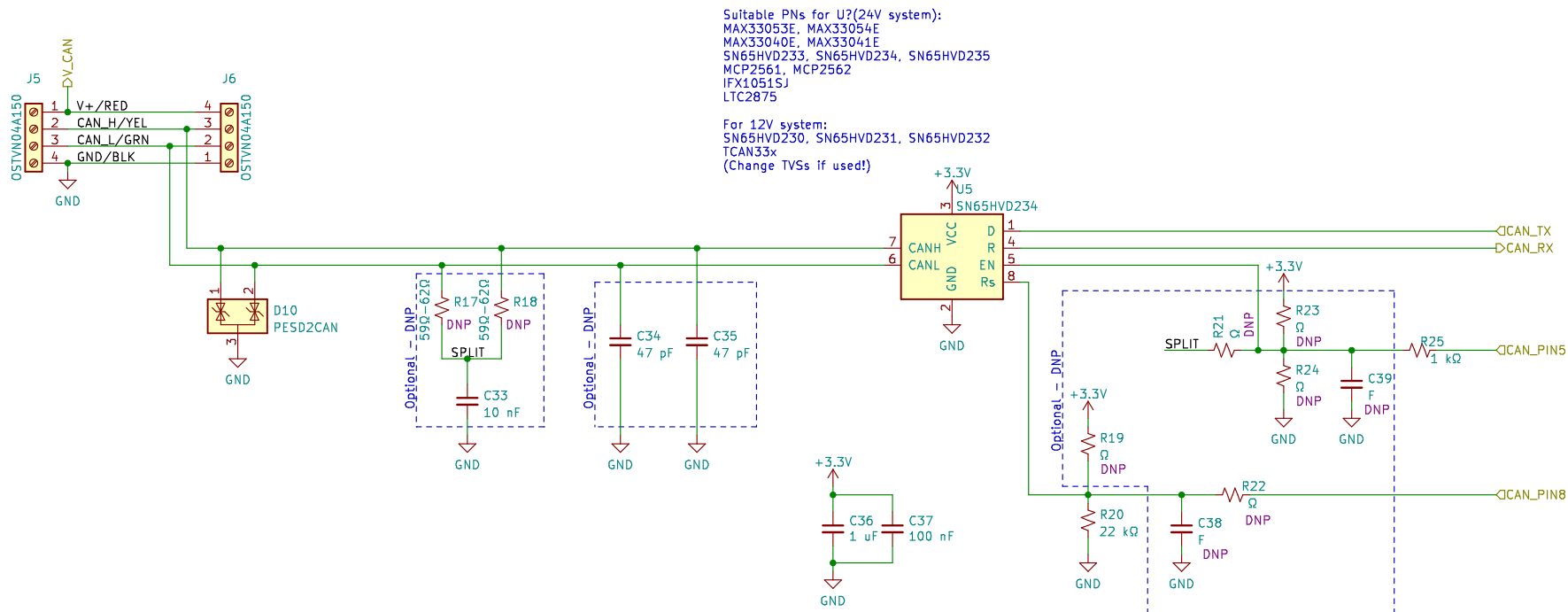
A1: Initial release

A2:

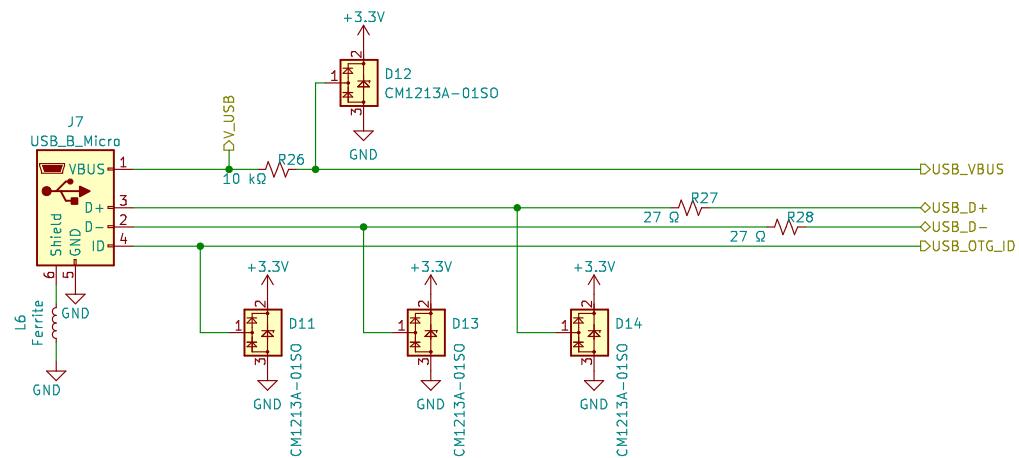
- VUSB bypasses inductor L2
- Reduce screw terminal hole size
- Thermally isolate SHT3x
- U1 footprint fix



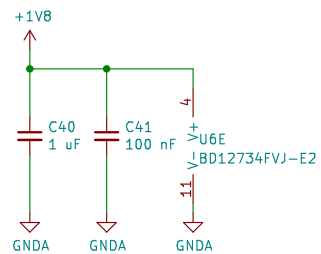
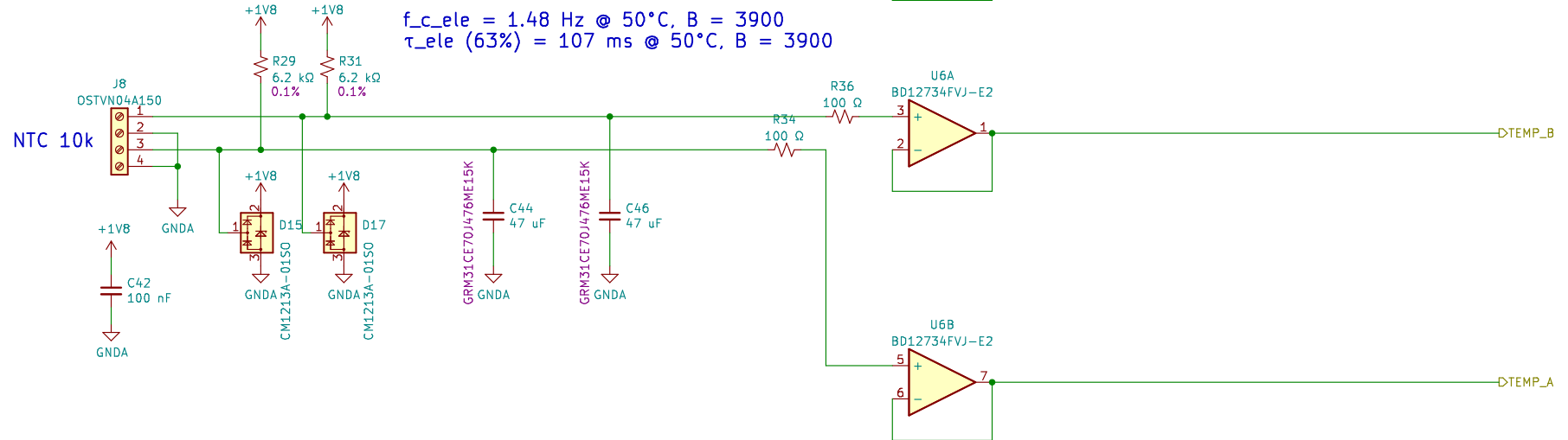
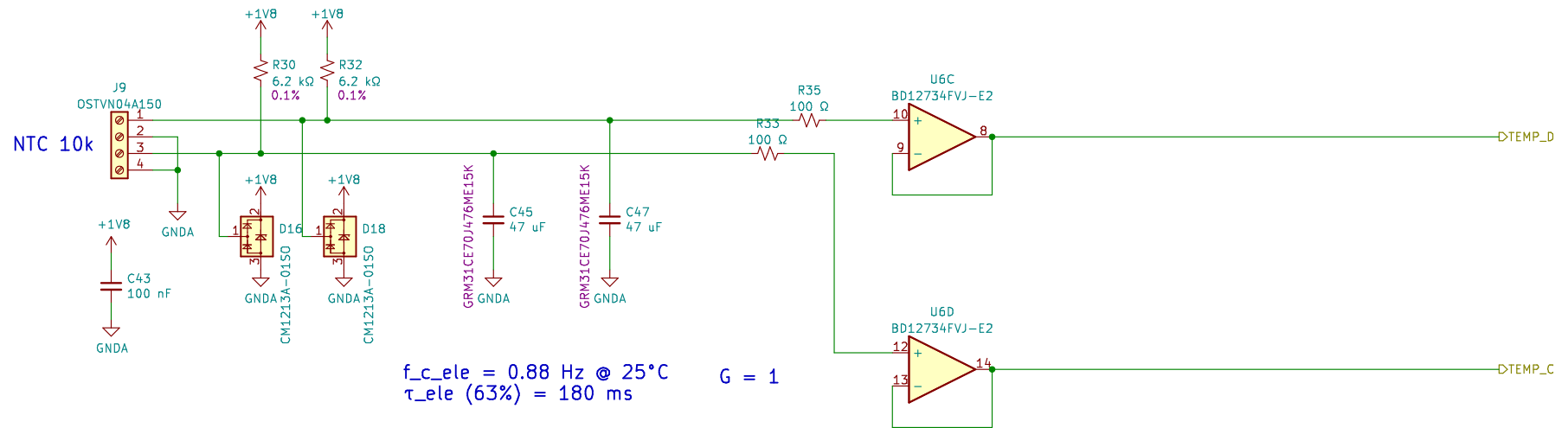
All capacitors X7R or COG unless otherwise noted.
All resistors 1% unless otherwise noted.



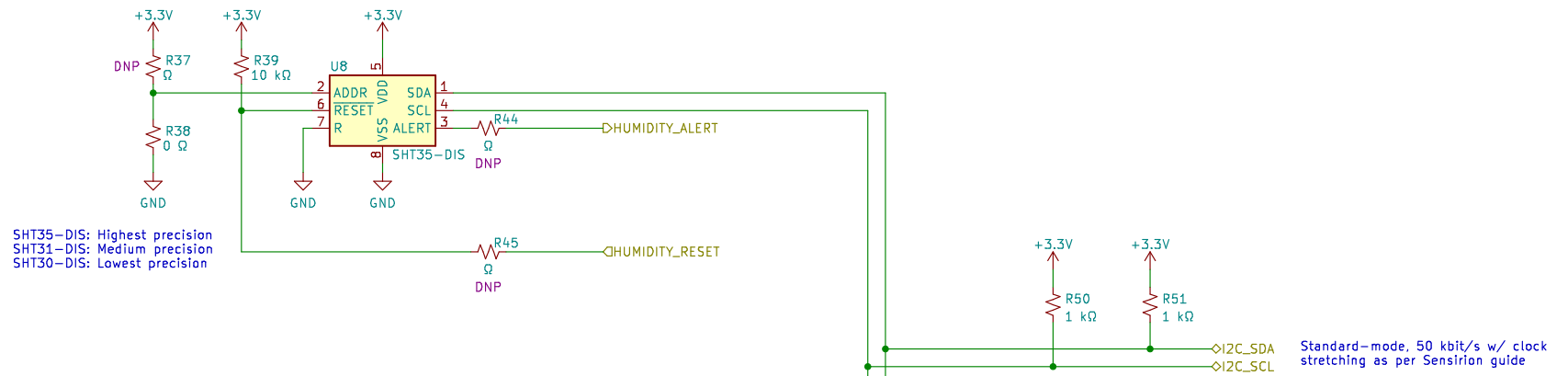
All capacitors X7R or COG unless otherwise noted.
 All resistors 1% unless otherwise noted.



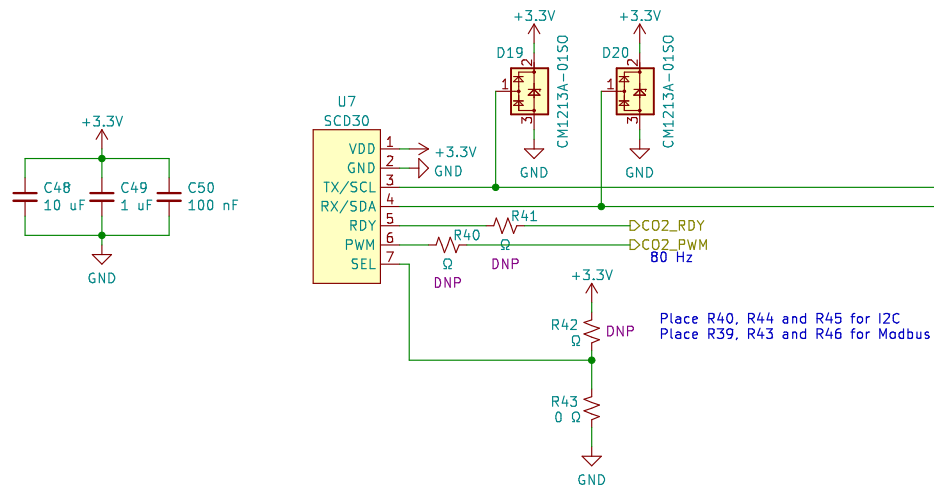
All capacitors X7R or COG unless otherwise noted.
All resistors 1% unless otherwise noted.



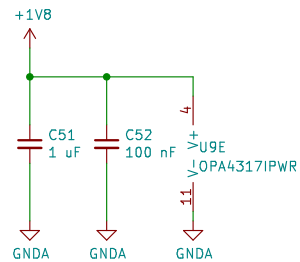
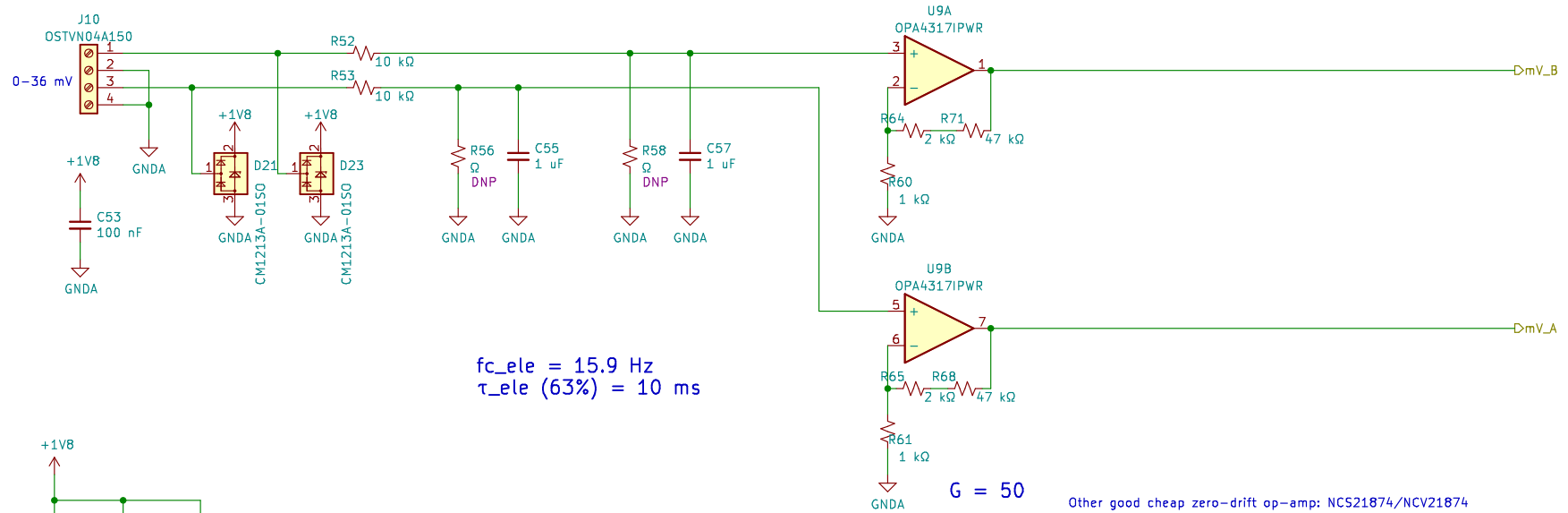
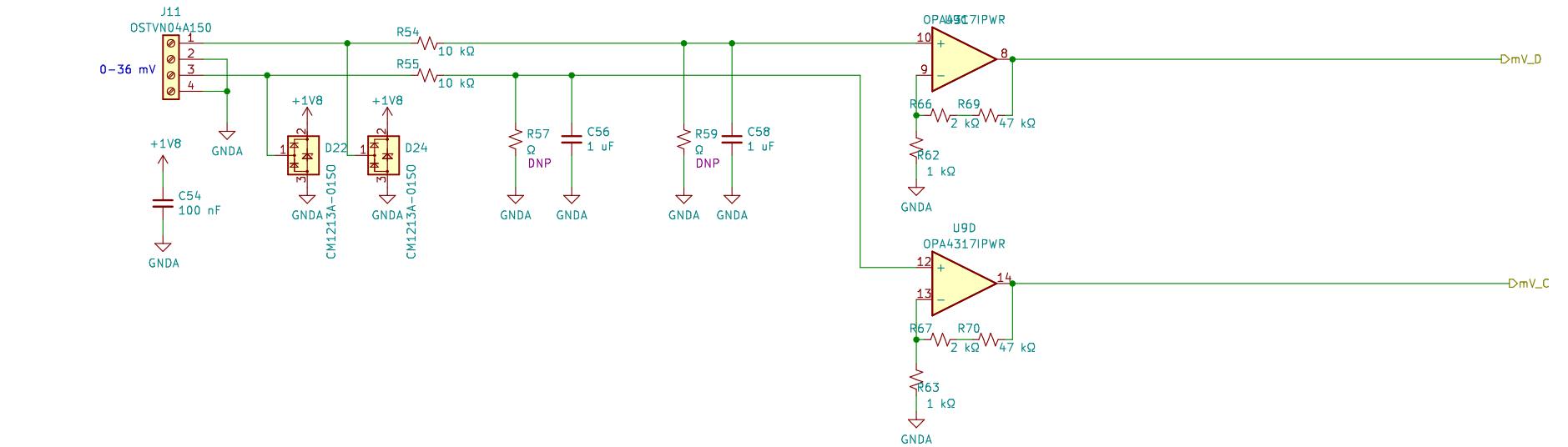
All capacitors X7R or COG unless otherwise noted.
 All resistors 1% unless otherwise noted.



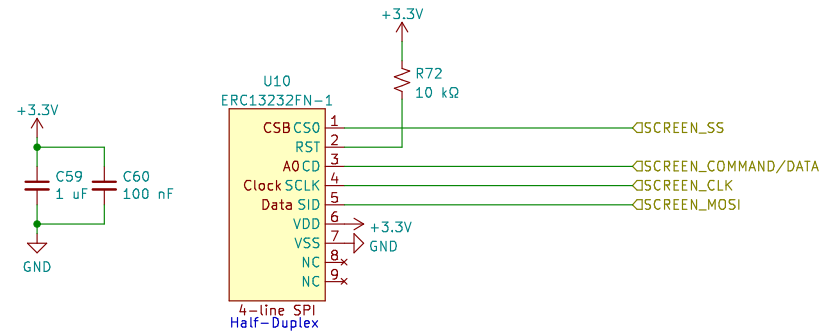
Place TVSs near exposed connector



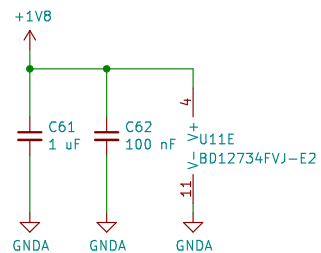
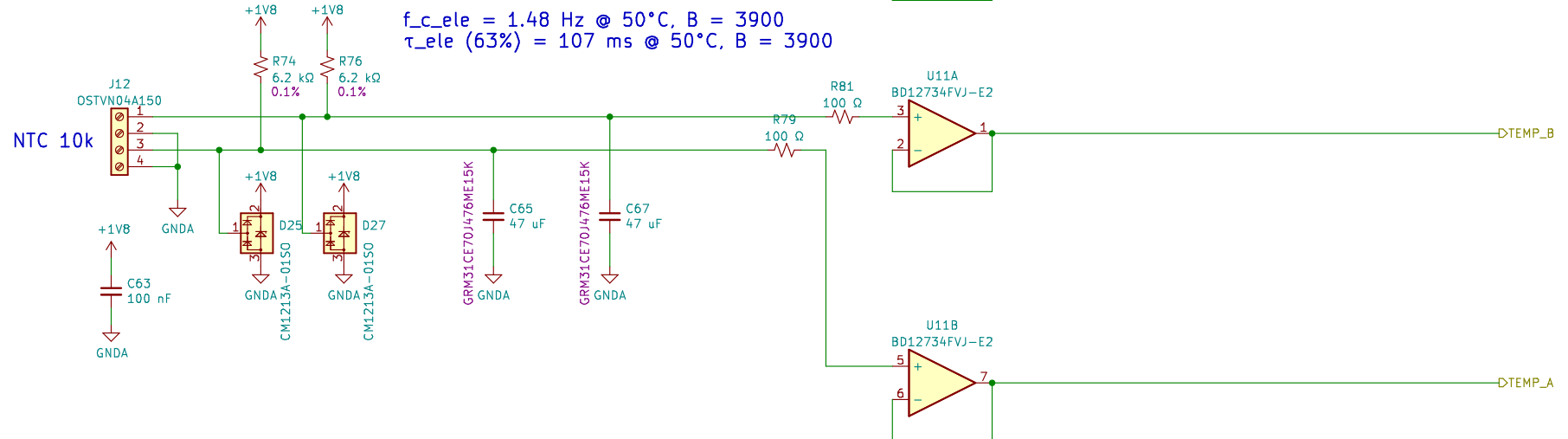
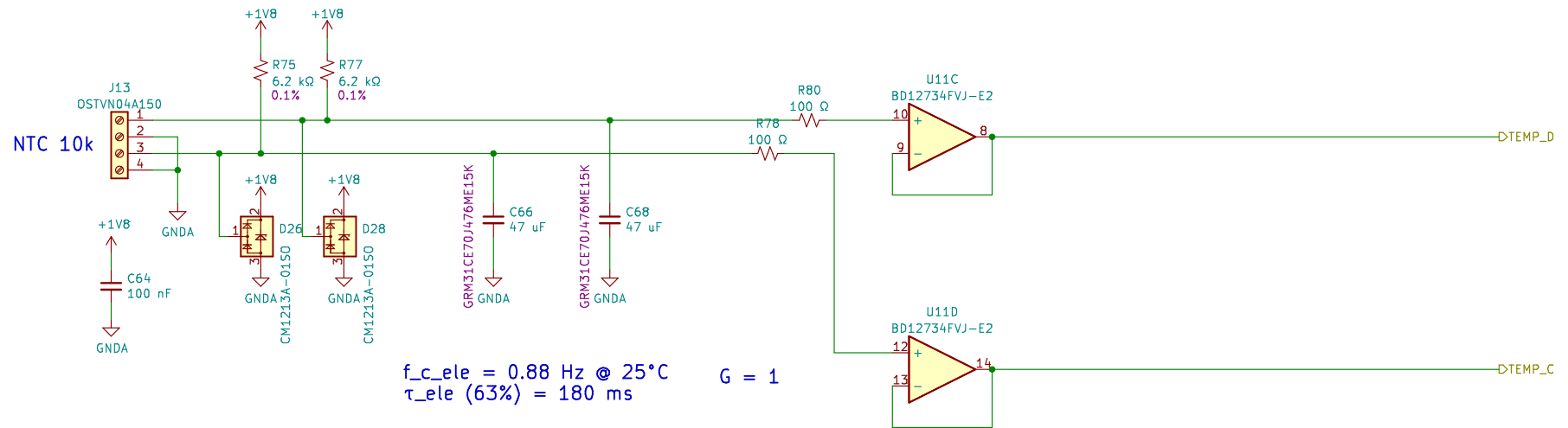
All capacitors X7R or C0G unless otherwise noted.
 All resistors 1% unless otherwise noted.



All capacitors X7R or C0G unless otherwise noted.
 All resistors 1% unless otherwise noted.



All capacitors X7R or C0G unless otherwise noted.
All resistors 1% unless otherwise noted.



All capacitors X7R or COG unless otherwise noted.
 All resistors 1% unless otherwise noted.