CSSE2010

CSSE2010/CSSE7201
Lecture 6

Sequential Circuits 1
Shift Registers

School of Information Technology and Electrical Engineering
The University of Queensland

Outline

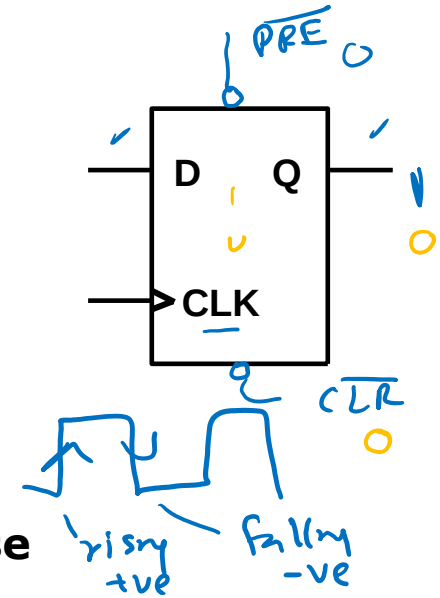
- Admin
- Sequential circuits
- Shift registers

Admin

- Quiz 2 is due this week Friday (12-Mar) 4pm
- Labs 6 and 7 for next week (week 4) has preparation tasks which should be attempted before coming to the labs.

Reminder
Memory element: D Flip Flop

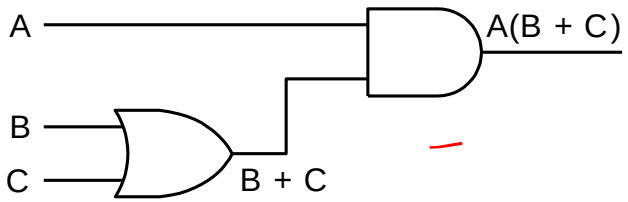
- **D** is input
- **Q** is output
- **CLK** (clock) is control input
- How does it work?
  - Q copies the value of D (and remembers it) whenever CLK goes from 0 to 1 (*rising edge*)



- **Only D Flip flops are discussed in this course**
- **Optional asynchronous SET and CLR inputs to set and clear the output Q even outside clock edges. The SET and CLR inputs are typically active-low.**
- **Using D flip flops one can design sequential circuits – e.g. counters**

Combinational vs. Sequential Circuits

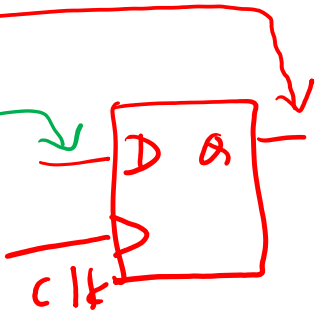
- **Combinational** Circuits (last week and earlier)
  - Logic gates only (no flip-flops)
  - Output is uniquely determined by the inputs
    - i.e. you'll always get the same output for a given set of inputs
  - Example:

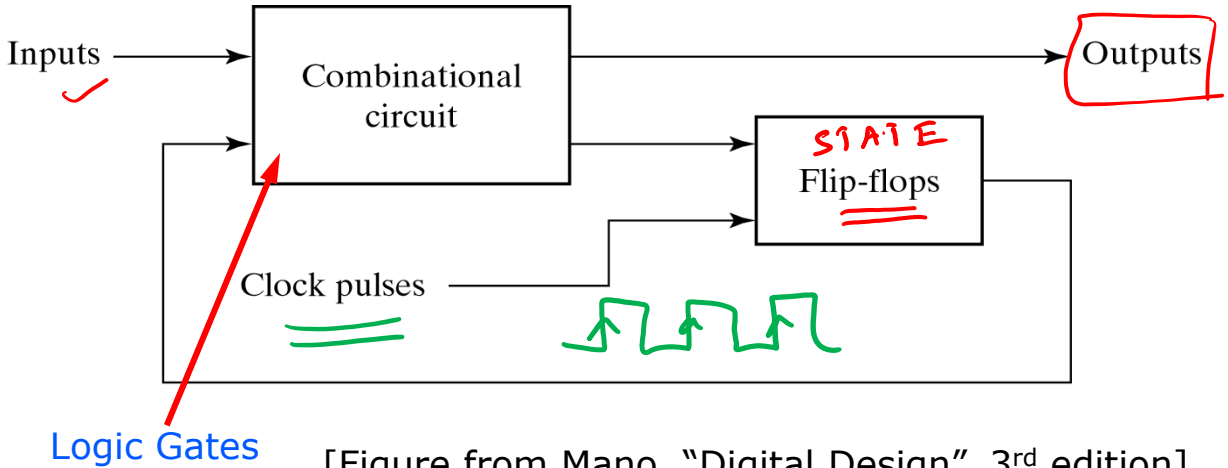


- **Sequential** Circuits
  - Include flip-flops
  - Output determined by current inputs and current **state** (values in the flip-flops)
  - Output can change when clock 'ticks'

Sequential Circuits

- **State** = value stored in flip-flops
- There is a notion of present state and next state
- Output depends on input and state
  - Or sometimes just the state
- Next state depends on inputs and state

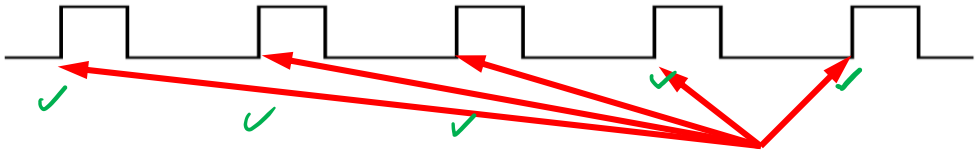




[Figure from Mano, "Digital Design", 3rd edition]

Synchronous Sequential Circuit

- Storage elements (flip-flops) can only change at discrete instants of time
- Assume
  - We have a clock signal:

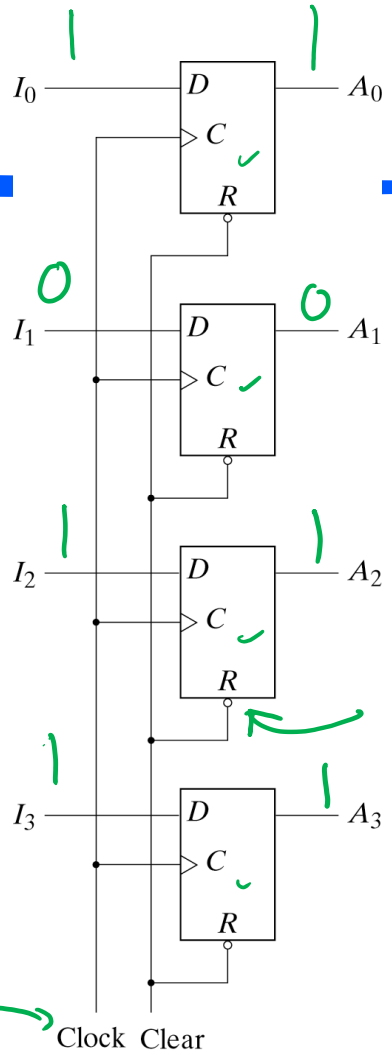


  - Output of storage elements change only on the edges of control signal
    - (compare with logic gates whose output changes whenever the input changes)

In a synchronous sequential circuit, all the sequential elements share a common clock signal. i.e., they are synchronised to a common clock.

Registers

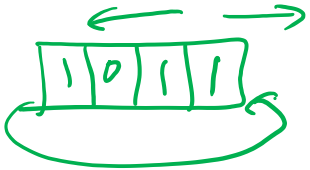
- A **register** is a group of flip-flops
  - *n*-bit register consists of *n* flip-flops capable of storing *n* bits
- Example
  - 4-bit register



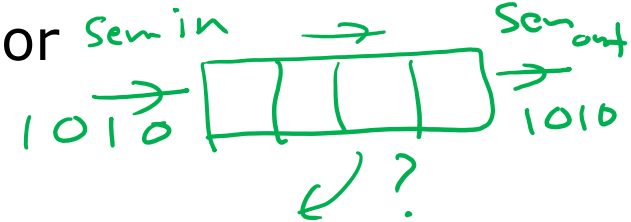
- A register is a sequential circuit *without* any combinational logic
- Registers are used to store binary information (data/instructions) inside a processor

[Mano, Digital Design, 3rd ed.]

Shift Register



- A shift register is a register which is capable of shifting its binary information in one or both directions



- Example:

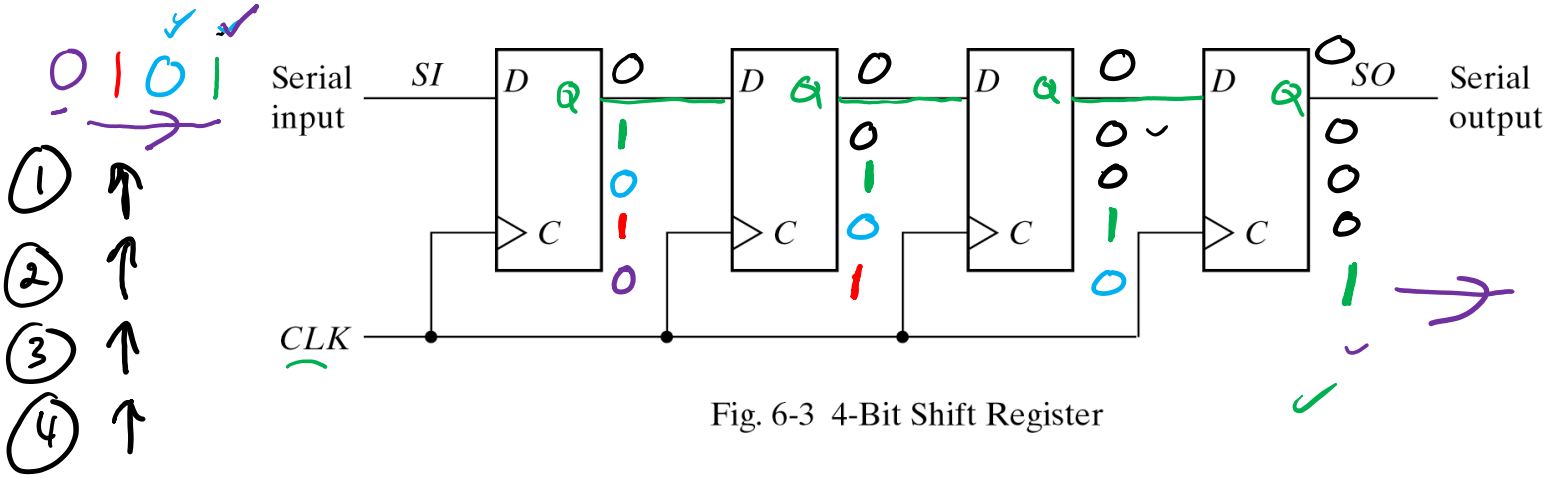
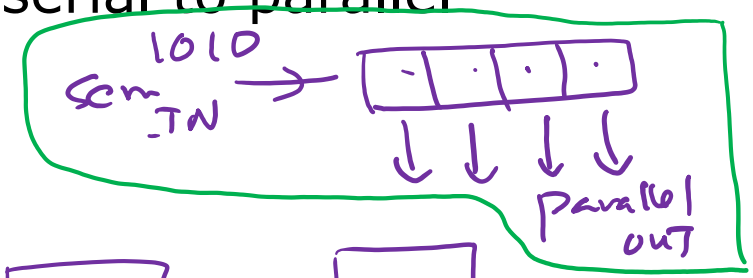


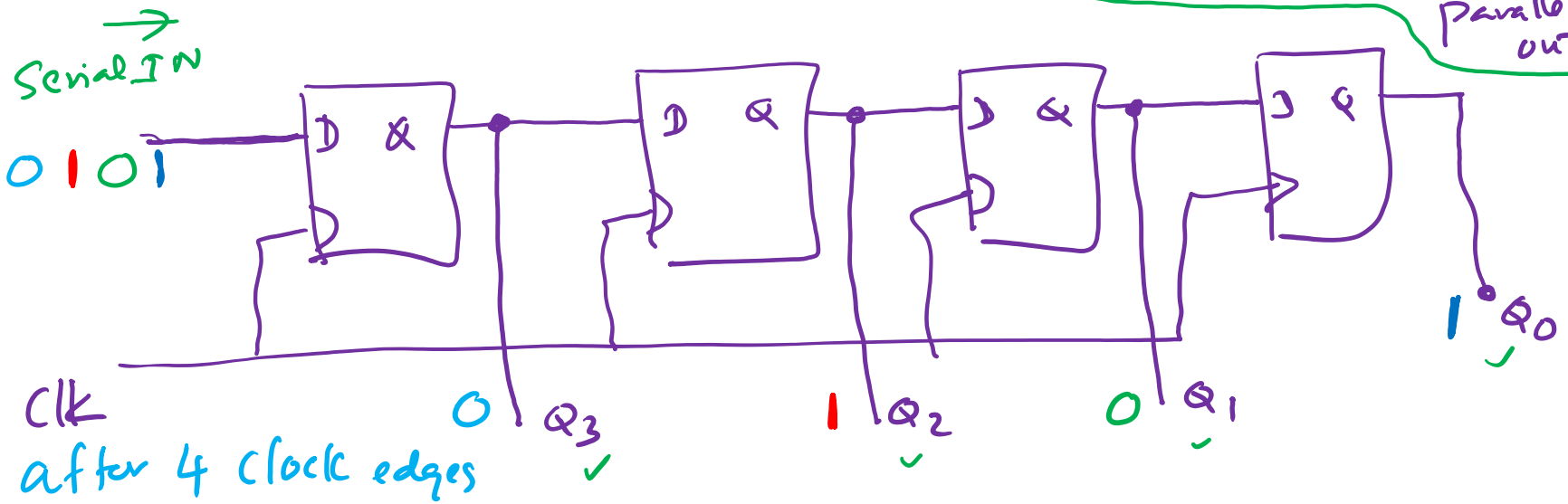
Fig. 6-3 4-Bit Shift Register

[Mano, Digital Design,3rd ed.]

Serial ⇔ Parallel Conversion

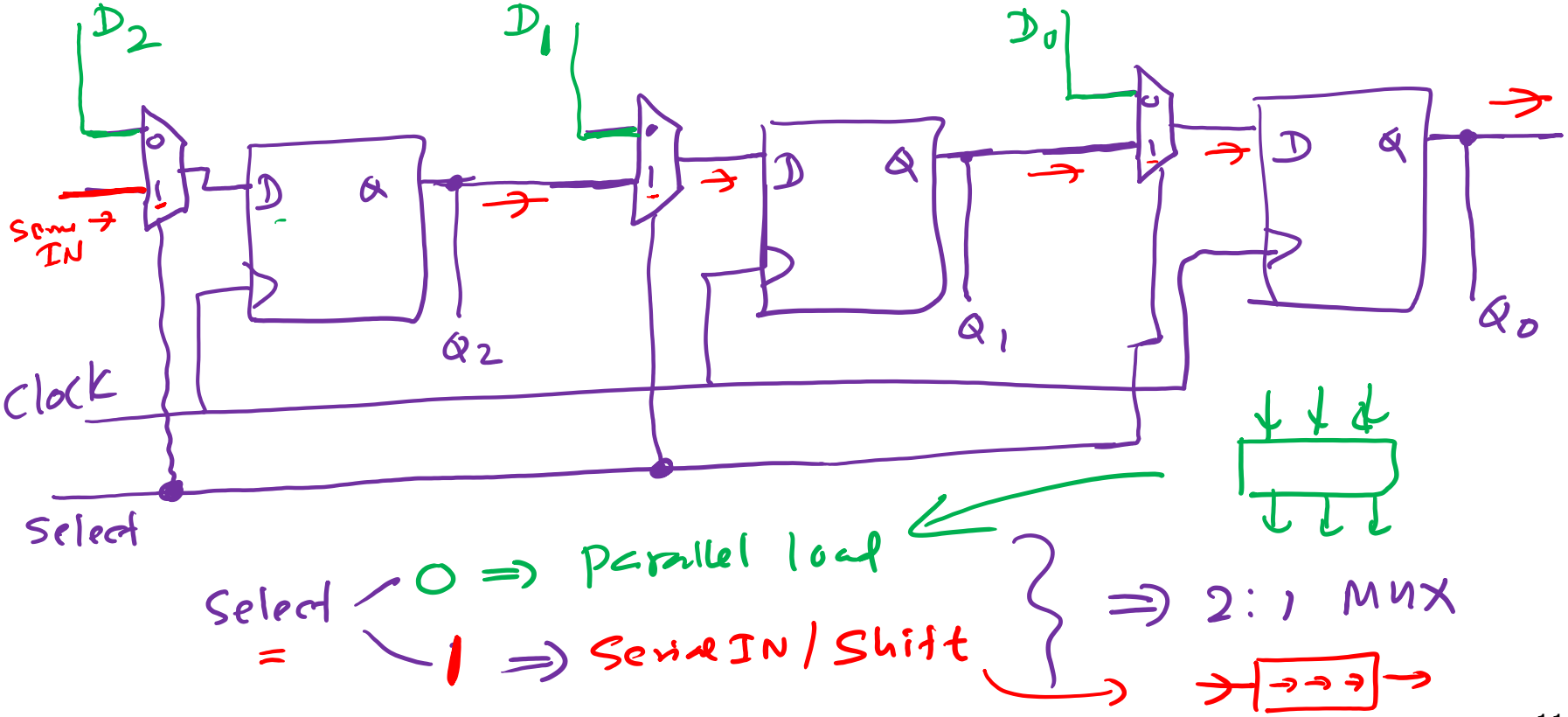
- Shift registers can be used to do serial to parallel conversion (and vice-versa)
- *(Figure to be drawn in class)*





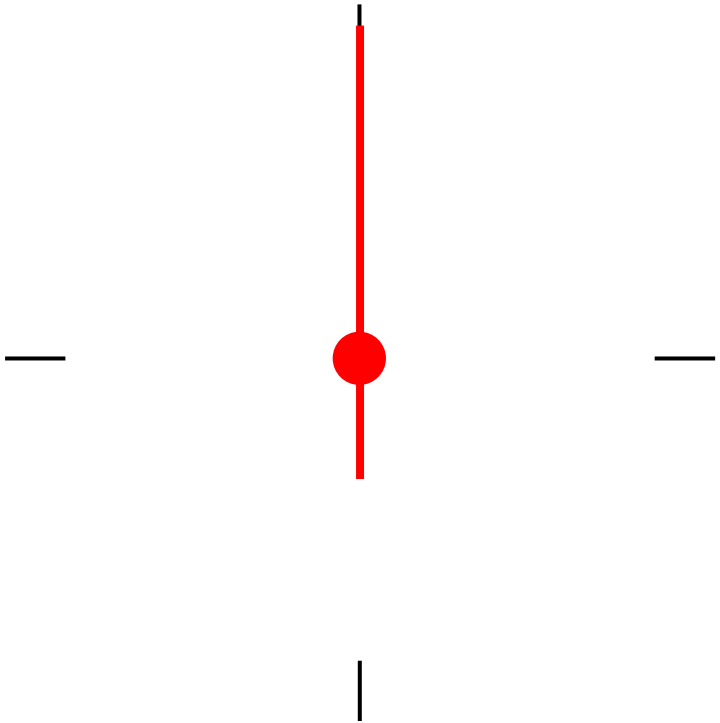
Parallel to Serial and Serial to Parallel

(3 bit)



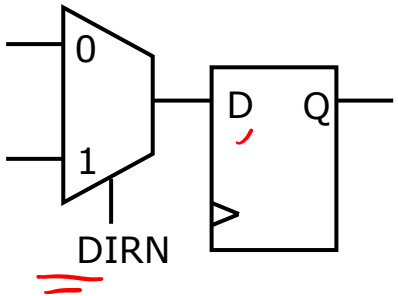
Short Break

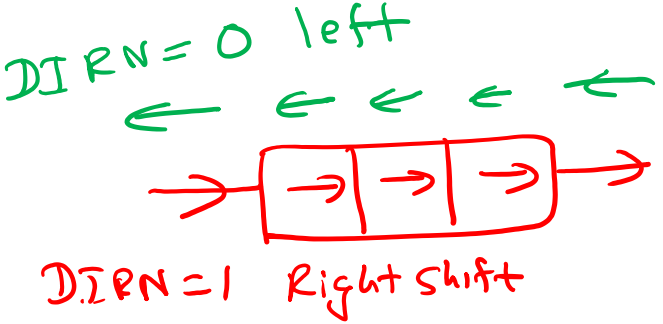
- Stand up and stretch



Exercise: Bidirectonal shift register

- Using same multiplexer concept, draw a 3-bit shift register which allows data to be shifted in either direction
- Hint: consider this element, where DIRN will be 0 for left shift, 1 for right shift

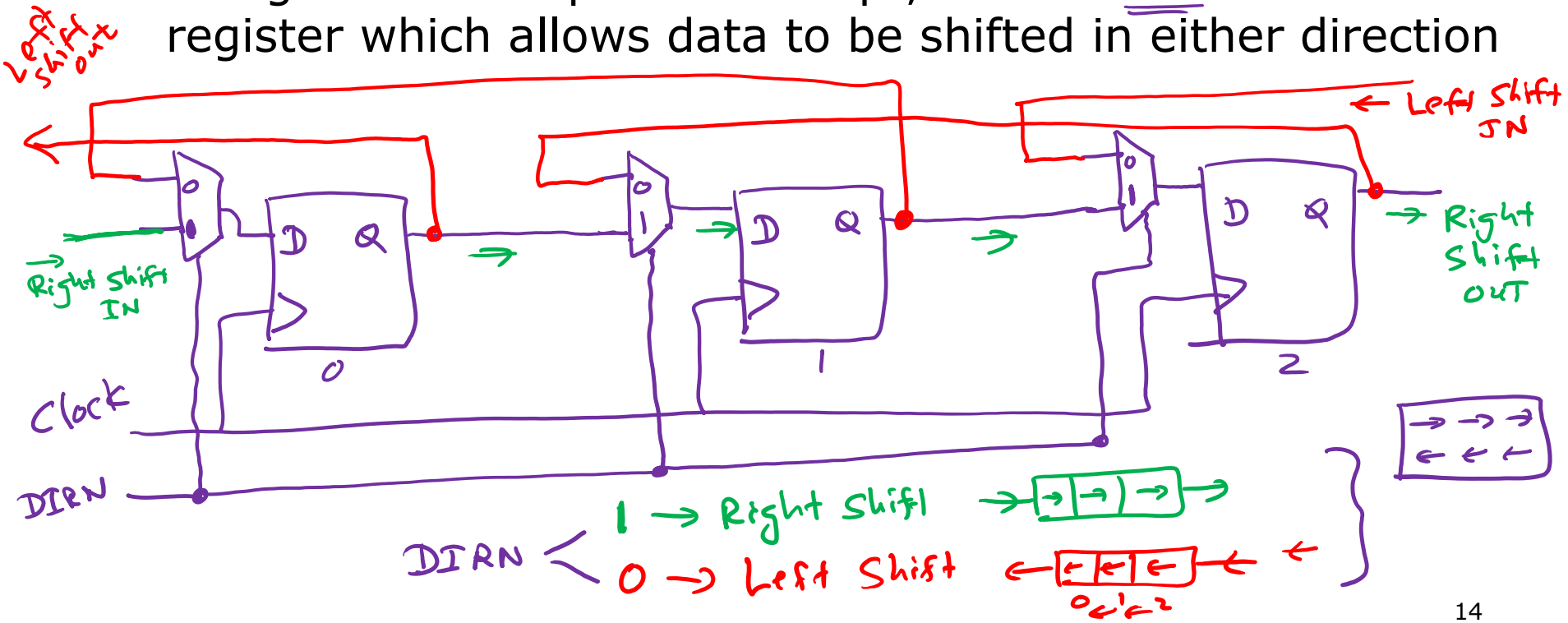




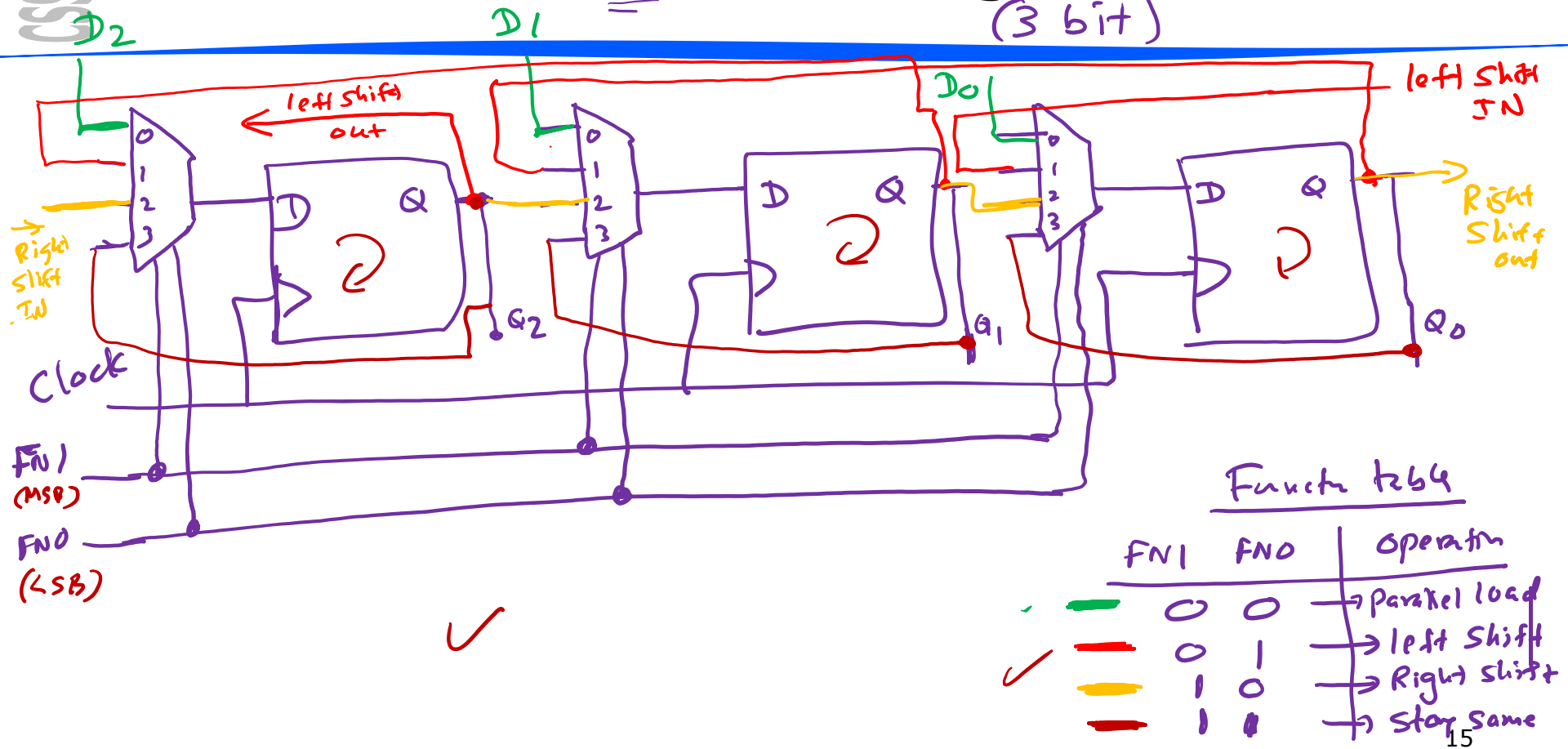
You have 2 minutes

Exercise: Bidirectonal shift register

- Using same multiplexer concept, draw a 3-bit shift register which allows data to be shifted in either direction



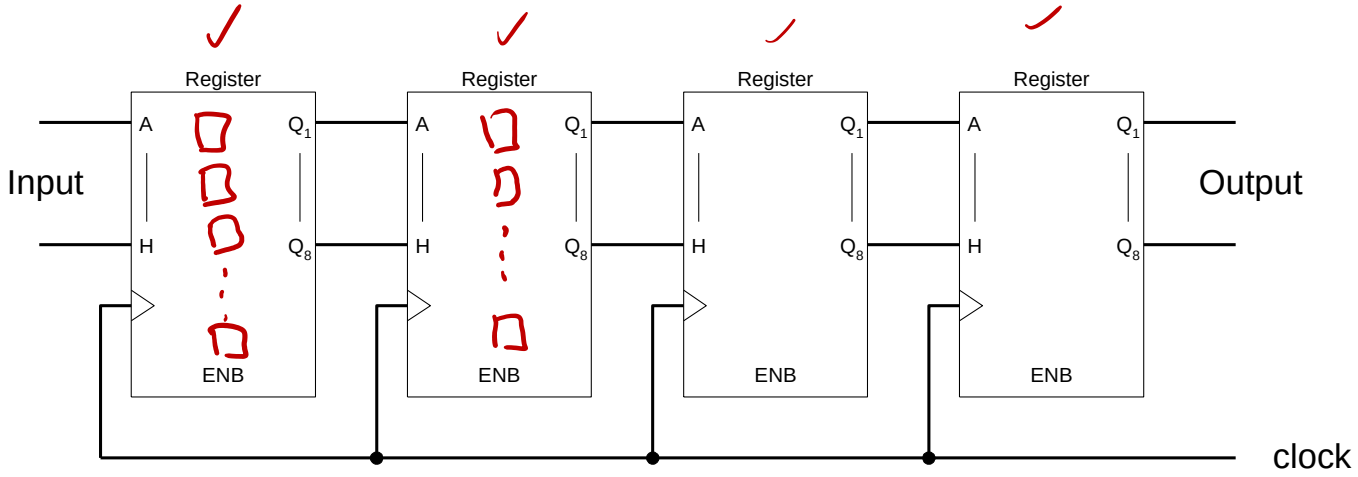
Universal Shift Register



Universal Shift Register

8-bit Wide Shift Register

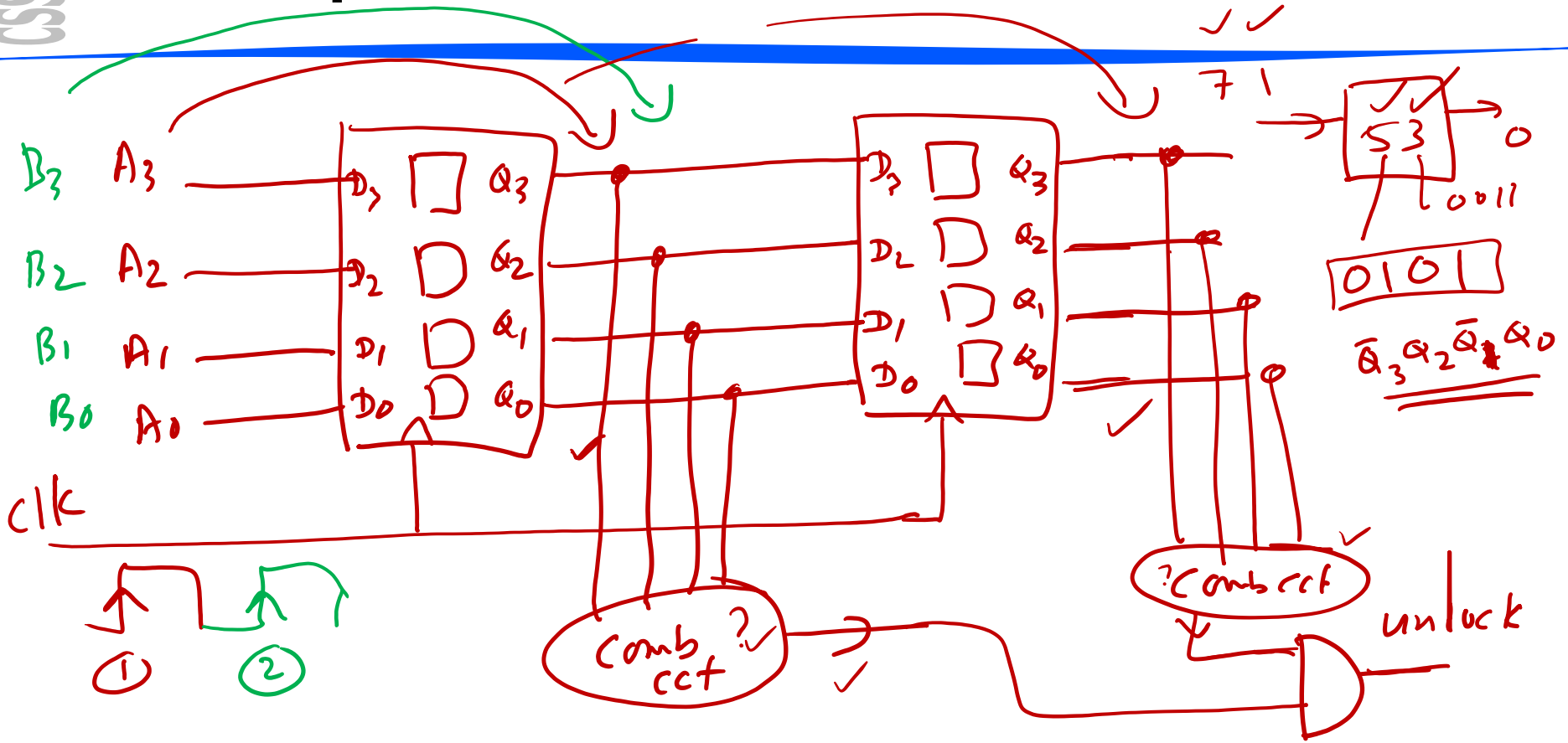
- Multiple bits shifted at a time
- Example 4-stage 8-bit queue:



Lab 06 Preparation Task – to be discussed in class

2-digit lock/unlock circuit: User inputs two decimal digital (4 bits each) AB in serial and the circuit should match the two input digits with a code (say CD) and unlock if the input matches with the code (i.e. AB=CD).

Lab 06 Preparation Task – to be discussed in class



Reminders

- Quiz 2 due Friday 4pm
- Lab 6/7 preparation tasks for next week