CSSE2010 / CSSE7201 – Introduction to Computer Systems
Exercises – Week Five
ALU, Memory

Exercises

Some of the questions below are taken from or based on questions in Tanenbaum, Structured Computer Organisation, 5th edition.

1. A small memory chip has 4096 cells each of 4 bits. How many address and data lines does it need? How many flip-flops are contained within this chip?
2. Which of the following are possible memory organisations? Which are reasonable? Explain.
   (a) 10-bit address, 1024 cells, 8-bit cell size
   (b) 10-bit address, 1024 cells, 12-bit cell size
   (c) 9-bit address, 1024 cells, 10-bit cell size
   (d) 11-bit address, 1024 cells, 10-bit cell size
   (e) 10-bit address, 10 cells, 1024-bit cell size
   (f) 1024-bit address, 10 cells, 10-bit cell size
3. Sometimes it is useful for an 8-bit ALU such as that presented in the week 5 lectures (made up of eight 1-bit ALUs) to generate the constant –1 as output. Give two different ways this can be done. For each way, specify the values of the six control signals (F_1, F_0, ENA, ENB, INVA, INC).
4. For the ALU shown in lectures, give three different combinations of the six control signals (F_1, F_0, ENA, ENB, INVA, INC) which will result in the output being B. (Hint: one answer is given in the table in the lecture notes. Which of the other functions, besides OR can be utilised to produce B?)

Additional Exercise

The exercise below goes beyond the learning objectives of the course but may help you develop a greater understanding of the course material.

5. A 16-bit ALU is built up of 16 1-bit ALUs, each having an add time of 10ns (nanosecond, 10^{-9} sec). If there is an additional 1ns delay for carry propagation time from one ALU to the next, how long does it take for the result of a 16-bit add to appear?