

CSSE2010/CSSE7201 Learning Lab 8

State Machines

School of Information Technology and Electrical Engineering
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Learning Lab 8 - State Machines

- State Machines
 - Two Design Exercises
 - Do hand design first state diagram → state table → next state logic and output logic
 - Implementation and test in Logisim
- This material is directly related to assignment 1 part 2.
- Also, watch LEC 08 Example FSM Design 1 & 2 videos on Blackboard.
- No polling questions today



Design Task 1 – Sequence Detector

- Draw a state diagram for a system that detects the sequence 001 in a series of bits
 - Input: S
 - Output: X

The output X is 1 whenever the sequence 001 is detected on the input S (i.e. 0 followed by 0 followed by 1).

Example input sequence S=00101010010001Example output sequence X=00100000010001



Design Task 1 – Sequence Detector

- Write down a 2-dimensional state table
- Choose a state encoding
 - State encoding = number of flip-flops and their values in each state
 - Examine different options for state encoding
- Write down a 1-dimensional state table using your encoding
- Determine Boolean expressions for the output (X) and the next state (flip-flop inputs, D's) in terms of the current state (flip-flop outputs, Q's) and input (S)
- Enter the circuit into Logisim and simulate it



Design Task 2 – Sequence Matching

- Consider a sequence matching system with
 - 2 inputs A, B
 - 2 outputs X, Y
 - X is 1 if A and B have been the same value (i.e. both 0 or both 1) twice or more in a row, otherwise 0
 - Y is 1 if the A and B values are different, otherwise 0
 - Initially the A and B values are assumed to have been different and Y should be 1
- Draw a state diagram and discuss with tutoring staff
- Implement:
 - Write down a 2-D state table
 - Choose a state encoding
 - Write down a 1-D state table
 - Determine Boolean expressions for the outputs and the next state (flip-flop inputs, D's) in terms of the current state (flip-flop outputs, Q's) and inputs
 - Enter the circuit into Logisim and simulate