CSSE2010/CSSE7201 Lecture 4

Combinational Logic

School of Information Technology and Electrical Engineering
The University of Queensland



Today...

- Admin
- Binary Subtractors
- More Combinational Logic Circuits
 - Multiplexers
 - Decoders
 - Timing diagram representations



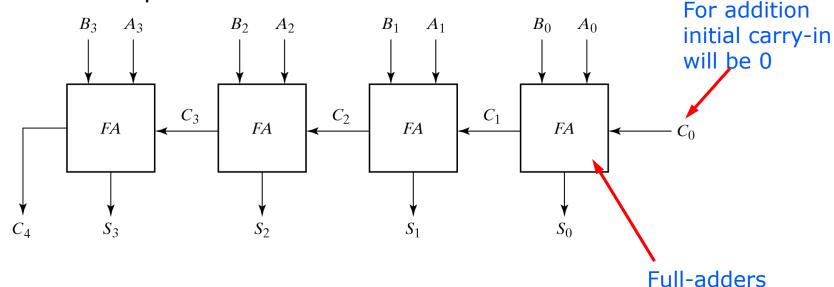
Admin

- Quiz 1 due on Friday 4pm no extensions for quizzes
- Lab 4 preparation task next week (week 3)
 - Will be Available on Blackboard: Learning Resources
 - Draw some circuit schematic diagrams
 - Bring to Lab 4 (Mon-Tue next week)
 - IN students use Logic ICs on breadboards or Logisim
 - EX students use Logisim software to simulate
- Supporting material for labs are now on Blackboard



Recall – Binary Adder

- Can cascade full adders to make binary adder
 - Example: for 4 bits...



This is a ripple-carry adder



Binary subtraction

- A-B usually implemented as A+(-B)
 - A and B are multi-bit quantities
 - "+" in this case means addition (not OR)
 - -B means negative B the two's complement of B
- Two's complement of B can be calculated by flipping bits and adding 1



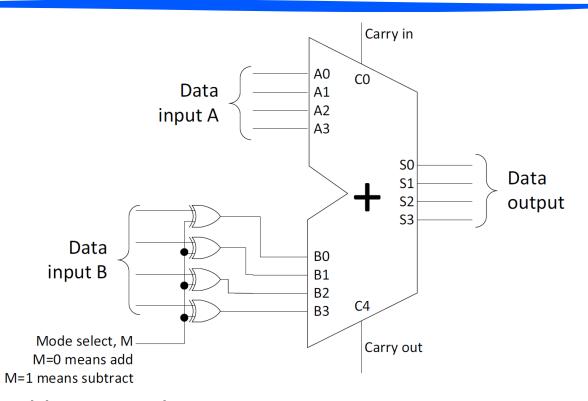
Binary subtraction (cont.)

 How we can use a gate to flip a bit – but only sometimes? i.e.

Z=not(B) when M is 1Z=B when M is 0



Adder-subtractor

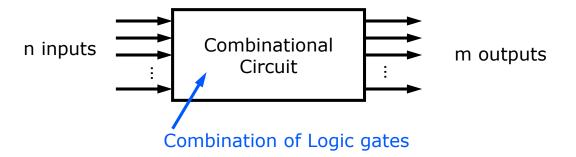


• What should carry-in be?



Combinational Circuits

Generally,



- Each output can be expressed as function of n input variables
- Output depends on current inputs only
- Can write truth table also:
 - n input columns
 - m output columns
 - 2ⁿ rows (i.e. possible input combinations)

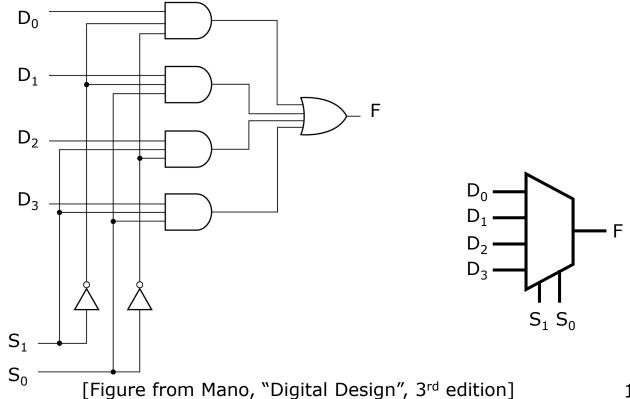


Multiplexer (or Mux)

- 2ⁿ data inputs
- 1 output
- n control (or select) inputs that select one of the inputs to be "sent" or "steered" to the output



4-to-1 Multiplexer Logic Circuit Implementation





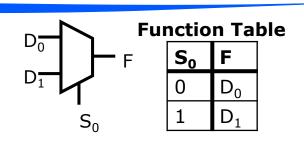
Clicker Question: 2-to-1 Multiplexer

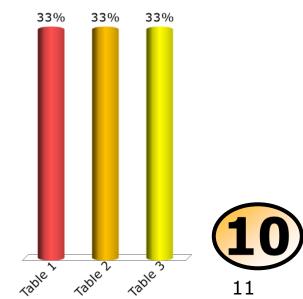
- Consider a 2-to-1 multiplexer
 - Data Inputs: D₀ and D₁
 - Control Input: S₀
 - Output: F
- What is the truth table that goes with this circuit?

1.	S ₀	Do	D_1	F
	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	0
	1	1	0	1
	1	1	1	1

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2.	S ₀	D_0	D_1	F	
	0	0	0	0	
	0	0	1	0	
	0	1	0	1	
	0	1	1	1	
	1	0	0	0	
	1	0	1	1	
	1	1	0	0	
	1	1	1	1	

Turis circuit:						
3.	S ₀	D_0	D_1	F		
	0	0	0	0		
	0	0	1	0		
	0	1	0	0		
	0	1	1	0		
	1	0	0	1		
	1	0	1	1		
	1	1	0	1		
	1	1	1	1		







Clicker Question (2)

Consider the multiplexer shown. What must the inputs A,B,C,D be so that the multiplexer output is $V = \overline{C} + C$

Sultiplexer output is
$$X = \overline{S_0} + S_1$$

$$B = 1$$

$$C = 3$$

$$D = 3$$

$$S_0$$

$$^{0\%}$$
 1.A=0, B=1, C=0, D=0

$$^{0\%}$$
 3.A=1, B=0, C=1, D=1





Short Break

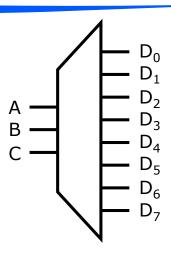
Stand up and stretch



Decoder

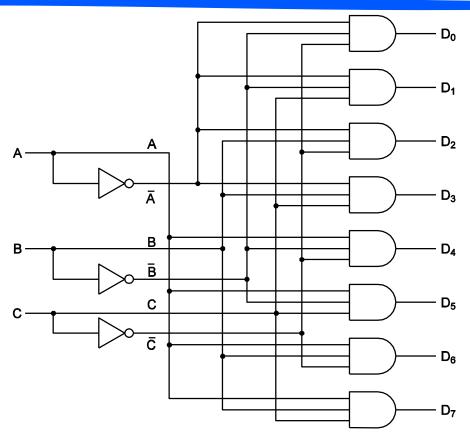
- Converts n-bit input to a logic-1 on exactly one of 2ⁿ outputs
- Example:3-to-8 decoder

Α	В	С	D_0	D_1	D ₂	D_3	D ₄	D ₅	D_6	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0



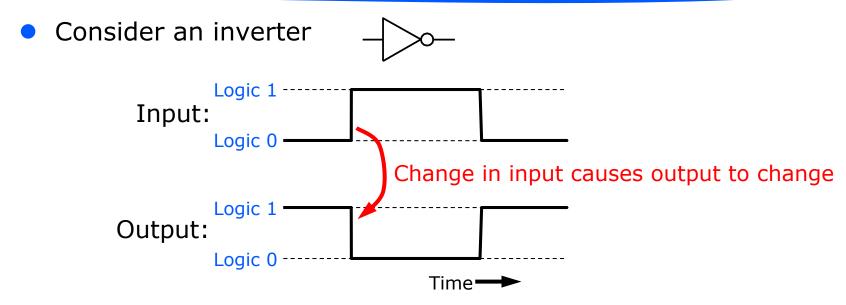


3-to-8 Decoder Logic Circuit Implementation





Another Logic Representation: Timing Diagram

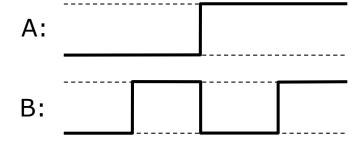


- Like a truth table, but graphical format
 - Input waveforms show all possible combinations



Consider a 2-input gate

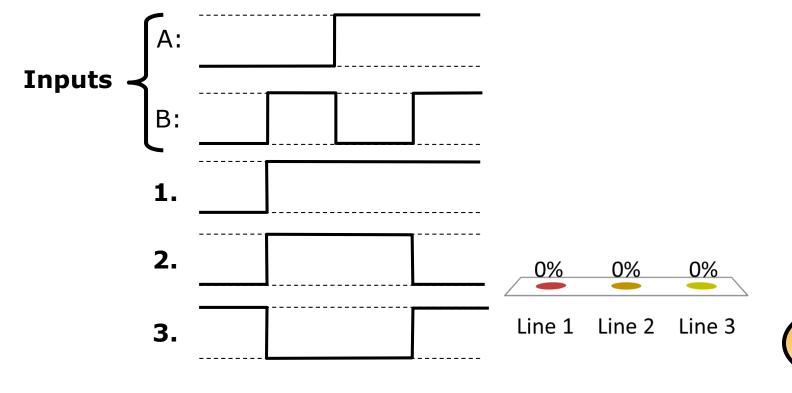
Possible inputs



All combinations of inputs are covered

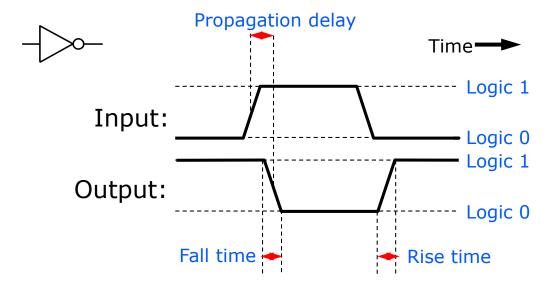


Which of the following is a timing diagram representation for an XOR gate?





Gates Aren't Perfect ... The Reality of Timing



- Propagation delay time for change in input to affect output
- Fall time time taken for output to fall from 1 to 0
- Rise time time for output to rise from 0 to 1



Things To Do

- Complete quiz 1 by Friday 4pm this week
- Homework Lab 4 preparation
 - By Lab 4 sessions on week 3
- Attempt the posted exercises and selfcheck questions
- Any doubts, use course consultation (need to book a time) or ask after the lecture.