

# CSSE2010 Assignment 1 – Part 2

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## Design

### 1. State Diagram

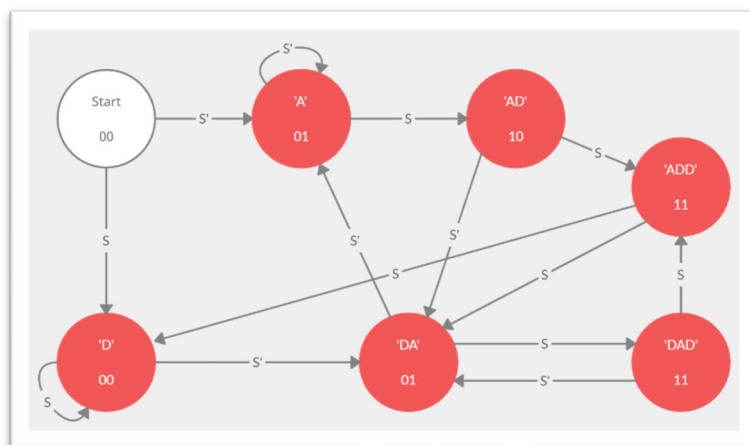
In the process of designing a circuit to detect the length of a word entered by a user, the different states of the machine first need to be determined.

As specified in the task sheet, the circuit must detect the following words (as described in the table) and output the length of these words:

Word	Word Length (Output)
"A"	1
"AD"	2
"ADD"	3
"DAD"	3

However, these are **not** all the states the circuit can exhibit. For example, in order to reach a state of "DAD", the circuit must be in the state of "D" then "DA" before it can be in a state of "DAD". Additionally, there must be a "Start" or empty state when the circuit is first powered on which indicates no characters have been inputted (i.e. the clock has not yet had its first rising edge).

Therefore, the possible states this machine can be in are defined below in the state diagram. The arrows represent the possible transitions that occur with  $S$  and  $\bar{S}$  representing the inputs of "D" and "A" respectively. Note that the output for the length will use two bits and follow the following encoding



Word Length	Encoding
0	00
1	01
2	10
3	11

## 2. Two-Dimensional (2D) State Table

Current State	Next State		Outputs	
	S	S'	X1	X0
Start	"D"	"A"	0	0
"A"	"AD"	"A"	0	1
"AD"	"ADD"	"DA"	1	0
"ADD"	"D"	"DA"	1	1
"D"	"D"	"DA"	0	0
"DA"	"DAD"	"A"	0	1
"DAD"	"ADD"	"DA"	1	1

## 3. State Encodings

One-Hot Encoding		Binary Encoding	
State	Encoding	State	Encoding
Start	0000001	Start	000
"A"	0000010	"A"	001
"AD"	0000100	"AD"	010
"ADD"	0001000	"ADD"	011
"D"	0010000	"D"	100
"DA"	0100000	"DA"	101
"DAD"	1000000	"DAD"	110
		Undefined	111

#### 4. State Tables for Encodings

##### One Hot-Encoding

State Name	Encoding							Input	Next State								Outputs	
	Q6	Q5	Q4	Q3	Q2	Q1	Q0	S	D6	D5	D4	D3	D2	D1	D0	X1	X0	
Start	0	0	0	0	0	0	1	S	0	0	1	0	0	0	0	0	0	
Start	0	0	0	0	0	0	1	~S	0	0	0	0	0	1	0	0	0	
"A"	0	0	0	0	0	1	0	S	0	0	0	0	1	0	0	0	1	
"A"	0	0	0	0	0	1	0	~S	0	0	0	0	0	1	0	0	1	
"AD"	0	0	0	0	1	0	0	S	0	0	0	1	0	0	0	1	0	
"AD"	0	0	0	0	1	0	0	~S	0	1	0	0	0	0	0	1	0	
"ADD"	0	0	0	1	0	0	0	S	0	0	1	0	0	0	0	1	1	
"ADD"	0	0	0	1	0	0	0	~S	0	1	0	0	0	0	0	1	1	
"D"	0	0	1	0	0	0	0	S	0	0	1	0	0	0	0	0	0	
"D"	0	0	1	0	0	0	0	~S	0	1	0	0	0	0	0	0	0	
"DA"	0	1	0	0	0	0	0	S	1	0	0	0	0	0	0	0	1	
"DA"	0	1	0	0	0	0	0	~S	0	0	0	0	0	1	0	0	1	
"DAD"	1	0	0	0	0	0	0	S	0	0	0	1	0	0	0	1	1	
"DAD"	1	0	0	0	0	0	0	~S	0	1	0	0	0	0	0	1	1	

##### Binary Encoding

State Name	Encoding			Input	Next State			Outputs	
	Q2	Q1	Q0	S	D2	D1	D0	X1	X0
Start	0	0	0	S	1	0	0	0	0
Start	0	0	0	~S	0	0	1	0	0
"A"	0	0	1	S	0	1	0	0	1
"A"	0	0	1	~S	0	0	1	0	1
"AD"	0	1	0	S	0	1	1	1	0
"AD"	0	1	0	~S	1	0	1	1	0
"ADD"	0	1	1	S	1	0	0	1	1
"ADD"	0	1	1	~S	1	0	1	1	1
"D"	1	0	0	S	1	0	0	0	0
"D"	1	0	0	~S	1	0	1	0	0
"DA"	1	0	1	S	1	1	0	0	1
"DA"	1	0	1	~S	0	0	1	0	1
"DAD"	1	1	0	S	0	1	1	1	1
"DAD"	1	1	0	~S	1	0	1	1	1
Undefined	1	1	1	S	1	0	0	0	0
Undefined	1	1	1	~S	0	0	1	0	0

## 5. Boolean Logic

## One Hot Encoding

$X_0 = 1$  when

$$\begin{aligned}
& \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 S} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 \bar{S}} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 S} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 \bar{S}} \\
& \quad + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 S} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 \bar{S}} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 S} \\
& \quad + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 \bar{S}} \\
= & \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 (S + \bar{S})} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 (S + \bar{S})} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 (S + \bar{S})} \\
& \quad + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 (S + \bar{S})} \\
= & \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0} + \overline{Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0} \\
= & \overline{Q_4 Q_2 Q_0 (Q_6 Q_5 Q_3 Q_1 + Q_6 Q_5 Q_3 Q_1 + Q_6 Q_5 Q_3 Q_1 + Q_6 Q_5 Q_3 Q_1)} \\
= & \overline{Q_4 Q_2 Q_0 (Q_6 Q_5 (Q_3 Q_1 + Q_3 Q_1) + Q_3 Q_1 (Q_6 Q_5 + Q_6 Q_5))} \\
= & \overline{Q_4 Q_2 Q_0 (Q_6 Q_5 (Q_3 \oplus Q_1) + Q_3 Q_1 (Q_6 \oplus Q_5))}
\end{aligned}$$

$X_1 = 1$  when

$$\begin{aligned}
& \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} \\
& \quad + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} \\
& = \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} (S + \overline{S}) + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} (S + \overline{S}) + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} (S + \overline{S}) \\
& = \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \\
& = \overline{Q_5} \overline{Q_4} \overline{Q_1} \overline{Q_0} (\overline{Q_6} \overline{Q_3} \overline{Q_2} + \overline{Q_6} \overline{Q_3} \overline{Q_2} + \overline{Q_6} \overline{Q_3} \overline{Q_2}) \\
& = \overline{Q_5} \overline{Q_4} \overline{Q_1} \overline{Q_0} (\overline{Q_6} (\overline{Q_3} \overline{Q_2} + \overline{Q_3} \overline{Q_2}) + \overline{Q_6} \overline{Q_3} \overline{Q_2}) \\
& = \overline{Q_5} \overline{Q_4} \overline{Q_1} \overline{Q_0} (\overline{Q_6} (\overline{Q_3} \oplus \overline{Q_2}) + \overline{Q_6} \overline{Q_3} \overline{Q_2})
\end{aligned}$$

$D_0 = 1$  never

 $D_1 = 1$  when

$$\begin{aligned} & \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} Q_0 \bar{S} + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} Q_1 \overline{Q_0} \bar{S} + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \bar{S} \\ &= \overline{Q_6} \overline{Q_4} \overline{Q_3} \overline{Q_2} \bar{S} (\overline{Q_5} \overline{Q_1} Q_0 + \overline{Q_5} Q_1 \overline{Q_0} + Q_5 \overline{Q_1} \overline{Q_0}) \\ &= \overline{Q_6} \overline{Q_4} \overline{Q_3} \overline{Q_2} \bar{S} (\overline{Q_5} (Q_1 Q_0 + Q_1 \overline{Q_0}) + Q_5 \overline{Q_1} \overline{Q_0}) \\ &= \overline{Q_6} \overline{Q_4} \overline{Q_3} \overline{Q_2} \bar{S} (\overline{Q_5} (Q_1 \oplus Q_0) + Q_5 \overline{Q_1} \overline{Q_0}) \end{aligned}$$

 $D_2 = 1$  when

$$\overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S$$

 $D_3 = 1$  when

$$\begin{aligned} & \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S \\ &= \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_1} \overline{Q_0} S (\overline{Q_6} Q_2 + \overline{Q_6} \overline{Q_2}) \\ &= \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_1} \overline{Q_0} S (Q_6 \oplus Q_2) \end{aligned}$$

$D_4 = 1$  when

$$\begin{aligned} & \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} Q_0 S + \overline{Q_6} \overline{Q_5} \overline{Q_4} Q_3 \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_6} \overline{Q_5} Q_4 \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S \\ &= \overline{Q_6} \overline{Q_5} \overline{Q_2} \overline{Q_1} S (\overline{Q_4} \overline{Q_3} Q_0 + \overline{Q_4} Q_3 \overline{Q_0} + Q_4 \overline{Q_3} \overline{Q_0}) \\ &= \overline{Q_6} \overline{Q_5} \overline{Q_2} \overline{Q_1} S (\overline{Q_4} (Q_3 Q_0 + Q_3 \overline{Q_0}) + Q_4 \overline{Q_3} \overline{Q_0}) \\ &= \overline{Q_6} \overline{Q_5} \overline{Q_2} \overline{Q_1} S (\overline{Q_4} (Q_3 \oplus Q_0) + Q_4 \overline{Q_3} \overline{Q_0}) \end{aligned}$$

$D_5 = 1$  when

$$\begin{aligned} & \overline{Q_6} \overline{Q_5} \overline{Q_4} \overline{Q_3} Q_2 \overline{Q_1} \overline{Q_0} \overline{S} + \overline{Q_6} \overline{Q_5} \overline{Q_4} Q_3 \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} + \overline{Q_6} \overline{Q_5} Q_4 \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} + Q_6 \overline{Q_5} \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} \\ &= \overline{Q_5} \overline{Q_1} \overline{Q_0} \overline{S} (\overline{Q_6} \overline{Q_4} \overline{Q_3} Q_2 + \overline{Q_6} \overline{Q_4} Q_3 \overline{Q_2} + \overline{Q_6} Q_4 \overline{Q_3} \overline{Q_2} + Q_6 Q_4 \overline{Q_3} \overline{Q_2}) \\ &= \overline{Q_5} \overline{Q_1} \overline{Q_0} \overline{S} (\overline{Q_6} \overline{Q_4} (\overline{Q_3} Q_2 + Q_3 \overline{Q_2}) + \overline{Q_3} \overline{Q_2} (\overline{Q_6} Q_4 + Q_6 \overline{Q_4})) \\ &= \overline{Q_5} \overline{Q_1} \overline{Q_0} \overline{S} (\overline{Q_6} \overline{Q_4} (Q_3 \oplus Q_2) + \overline{Q_3} \overline{Q_2} (Q_6 \oplus Q_4)) \end{aligned}$$

$D_6 = 1$  when

$$\overline{Q_6} Q_5 \overline{Q_4} \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0} S$$

Binary Encoding

$X_0 = 1$  when

$$\begin{aligned} & \overline{Q_2} \overline{Q_1} Q_0 S + \overline{Q_2} \overline{Q_1} Q_0 \overline{S} + \overline{Q_2} Q_1 Q_0 S + \overline{Q_2} Q_1 Q_0 \overline{S} + Q_2 \overline{Q_1} Q_0 S + Q_2 \overline{Q_1} Q_0 \overline{S} + Q_2 Q_1 \overline{Q_0} S + Q_2 Q_1 \overline{Q_0} \overline{S} \\ &= \overline{Q_2} \overline{Q_1} Q_0 (S + \overline{S}) + \overline{Q_2} Q_1 Q_0 (S + \overline{S}) + Q_2 \overline{Q_1} Q_0 (S + \overline{S}) + Q_2 Q_1 \overline{Q_0} (S + \overline{S}) \end{aligned}$$

$X_1 = 1$  when

$$\begin{aligned} & \overline{Q_2} Q_1 \overline{Q_0} S + \overline{Q_2} Q_1 \overline{Q_0} \overline{S} + \overline{Q_2} Q_1 Q_0 S + \overline{Q_2} Q_1 Q_0 \overline{S} + Q_2 \overline{Q_1} \overline{Q_0} S + Q_2 \overline{Q_1} \overline{Q_0} \overline{S} \\ &= \overline{Q_2} Q_1 \overline{Q_0} (S + \overline{S}) + \overline{Q_2} Q_1 Q_0 (S + \overline{S}) + Q_2 \overline{Q_1} \overline{Q_0} (S + \overline{S}) \\ &= \overline{Q_2} Q_1 \overline{Q_0} + \overline{Q_2} Q_1 Q_0 + Q_2 \overline{Q_1} \overline{Q_0} \\ &= \overline{Q_2} (Q_1 \overline{Q_0} + Q_1 Q_0) + Q_2 \overline{Q_1} \overline{Q_0} \\ &= \overline{Q_2} (Q_1 (\overline{Q_0} + Q_0)) + Q_2 \overline{Q_1} \overline{Q_0} \\ &= \overline{Q_2} (Q_1) + Q_2 \overline{Q_1} \overline{Q_0} \\ &= \overline{Q_2} Q_1 + Q_2 \overline{Q_1} \overline{Q_0} \\ &= Q_1 (\overline{Q_2} + Q_2 \overline{Q_0}) \\ &= Q_1 (\overline{Q_2} + \overline{Q_0}) \end{aligned}$$

$D_0 = 1$  when

$$\begin{aligned} & \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} + Q_2 \overline{Q_1} \overline{Q_0} \overline{S} + \overline{Q_2} \overline{Q_1} Q_0 \overline{S} + Q_2 \overline{Q_1} Q_0 \overline{S} + \overline{Q_2} Q_1 \overline{Q_0} \overline{S} + Q_2 Q_1 \overline{Q_0} \overline{S} + \overline{Q_2} Q_1 Q_0 \overline{S} + Q_2 Q_1 Q_0 \overline{S} \\ &= \overline{Q_1} \overline{Q_0} \overline{S} (\overline{Q_2} + Q_2) + \overline{Q_1} Q_0 \overline{S} (\overline{Q_2} + Q_2) + Q_1 \overline{Q_0} \overline{S} (\overline{Q_2} + Q_2) + Q_1 Q_0 \overline{S} (\overline{Q_2} + Q_2) \\ &= \overline{Q_1} \overline{Q_0} \overline{S} + \overline{Q_1} Q_0 \overline{S} + Q_1 \overline{Q_0} \overline{S} + Q_1 Q_0 \overline{S} \\ &= \overline{Q_1} \overline{S} (\overline{Q_0} + Q_0) + Q_1 \overline{S} (\overline{Q_0} + Q_0) + Q_1 Q_0 \overline{S} \\ &= \overline{Q_1} \overline{S} + Q_1 \overline{Q_0} + Q_1 Q_0 \overline{S} \\ &= Q_1 (\overline{Q_0} + Q_0 \overline{S}) + \overline{Q_1} \overline{S} \\ &= Q_1 (\overline{Q_0} + \overline{S}) + \overline{Q_1} \overline{S} \end{aligned}$$

$D_1 = 1$  when

$$\begin{aligned}
 & \overline{Q_2} \overline{Q_1} Q_0 S + \overline{Q_2} Q_1 \overline{Q_0} S + Q_2 \overline{Q_1} Q_0 S + Q_2 Q_1 \overline{Q_0} S \\
 &= S(\overline{Q_2} \overline{Q_1} Q_0 + \overline{Q_2} Q_1 \overline{Q_0} + Q_2 \overline{Q_1} Q_0 + Q_2 Q_1 \overline{Q_0}) \\
 &= S(\overline{Q_1} Q_0 (\overline{Q_2} + Q_2) + Q_1 \overline{Q_0} (\overline{Q_2} + Q_2)) \\
 &= S(\overline{Q_1} Q_0 + Q_1 \overline{Q_0}) \\
 &= S(Q_1 \oplus Q_0)
 \end{aligned}$$

$D_2 = 1$  when

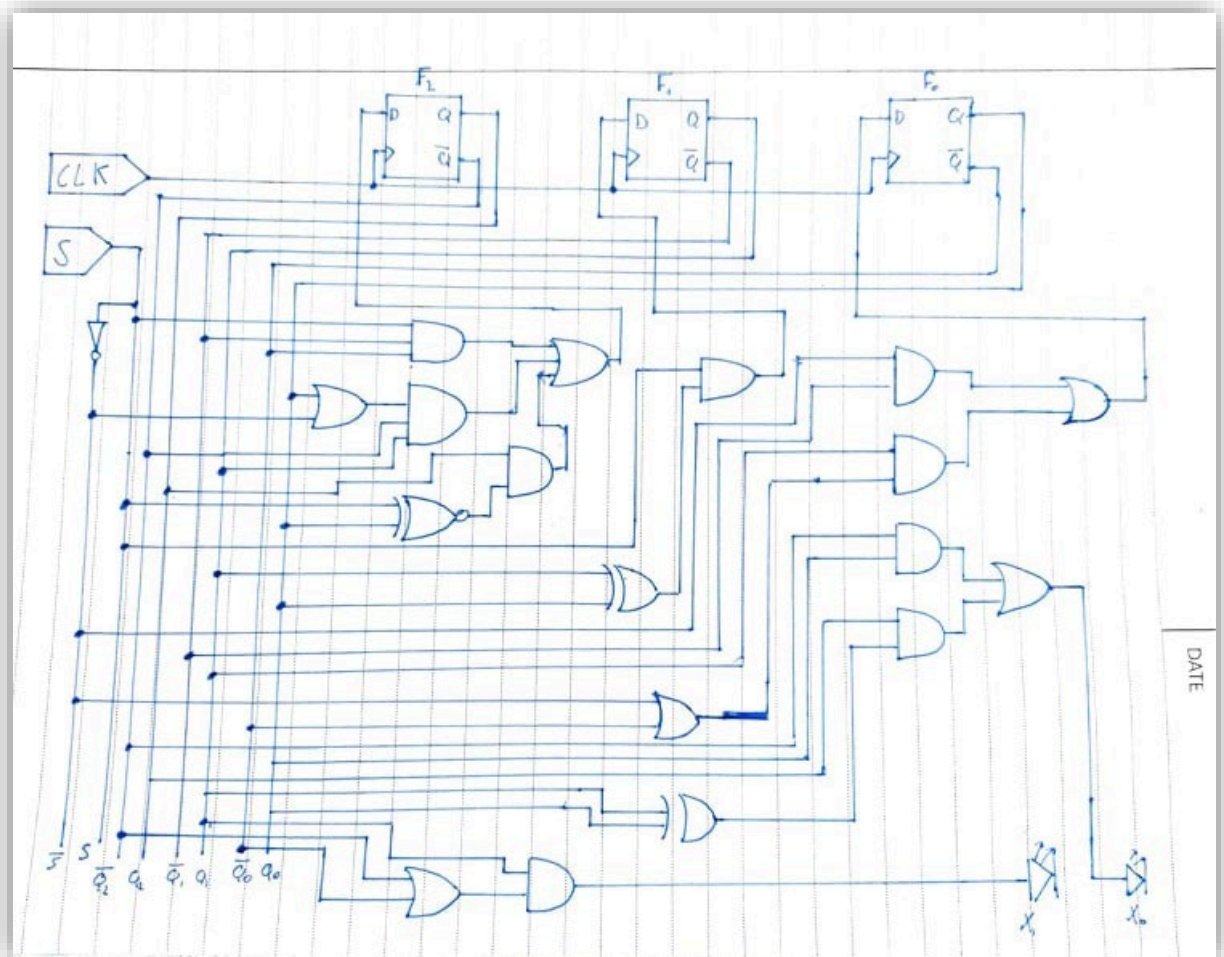
$$\begin{aligned}
 & \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_2} Q_1 \overline{Q_0} \overline{S} + \overline{Q_2} Q_1 Q_0 S + \overline{Q_2} Q_1 Q_0 \overline{S} + Q_2 \overline{Q_1} \overline{Q_0} S + Q_2 \overline{Q_1} \overline{Q_0} \overline{S} + Q_2 \overline{Q_1} Q_0 S + Q_2 \overline{Q_1} Q_0 \overline{S} \\
 & \quad + Q_2 Q_1 \overline{Q_0} S + Q_2 Q_1 \overline{Q_0} \overline{S} \\
 &= \overline{Q_2} \overline{Q_1} \overline{Q_0} S + \overline{Q_2} \overline{Q_1} \overline{Q_0} \overline{S} + \overline{Q_2} Q_1 Q_0 S + \overline{Q_2} Q_1 Q_0 \overline{S} + Q_2 \overline{Q_1} \overline{Q_0} S + Q_2 \overline{Q_1} \overline{Q_0} \overline{S} + Q_2 \overline{Q_1} Q_0 S + Q_2 \overline{Q_1} Q_0 \overline{S} \\
 & \quad + Q_2 Q_1 \overline{Q_0} S + Q_2 Q_1 \overline{Q_0} \overline{S} \\
 &= \overline{Q_1} \overline{Q_0} S (Q_2 + \overline{Q_2}) + \overline{Q_2} Q_1 Q_0 (S + \overline{S}) + Q_2 \overline{Q_0} \overline{S} (\overline{Q_1} + Q_1) + Q_2 Q_0 S (\overline{Q_1} + Q_1) + \overline{Q_2} Q_1 \overline{Q_0} \overline{S} \\
 &= \overline{Q_2} Q_1 Q_0 + \overline{Q_2} Q_1 \overline{Q_0} \overline{S} + Q_2 \overline{Q_0} \overline{S} + Q_2 Q_0 S + \overline{Q_1} \overline{Q_0} S \\
 &= \overline{Q_2} Q_1 (Q_0 + \overline{Q_0} \overline{S}) + Q_2 (\overline{Q_0} \overline{S} + Q_0 S) + \overline{Q_1} \overline{Q_0} S \\
 &= \overline{Q_2} Q_1 (Q_0 + \overline{Q_0} \overline{S}) + Q_2 (\overline{Q_0} \oplus S) + \overline{Q_1} \overline{Q_0} S \\
 &= \overline{Q_2} Q_1 (Q_0 + \overline{S}) + Q_2 (\overline{Q_0} \oplus S) + \overline{Q_1} \overline{Q_0} S
 \end{aligned}$$

## 6. Chosen Encoding

The logic expressions for both binary and one-hot encoding have been computed above. It has been chosen to go with **binary encoding** for the build of this circuit as it requires fewer flip flops and a much simpler logic design. More explanation of this reasoning can be found in the questions section of this assignment.

## 7. Logic Diagram

Before the circuit could be built on Logisim, a logic diagram was drawn from the logic expressions determined previously.



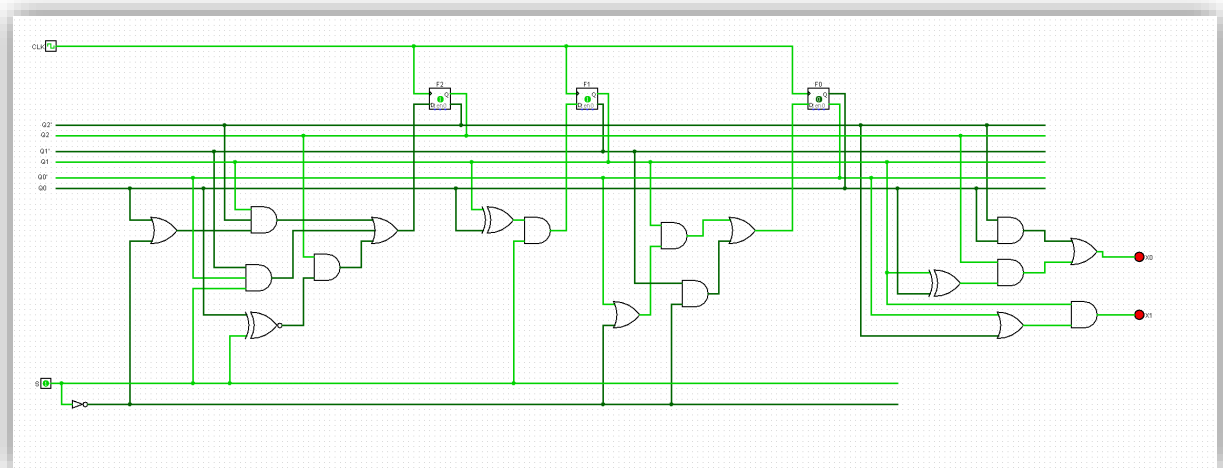
## Simulation

The circuit was replicated in Logisim – an open source program to simulate logical circuits. The file is attached below:



DetectorCircuit.circ

A screenshot of the circuit in Logisim is also shown below



## Questions

### 1. Why did you choose the encoding you did in step 6?

Binary encoding was chosen for this circuit for a number of reasons:

- Uses fewer flip-flops (3) over one-hot encoding (7)
- Boolean logic for the outputs  $X_1$ ,  $X_0$  as well as for the next state logic  $D_0$  to  $D_2$  is far less complex with binary encoding. This is because the logic for one-hot encoding must deal with more bits than in binary encoding which is inefficient for this circuit.
- One-hot encoding would require a lot of not gates because only one  $Q_i$  can be a 1 at any given time. Therefore, in the sum of products, each of the remaining  $Q_i$  outputs need to be negated (if not using flip flops with a  $\bar{Q}_i$  output).



2. If you were to build this circuit physically using 74 series chips in the CSSE2010 kit, how many chips would you need to use? Justify.

Gates required for this logic implementation:

- 11x AND\*
- 7x OR\*
- 2x XOR
- 1x XNOR
- 1x NOT

\* As this circuit is only being simulated, some gates are of the three-input type. However, the 74 series chips only have gates of the two-input type. Therefore, a three input AND or OR gate would actually require two 2-input gates. Hence the number of gates is greater than the number of gates in the circuit diagram.

Memory chips required for this logic implementation:

- 3x D flip flops

The number of chips required are summarised below:

- 3x 74HCT08 Quad 2-input AND gate
- 2x 74HCT32 Quad 2-input OR gate
- 1x 74HCT86 Quad 2-input XOR gate
- 1x 74HCT04 Hex Inverter\*\*
- 1x 74HCT175 Quad D-Type Flip-Flop

\*\* The 74 series chips do not include an XNOR chip. Therefore, the one XNOR gate in this circuit implementation could be achieved with an XOR gate with the same inputs with the output connected to a NOT gate and then to its destination.

Therefore, in total, x8, 74 series chips would be required to build this circuit with the specified encoding and logic implementation. Note that this is in addition to the IO board supplied in the CSSE2010 kit.

### 3. How did you test your Logisim circuit to ensure it works properly?

As the circuit wasn't build physically, rather it was simulated using software. Therefore, proper testing of the circuit is imperative to ensure its functionality is exactly as expected. Fortunately, in the process of building this circuit, I have drawn a 1D state table for the binary encoding which makes it easy to test each and every transition possible. There are seven (eight with the undefined 111 state) states in this circuit with one binary input. Therefore, there are  $8 \times 2 = 16$  possible transitions that need to be tested. These can also be visualised using the state diagram.

Each state transition was tested, and the results are summarised in the table below.

Logic Testing  
Binary Encoding

State Name	Current State (Output)		Input	Expected Output		Tested Output		Test = Expected
	X1	X0		X1	X0	X1	X0	
Start	0	0	S	0	0	0	0	1
Start	0	0	~S	0	0	0	0	1
"A"	0	1	S	0	1	0	1	1
"A"	0	1	~S	0	1	0	1	1
"AD"	1	0	S	1	0	1	0	1
"AD"	1	0	~S	1	0	1	0	1
"ADD"	1	1	S	1	1	1	1	1
"ADD"	1	1	~S	1	1	1	1	1
"D"	0	0	S	0	0	0	0	1
"D"	0	0	~S	0	0	0	0	1
"DA"	0	1	S	0	1	0	1	1
"DA"	0	1	~S	0	1	0	1	1
"DAD"	1	1	S	1	1	1	1	1
"DAD"	1	1	~S	1	1	1	1	1
Undefined	0	0	S	0	0	0	0	1
Undefined	0	0	~S	0	0	0	0	1