CSSE2010

Welcome!

# CSSE2010/CSSE7201
# Learning Lab 7

# Counter Circuits

http://responsewaresg.net

**Session ID: CSSE2010EXT**

School of Information Technology and Electrical Engineering
The University of Queensland

# Today

- Counter Circuits
  - Review of Preparation Task
  - Polling questions
  - Design
  - Build and test or Simulation (Logisim)
- Don’t forget preset/clear inputs on flip-flops

# Peer Review of Circuit Schematics

- Check the circuit schematic
  - Naming of inputs and outputs
  - Identification of chips (U1, U2 etc) and gates within chips where applicable (:A, :B etc)
  - Identification of types of chips (74HCT00 etc.)
  - Numbering of pins (including for IO board)
  - Power supply connections
  - **Circuit functionality – will it do what was asked?**
- Check schematic guide and device pinouts on Blackboard for more detail
- Ask a tutor if necessary
- Online sessions – talk to other people in your breakout room and discuss among yourselves and make sure you have a correct design on paper

# Preparation Survey: How many 74 series logic chips did your circuit schematic use?


1x 74HCT 125 Quad DPT
1x 74HCT86 Quad XOR gate

0

2 | 000->011->010->110->100->001->111->000->...

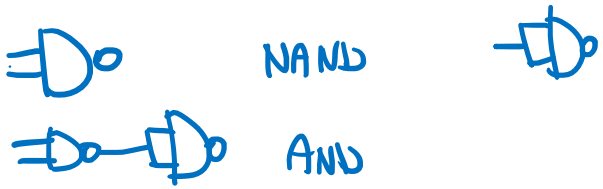
# Prep Task

| $Q_2$ | $Q_1$ | $Q_0$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | x | x | x |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

$$D_2 = \bar{Q}_2\bar{Q}_1Q_0 + \bar{Q}_2Q_1\bar{Q}_0 + Q_2Q_1\bar{Q}_0 + Q_2\bar{Q}_1Q_0$$
$$= \bar{Q}_2(\bar{Q}_1Q_0 + Q_1\bar{Q}_0) + Q_2(Q_1\bar{Q}_0 + \bar{Q}_1Q_0)$$
$$= \bar{Q}_2(Q_1 \oplus Q_0) + Q_2(Q_1 \oplus Q_0)$$
$$= (Q_1 \oplus Q_0)(\bar{Q}_2 + Q_2) = Q_1 \oplus Q_0$$
$$= \bar{Q}_2(Q_1 \oplus Q_0) + Q_1\bar{Q}_0$$

$$D_1 = \bar{Q}_2\bar{Q}_1\bar{Q}_0 + \bar{Q}_2\bar{Q}_1Q_0 + \bar{Q}_2Q_1\bar{Q}_0 + \bar{Q}_2Q_1Q_0$$
$$= \bar{Q}_2(\bar{Q}_1\bar{Q}_0 + \bar{Q}_1Q_0 + Q_1\bar{Q}_0 + Q_1Q_0)$$
$$= \bar{Q}_2(\bar{Q}_1(\bar{Q}_0 + Q_0) + Q_1(\bar{Q}_0 + Q_0))$$
$$= \bar{Q}_2$$

| $Q_2$ | $Q_1$ | $Q_0$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | X | X | X |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |




| A | B | $A \oplus B$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

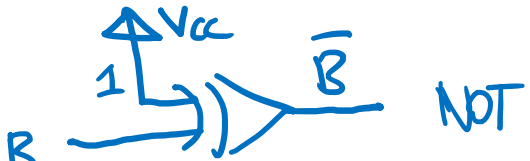
$$D_0 = \bar{Q}_2\bar{Q}_1\bar{Q}_0 + \bar{Q}_2\bar{Q}_1Q_0 + Q_2\bar{Q}_1\bar{Q}_0 + Q_2\bar{Q}_1Q_0$$

$$= \bar{Q}_2\bar{Q}_1(\bar{Q}_0 + Q_0) + Q_2\bar{Q}_1(\bar{Q}_0 + Q_0)$$

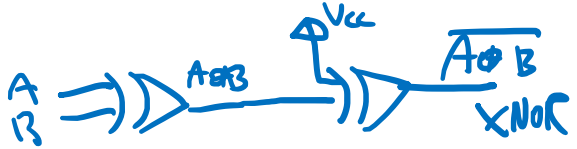
$$= \bar{Q}_2\bar{Q}_1 + Q_2\bar{Q}_1 = \bar{Q}_1 \rightarrow 1 \text{ XOR gate}$$

$D_1 = \bar{Q}_2 \rightarrow 1$ XOR gate

$D_2 = Q_1 \oplus Q_0 \rightarrow 1$ XOR gate operation







# Which of the following best describes the behaviour of a 2-bit up/down binary counter? (U is an input)

U=1 -> count up

U=0 -> count down

| | | |
|---|---|---|
| 0% | 1. | U=1: $Q_1Q_0$: 00→01→10→11→00<br>U=0: $Q_1Q_0$: 00→01→10→11→00 |
| ✓ 100% | 2. | U=1: $Q_1Q_0$: 00→01→10→11→00 ✓<br>U=0: $Q_1Q_0$: 00→11→10→01→00 ✓ |
| 0% | 3. | U=1: $Q_1Q_0$: 00→11→10→01→00<br>U=0: $Q_1Q_0$: 00→01→11→10→00 |
| 0% | 4. | U=1: $Q_1Q_0$: 00→01→10→11→00<br>U=0: $Q_1Q_0$: 00→10→11→01→00 |
| 0% | 5. | I don't know |

-2 -> 1

up: 00 -> 01 -> 10 -> 11 -> 00

Down: 00 -> 11 -> 10 -> 01 -> 00

0

# Up/Down Counter

- Complete the truth table for a 2 bit up/down binary counter
  - (U=1 counts up, U=0 counts down)
- Work out logic functions for D1 and D0 in terms of U, Q1, Q0
  - Sum of products
  - Simpler expression?

| Input | Current State | | Next State | |
|---|---|---|---|---|
| U | Q1 | Q0 | D1 | D0 |
| 0 | 0 | 0 | 3 1 | 1 |
| 0 | 1 | 0 | 0 0 | 0 |
| 0 | 2 | 1 | 1 0 | 1 |
| 0 | 3 | 1 | 2 1 | 0 |
| 1 | 0 | 0 | 1 0 | 1 |
| 1 | 1 | 0 | 2 1 | 0 |
| 1 | 2 | 1 | 3 1 | 1 |
| 1 | 3 | 1 | 0 0 | 0 |

Down

Up

| Input | Current State | | Next State | |
|---|---|---|---|---|
| U | Q1 | Q0 | D1 | D0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 2 | 1 | 0 | 1 |
| 0 | 3 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 2 | 1 | 0 | 1 |
| 1 | 3 | 1 | 0 | 0 |

$$D_1 = \bar{U}\bar{Q}_1\bar{Q}_0 + \bar{U}Q_1Q_0 + U\bar{Q}_1Q_0 + UQ_1\bar{Q}_0$$

$$= \bar{U}(\bar{Q}_1\bar{Q}_0 + Q_1Q_0) + U(\bar{Q}_1Q_0 + Q_1\bar{Q}_0)$$

(XNOR, XOR)

$$= \bar{U}\overline{(Q_1 \oplus Q_0)} + U(Q_1 \oplus Q_0)$$

$$= \overline{U \oplus (Q_1 \oplus Q_0)} = \overline{U \oplus Q_1 \oplus Q_0}$$

$$D_0 = \bar{Q}_0 \quad \text{by inspection}$$

$$D_0 = \bar{U}\bar{Q}_1\bar{Q}_0 + \bar{U}Q_1\bar{Q}_0 + U\bar{Q}_1\bar{Q}_0 + UQ_1\bar{Q}_0$$

$$= \bar{U}\bar{Q}_0(\bar{Q}_1 + Q_1) + U\bar{Q}_0(\bar{Q}_1 + Q_1)$$

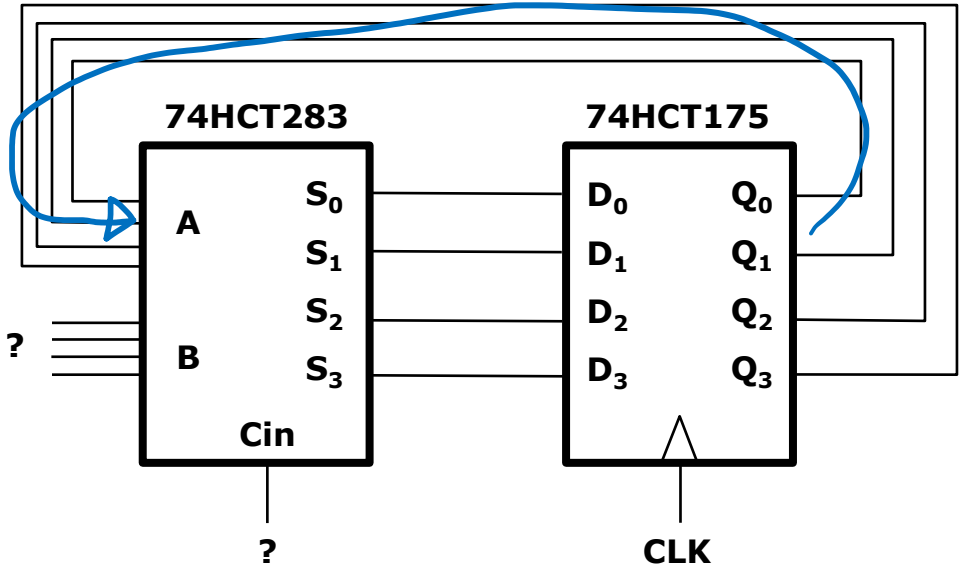
$$= \bar{U}\bar{Q}_0 + U\bar{Q}_0$$

$$= \bar{Q}_0(\bar{U} + U)$$

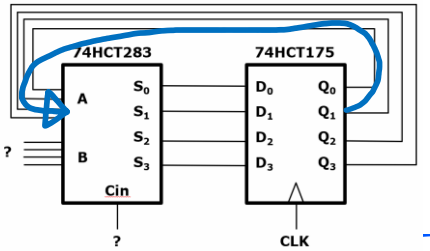
$$= \bar{Q}_0$$

# Consider a 4-bit up/down counter built out of a 4-bit adder (e.g. 74HCT283) and 4 flip-flops (e.g. 74HCT175)

- Adder output is connected to flip-flop inputs ✓
- Current count (flip-flop outputs) connected to one 4-bit adder input (A)
- What needs to be on the other 4-bit adder input (B) & Cin?
  - When counting up? ✓
  - When counting down? ✓
  - ➔ Clicker question



# If Cin is 0, what needs to be on the B input?




| | | | |
|---|---|---|---|
| 5% | 1. | Up: 1000 | Down: 0001 |
| 5% | 2. | Up: 0001 | Down: 1000 |
| ✓ 74% | 3. | Up: 0001 ✓ | Down: 1111 ✓ |
| 5% | 4. | Up: 1111 | Down: 0001 |
| 11% | 5. | Up: 0001 | Down: 1110 |
| 0% | 6. | Up: 0001 | Down: 0001 |

Unsigned
15: 1 1 1 1
5: + 0 1 0 1
20: 0 1 0 0 = 4

0

# Tasks

- 4 bit up/down counter built from 4-bit adder
  - Draw the circuit in Logisim
    - Use the "Adder" component ✓
    - Work out how splitters work for wiring ✓
    - Simulate it & verify behaviour is as expected ✓
  - Draw a circuit schematic diagram
    - Use button for clock, switch for up/down input ✓
    - Have it checked by a tutor then build & test it
- Build/simulate your preparation task 3-bit counter and test it ✓
- Draw a circuit schematic for your 2-bit up/down counter
  - Test this 2-bit up/down counter either in simulation or by building the circuit ✓