CSSE2010/CSSE7201 – Introduction to Computer Systems
Semester Two, 2021

Lab 7 Preparation Task

You should complete a circuit schematic diagram as described below before your lab 7 session in week 4. You should consult the device pinout information on Blackboard. You will be either constructing or simulating this circuit (or a similar circuit) during the prac session.

Design and draw a circuit schematic diagram for a **3-bit synchronous counter** which counts through the sequence below. You must use a push button for the clock signal; a single switch to allow your counter to be preset (i.e. to 111); and a single switch to allow your counter to be cleared (i.e. to 000). Your count output should be shown on three LEDs. Your schematic should clearly indicate which output bit is the most significant (label it Q2) and which is the least significant (label it Q0). The middle output bit should be labelled Q1. Your allocated sequence has seven binary numbers; you may choose to do whatever you like with the missing number – i.e., if the counter ever has this value then we don't care what the next count value is. It is recommended that you simulate your circuit using Logisim to ensure it counts through the expected sequence. External mode students, you should verify the functionality in Logisim.

Last digit of your 8-digit UQ student number	Count sequence
0	111->011->101->110->001->000->010->111->…
1	111->010->101->110->100->000->001->111->…
2	000->011->010->110->100->001->111->000->…
3	111->100->101->000->110->001->011->111->…
4	000->101->011->010->001->110->100->000->…
5	000->110->001->100->111->011->010->000->…
6	111->010->000->110->001->101->100->111->…
7	111->001->110->101->100->000->010->111->…
8	111->000->001->101->011->110->100->111->…
9	000->100->001->110->101->011->010->000->…