CSSE2010

Welcome!

CSSE2010/CSSE7201
Learning Lab 5

Logisim & Flip-flops

http://responsewaresg.net

Session ID: CSSE2010EXT

School of Information Technology and Electrical Engineering
The University of Queensland

Learning Lab 5 - Flip-flops

- Recall: there are two types of logic circuits. Combinational and sequential
- The basic building block of sequential circuits are flip flops (stores 1-bit of information)
- Today's lab: simulate circuits having D-flip flops using Logisim

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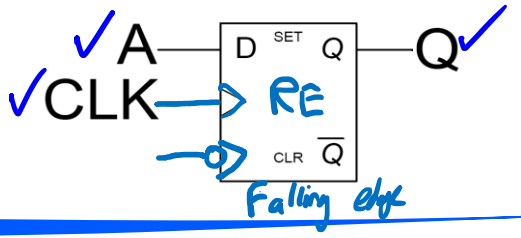
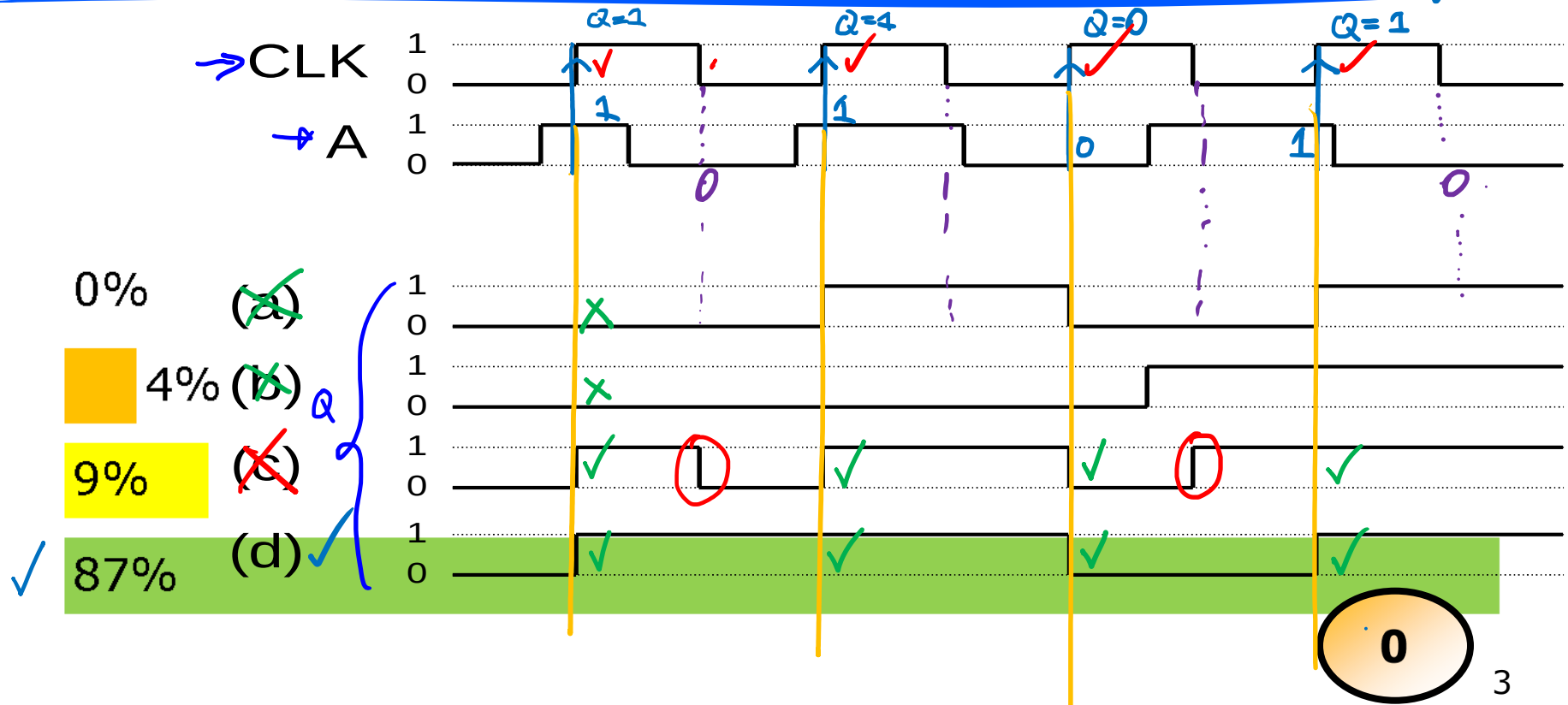
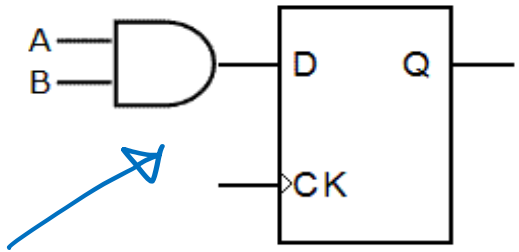
Which diagram captures the behaviour of this circuit?





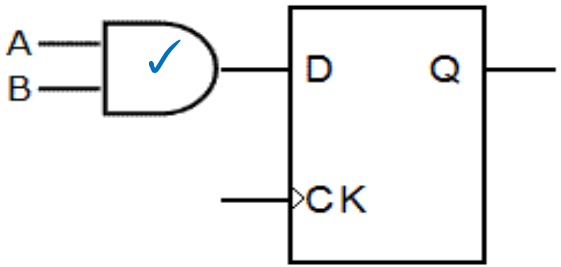
Logisim

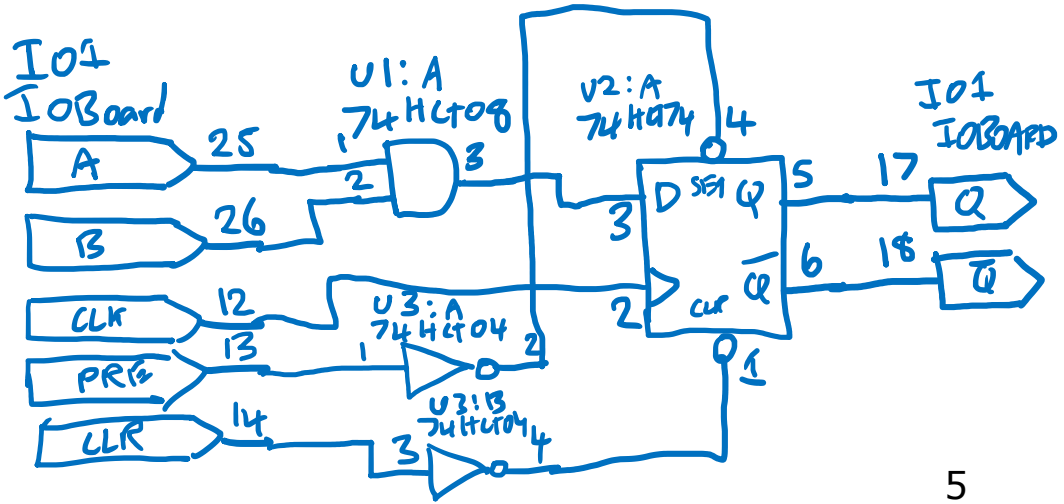
- Go through the Logisim tutorial if you haven't done already
- 3 Tasks
- Draw and simulate
  1. ~~A 2-input NOR gate~~
  2. ✓ An RS-Latch (two cross coupled NOR gates)
  3. ✓ A D-Flip-flop circuit:
     - Make sure you work out what all of the inputs on the Logisim D Flip-flop do ✓



D-Flip-flop circuit

- Consider Circuit (below)
- Draw a circuit schematic diagram that ✓
  - Uses a 74HCT74 (and other chips as needed) ✓
  - Uses pushbuttons for CLK (CK), PRE and CLR inputs
    - Consider inverters between buttons and PRE/CLR inputs. Why? ✓✓ ↳ refer to schematic
  - Uses switches for A and B inputs ✓
  - Uses LEDs for Q and Q' outputs ✓
- Have schematic checked by a tutor
- Build/simulate the circuit & test it





Latch circuit

- Design a latch out of cross-coupled NAND gates ✓
- Predict its behaviour ✓
  - How can you set it or reset it? ✓
- Draw a circuit schematic ✓
- Build/simulate it ✓
- Test it

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

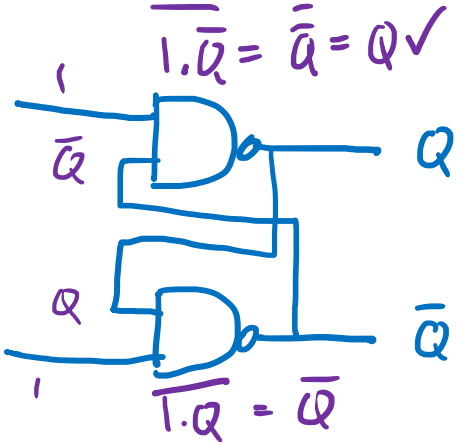
Set → memory

Set → reset → memory

A	B	Q	$\bar{Q}$
0	0	1	0
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	Q	$\bar{Q}$

set
Reset
Invalid
memory

R S



A	B	Q	$\bar{Q}$	
0	0	1	1	
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	$\bar{Q}$	Memory

S →
R →
M →

- Reset
- set
- Memory
- Single bit transition

Set ↔ memory, reset ↔ memory