THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

This exam paper must not be removed from the venue

Venue _____

Seat Number _____

Student Number |__|__|__|__|__|__|__|__|

Family Name _____

First Name _____

School of Information Technology and Electrical Engineering

SAMPLE MID-SEMESTER EXAMINATION #4

Semester One Mid-semester Examinations, 2020

CSSE2010/CSSE7201 Introduction to Computer Systems

This paper is for St Lucia Campus students.

Examination Duration: 60 minutes

Reading Time: 10 minutes

Exam Conditions:

This is an Open Book Examination

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

Calculators - Casio FX82 series or UQ approved (labelled)

Materials To Be Supplied To Students:

1 x Multiple Choice Answer Sheet

Instructions To Students:

Answer all questions on the supplied "True/False and Multiple Choice Answer Sheet".

Choose the answer which best answers the question or completes the statement. Correct answers will be awarded one mark. Incorrect, missing or multiple answers will be awarded zero marks.

Total number of questions for the paper: 25

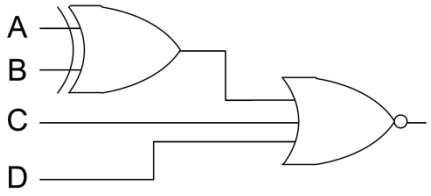
1. What is -34_{10} expressed in 7-bit excess-64 format?
   (a) 0011110
   (b) 0100010
   (c) 1011101
   (d) 1011110
   (e) 1100010

2. 95_{16} is equal to
   (a) 10100101_2
   (b) 137_8
   (c) 141_{10}
   (d) 225_8
   (e) None of the above

3. A 4-bit number in ones' complement format can represent integers from
   (a) -15 to 15
   (b) -8 to 7
   (c) -7 to 7
   (d) -7 to 8
   (e) 0 to 15

4. Which of the following statements about number representations is false?
   (a) The 8-bit number 01100110 is even when considered to be in unsigned, signed-magnitude, ones' complement, two's complement or excess-128 formats
   (b) An n-bit excess 2^{n-1} number can be converted to two's complement representation by inverting the most significant bit
   (c) An 8-bit ones' complement number can be converted to 9-bit ones' complement representation by prepending a copy of the most significant bit
   (d) An 8-bit two's complement number can be converted to 9-bit two's complement representation by prepending a copy of the most significant bit
   (e) None of the above

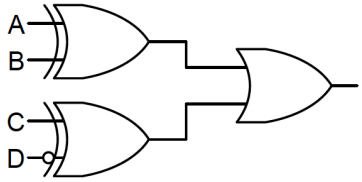
5. What function is implemented by the following circuit?

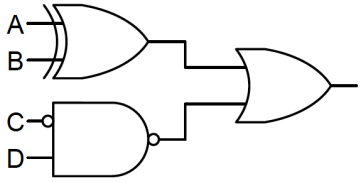


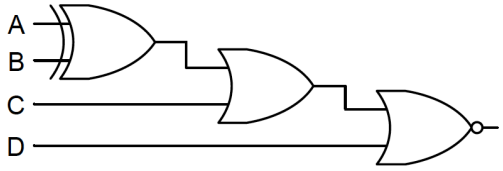
   (a) $(A \oplus B) + C + D$
   (b) $\overline{A \oplus B} + \overline{C} + \overline{D}$
   (c) $\overline{(A \oplus B) + (C + D)}$
   (d) $(A \oplus B).\overline{C}.\overline{D}$
   (e) $\overline{\overline{A \oplus B}.(C + D)}$

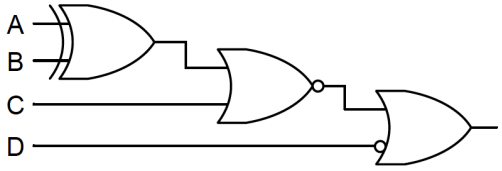
6. Which of the following logic functions is identical to $\overline{\overline{\overline{A} + \overline{B} + C} + \overline{B}.\overline{C}}$?
   (a) 0
   (b) $B.C$
   (c) $A.B.C$
   (d) $\overline{B} + \overline{C}$
   (e) None of the above

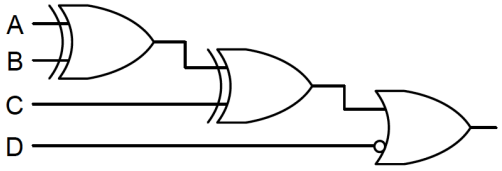
7. Which of the following logic circuits is an implementation of the function $(A \oplus B) + C + \bar{D}$?

(a)


(b)


(c)


(d)


(e)


8. Which of the following truth tables is equivalent to the function $X = (A.\bar{B} + C).\overline{(B + A.\bar{C})}$

(a)

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

(b)

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

(c)

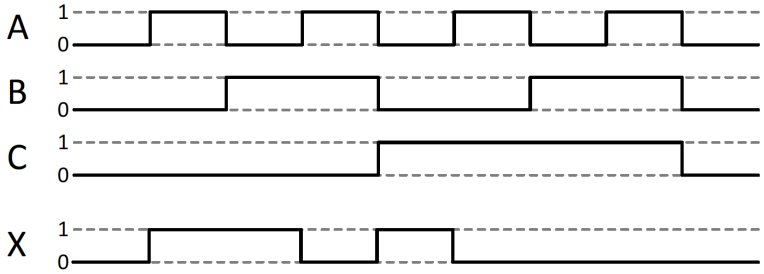
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

(d)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

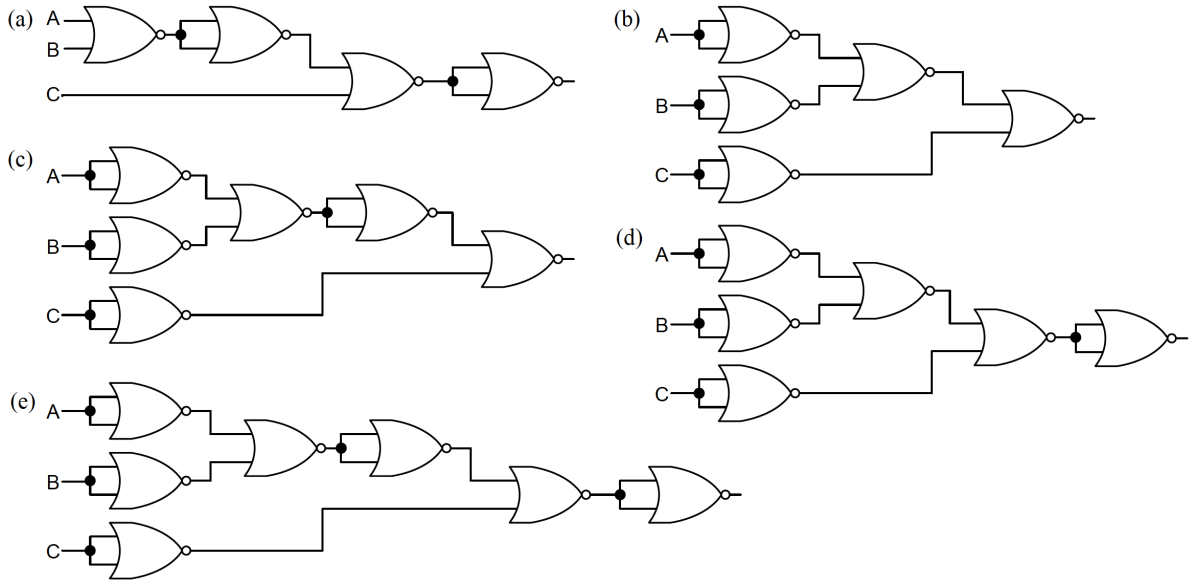
(e) None of the above

9. What logic function does the following timing diagram represent?



(a) $A \oplus B \oplus C$
(b) $A.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + \bar{A}.\bar{B}.C$
(c) $A.B.\bar{C} + A.\bar{B}.C + \bar{A}.B.C$
(d) $A.\bar{B}.\bar{C} + \bar{A}.B.C + \bar{A}.\bar{B}.C$
(e) None of the above

10. Which of the following circuits implements a 3 input NAND gate ($\overline{A.B.C}$) using only 2-input NOR gates?



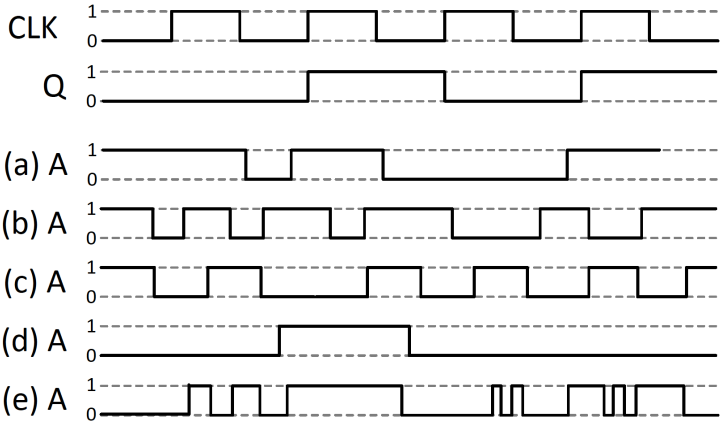
11. Consider the logic function represented by the following truth table:

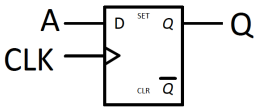
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Which of the following expressions is NOT equivalent to this function?

(a) $\bar{B} + \bar{A}.\bar{C}$
(b) $\bar{A}.\bar{B} + \bar{A}.\bar{C} + A.\bar{B}$
(c) $\bar{A}.\bar{B}.\bar{C} + \bar{B}$
(d) $\bar{B}.C + \bar{A}.\bar{C} + \bar{B}.\bar{C}$
(e) $\bar{A}.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C + A.\bar{B}.C$

12. Consider the flip-flop circuit shown below and the associated CLK and output (Q) signals. Which timing diagram shows input (A) values over time which would have resulted in the given output (Q).



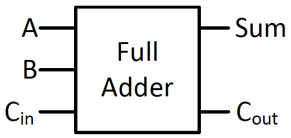


13. What's the result of adding the 6-bit two's complement numbers 101101 and 110011?
    (a) 000000
    (b) 010000
    (c) 100000
    (d) 111110
    (e) 111111

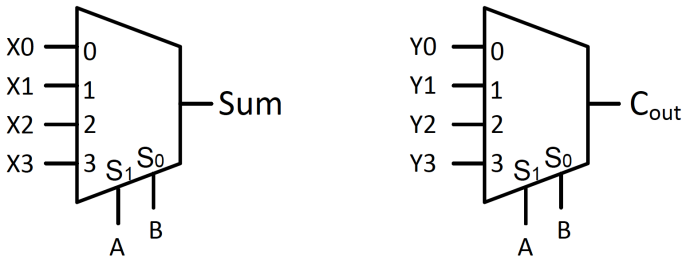
14. Which of the following operations will result in an overflow in 6-bit two's complement arithmetic?
    (a) 011111 – 010010
    (b) 101011 – 111000
    (c) 110100 – 000111
    (d) 010101 + 111111
    (e) None of the above

15. Consider the binary addition operation 1010 + 0110. Which of the following statements is true if the numbers are interpreted as two's complement?
    (a) The result is negative and no overflow occurs
    (b) The result should be negative but overflow occurs
    (c) The result is positive and no overflow occurs
    (d) The result should be positive but overflow occurs
    (e) The result is zero

16. Consider the full-adder shown below:



In the multiplexer circuit below, what values do the multiplexer inputs X0,X1,X2,X3 and Y0,Y1,Y2,Y3 need to take on in order for the circuit to implement a full-adder?



(a)

X0	**0**	Y0	**0**
X1	**1**	Y1	**0**
X2	**1**	Y2	**0**
X3	**0**	Y3	**1**

(b)

X0	C_{in}	Y0	**0**
X1	$\overline{C_{in}}$	Y1	C_{in}
X2	$\overline{C_{in}}$	Y2	C_{in}
X3	C_{in}	Y3	**1**

(c)

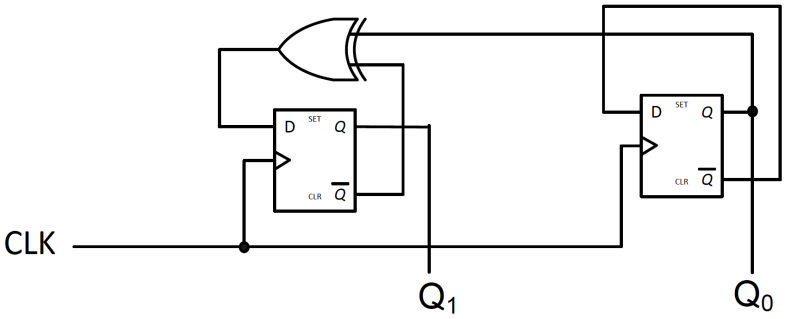
X0	**0**	Y0	**0**
X1	$\overline{C_{in}}$	Y1	C_{in}
X2	$\overline{C_{in}}$	Y2	C_{in}
X3	**1**	Y3	**1**

(d)

X0	C_{in}	Y0	**0**
X1	**1**	Y1	$\overline{C_{in}}$
X2	**1**	Y2	$\overline{C_{in}}$
X3	C_{in}	Y3	C_{in}

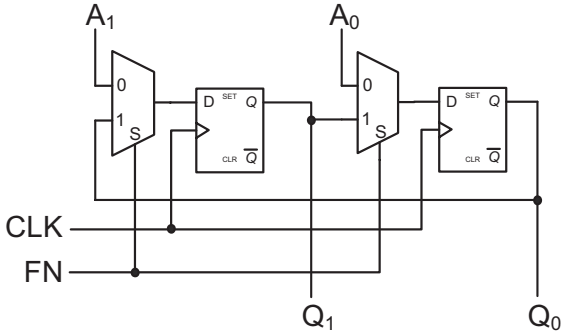
(e) None of the above

17. What sequence will the following synchronous counter count through, if it starts at $Q_1Q_0 = 00$?



(a) Q_1Q_0: 00 → 11 → 10 → 01 → 00 → …
(b) Q_1Q_0: 00 → 11 → 10 → 11 → 10 → …
(c) Q_1Q_0: 00 → 01 → 10 → 11 → 00 → …
(d) Q_1Q_0: 00 → 01 → 00 →…
(e) Q_1Q_0: 00 → 11 → 00 →…

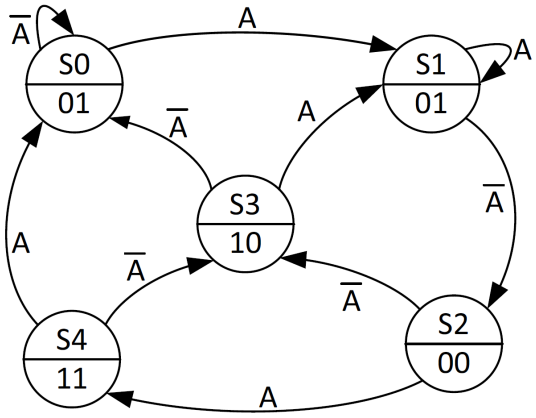
18. Consider the circuit below. If A_1 is 0 and A_0 is 1, what are the values of Q_1 and Q_0 after four rising clock edges if FN is 0 for one rising clock edge then 1 for three rising clock edges?



(a) $Q_1 = 0$ $Q_0 = 0$
(b) $Q_1 = 0$ $Q_0 = 1$
(c) $Q_1 = 1$ $Q_0 = 0$
(d) $Q_1 = 1$ $Q_0 = 1$
(e) Insufficient information is provided to determine the values

19. Consider the state machine represented by the state diagram below:

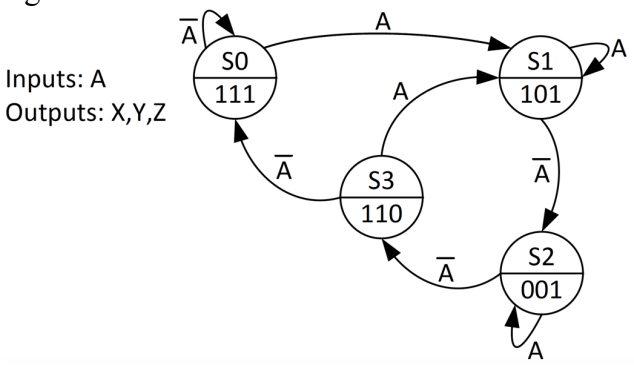
Inputs: A
Outputs: X,Y



What sequence of states is traversed if the machine starts in state S1 and A goes through the sequence 101010101?

(a) S1→S2→S4→S3→S1→S2→S4→S3→S1→S2
(b) S1→S1→S2→S3→S1→S2→S4→S3→S1→S2
(c) S1→S1→S2→S4→S3→S1→S2→S4→S3→S1
(d) S1→S1→S2→S4→S0→S0→S1→S2→S4→S3
(e) None of the above

20. Consider the state diagram below.



Which of the following is an equivalent state table?

(a)

Current State	Input (A)	Next State	Outputs (X,Y,Z)
S0	0	S0	111
S0	1	S1	111
S1	0	S1	101
S1	1	S2	101
S2	0	S3	001
S2	1	S2	001
S3	0	S0	110
S3	1	S1	110

(b)

Current State	Input (A)	Next State	Outputs (X,Y,Z)
S0	0	S0	111
S0	1	S1	111
S1	0	S2	101
S1	1	S1	101
S2	0	S3	001
S2	1	S2	001
S3	0	S1	110
S3	1	S0	110

(c)

Current State	Next State		Outputs (X,Y,Z)
	A=0	A=1	
S0	S0	S1	111
S1	S2	S1	101
S2	S2	S3	001
S3	S0	S1	110

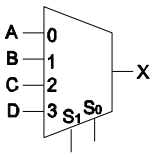
(d)

Current State	Next State		Outputs (X,Y,Z)
	A=0	A=1	
S0	S0	S1	111
S1	S2	S1	101
S2	S3	S2	001
S3	S0	S1	110

(e) None of the above

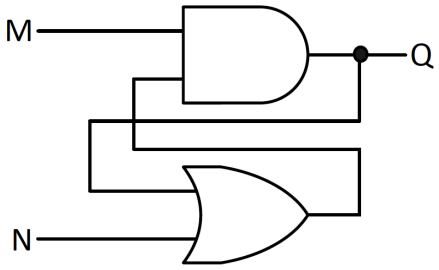
21. What's the minimum number of flip-flops needed to build the state machine shown in question 20?
    (a) 1
    (b) 2
    (c) 3
    (d) 4
    (e) 5

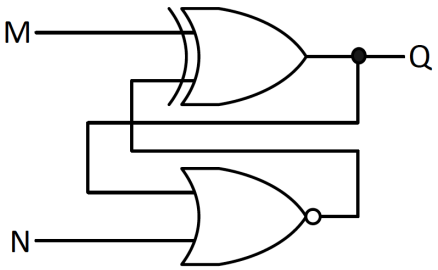
22. Consider the following multiplexer. What must the inputs A,B,C,D be so that the multiplexer implements the function $X = \overline{S_0} + S_1$?

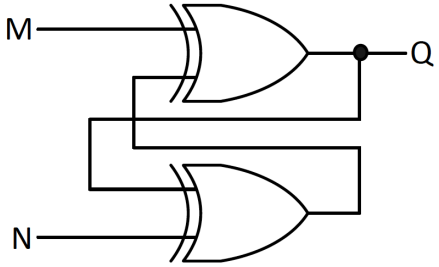


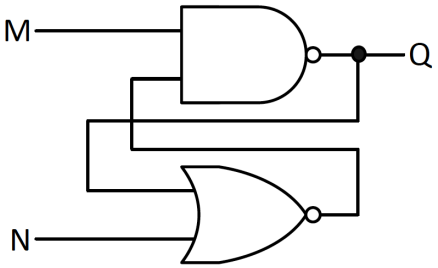
    (a) A=0, B=1, C=0, D=0
    (b) A=0, B=1, C=1, D=1
    (c) A=1, B=0, C=1, D=1
    (d) A=1, B=1, C=0, D=1
    (e) None of the above

23. Which of the following circuits is capable of acting as a latch? i.e. it has combinations of inputs (M,N) which allow a bit (0 or 1) to be stored, the latch to be set (Q=1) with a single input transition, and the latch to be cleared (Q=0) with a single input transition?

(a)


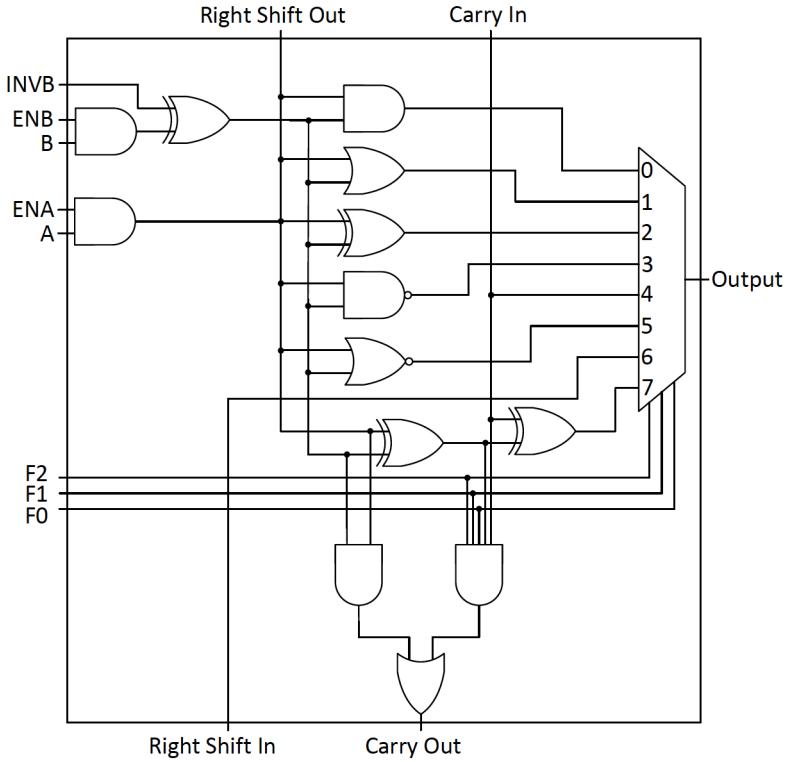
(b)


(c)


(d)


(e) None of the above

24. Consider the ALU bit slice below.



For an ALU made up of 8 of the bit slices above, which of the following control input settings will result in the ALU output being $\bar{A}.B$? (The "Right Shift In" control input refers to that for the most significant bit; the "Carry in" control input refers to that for the least significant bit.)

(a) ENA = 1, ENB = 1, INVB = 0, $F_2 = 0$, $F_1 = 0$, $F_0 = 0$, Right Shift In = 0, Carry in = 0
(b) ENA = 1, ENB = 1, INVB = 1, $F_2 = 0$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 1
(c) ENA = 1, ENB = 1, INVB = 0, $F_2 = 0$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 1
(d) ENA = 1, ENB = 1, INVB = 1, $F_2 = 1$, $F_1 = 0$, $F_0 = 1$, Right Shift In = 0, Carry in = 0
(e) ENA = 1, ENB = 1, INVB = 1, $F_2 = 1$, $F_1 = 1$, $F_0 = 1$, Right Shift In = 0, Carry in = 1

25. For the ALU in question 24, which of the following bitwise logical operations can NOT be performed?
    (a) $\overline{A} + B$
    (b) $A \oplus \overline{B}$
    (c) $\overline{A} \oplus B$
    (d) $\overline{A.B}$
    (e) All of the above operations can be performed

