CSSE2010 / CSSE7201 – Introduction to Computer Systems
Exercises – Week Three
Timing Diagrams, Flip-flops and Shift Registers

Exercises

Some of the questions below are taken from or based on questions in Tanenbaum, Structured Computer Organisation, 5th edition. A number of questions are taken from or based on questions from "Digital Design", 3rd edition by M. Morris Mano, Prentice-Hall, 2002 and from "Logic and Computer Design Fundamentals," 2nd edition by Mano and Kime, Prentice Hall, 2001.

1. Draw a timing diagram representation of:
   (a) a 3-input XOR gate (i.e. 3-input "odd function")
   (b) the function $F = XY + \overline{Y}Z$
2. Draw an SR Latch made from NAND gates rather than NOR gates (as shown in lectures). Write down the truth table also.
3. The content of an 8-bit register is 01011010. The register is shifted ten times to the right with the serial input being 1100111010 (i.e. 1 is shifted in first etc.). What is the content of the register after each shift?
4. In the lecture we saw how to use multiplexers and flip-flops to build shift registers. Consider now a more general shift register (or *universal shift register*) that has both parallel load and bidirectional shifting capabilities according to the following table. (S_1 and S_0 are the control inputs which determine the operation of the universal shift register.)

S1	S0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

   Show how this 4-bit universal shift register can be built from 4-to-1 multiplexers and D flip-flops. (This is a variation on the universal shift register seen in lectures.)