CSSE2010

Welcome!

CSSE2010/CSSE7201
Learning Lab 3

Binary Arithmetic ✓

http://responsewaresg.net

Session ID: CSSE2010EXT

School of Information Technology and Electrical Engineering
The University of Queensland

Learning Lab 3
Binary Arithmetic

- Binary arithmetic revision ✓
- Circuits which do arithmetic ✓
- IN students – use Logic Ics or Logisim
- EX students – use Logisim ✓

What is -16 (base 10) expressed in 8-bit two's complement format?

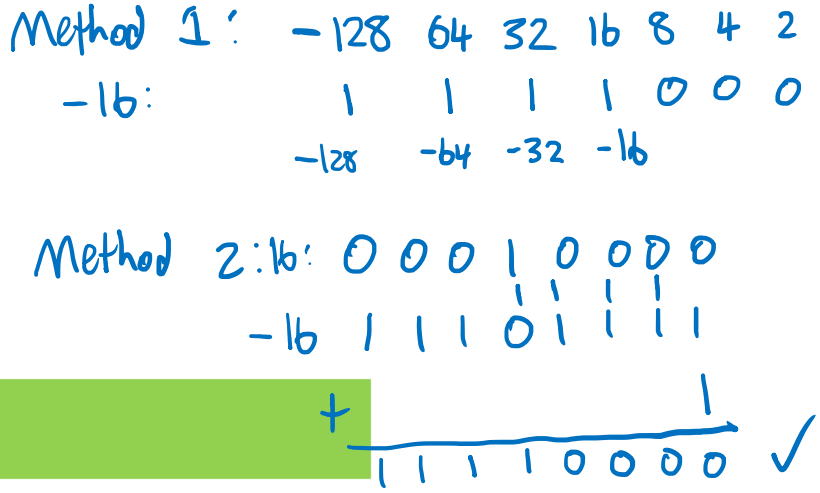
6% A. 10010000

13% B. 11101111

16% C. 10010001

65% ✓ D. 11110000 ✓

0% E. I don't know



0

What is the result of adding the 6-bit two's complement numbers 001110 and 110100?

39%	A.	000010 with overflow
52%	B.	000010 with no overflow
6%	C.	000110 with overflow
0%	D.	000110 with no overflow
0%	E.	001100 with overflow
0%	F.	001100 with no overflow
0%	G.	111110 with overflow
3%	H.	111110 with no overflow
0%	I.	I don't know

Cin of MSB

Cout of MSB

```
  1 1 1
  0 0 1 1 1 0
+ 1 1 0 1 0 0
-------------
  0 0 0 0 1 0
```

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	0

at MSB, Cin ≠ Cout

↳ overflow has occurred

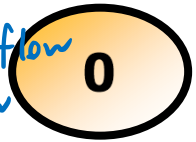
Cin ⊕ Cout = 0 → no overflow

= 1 → overflow

+ve + -ve, -ve + +ve → never overflow

-32 to 31 : 31 + 0 → 31

-32 + 0 → -32



MSB 0 -> +ve number
1 -> -ve number

Which of the following operations will result in an overflow in 4-bit two's complement arithmetic?

46% A. 0100 + 0101 Could overflow

19% B. 0100 – 0101 +ve -+ve +ve + -ve -> cannot overflow

5% C. 1001 – 0001 -ve - +ve -ve + -ve -> could overflow

3% D. 1001 + 0001 -ve + +ve -> cannot overflow

27% E. None of the above

0% F. I don't know

0 1 0 0 +ve
+ 0 1 0 1 +ve
-> -> 1 0 0 1 -ve

Cin MSB = 1
Cout MSB = 0
1 ≠ 0 -> overflow has occurred

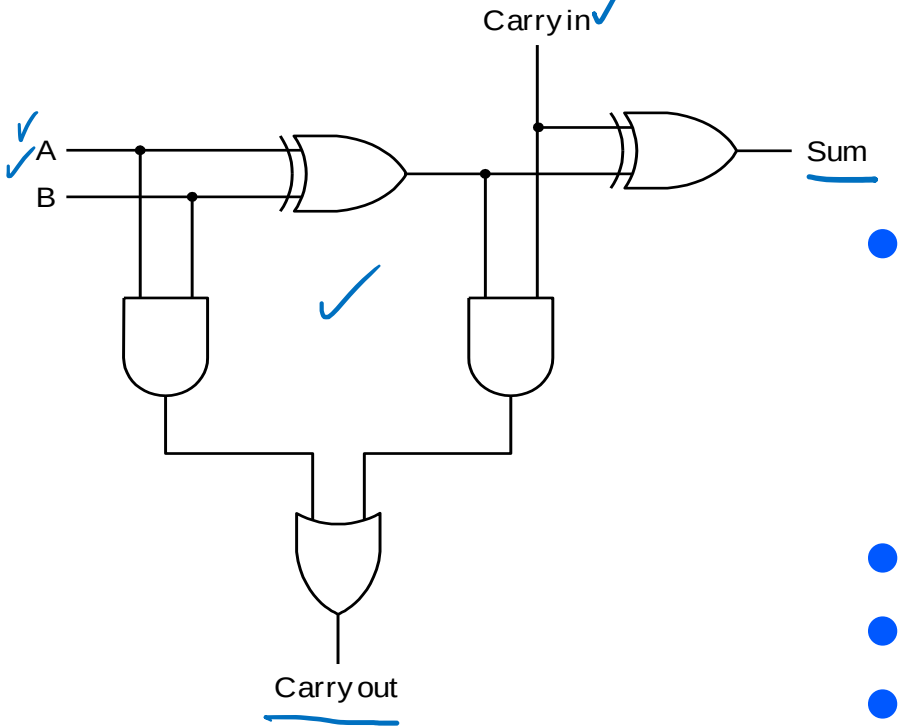
1 1 1 1
1 0 0 1
+ 1 1 1 0
+ 1
1 0 0 0 ✓

1 0 0 1
- 0 0 0 1
1 0 0 0 V

0 1 0 0
- 0 1 0 1
0 0 0
0 0 1 0 0
+ 1 0 1 0
1
1 1 1 1

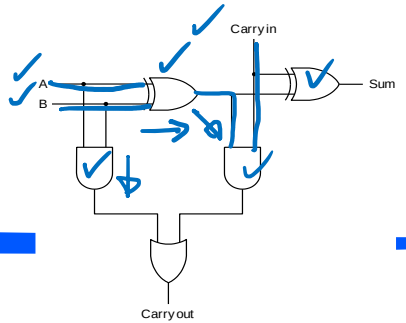
0

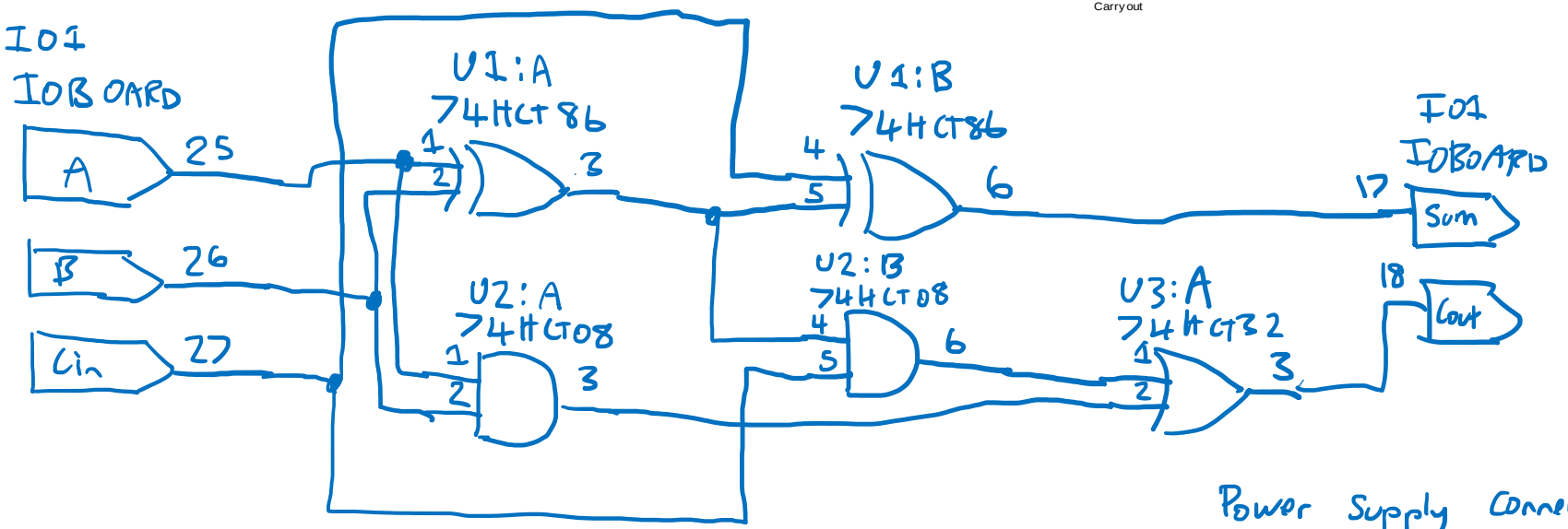
1-bit Full Adder (from lecture)



- Draw a circuit schematic diagram for a circuit which implements a full adder
  - Use switches for the 3 inputs and LEDs for the 2 outputs
- Have it checked by a tutor
- Build it or simulate it
- Test it systematically

Circuit schematic



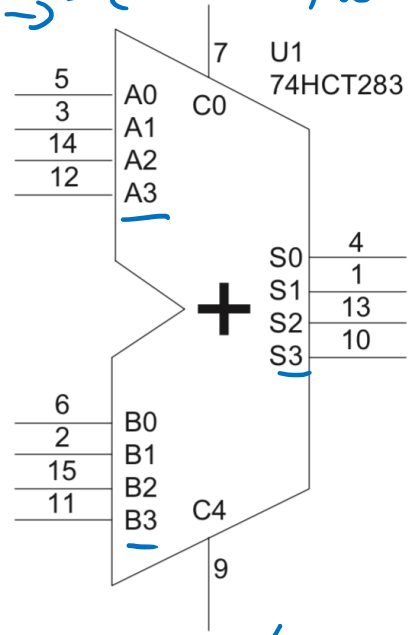


Power Supply Connections

74HCT08, 74HCT32, 74HCT86 } Vcc: 14, GND: 7

4-bit adder: 74HCT283

- 74HCT283 = Single chip 4-bit adder
- Draw a circuit schematic that uses this chip to add two 4-bit numbers (on switches) and shows the result (4-bit output and carry out) on LEDs. Connect the carry-in to a push button
  - Use the symbol shown here
    - See details on Blackboard
    - Don't forget power supply connections (16 pin chip)
- Have the schematic checked by a tutor
- Wire up and test the circuit or simulate the circuit
  - Try some unsigned and two's complement test cases
    - Are the results as you expect?
- Extension – add a 2's complement overflow detector circuit with LED output



EX students: use Logisim adder block with gates as required to simulate