CSSE2010

Welcome!

CSSE2010/CSSE7201
Learning Lab 4

Combinational Logic Circuits

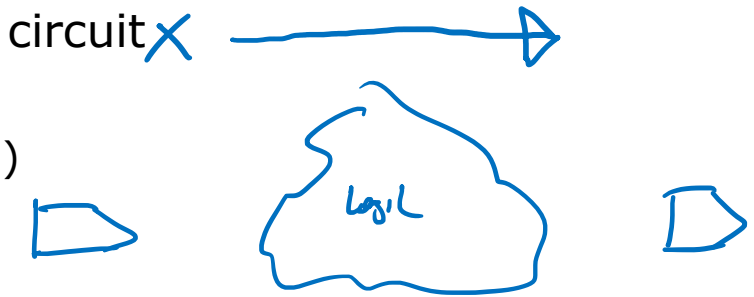
School of Information Technology and Electrical Engineering
The University of Queensland

Learning Lab 4
Combinational Logic

- Complete the lab 4 preparation tasks.✓
- Make sure that you have correctly drawn circuit schematics for the 3 circuits mentioned in the preparation task.✓
- Get tutor help to verify your schematic diagrams.✓
- **IN students**: construct the circuits on breadboard and verify the functionality or use Logisim
- **EX students**: Create the circuits in Logisim and verify the functionality in simulation.✓

Circuit Construction Advice

- Try to keep circuits neat
  - Use the shortest wires you can
- Turn the power off before you change the circuit
- Debugging
  - Use the logic probe (PR pin on the IO board)
  - Be systematic
    - Check power/ground connections first
    - Start at the inputs, work towards outputs



- **EX students:** keep your Logisim files organised as you will be doing this for the coming labs and you will need your files to revise things for assignment 1.
- **IN students:** You may take photos/videos of your circuit before disconnecting as this might help you to revise things for your lab assignment 1. If you don't have a kit, use Logisim and keep your design files organised.

For Each Circuit

- Make sure you have a correct schematic before you build
- Decide your test procedure – what truth table are you expecting?
- Build/simulate your circuit
- Test systematically

Don't expect things to always work in the first instance. If things don't work, troubleshoot systematically. Troubleshooting is also a part of your learning. A neatly drawn circuit schematic will always help when troubleshooting.

CSSE2010

Circuit Construction Advice

- Try to keep circuits neat
  - Use the shortest wires you can
- Turn the power off before you change the circuit
- Debugging
  - Use the logic probe (PR pin on the IO board)
  - Be systematic
    - Check power/ground connections first
    - Start at the inputs, work towards outputs