CSSE2010

CSSE2010/CSSE7201
Lecture 23

File Systems, Buses & Chipsets

School of Information Technology and Electrical Engineering
The University of Queensland

Virtual I/O - Files

- User/programmer do not want to worry about unit numbers, heads, cylinders, sectors, timeout errors, retries, etc.
- Common I/O abstraction is the file
  - To the Operating System, a file is just a sequence of bytes
    - Any structure is up to the application program

File System

- Computers easier to use (and program) when files have names
- **File system**
  - Associates files (collections of sectors) with names and directories
- Some sectors used for index information (e.g. File Allocation Table)
- Other sectors store the files themselves
- Many different file systems
  - FAT, FAT32, NTFS, exFAT, EXT2, EXT3, EXT4, APFS, HFS+, UFS, ZFS, …

Disk Formatting

- **Low level format**
  - Reinitialises all sectors
    - Preambles, data (empty), ECCs
  - No file system
- **High level format**
  - Creates empty file system
  - Only writes index/table sectors

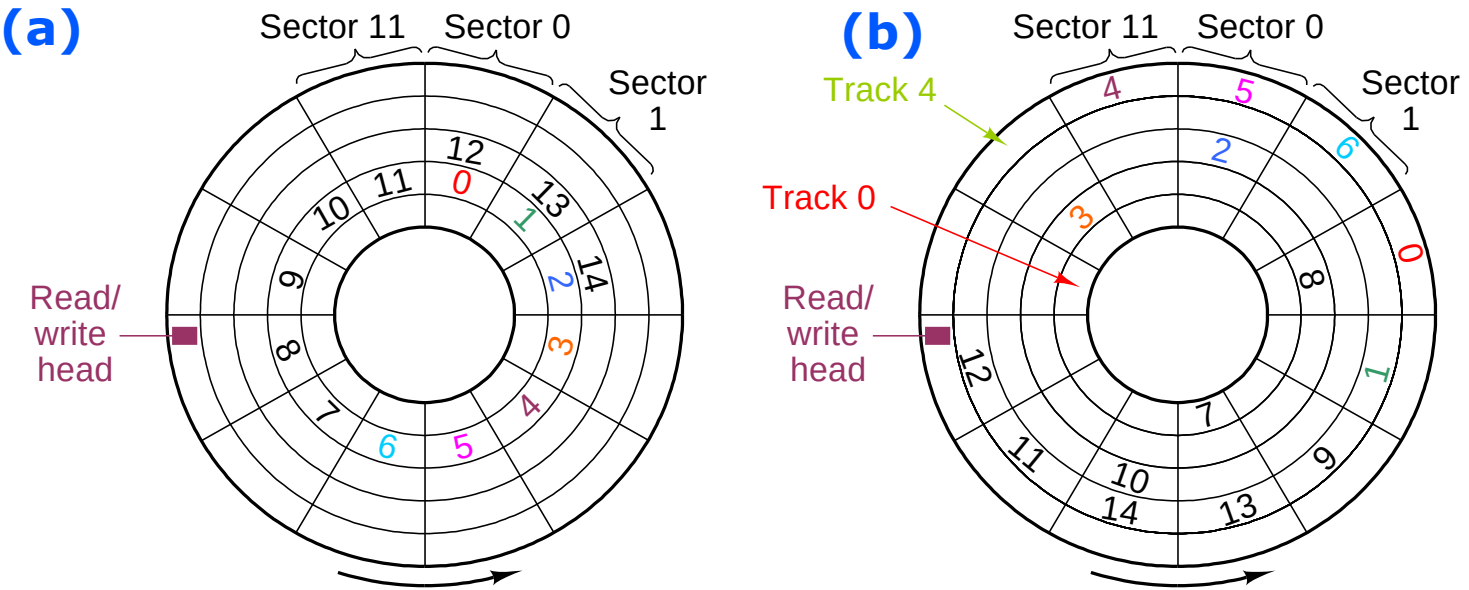
- Deleting a file doesn't mean it's gone!
  - OS may just delete the index entry, not overwrite the sectors where actual data stored

Files

- OS allows file names (e.g. FinalReport.doc) rather than cylinder and sector numbers
- File storage is allocated in **blocks** or allocation units
- Block could be as small as 1 sector or could be several consecutive sectors
  - Block sizes typically 512 bytes to 32kB
- OS maintains map from file name to a set of blocks
  - To help users, a hierarchy of directories (folders) can be used
- Larger block sizes reduce the size of this map, but increases wasted space at EOF
  - *To be illustrated in class*

Block Size and Wasted Space

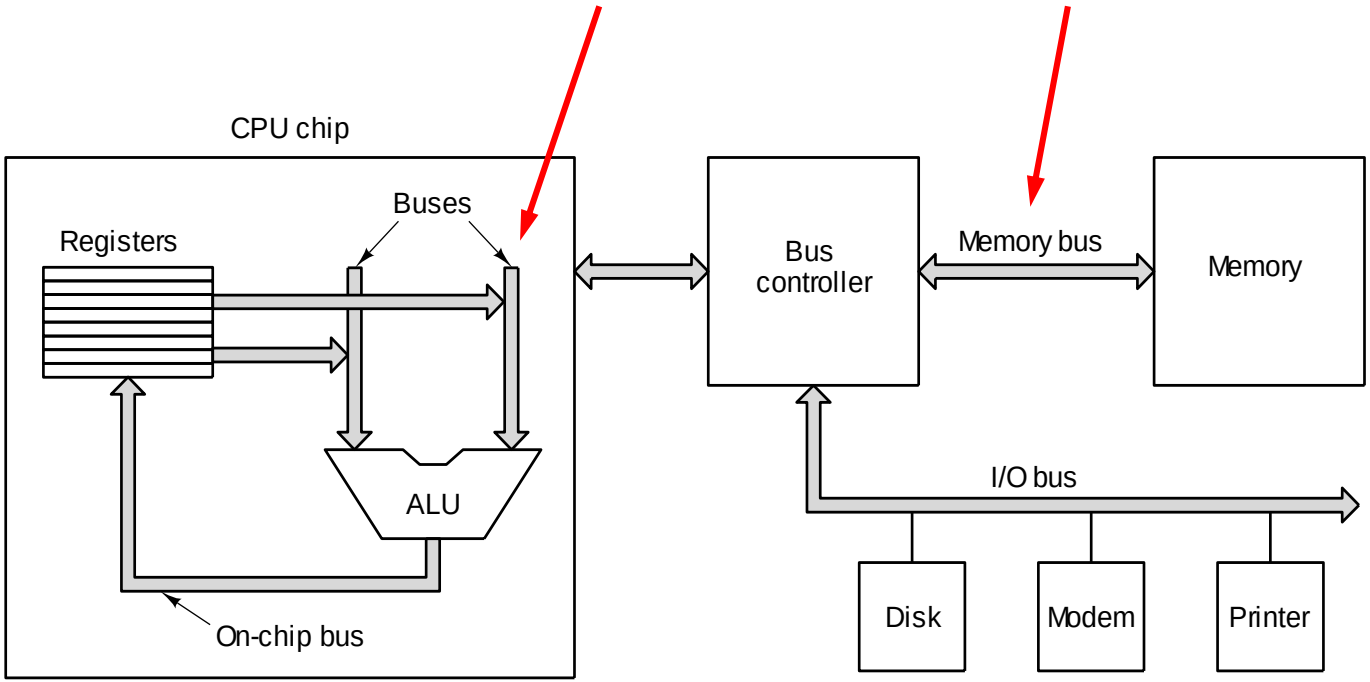
Disk Allocation



- Two possible allocations of 15 sectors (assume 1 block = 1 sector)
- (a) is ideal but unlikely as disks become fragmented (e.g. (b))
- Fragmentation → slow access (seek time and rotational latency)

Buses are Everywhere...

- Buses are both internal and external to the CPU

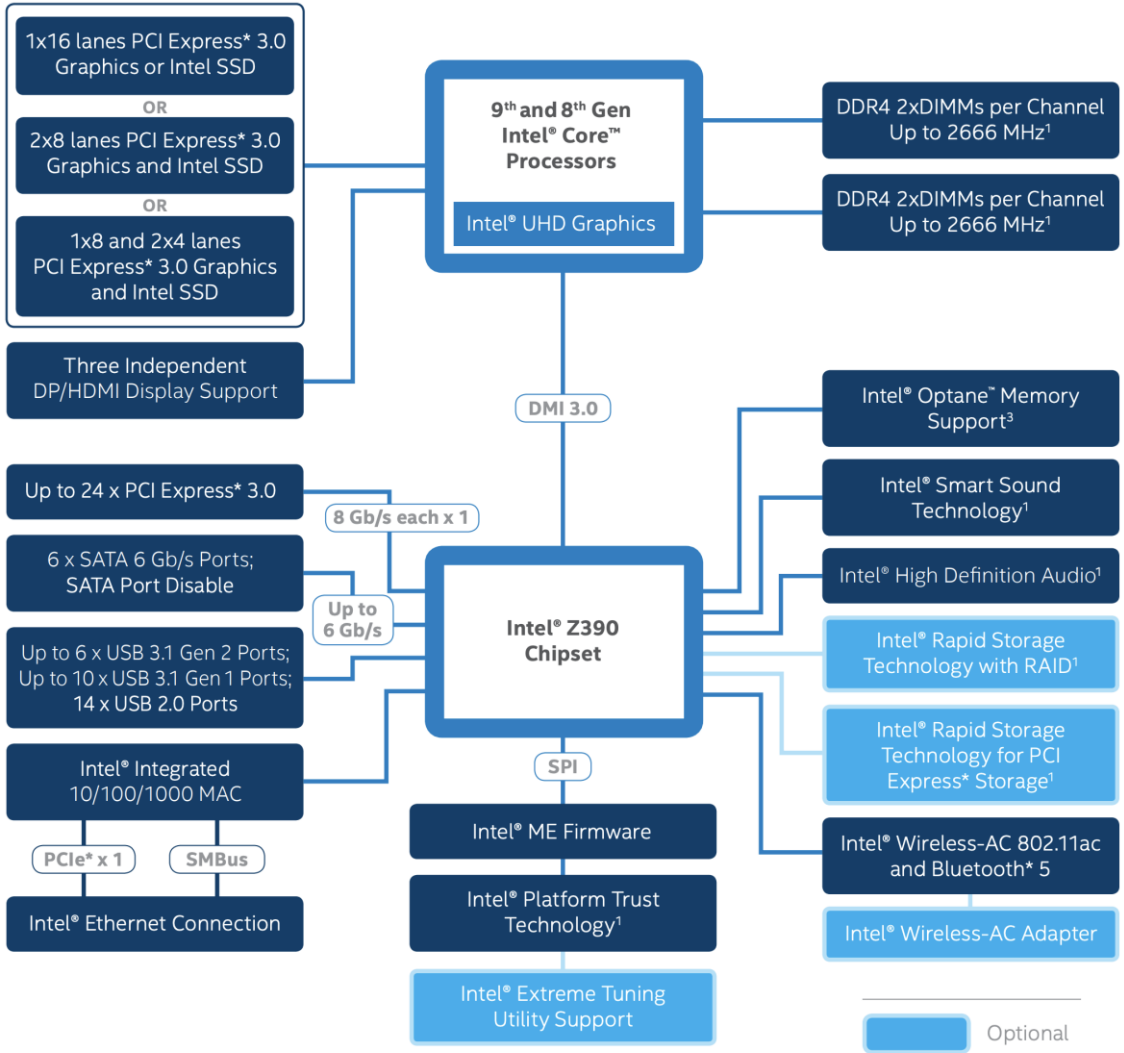


Bus Controller

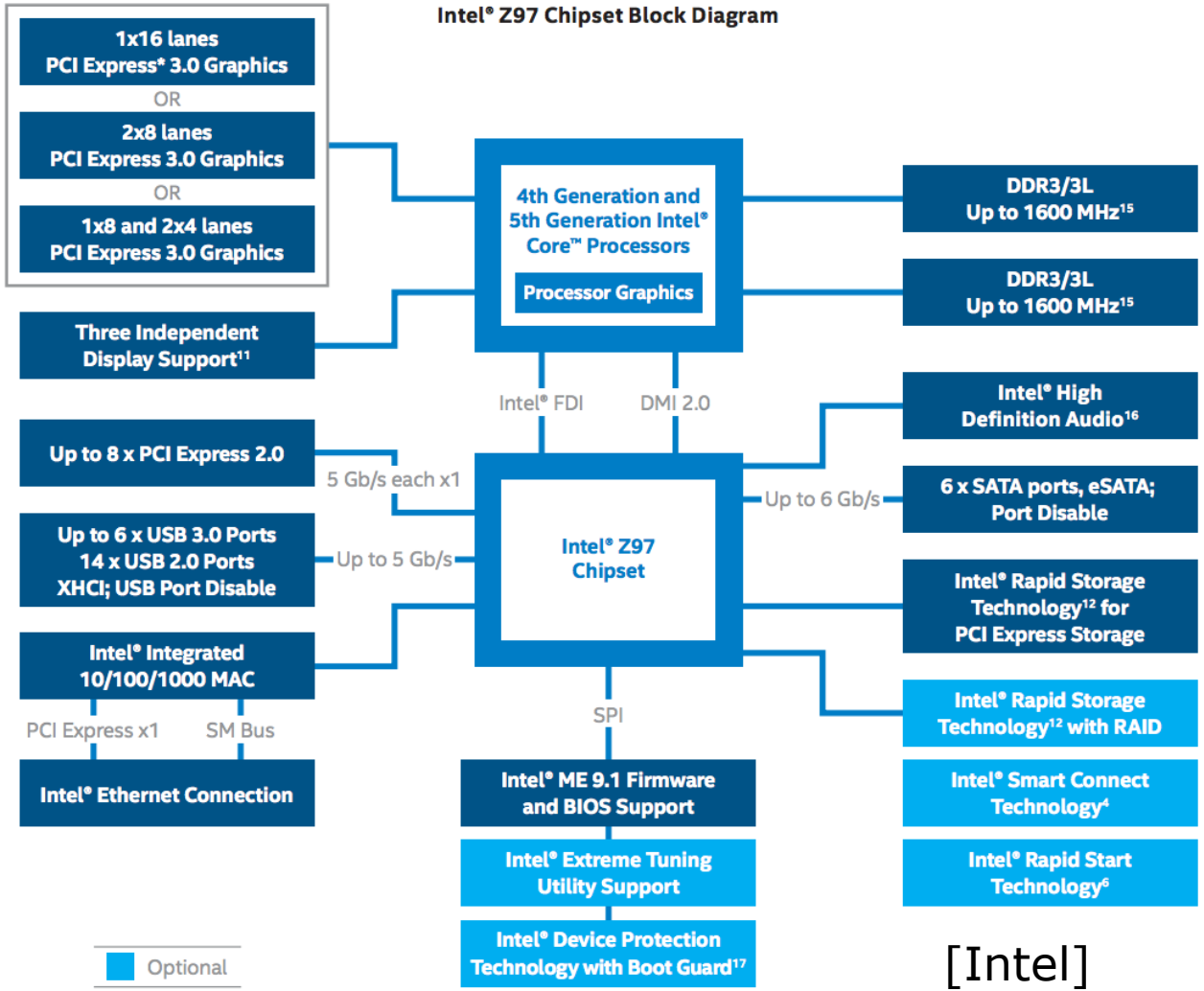
- In the PC world, Bus Controller is called a **chipset**
- Particular chipsets support particular bus standards
- Memory:
  - DDR4-RAM, DDR3, DDR2, …
- I/O:
  - PCI Express, USB, SATA, PCI, …

Intel Z390 Chipset

(Late 2018)



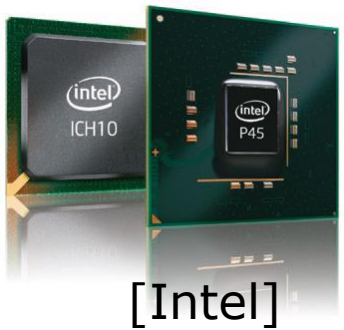
[Intel]


Intel® Z97 Chipset Block Diagram
1x16 lanes
PCI Express* 3.0 Graphics
OR
2x8 lanes
PCI Express 3.0 Graphics
OR
1x8 and 2x4 lanes
PCI Express 3.0 Graphics
Three Independent
Display Support[11]
Up to 8 x PCI Express 2.0
Up to 6 x USB 3.0 Ports
14 x USB 2.0 Ports
XHCI; USB Port Disable
Intel® Integrated
10/100/1000 MAC
PCI Express x1
SM Bus
Intel® Ethernet Connection
4th Generation and
5th Generation Intel®
Core™ Processors
Processor Graphics
Intel® FDI
DMI 2.0
5 Gb/s each x1
Up to 5 Gb/s
Intel® Z97
Chipset
SPI
Intel® ME 9.1 Firmware
and BIOS Support
Intel® Extreme Tuning
Utility Support
Intel® Device Protection
Technology with Boot Guard[17]
DDR3/3L
Up to 1600 MHz[15]
DDR3/3L
Up to 1600 MHz[15]
Intel® High
Definition Audio[16]
Up to 6 Gb/s
6 x SATA ports, eSATA;
Port Disable
Intel® Rapid Storage
Technology[12] for
PCI Express Storage
Intel® Rapid Storage
Technology[12] with RAID
Intel® Smart Connect
Technology[4]
Intel® Rapid Start
Technology[6]
Optional

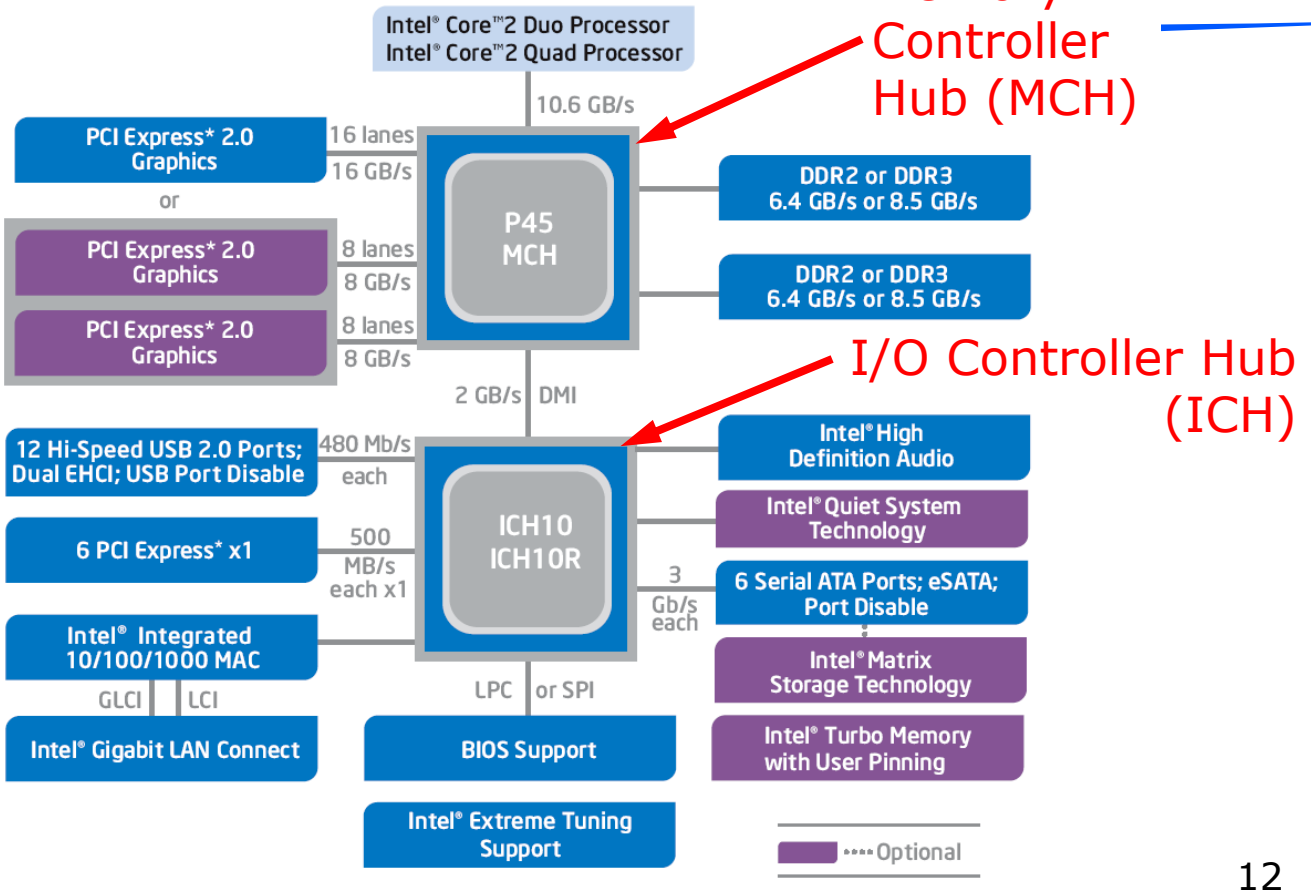
[Intel]

Intel P45 Express Chipset

Last chipset to use MCH/ICH (2008)



[Intel]

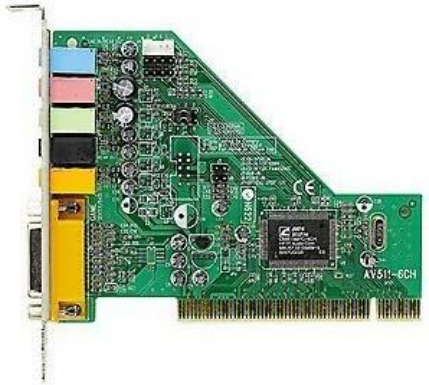


Peripheral Buses (or I/O buses)

- **Peripheral** = External input/output device
- Peripheral bus = input/output bus
- Examples:
  - PCI Express
  - PCI
  - USB
  - Firewire
  - SATA
  - SCSI
- And some "dead" ones:
  - ISA, EISA, Omnibus, Unibus, Multibus, MCA, Nubus, AGP, …

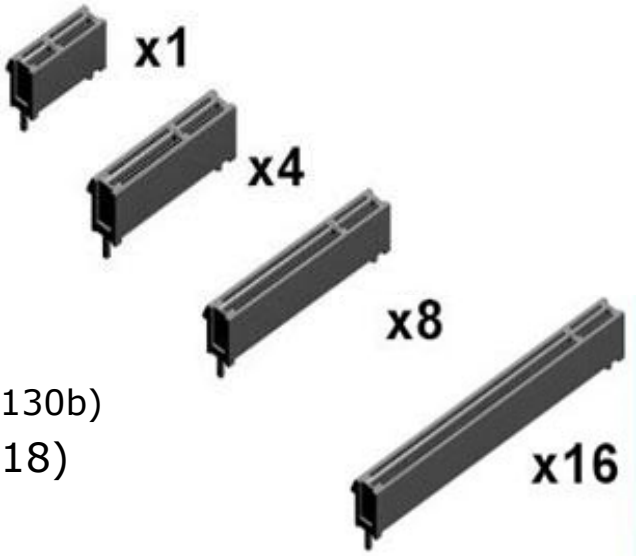
PCI Bus

- **P**eripheral **C**omponent **I**nterconnect bus
- Patented by Intel, but in public domain
  - PCI 1
    - 32 bits wide, 33MHz ➔ 132MB/sec max transfer rate
  - PCI 2.2
    - up to 64 bits, 66MHz ➔ 528MB/sec max transfer rate
  - 32 bit cards have 120 pins; 64 bit cards have an extra 64-pin connector
- It is a parallel bus
- 5V and 3.3V options



PCI Express (PCIe) Bus

- High-speed, serial bus standard
- x1 version = 2 Gbits/second
- x16 version =
  32 Gbits/second =
  4 GBytes/second



- PCI Express 2.0 (2007)
  - doubles the data rates above
- PCI Express 3.0 (2010)
  - 8 GT/second (GigaTransfers – using 128b/130b)
- PCI Express 4.0 (standard ratified Jan 2018)
  - double PCIe 3.0
- PCI Express 5.0 (expected 2019)
  - double again

Standard released 29 May 2019
PCI Express 6.0 expected 2021

Universal Serial Bus (USB)

- Originally only 4 wires (power, ground, data x 2)
- Devices can be powered from cable
- Up to 127 devices
- Hot-pluggable (i.e. can plug in/out whilst power is on)
- USB1.0 (1996, updated to v1.1, 1998)
  - 1.5Mbits/sec (**low-speed**)
  - 12Mbits/sec max (1.5MB/sec, **full-speed**)
- USB2.0 (2000)
  - 480Mbits/sec max (**hi-speed**)
- USB3.0 (2008, 9 wires, different connector)
  - 5Gbits/sec (**super-speed**) (full duplex)
- USB3.1 – 10Gbps (2013)
- USB3.2 – 10Gbps and 20Gbps over USB-C connector (2017)

Rates are data signaling rates

Realistic Transfer Rates

- Most buses can't achieve maximum transfer rates in real-life situations
  - Communication occurs in both directions
  - Buses are often shared between multiple devices