CSSE2010/CSSE7201 – Introduction to Computer Systems
Semester One, 2019

Lab 4 Preparation Task

You should complete three circuit schematic diagrams as listed below before your Monday/Tuesday/Wednesday lab session in week 3 of semester (**Monday 11 March to Wednesday 13 March**). You should consult the device pinout information on Blackboard. You will be constructing these circuits during the prac session.

Circuit 1

Draw a circuit schematic diagram for a 2-to-1 multiplexer that uses only 2-input NAND gates. The data inputs should be connected to push buttons. The select input should be connected to a switch. The output should be connected to an LED.

Circuit 2

Draw a circuit schematic diagram for a 2-to-4 decoder - using whichever logic gates you prefer (from those available in the CSSE2010/CSSE7201 lab). The two inputs should be connected to switches. The outputs should be connected to LEDs.

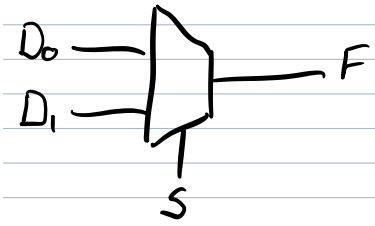
A 2-to-4 decoder has the following truth table (labelling inputs A1, A0 and outputs X0, X1, X2, X3):

A1	A0	X0	X1	X2	X3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit 3

Using a 74HCT04, 74HCT157 and a 74HCT283, draw a circuit schematic diagram for a circuit which can act as a 4-bit two's complement adder or subtractor. The output (4-bits from the 74HCT283, which should be shown on LEDs) will have the value A+B or A-B (where A and B are the 4-bit inputs which are taken from switches). A push button input (M, mode) will determine whether the circuit performs addition or subtraction - if the value is 0, addition will be performed; if the value is 1, subtraction will be performed by calculating A+(-B). The circuit is similar to that shown in lecture 4 (Wednesday 6 March) except the selection of the "B" input bits as B or not(B) is to be performed using multiplexers instead of XOR gates. (The 74HCT157 is a quad 2-to-1 multiplexer with a shared select input.) The carry output should be shown on a LED also.

Circuit 1 – 2-1 Multiplexer



Function Table

S	F
0	D_0
1	D_1

Truth Table

S	D_1	D_0	F
0	0	0	0
0	0	1	1 ←
0	1	0	0
0	1	1	1 ←
1	0	0	0
1	0	1	0
1	1	0	1 ←
1	1	1	1 ←

$$F = \bar{S}\bar{D_1}D_0 + \bar{S}D_1D_0 + S\bar{D_1}\bar{D_0} + SD_1D_0$$

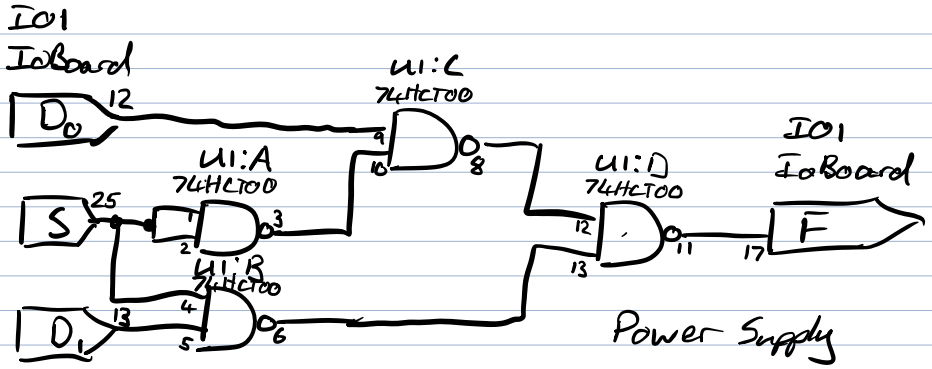
Distributative law	A + BC = (A + B)(A + C)	A(B + C) = AB + AC

$$= \bar{S}D_0(\bar{D_1} + D_1) + SD_1(\bar{D_0} + D_0)$$

$$= \bar{S}D_0 + SD_1$$

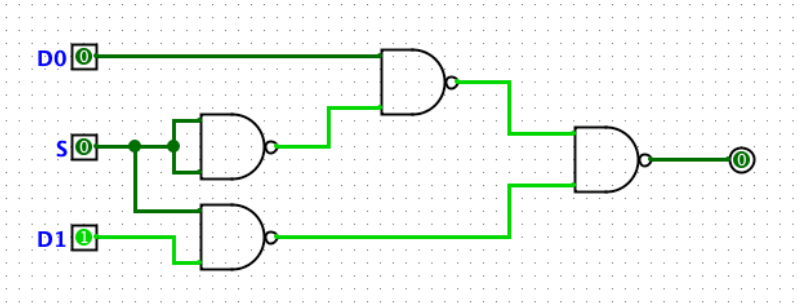
$$= \overline{\bar{S}D_0} \cdot \overline{SD_1}$$

OR = AND (De Morgans Law)

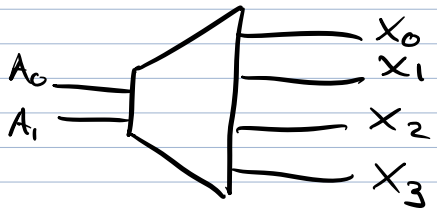


Power Supply

74HCT00 Vcc: Pin 14
GND: Pin 7



Circuit 2



A1	A0	X0	X1	X2	X3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$X_0 = \bar{A}_1 \bar{A}_0$

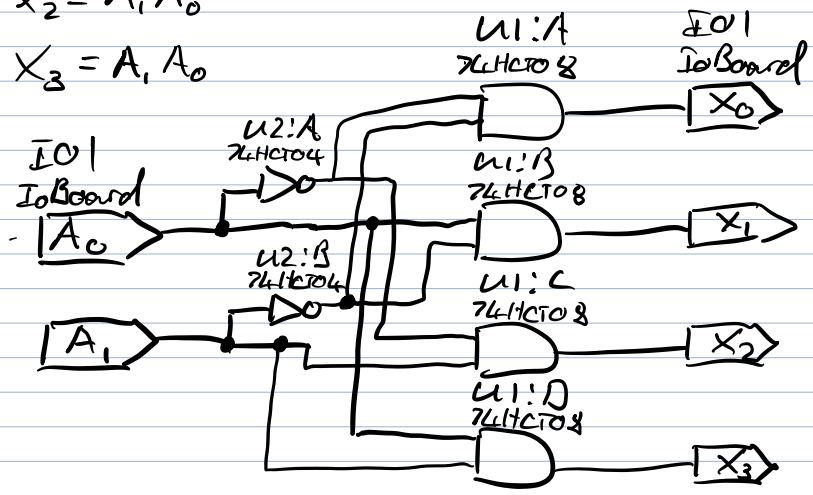
$X_1 = \bar{A}_1 A_0$

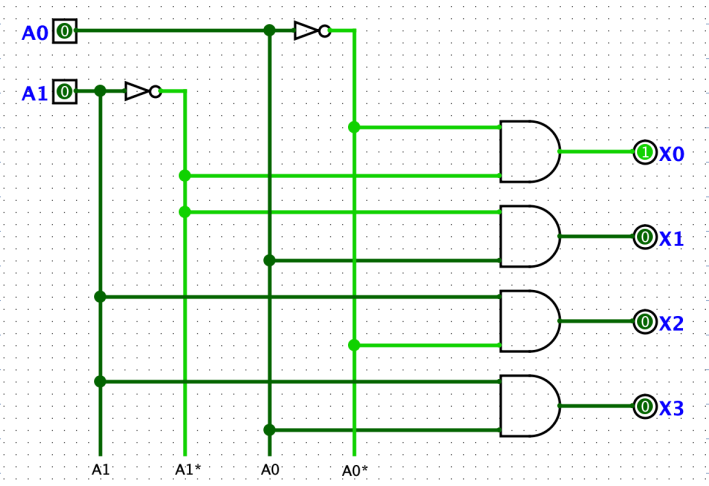
$X_2 = A_1 \bar{A}_0$

$X_3 = A_1 A_0$

Power

74HCT04 } Vcc: Pin 14
74HCT08 } GND: Pin 7





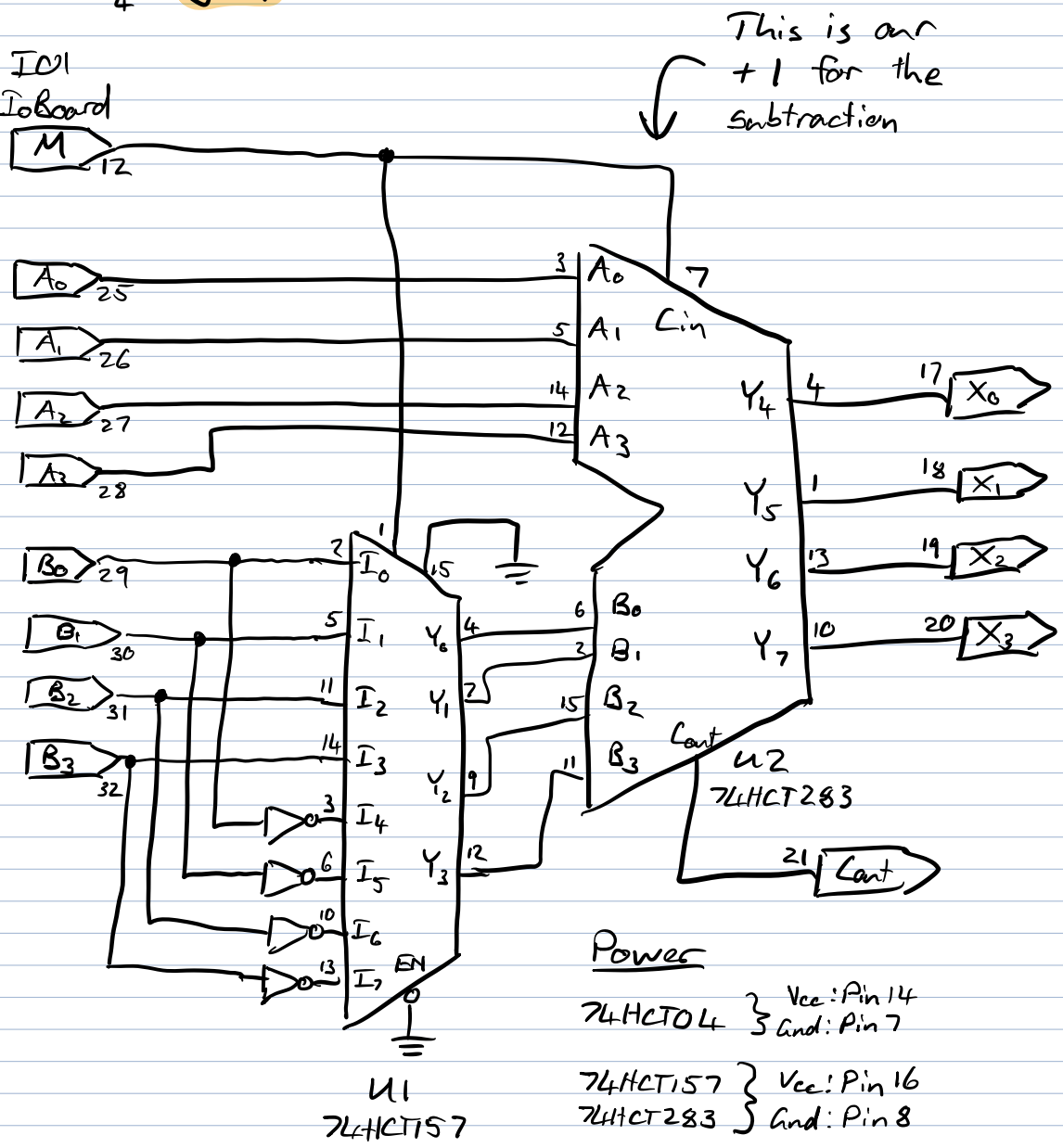
Circuit 3 - 4-bit adder/subtractor (2's comp)

$S_4 = A_4 + B_4$ Addition

or

$S_4 = A_4 + (-B)$ Subtraction

$= A_4 + \bar{B} + 1$

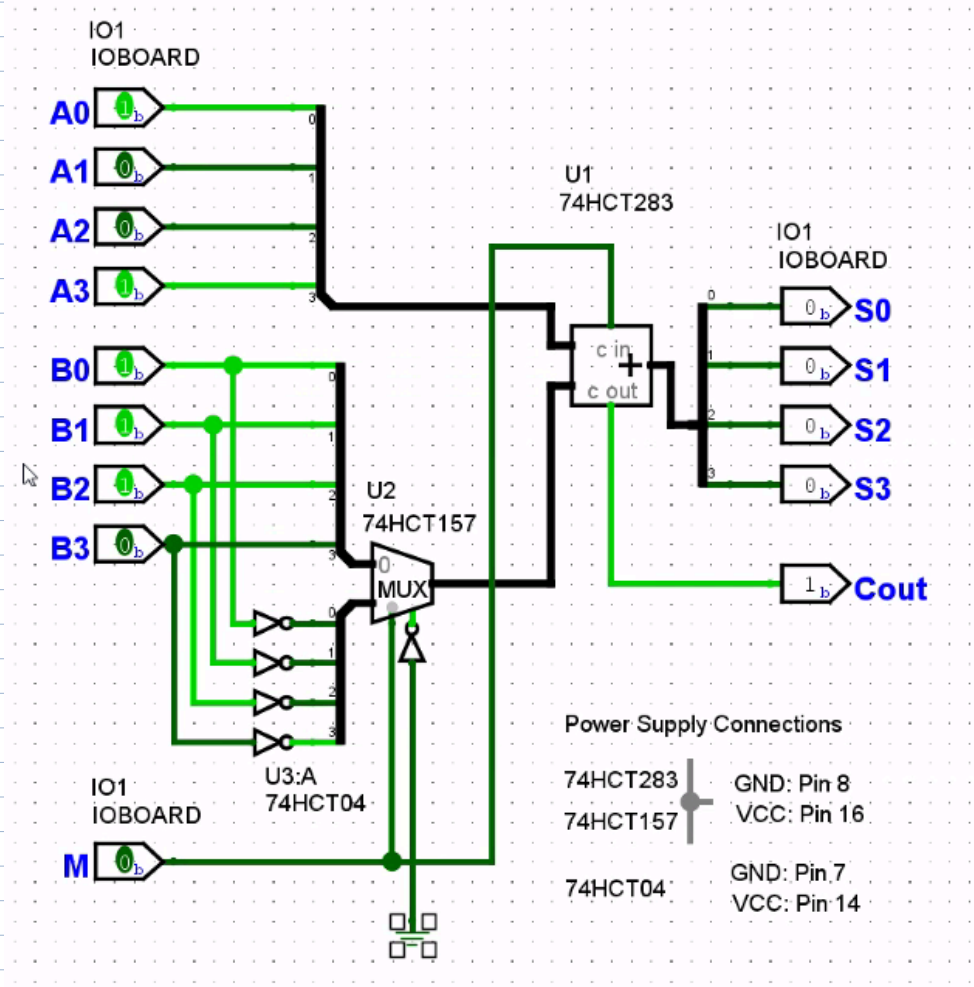


Power

74HCT04 } Vcc: Pin 14, Gnd: Pin 7

74HCT157 } Vcc: Pin 16

74HCT283 } Gnd: Pin 8


IO1
IOBOARD
A0
A1
A2
A3
B0
B1
B2
B3
U1
74HCT283
c in
c out
IO1
IOBOARD
S0
S1
S2
S3
Cout
U2
74HCT157
MUX
U3:A
74HCT04
IO1
IOBOARD
M
Power Supply Connections
74HCT283
74HCT157
GND: Pin 8
VCC: Pin 16
74HCT04
GND: Pin 7
VCC: Pin 14