# CSSE2010 / CSSE7201 – Introduction to Computer Systems
# Exercises – Week Thirteen
# Buses, Pipelines, Floating Point

## *Exercises*

1. Calculate how long it would take to transfer 100Mbytes (100 x $10^6$ bytes) over
   (a) a 32-bit 33MHz PCI 1 bus
   (b) a 64-bit 66MHz PCI 2.2 bus
   (c) a PCI Express (PCIe, version 1) x1 bus
   (d) USB full-speed bus
   (e) USB hi-speed bus
   Assume that it is possible to sustain the maximum possible transfer rate for the whole transfer. (This is unlikely in practice.)
2. A certain processor has a pipeline composed of four stages, labeled "fetch", "decode", "operand fetch" and "execute". Each of these has a latency (total time) of 1, 1, 2, and 3 clock cycles respectively. (The operand fetch and execute stages are themselves pipelined with substages taking one clock each.)
   (a) Draw a diagram of a stream of instructions (ignore branches) flowing through the pipeline, showing individual instructions and how they progress through the pipeline over time.
   (b) How long does it take for the first instruction to progress through the pipeline?
   (c) What is the latency of this pipeline?
   (d) What is the maximum throughput of this pipeline, (i.e. assuming no stalls)?
3. What is the decimal value of the IEEE floating point number 0xBF800000?
4. What are the IEEE single and double precision floating point representations (in hexadecimal) of
   (a) –3.25
   (b) +75.125