CSSE2010/CSSE7201
Lecture 25

Exam Info/Pipelining

School of Information Technology and Electrical Engineering
The University of Queensland

Admin/Reminders

- Assignment 2 is due Monday 01/11/21 4:00PM Brisbane time. Submission is open and please read the submission instructions given in the assignment specification document
- Penalties apply for late submissions (i.e. 10% plus 10% per calendar day or part thereof) as well as for compilation errors and warnings. Late penalties do not apply if you have an extension approved. Any extension requests must be submitted via my-UQ, **before the deadline** with a valid reason.
- Keep backups and have a working version of your Microchip studio project and a series of backups with data/time stamped.

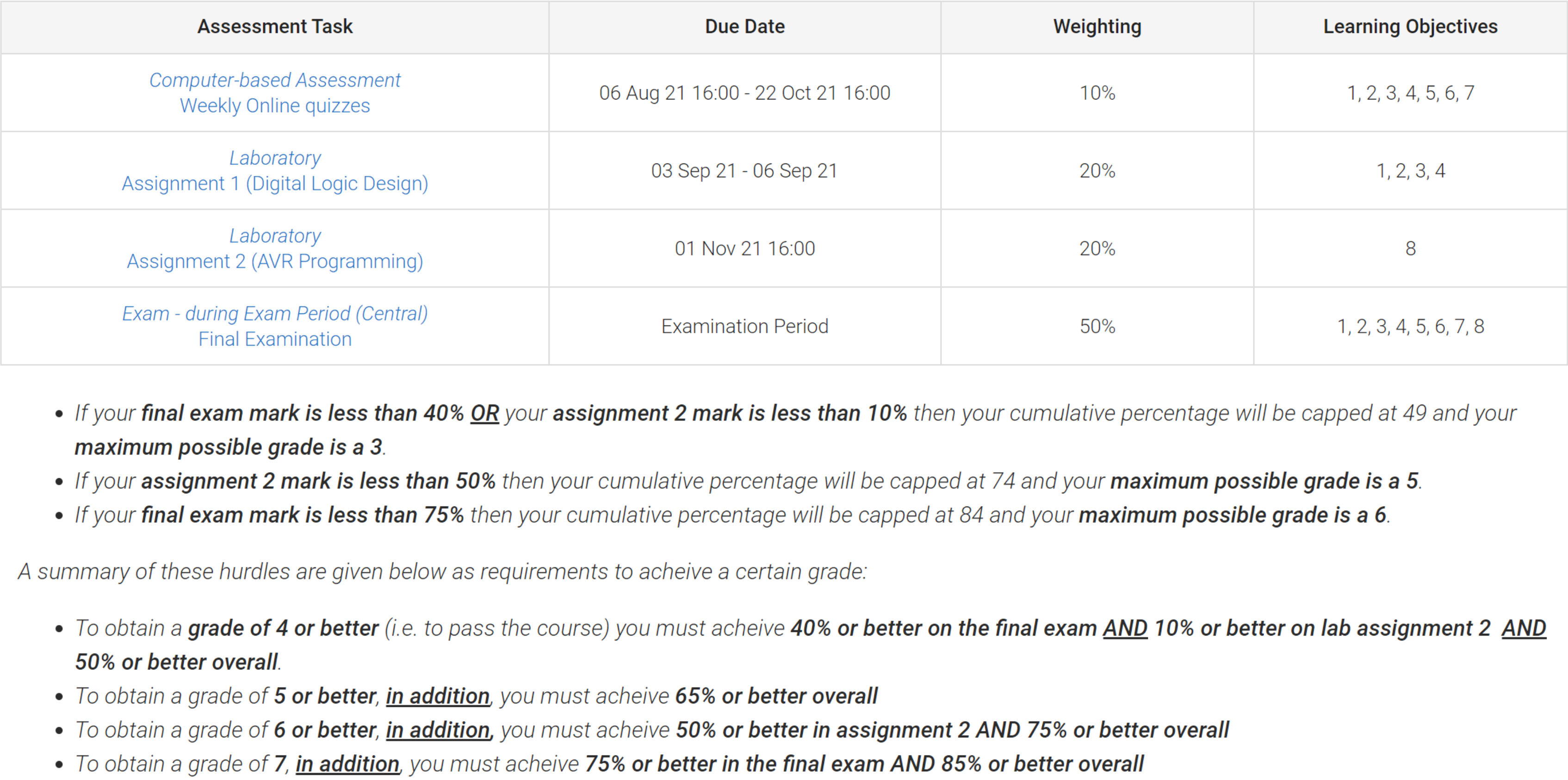
Admin/Reminders

- IN students – kit return information is posted on Blackboard. Please return your kits by 12PM Friday 5th November 2021

Admin/Reminders

- Final Exam
  - IN – paper based 2-hour written exam, invigilated, on-campus. EX students who have been approved can also sit this exam.
  - EX- online invigilated 2-hour exam (ProctorU) on a separate exam Blackboard site.
  - Both versions are open book – any printed material is allowed. It is recommended that you have printed versions of AVR I/O register summary (4-pages) and AVR instruction set summary (5 pages) with you.
  - Past exam papers will be provided on Blackboard and an exam review session will be held during the revision week (i.e. next week).

Admin/Reminders



Assessment Task	Due Date	Weighting	Learning Objectives
Computer-based Assessment Weekly Online quizzes	06 Aug 21 16:00 - 22 Oct 21 16:00	10%	1, 2, 3, 4, 5, 6, 7
Laboratory Assignment 1 (Digital Logic Design)	03 Sep 21 - 06 Sep 21	20%	1, 2, 3, 4
Laboratory Assignment 2 (AVR Programming)	01 Nov 21 16:00	20%	8
Exam - during Exam Period (Central) Final Examination	Examination Period	50%	1, 2, 3, 4, 5, 6, 7, 8

- *If your **final exam mark is less than 40% OR** your **assignment 2 mark is less than 10%** then your cumulative percentage will be capped at 49 and your **maximum possible grade is a 3**.*
- *If your **assignment 2 mark is less than 50%** then your cumulative percentage will be capped at 74 and your **maximum possible grade is a 5**.*
- *If your **final exam mark is less than 75%** then your cumulative percentage will be capped at 84 and your **maximum possible grade is a 6**.*

A summary of these hurdles are given below as requirements to acheive a certain grade:

- *To obtain a **grade of 4 or better** (i.e. to pass the course) you must acheive **40% or better on the final exam AND 10% or better on lab assignment 2 AND 50% or better overall**.*
- *To obtain a grade of **5 or better, in addition**, you must acheive **65% or better overall***
- *To obtain a grade of **6 or better, in addition,** you must acheive **50% or better in assignment 2 AND 75% or better overall***
- *To obtain a grade of **7, in addition**, you must acheive **75% or better in the final exam AND 85% or better overall***

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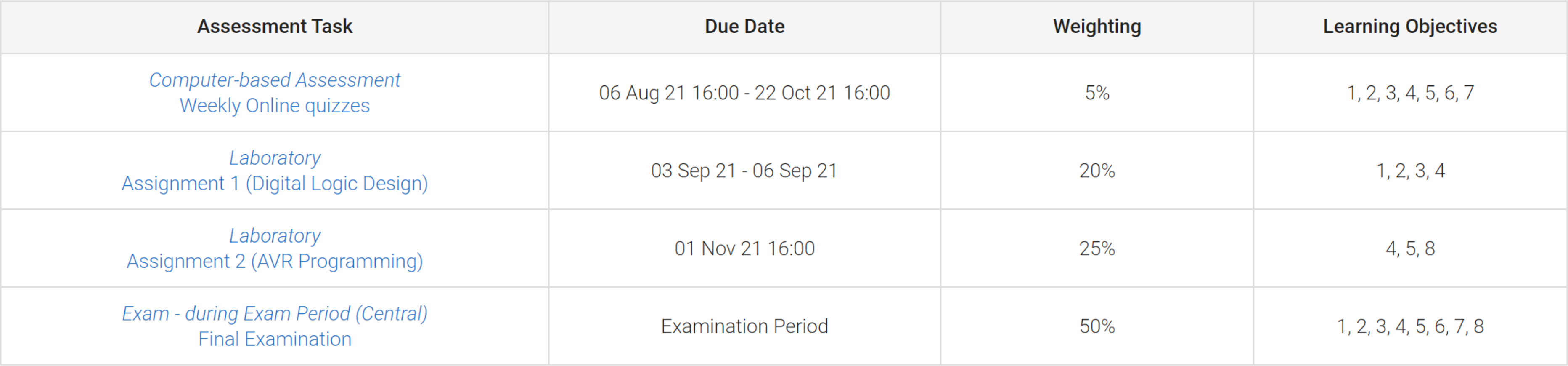
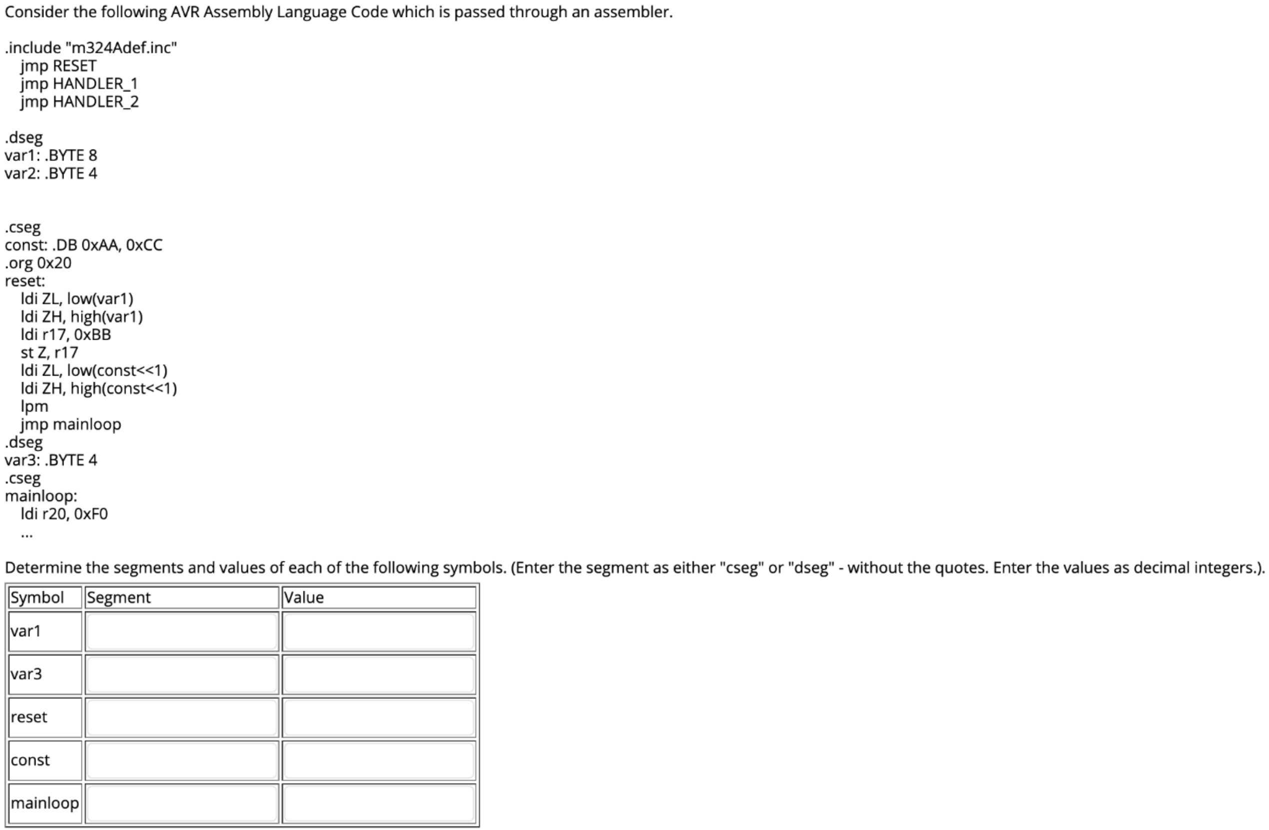


Assessment Task	Due Date	Weighting	Learning Objectives
Computer-based Assessment Weekly Online quizzes	06 Aug 21 16:00 - 22 Oct 21 16:00	5%	1, 2, 3, 4, 5, 6, 7
Laboratory Assignment 1 (Digital Logic Design)	03 Sep 21 - 06 Sep 21	20%	1, 2, 3, 4
Laboratory Assignment 2 (AVR Programming)	01 Nov 21 16:00	25%	4, 5, 8
Exam - during Exam Period (Central) Final Examination	Examination Period	50%	1, 2, 3, 4, 5, 6, 7, 8

Quiz 10 question



Consider the following AVR Assembly Language Code which is passed through an assembler.

```
.include "m324Adef.inc"
   jmp RESET
   jmp HANDLER_1
   jmp HANDLER_2

.dseg
var1: .BYTE 8
var2: .BYTE 4


.cseg
const: .DB 0xAA, 0xCC
.org 0x20
reset:
   ldi ZL, low(var1)
   ldi ZH, high(var1)
   ldi r17, 0xBB
   st Z, r17
   ldi ZL, low(const<<1)
   ldi ZH, high(const<<1)
   lpm
   jmp mainloop
.dseg
var3: .BYTE 4
.cseg
mainloop:
   ldi r20, 0xF0
   ...
```

Determine the segments and values of each of the following symbols. (Enter the segment as either "cseg" or "dseg" - without the quotes. Enter the values as decimal integers.).

Symbol	Segment	Value
var1		
var3		
reset		
const		
mainloop		

A 1TB (10^{12}) byte hard disk has 4kB blocks and holds 800,000 files with random sizes but an average size of 399kB. How much wasted space is there within the used blocks? (1kB = 1024 bytes)

- 13% A. 10^{12}/1024 - 800,000x399 kB
- 13% B. 800,000 x 399kB
- 13% C. 800,000 x 1kB
- 13% D. 800,000 x 2kB
- 13% E. 800,000 x 4kB
- 13% F. 399 x 2kB
- 13% G. 399 x 4kB
- 13% H. None of the above

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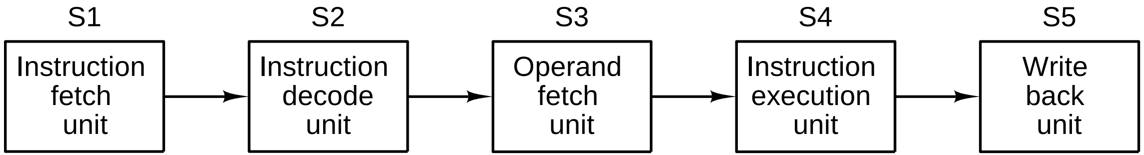
Pipelining

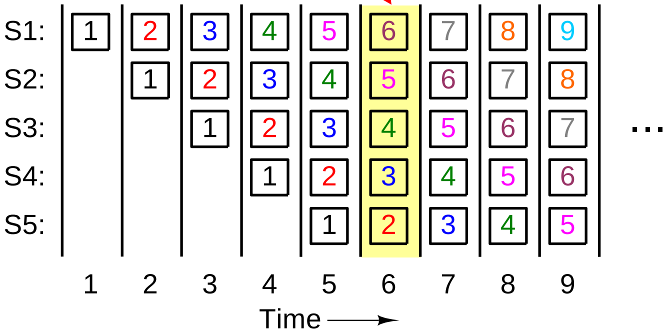
- Modern processors use the concept of pipelining extensively
- Example: five stage pipeline



(a)

At any one time up to five instructions are being executed

- one in each stage of the pipeline



	1	2	3	4	5	6	7	8	9
S1:	1	2	3	4	5	6	7	8	9
S2:		1	2	3	4	5	6	7	8
S3:			1	2	3	4	5	6	7
S4:				1	2	3	4	5	6
S5:					1	2	3	4	5

...

Time →

(b)

Why Pipelining?

- **Higher clock rate** (i.e. reduced clock cycle time)
  - Maximum clock rate determined by most complex logic path in circuit
    - Breaking up logic paths (into stages) allows faster clock
  - (By itself, clock rate is meaningless though)
- **Higher throughput**
  - More instructions executed per unit time
  - Achieve one instruction per cycle (if pipeline is full)

- Note: Latency (time per instruction) is the same or worse than non-pipelined processor

Pipelining Example

Pipelining (cont.)

- Even AVR has a small (2-stage) pipeline
  - Fetch and execute are separate stages
- At a branch, have to guess which instructions to continue putting into the pipe
  - If you guess wrong, have to throw away instructions which have started processing
  - Hence branch prediction is important