THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

This exam paper must not be removed from the venue

Venue _____

Seat Number _____

Student Number |__|__|__|__|__|__|__|__|

Family Name _____

First Name _____

School of Information Technology and Electrical Engineering

SAMPLE MID-SEMESTER EXAMINATION #6

Semester One Mid-semester Examinations, 2020

CSSE2010/CSSE7201 Introduction to Computer Systems

This paper is for St Lucia Campus students.

Examination Duration: 60 minutes

Reading Time: 10 minutes

Exam Conditions:

This is an Open Book Examination

Materials Permitted In The Exam Venue:

(No electronic aids are permitted e.g. laptops, phones)

Calculators - Casio FX82 series or UQ approved (labelled)

Materials To Be Supplied To Students:

1 x Multiple Choice Answer Sheet

Instructions To Students:

Answer all questions on the supplied "True/False and Multiple Choice Answer Sheet".

Choose the answer which best answers the question or completes the statement. Correct answers will be awarded one mark. Incorrect, missing or multiple answers will be awarded zero marks.

Total number of questions for the paper: 25

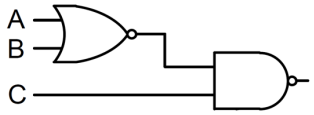
1. What is -73_{10} expressed in 8-bit two's complement format?
   (a) 01001000
   (b) 01001001
   (c) 10110110
   (d) 10110111
   (e) 11001001

2. What is the minimum number of hexadecimal digits needed to represent the octal number 120105?
   (a) 4
   (b) 5
   (c) 6
   (d) 18
   (e) None of the above

3. A 6-bit number in excess-32 format can represent integers from
   (a) –32 to 31
   (b) –31 to 32
   (c) –32 to 32
   (d) 0 to 63
   (e) None of the above

4. How can <u>any</u> n-bit ones' complement number be converted to an (n+1)-bit two's complement representation?
   (a) By prepending 0 and adding 1
   (b) By prepending the sign-bit, flipping all the bits and then adding 1
   (c) By prepending the sign-bit
   (d) By prepending the sign-bit and adding 1
   (e) By prepending the sign-bit and adding the value of the sign-bit

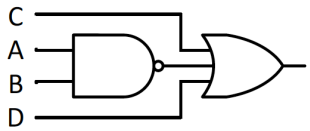
5. What function is implemented by the following circuit?

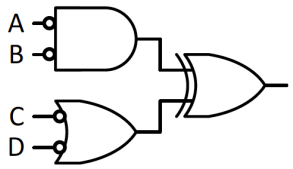


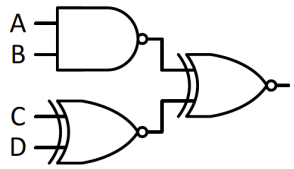
   (a) $\overline{A.B.C}$
   (b) $\overline{\overline{A+B}.C}$
   (c) $\overline{\overline{A}+\overline{B}.C}$
   (d) $\overline{(\overline{A}+\overline{B}).C}$
   (e) $\overline{\overline{A.B}+C}$

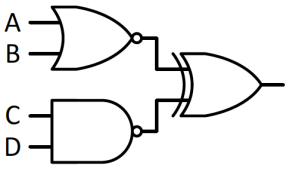
6. Which of the following logic functions is identical to $\overline{(A+B).(\overline{A}+B+C)}$?
   (a) $\overline{B}$
   (b) $\overline{A}.\overline{B}.\overline{C}$
   (c) $\overline{A}.\overline{B}+\overline{B}.\overline{C}$
   (d) $\overline{A}+\overline{B}+\overline{C}$
   (e) None of the above

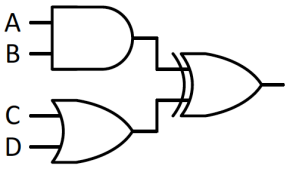
7. Which of the following logic circuits is an implementation of the function $(\overline{A.B}) \oplus (\overline{C+D})$?

(a) 

(b) 

(c) 

(d) 

(e) 

8. Which of the following truth tables is equivalent to the function

$X = (\overline{\overline{A}.\overline{C}}).(\overline{\overline{A}.B} + \overline{C}.B)$

(a)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(b)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(c)

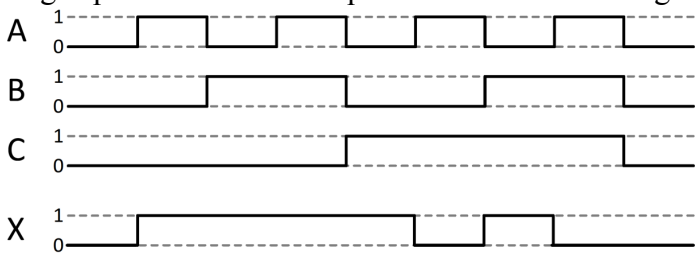
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(d)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(e) None of the above

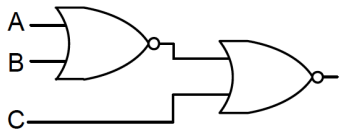
9. Which of the following expressions is NOT equivalent to the following timing diagram?

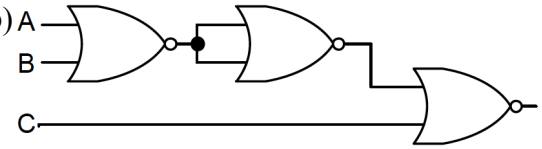


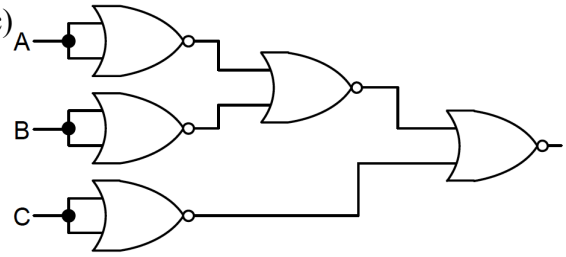
(a) $A.\bar{C} + B.\bar{C} + \bar{A}.B + \bar{A}.C$
(b) $(A \oplus C) + \bar{A}.B.\bar{C}$
(c) $A.\bar{B}.\bar{C} + B.\bar{C} + \bar{A}.C$
(d) $A.\bar{B}.\bar{C} + A.B.\bar{C} + \bar{A}.B + \bar{A}.\bar{B}.C$
(e) All of the above are equivalent to the timing diagram

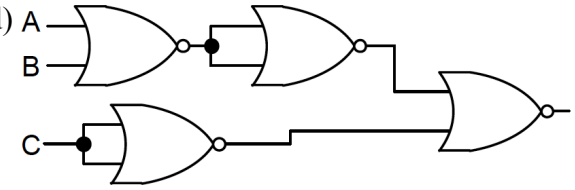
10. Which of the following logic functions is identical to $\overline{(A+\bar{C}).(\bar{A}+B.\bar{C})}$?
(a) $A.\bar{B} + C$
(b) $\bar{A}.B + C$
(c) $A.\bar{B} + A.C$
(d) $\bar{A}.C + B.\bar{C}$
(e) None of the above

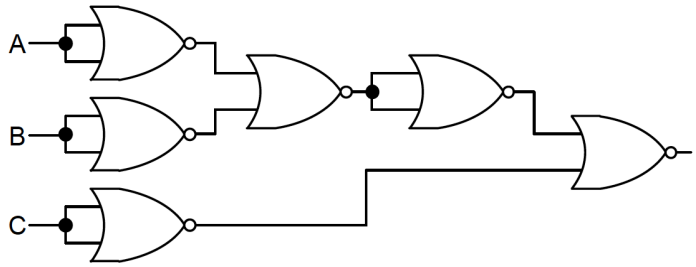
11. Which of the following circuits implements a 3 input NOR gate ($\overline{A + B + C}$) using only 2-input NOR gates?

(a)


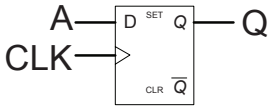
(b)


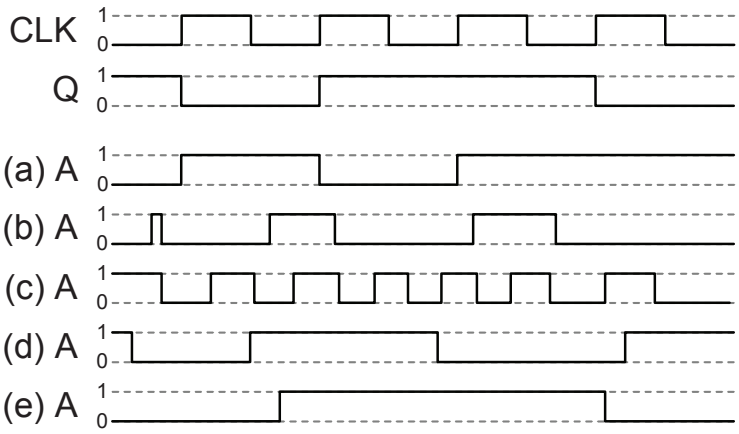
(c)


(d)


(e)


12. Consider the flip-flop circuit shown below and the associated CLK and output (Q) signals. Which timing diagram shows input (A) values over time which would have resulted in the given output (Q).



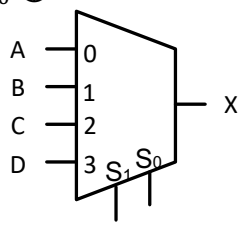


13. What is the result of adding the 6-bit two's complement numbers 101010 and 110011?
    (a) 011100
    (b) 011101
    (c) 011110
    (d) 111011
    (e) None of the above

14. Which of the following operations will result in an overflow in 5-bit two's complement arithmetic?
    (a) 01010 – 01110
    (b) 10111 – 11100
    (c) 11010 – 00111
    (d) 01011 + 11111
    (e) None of the above

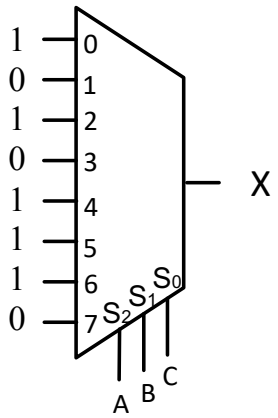
15. Consider the binary addition operation 010111 + 001001. Which of the following statements is true if the numbers are interpreted as two's complement?
    (a) The result is positive and no overflow occurs
    (b) The result should be positive but overflow occurs
    (c) The result is negative and no overflow occurs
    (d) The result should be negative but overflow occurs
    (e) The result is zero

16. Consider the following multiplexer. What must the inputs A,B,C,D be so that the multiplexer implements the function $X = S_1 \oplus S_0 \oplus \overline{G}$?



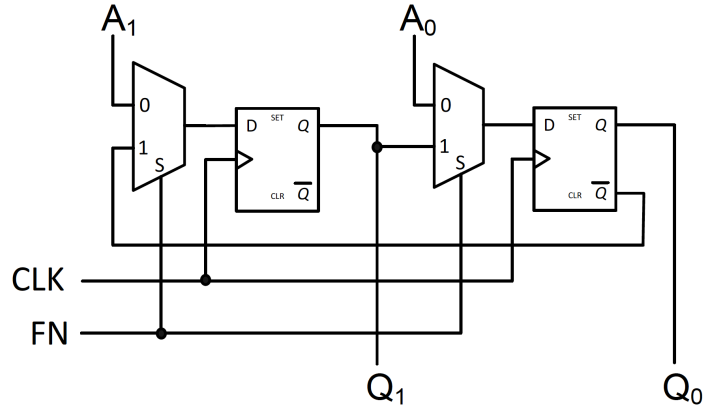
    (a) A= 0 B= 1 C= 1 D= 0
    (b) A= G B= $\overline{G}$ C= $\overline{G}$ D= G
    (c) A= $\overline{G}$ B= 1 C= 1 D= 1
    (d) A= $\overline{G}$ B= G C= G D= $\overline{G}$
    (e) None of the above

17. Consider the following multiplexer. Which of the following statements is TRUE? (+ indicates the logical OR operation)



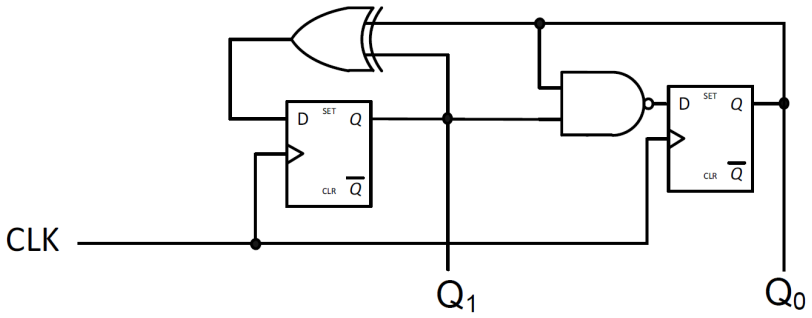
    (a) If A is 0, $X = \overline{C}$ If A is 1, $X = \overline{\overline{B + C}}$
    (b) If A is 0, $X = \overline{B}$ If A is 1, $X = \overline{\overline{B + C}}$
    (c) If A is 0, $X = \overline{C}$ If A is 1, $X = \overline{\overline{B.C}}$
    (d) If A is 0, $X = C$ If A is 1, $X = \overline{\overline{B.C}}$
    (e) None of the above

18. Consider the circuit below. If A_1 is 1 and A_0 is 0, what are the values of Q_1 and Q_0 after four rising clock edges if FN is 0 for one rising clock edge then 1 for three rising clock edges?



(a) $Q_1 = 0$ $Q_0 = 0$
(b) $Q_1 = 0$ $Q_0 = 1$
(c) $Q_1 = 1$ $Q_0 = 0$
(d) $Q_1 = 1$ $Q_0 = 1$
(e) Insufficient information is provided to determine the values

19. What sequence will the following synchronous counter count through, if it starts at $Q_1Q_0 = 00$?

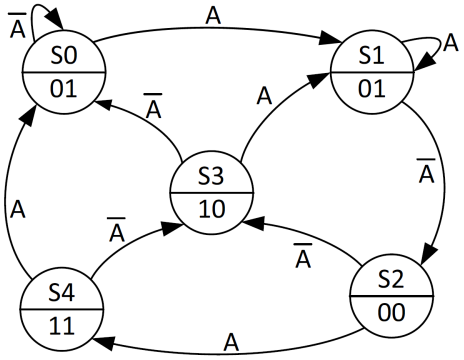


(a) Q_1Q_0: 00 → 10 → 01 → 11 → 00 → …
(b) Q_1Q_0: 00 → 10 → 11 → 00 → …
(c) Q_1Q_0: 00 → 01 → 10 → 11 → 00 → …
(d) Q_1Q_0: 00 → 01 → 11 → 00 → …
(e) None of the above

20. What is the minimum number of flip-flops needed to implement a state machine whose outputs always go through the sequence:
00001→00011→00111→11000→10000→00000→00001→… ?
(a) 3
(b) 4
(c) 5
(d) 6
(e) None of the above

21. Consider the state diagram below.

Inputs: A
Outputs: X,Y



Which of the following is an equivalent state table?

(a)

Current State	Input (A)	Next State	Outputs (X,Y)
S0	0	S0	01
S0	1	S1	01
S1	0	S2	01
S1	1	S1	01
S2	0	S3	00
S2	1	S4	00
S3	0	S0	10
S3	1	S1	10
S4	0	S0	11
S4	1	S3	11

(b)

Current State	Input (A)	Next State	Outputs (X,Y)
S0	0	S0	01
S0	1	S1	01
S1	0	S2	01
S1	1	S2	01
S2	0	S3	00
S2	1	S4	00
S3	0	S0	10
S3	1	S1	10
S4	0	S3	11
S4	1	S0	11

(c)

Current State	Next State		Outputs (X,Y)
	A=0	A=1	
S0	S0	S1	01
S1	S2	S1	01
S2	S3	S4	00
S3	S0	S1	10
S4	S3	S0	11

(d)

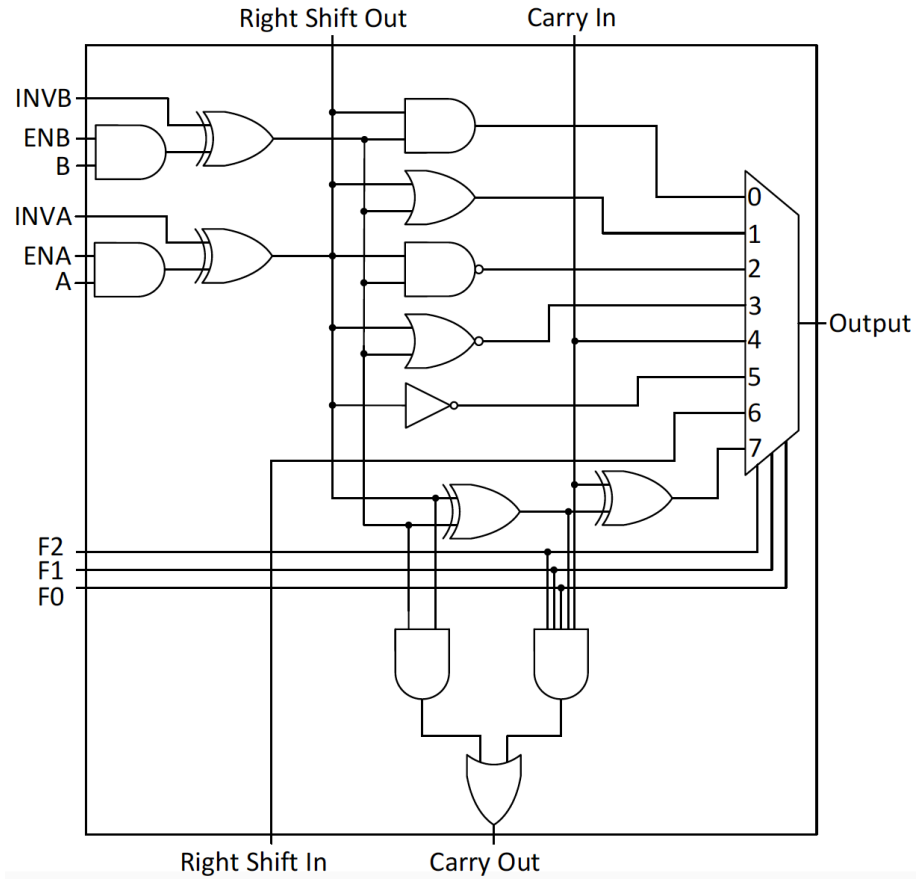
Current State	Next State		Outputs (X,Y)
	A=0	A=1	
S0	S0	S1	01
S1	S2	S1	10
S2	S3	S4	00
S3	S0	S1	10
S4	S3	S0	11

(e) None of the above

22. What is the minimum number of flip-flops needed to build the state machine shown in question 21?
    (a) 1
    (b) 2
    (c) 3
    (d) 4
    (e) 5

23. Consider the state machine represented by the state diagram in question 21 above. What sequence of states is traversed if the machine starts in state S3 and A goes through the sequence 10001 (i.e. 1 followed by three 0s followed by a 1)?
    (a) S3→S0→S0→S0→S0→S1
    (b) S3→S1→S2→S3→S0→S1
    (c) S3→S1→S2→S4→S3→S1
    (d) S3→S0→S1→S2→S3→S1
    (e) None of the above

24. Consider the ALU bit slice below.



For an ALU made up of 8 of the bit slices above, which of the following control input settings will NOT result in the ALU output being $\overline{B}$? (The "Right Shift In" control input refers to that for the most significant bit; the "Carry in" control input refers to that for the least significant bit.)

(a) ENA=0 INVA=0 ENB=1 INVB=0 F_2=0 F_1=1 F_0=1 Right Shift In=0 Carry in=0
(b) ENA=0 INVA=0 ENB=1 INVB=1 F_2=0 F_1=0 F_0=1 Right Shift In=0 Carry in=0
(c) ENA=0 INVA=1 ENB=1 INVB=0 F_2=0 F_1=1 F_0=0 Right Shift In=0 Carry in=0
(d) ENA=0 INVA=1 ENB=1 INVB=1 F_2=0 F_1=0 F_0=0 Right Shift In=0 Carry in=0
(e) All of the above result in the ALU output being $\overline{B}$

25. For the ALU in question 24, which of the following control input settings will result in the ALU output being $A.B$?

(a) ENA=1 INVA=0 ENB=1 INVB=0 F_2=0 F_1=0 F_0=1 Right Shift In=0 Carry in=0
(b) ENA=1 INVA=0 ENB=1 INVB=0 F_2=0 F_1=1 F_0=0 Right Shift In=0 Carry in=0
(c) ENA=1 INVA=0 ENB=1 INVB=0 F_2=0 F_1=1 F_0=1 Right Shift In=0 Carry in=0
(d) ENA=1 INVA=1 ENB=1 INVB=1 F_2=0 F_1=1 F_0=1 Right Shift In=0 Carry in=0
(e) None of the above