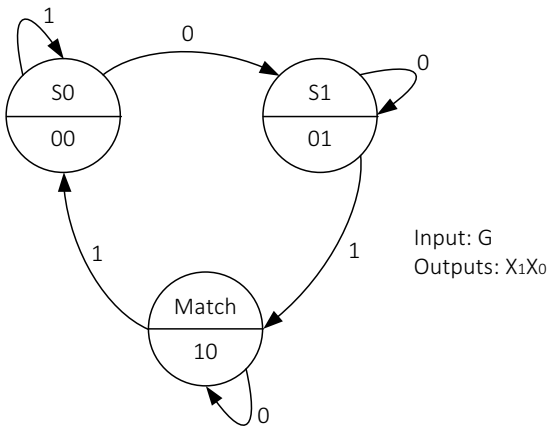
CSSE2010 / CSSE7201 – Introduction to Computer Systems
Exercises – Week Four
Counters and State Machines

Exercises

Some of the questions below are taken from or based on questions in Tanenbaum, Structured Computer Organisation, 5th edition.

1. Draw the logic diagram for a 3-bit synchronous counter which counts backwards (111→110→101→100→011→010→001→000→111→…). Hint: Start by writing down a truth table of current value and next value as done in the lecture for the 2-bit synchronous counter.
2. Draw the logic diagram for a 3-bit synchronous counter which counts in the sequence 000→001→010→100→110→000→… (i.e. 0,1,2,4,6).
3. For the state diagram below, construct both a one-dimensional and two-dimensional state table.



4. Design a state machine which implements a counter which counts through the output sequence 0000→0001→0011→0111→1111→1110→1100→1000→0000… There are two inputs: RUN and RESET. If RUN is 1 and RESET is 0, the counter counts through the sequence given. If RESET is 1, independent of the value of RUN, the counter returns to output 0000. If both RUN and RESET are 0, the counter output remains the same. Show
   - A state diagram
   - A state table (two dimensional)
   - Your chosen state encoding
   - A sequential circuit which implements this behaviour