

VLSI - Assignment 1

Sreeja Guduri (2021102007)

In the 4th question of the assignment, we are asked to find the propagation delay of a NAND gate, under different parameter changes.

We use ngspice to simulate the NAND gate and use the 22nm technology mode for the MOSFETS.

Question a

1. The width of the 4 different MOSFETS are changed from 22nm to 220nm in steps of 22nm. The propagation delay is then calculated by measuring rise and fall times at half the input and output waveforms.
2. The analysis is done for all the MOSFETS and we notice that as the width of the pmos increases, the value of 'tfalla' increases and that of 'triseb' decreases.
3. The opposite is the case for an nmos transistor. The value of 'tfalla' decreases and that of 'triseb' increases.

Question b

1. Temperature plays a huge role on the propagation delay of the NAND gate. To simulate this, I used a python code 'rand.py' to generate a list of random temperatures between 0 and 80, and store them in a text file called 'temp.txt'
2. Then, using a python file called 'script.py' I change the values of temperatures in my ngspice netlist and run the code.

NOTE:

- To get the output for the next temperature, just input 'quit' into the ngspice interface
- My code finds the output for 10 distinct, random temperature values but it can be changed to compute more temperature values.

3. We notice that as temperature increases, the propagation delay of the NAND gate decreases.

Question c

1. The subcircuit 'nand.sub' is the same NAND gate implementation we used in the other questions, except now we can use it as it's own element in ngspice.
2. The C17 benchmark circuit has 5 inputs and 2 outputs.