Capacitance Model → V imp!!!

learn all equations (!!!)

C_{sb}, C_{db} eqns → in slides.

Design

* Project 1 : Developing a model

- Should be valid for 45nm, 32nm, 22nm, 16nm . (all)

CMOS → 45nm → 32nm → 22nm

FinFET → 16nm → 10nm → 7nm

→ LP → HP → MGK

→ 1V , 0.9V , 0.8V

} possible combinations

* Power/current leakage estimation model

VLSI Design

MOSFET-1 (Lecture 16)

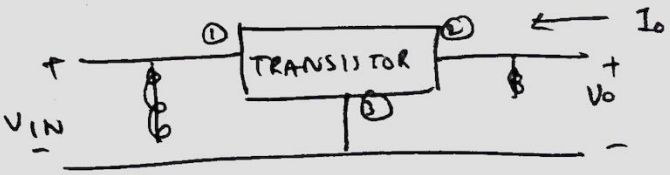
NOTE: No resistive load inverter; no small signal analysis.

p1 ✓ p2 (?) p3 ✓ p4 (½) p5 (½) ✗

* We want to understand how MOSFETs work at a very basic level; look at some models of MOSFETs.

* A transistor must have at least 3 terminals, and:

Current I_o is much more sensitive to V_{IN} than V_o.



i.e., $\frac{\partial I_o}{\partial V_{in}} \gg \frac{\partial I_o}{\partial V_o}$

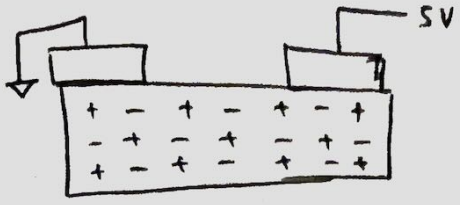
$\frac{\partial I_o}{\partial V_{in}}$ → transconductance

$\frac{\partial I_o}{\partial V_o}$ → output conductance.

NOTE: MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor. What is Field Effect?

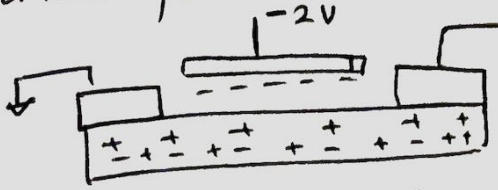
Field Effect Principle: Modulation of conductivity using $\vec{E}$.

w/o plate:



→ Current, I, is dependent on linear r/s w/ V & R; R is determined by factors $\frac{\rho L}{A}$.

Adding a metal plate:



All the -ve charges are attracted towards plate; capacitor-like structure is formed. As the -ve charges are no longer part of the semiconductor, it's conductivity has been changed.

* Also, if we conversely add +ve charge, then we ~~decrease~~ increase the conductivity; by increasing the no. of e^- in the system (as the +ve charge would be concentrated towards the plate.

∴ We see that we have achieved transconductance in this structure [i.e, ~~volta~~ current flowing b/w two terminals is affected by voltage applied across another pair of terminals]

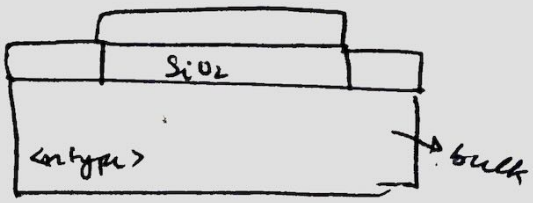
* In short, FEP states that by applying an electrostatic field, the ~~trans~~ ~~conductance~~ conductivity can be modulated.

* FEP: The flow of electric current ~~conta~~ b/w two terminals of an electrode can be controlled by establishing a third potential b/w the two terminals.

Structure of MOSFET :-

* How to place the plate close to the channel? — Can be done by adding an thin layer oxide (SiO_2) b/w plate & channel.

NOTE:

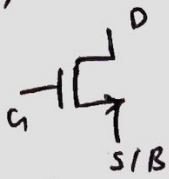


MOSFET as switch:

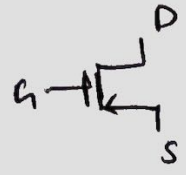
If high -ve voltage is applied to gate, then the channel that exists b/w drain & source is depleted of e^-; and so no current flows b/w drain & source, so MOSFET is off.

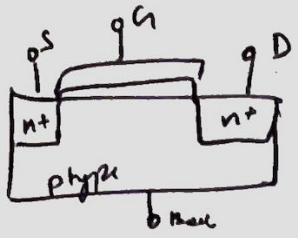
Similarly, if gate voltage is 0, then channel exists b/w drain & source, so MOSFET is on.

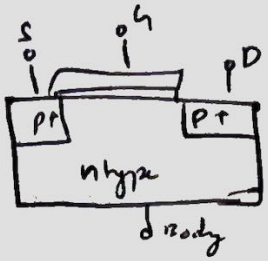
NMOS:



PMOS:







Inversion charge per area:

$$Q_{inv} = -C_{ox}(V_{GS} - V_{THN}) \quad [\text{for n MOS}]$$

When $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

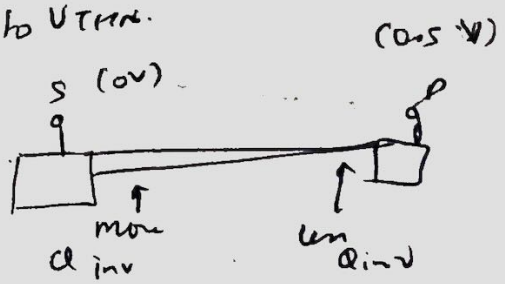
This eqn starts to break down as V_{GS} gets close to V_{THN}.

This is with $V_{BS} = 0$ & $V_S = 0$.

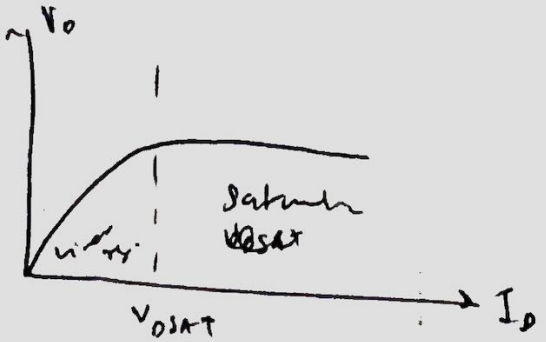
* If we apply a drain charge,

$$Q_{inv} = -C_{ox}(V_{GS} - V_{TH} - V(x))$$

where $V(x)$ = channel voltage.



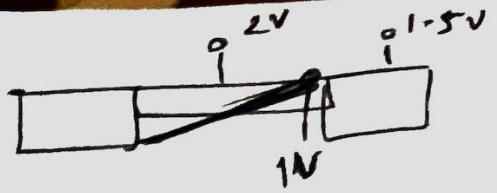
V_D vs. I_D:



In linear region,
MOSFET acts like resistor
(resistance increases w/ current)

In Sat. region, → Amplification
MOSFET acts as current source (current stays constant w/ varying voltage)

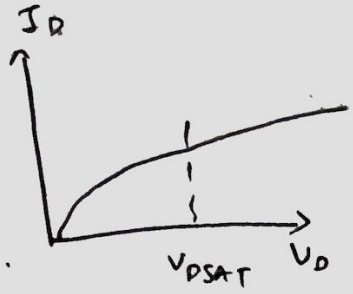
If $V_D > V_{DSAT}$, the pinchoff point moves left, towards source.



Channel Length Modulation:

- Originally, channel was of length L; now due to pinchoff point shift, new channel length is:

$$L' = L - \Delta L \qquad (\Delta L = \text{length of pinchoff region})$$



As a result, current increases a little bit, even in saturation region.

Threshold voltage:

$$V_{THN} = V_{THNO} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

(constant)

(γ, ϕ_F are body parameter & surface potential)

$\therefore$ V_{THN} can be modified by changing V_{SB} i.e. source to body voltage.

$\therefore$ If we short source & body, then $V_{SB} = 0$, so $V_{THN} = V_{THNO}$ (constant).

Regions of Operation of MOSFET

① Cutoff

$V_{GS} < V_{THN}$

② Linear

$V_{GS} > V_{THN}$

$V_{DS} < V_{DSAT}$

③ Saturation

$V_{GS} > V_{THN}$

$V_{DS} > V_{DSAT}$

Current Equations

Saturation: If $V_{GS} > V_{THN}$ & $V_{DS} > V_{DSAT}$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Linear: If $V_{GS} > V_{THN}$ and $V_{DS} < V_{DSAT}$

$I_D =$

Cutoff: If $V_{GS} < V_{THN}$

NOTE: Output characteristics

I_D vs. V_{DS}

Transfer characteristics: I_D vs. V_{GS}

Triode / Linear region

* Condition: $V_{GS} > V_{THN}$; $V_{DS} < V_{DSAT}$

$$I_D = \mu_N C_{ox} \frac{W}{L} \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$\mu_n C_{ox} = k_{PN}$

Saturation region:

* Condition: $V_{GS} > V_{THN}$; $V_{DS} > V_{GS} - V_{THN}$

$$I_D = \frac{1}{2} \mu_N C_{ox} \frac{W}{L} (V_{GS} - V_{THN})^2$$

Note: Source & Drain are interchangeable. $V_S < V_D$.

* Diode functionality: Short gate & drain.

Temperature Dependence

Saturation Current: $I_D = \frac{K_{PN}}{2} \propto \frac{W}{L} \times (V_{GS} - V_{THN})^2$

K_{PN} & V_{THN} → affected by temperature.

Both decrease w/ temp; but as we see from the eq^n, one decreases current & one increases current.

So, now V_{GS} comes into play. If V_{GS} is close to value of V_{THN}, then V_{THN} doesn't affect ~~temp~~ current much, but if $V_{GS} \gg V_{THN}$, then ~~temp~~ current is affected.

Temp ↑

↳ ∗KPN & V_{THN} ↓

↳ I_{inc} ↑ ↳ I_{dec} ↓

↳ If V_{GS} close to V_{THN},

↳ or I ↑

overall redd

(refer to eqn).

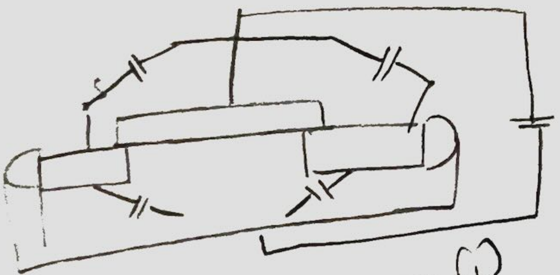
Subthreshold region:

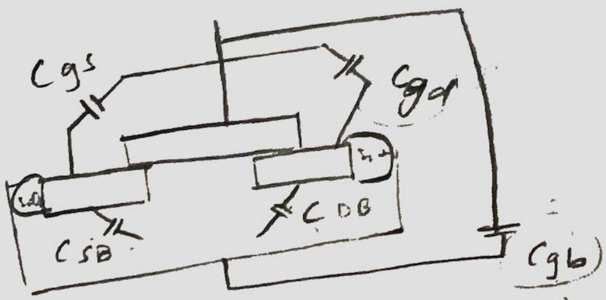
MOSFET acts like a BJT:

BJT : $I_C = I_S \, e^{V_{BE}/V_T}$

MOS : $I_{DS} = I_S \, e^{V_{GS}/nV_T}$

Capacitance Model





① $C_{gd} = C_{GDO} W$.

② $C_{gs} = C_{gso} W + \frac{2}{3} \mu_N C_{ox} W L$

③ $C_{gb} = C_{gbo} L$

④
$$C_{db} = \frac{C_j A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}} + \frac{C_{jsw} P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}}$$

⑤
$$C_{sb} = \frac{C_j A_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{jsw} P_S}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}$$

① Capacitance
② V_{THN}
③ 3 regions
④ CLM formula