Mid-Sem: Digital VLSI Design (S23.ECE463)

Max. Time: 90 Mins [11:30 AM to 01:00 PM] Max. Marks: 40 Date: 01/03/2023

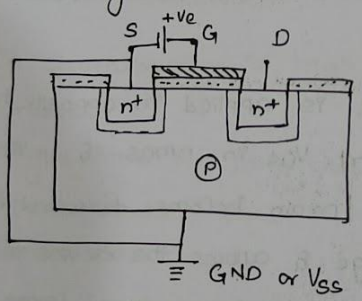
NOTE: No query allowed during exam. Write your assumptions (if any) for each question.

Q.1. What is a body voltage? What body voltage would you apply for a (1) n-MOS and (2) p-MOS? Why? What happens if this body voltage is reversed? **[1+1+1+1+2=6 Marks]**

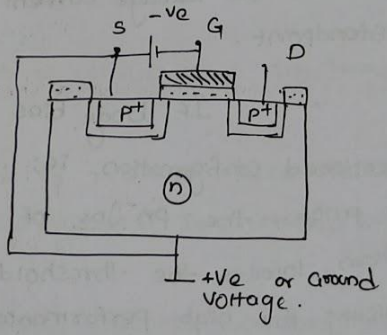
Solution:

Q1) Body bias voltage V_{SB} is applied between Source and body of the MOSFET. Because of the voltage difference between the source voltage (V_s) and body voltage (V_b) affects threshold voltage V_t, the body can be thought of as a second gate that helps to determine how a transistor turns on and off.

Under normal operation, an unbiased device has a matching V_s and V_b. Altering the voltage of the device's bulk connection places the device into either a forward or reverse body bias condition, changing the effective V_t required to turn the device on. While V_s remains at nominal voltage, V_b will be either higher or lower than V_s.



nMOS
when $V_{GS} < V_t$



pMOS
when $|V_{GS}| < |V_t|$

for ideal operation of MOSFET, when $V_{GS} \geq V_t$, channel should be formed & with V_{DS} voltage (+ve for nMOS, -ve for PMOS) it starts conducting.

⇒ for nMOS, channel constitutes of e^-s & for pmos channel is formed with holes.

⇒ The depletion region around Source/Drain is formed within MOSFET, which inturn forms Pn junctions.

⇒ The pn junctions or Source/Drain regions need to be connected in reverse bias configuration to avoid leakage current that flows across body ie; from source/drain to body.

⇒ Generally, Source & bias/body are shorted & connected to ground. In nMOS ⇒ $V_{GS} > V_{SB}$ with +ve voltage at V_{GS}.

⇒ Source & body are shorted & connected to +ve voltage (or ground) in pmos device ⇒ $|V_{GS}| < |V_{SB}|$ with -ve voltage at V_{GS} to maintain reverse bias configuration in the body.

V_{SB} can be made more -ve by increasing -ve voltage at the body terminal shorted to source in nmos or can be made more +ve in pmos which in turn affects the threshold voltage as below.

⇒ It raises the required V_t for the device to turn on. This increased V_t increases the time taken for the device to turn on. V_t increases due to the increase in the depletion region around Source/Drain because of more -ve voltage applied at body bias. But, it also lowers the leakage current which is useful from a power efficiency standpoint.

If body bias voltage is applied in opposite to above mentioned configuration ie; +ve w.r.t V_{GS} in nmos & -ve w.r.t $|V_{GS}|$ in pmos, the pn jns of Source/Drain become forward biased which in turn lowers the threshold voltage & allows the device to turn on quickly for high performance, but the device has large leakage currents flowing across the device.

Q.2. Due to scaling, the channel length of a MOSFET has decreased by 2, but the supply voltage is almost the same. **[6 Marks]**

a. What is the electric field in the channel before and after scaling?
b. What are the potential issues due to scaling?
c. What are the possible measures to reduce/eliminate the issue?

Solution:

④ Given, channel length for MOS has decreased by 2. No change in supply voltage.

(a) Charge induced in the channel due to gate voltage is due to the voltage difference between gate and the channel, V_{gs}.

→ The voltage along the channel varies linearly with distance x from the source due to IR drop in the channel & assuming that the device is not saturated then the average value is $V_{ds}/2$.

The effective gate voltage $V_g = V_{gs} - V_t$, threshold voltage needed to invert the charge under the gate & establish channel.

$$E_g = \frac{\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)}{D} \rightarrow (1)$$

average Electric field in the channel

D = oxide thickness.

Charge/unit area $= E_g \varepsilon_{ins} \varepsilon_0$. → (2)

$\therefore E_g \propto \frac{1}{L}$

→ Q_c = charge in the channel $= E_g \varepsilon_{ins} \varepsilon_0 W L$ → (3)

$C = \frac{\varepsilon A}{D}$

$\frac{Q}{V} = \frac{\varepsilon_0 \varepsilon_{ins} WL}{D}$

$Q = \varepsilon_0 \varepsilon_{ins} WL E_g \quad \therefore E_g = \frac{V}{D}$

$\Rightarrow E_g = \frac{Q_c}{\varepsilon_0 \varepsilon_{ins} WL}$; $E_g \propto \frac{1}{L}$

If $L' = L/2 \quad \therefore E_g \propto \frac{2}{L}$ ⇒ Electric field in the channel increased. It became twice.

Electric field in the channel doubled with scale down.

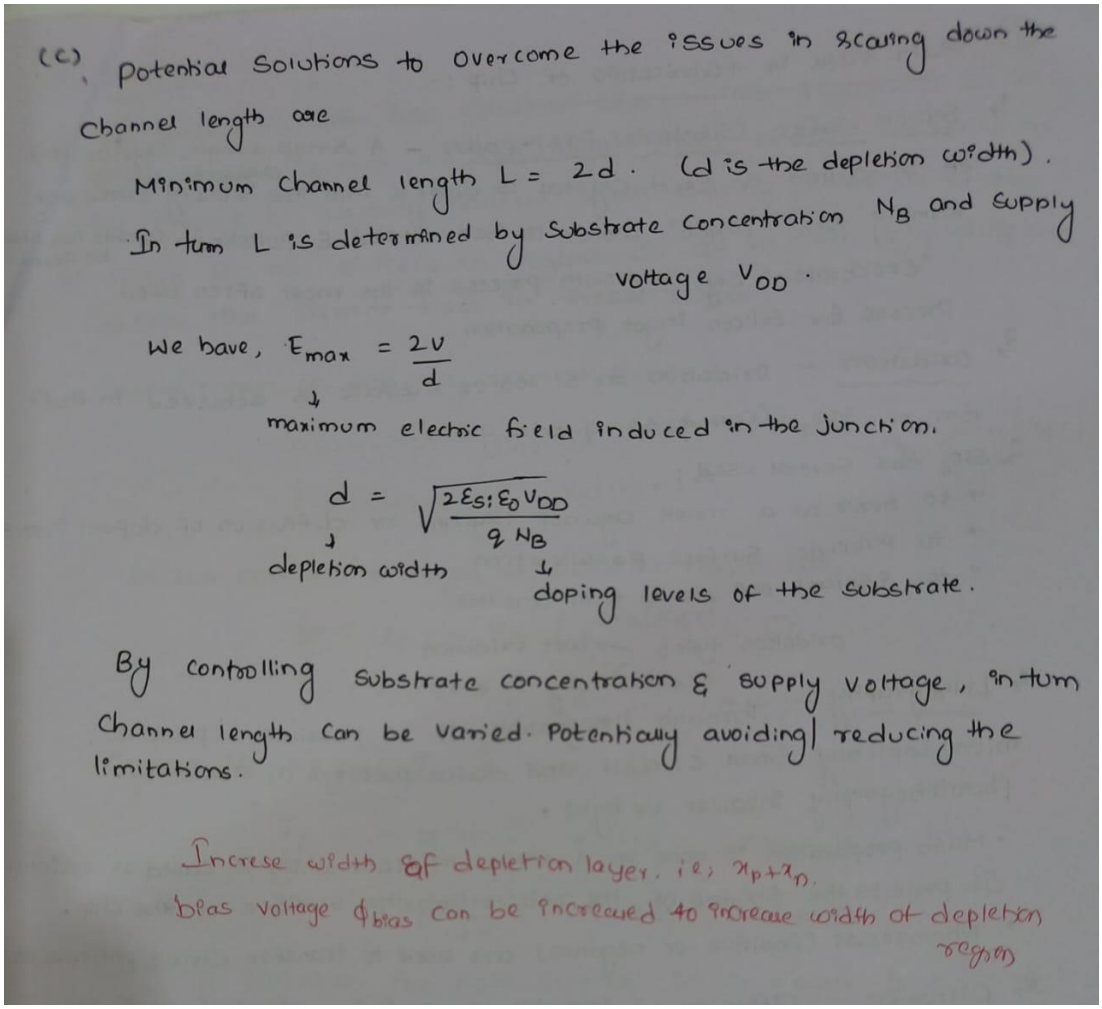
(b) As the channel length is scaled down,

i) the edge of the depletion region around the source comes closer to that around the drain.

Which inturn causes reduction in threshold voltage ; second order effects

Leakage increases. Cause velocity saturation, mobility degradation etc.

- Source to drain tunneling where Gate has less control on the channel & causes inturn subthreshold leakage current.
- Punchthrough.



Q.3. An nMOS transistor has a threshold voltage of 0.4 V and a supply voltage of V_{DD} = 1.2 V. A circuit designer is evaluating a proposal to reduce V_T by 100 mV to obtain faster transistors. **[6 Marks]**

a. By what factor would the saturation current increase (at Vgs = Vds = V_{DD}) if the transistor were ideal?
b. By what factor would the subthreshold leakage current increase at room temperature at Vgs = 0? Assume n = 1.4.
c. By what factor would the subthreshold leakage current increase at 120 °C? Assume the threshold voltage is independent of temperature.

Solution:

Q3

a)

Saturation Current I_D

$$I_D = \frac{1}{2} \mu_n C_{ox} (W/L) (V_{GS} - V_{TH})^2$$

$$I_D' = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH} - 100m)^2$$

$$\frac{I_D}{I_D'} = \frac{(V_{DD} - V_{TH})^2}{(V_{DD} - V_{TH} + 100m)^2}$$

$$= \left(\frac{V_{DD} - V_{TH}}{V_{DD} - V_{TH} + 100m}\right)^2$$

$$= \left(\frac{0.8}{0.9}\right)^2$$

$$\boxed{I_D' = \left(\frac{9}{8}\right)^2 I_D} \approx 1.2 \times I_D$$

b) Subthreshold current is given by

$$i_D = \mu_n C_{ox} \left(\frac{W}{L}\right)\left(\frac{kT}{q}\right)^2 (\eta - 1) \exp\left(\frac{V_{GS} - V_T}{\eta V_T}\right)$$

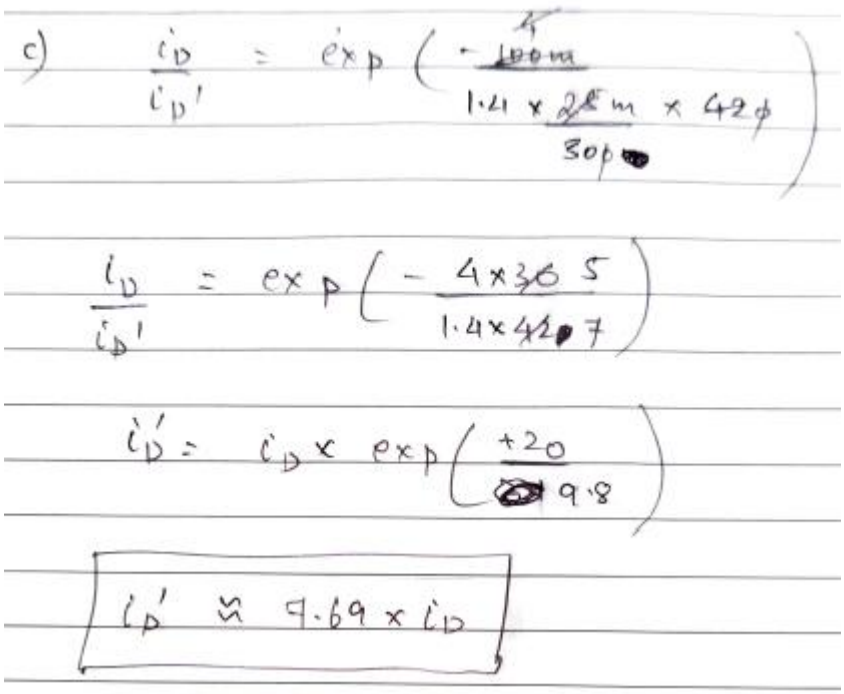
$$\frac{i_D}{i_D'} = \exp\left(\frac{-V_T}{\eta V_t} + \frac{V_T'}{\eta V_t}\right)$$

$$= \exp\left(\frac{-100\,mV}{\eta V_T}\right) ; \; V_T \approx 25\,mV \; @ \; T = 300\,K$$

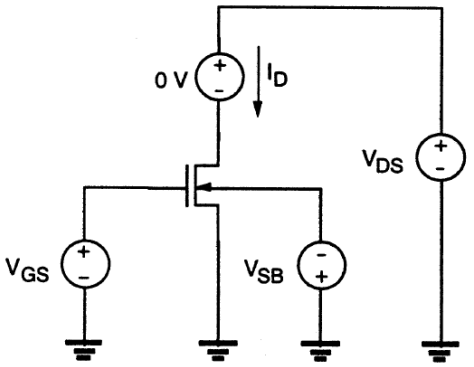
$$\frac{i_D}{i_D'} = \exp\left(\frac{-4}{1.4}\right)$$

$$i_D' = \exp\left(\frac{4}{1.4}\right) i_D$$

$$\approx 17.4 \times i_D$$



Q.4. A set of I-V characteristics of an nMOS transistor at room temperature are shown in below (in Table) for different biasing conditions. Fig. shows measurement setup. Using the data, find the threshold voltage V_{T0} **[4 Marks]**



V_{GS}	V_{DS}	V_{SB}	I_D (μA)
4V	4V	0.0V	256
5V	5V	0.0V	441
4V	4V	2.6V	144
5V	5V	2.6V	256

Solution:

(a) Find V_{T0}

For both case 1 (Row1) and case 2(Row2), the transistor operates in saturation region, using equation (3.62)

$$I_D(sat) = \frac{k_n}{2}(V_{GS} - V_{T0})^2$$

$$\frac{I_D(Row1)}{I_D(Row2)} = \frac{(4 - V_{T0})^2}{(5 - V_{T0})^2} = \frac{256}{441}$$

$$\frac{4 - V_{T0}}{5 - V_{T0}} = \pm\frac{16}{21}$$

The correct solution is:

$$V_{T0} = 0.8[V]$$

Q.5. Consider a resistive-load inverter with V_{DD}=5V, transconductance (k_n') = 20 µA/V^2, V_{T0}= 0.8 V, R_L= 200 KΩ, and W/L=2. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) and on the VTC and find the noise margin of the circuit.
Are your calculated noise margins good? Please comment on the quality of the inverter design, and how can you improve it? **[8 Marks]**

Solution:

When the input voltage is low, i.e., when the driver nMOS transistor is cut-off, the output high voltage can be found as

$$V_{OH} = V_{DD} = 5 \text{ V}$$

Note that in this resistive-load inverter example, the transconductance of the driver transistor is $k_n = k_n'(W/L) = 40 \text{ µA/V}^2$ and, hence, $(k_n R_L) = 8 \text{ V}^{-1}$.

The output low voltage V_{OL} is calculated by using (5.18):

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$= 5 - 0.8 + \frac{1}{8} - \sqrt{\left(5 - 0.8 + \frac{1}{8}\right)^2 - \frac{2 \cdot 5}{8}}$$

$$= 0.147 \text{ V}$$

The critical voltage V_{IL} is found using (5.22), as follows.

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L} = 0.8 + \frac{1}{8} = 0.925 \text{ V}$$

Finally, the critical voltage V_{IH} can be calculated by using (5.30).

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} = 0.8 + \sqrt{\frac{8}{3} \cdot \frac{5}{8}} - \frac{1}{8} = 1.97 \text{ V}$$

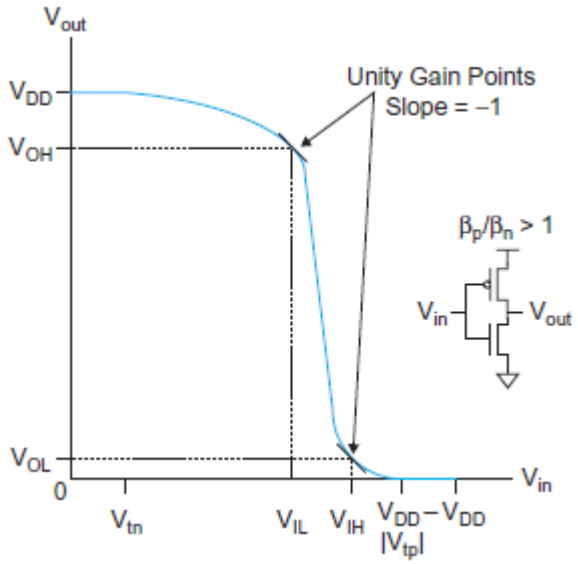
Now, the noise margins can be found, according to (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 0.93 - 0.15 = 0.78 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.97 = 3.03 \text{ V}$$

At this point, we can comment on the quality of this particular inverter design for DC operation. Notice that the noise margin NM_L found here is quite low, and it may eventually lead to misinterpretation of input signal levels. For better noise immunity, the noise margin for "low" signals should be at least about 25% of the power supply voltage V_{DD}, i.e., about 1.25 V.

If either NM_L or NM_H for a gate are too small, the gate may be disturbed by noise that occurs on the inputs. An unskewed gate has equal noise margins, which maximizes immunity to arbitrary noise sources. If a gate sees more noise in the high or low input state, the gate can be skewed to improve that noise margin at the expense of the other. Note that if $|V_{tp}| = V_{tn}$, then NM_H and NM_L increase as threshold voltages are increased.



CMOS Inverter Noise margins

Noise margins increase as K_nR_L increases for typical values being greater than 2. Alternatively, conventional static CMOS circuits have great noise margins (V_{OH} min is closer to the power supply voltage and V_{OL} max is closer to zero), which can be employed. They are minimally sensitive to variations in transistor parameters and will eventually recover even if a noise event occurs.

Q 6. Answer the following questions **[8 + 2=10 Marks]**

(a) The capacitances in MOSFET occurs due to _____IV_____

i. Interconnects
ii. Difference in Doping concentration
iii. Difference in dopant materials
iv. All of the mentioned

(b) The parasitic capacitances found in MOSFET are _____I_____

i. Oxide related capacitances
ii. Inter electrode capacitance
iii. Electrolytic capacitance
iv. All of the mentioned

(c) In Cut-off region (assume MOS is in accumulation), the capacitance Cgs will be equal to II

i. $2C_{GD0}$
ii. $C_{GS0}.W$
iii. C_{GB}
iv. All of the mentioned

(d) In cut-off region (assume MOS is in accumulation), the value of gate to substrate capacitance is equal to _____III_____

i. Cox.(W- L)

ii. $C_{GB0}.L + Cox\ W/\ L$
iii. $C_{GB0}.L + Cox^{*}\ W^{*}L$
iv. 0

(e) In linear mode operation, the parasitic capacitances that exists are _____IV_____

i. Nonzero Gate to source capacitance
ii. Nonzero Gate to drain capacitance
iii. Zero gate to substrate capacitance
iv. All of the mentioned

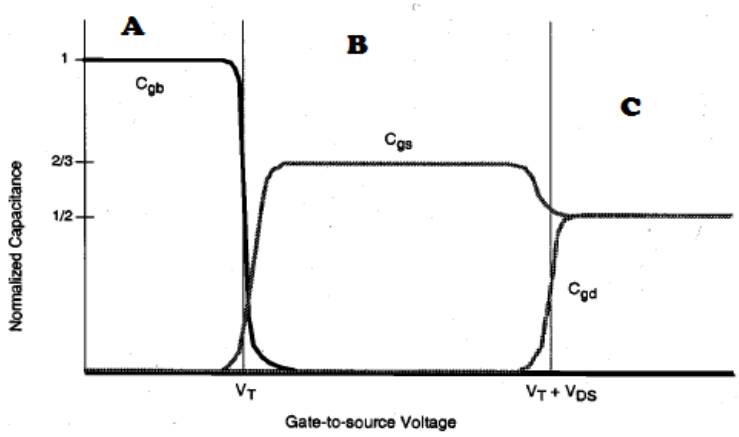
(f) In saturation mode operation, gate to drain capacitance (channel) is zero due to__II____

i. Gate and drain are interconnected
ii. Channel length is reduced
iii. Inversion layer doesn't exist
iv. Drain is connected to ground

(g) When MOSFET is operating in saturation region, the gate to source capacitance (channel) is? II

i. 1/2*Cox*W*L
ii. 2/3*Cox*W*L
iii. Cox*W*L
iv. 1/3*Cox*W*L

(h) In the below graph, the regions marked as A, B, C are? II



i. A : Saturation, B : Linear, C : Cut-off
ii. A : Cut-off, B : Linear, C : Saturation
iii. A : Linear, B : Saturation, C : Cut-off
iv. None of the mentioned

Hint: Analyse the graph from the gate to source voltage on x axis and regions can be determined.

(i) What will be the behaviour in different situations below (increase, decrease, or not change)?

1. If the width of a transistor increases, the current will ……Increase……
2. If the length of a transistor increases, the current will ……Decrease……

3. If the supply voltage of a chip increases, the maximum transistor current will..Increase.
4. If the width of a transistor increases, its gate capacitance will ……Increase……
5. If the length of a transistor increases, its gate capacitance will ……Increase……
6. If the supply voltage of a chip increases, the gate capacitance of each transistor will…Not change