ASADI: Accelerating Sparse Attention using Diagonal-based In-situ Computing

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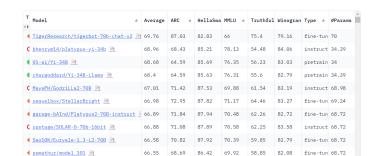
- 1 Background
- Motivations
- 3 DIA-based PUM
- Architecture and Dataflow
- **Evaluation**

Background •000000

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Transformer-based [1] large models achieve SOTA

performance on various NLP and CV tasks



67.41

83.13

Figure 1: From HuggingFace's Open LLM Leaderboard [2]



fine-tun 68.76

80.11

56.18

◆ OpenBuddy/openbuddy-llama2-70b-v10.1- 66.47

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Transformer and Attention Mechanism

 Attention mechanism with quadratic complexity to sequence length is the bottleneck of Transformer-based models

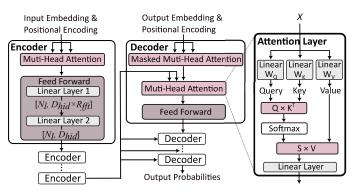


Figure 2: End-to-end Transformer



Basics of Sparse Attention

Background

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 Sparse attention is proposed to reduce computational complexity by pruning weak connected tokens, e.g., Longformer [3], DOTA [4], and Sanger [5]

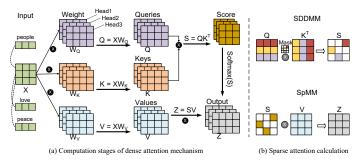


Figure 3: (a) Multi-head attention mechanism, and (b) Converting GEMM to SDDMM and SpMM



Evaluation

Basics of Sparse Attention

- Two types of sparse attention:
- Static sparse: Pre-determining the sparse mask matrix before receiving the input sequences, e.g., Longformer [3]
- Dynamic sparse: Employing a quantize-and-pruning phase to determine the sparse mask matrix, e.g., Sanger [5]

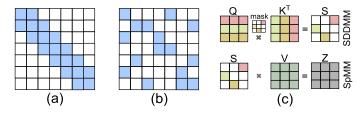


Figure 4: (a) Mask matrix of Longformer, (b) Mask matrix of Sanger, (c) Converting GEMM to SDDMM and SpMM

- The most popular compression formats are CSR, CSC, and COO, and we use CSR as an example
- This paper focuses on diagonal locality, so we also introduce DIA format

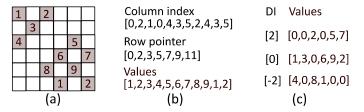


Figure 5: (a) An example of sparse mask matrix, (b) CSR format, and (c) DIA format

Basics of Memroy-centric Computing

- Sparse attention produces many irregular intermediate matrices, making it a memory-intensive kernel
- Memory-centric platforms are promising to accelerate memory-intensive kernels, such as PIM and PUM
- This paper focuses on PUM (processing-using-memory), i.e., in-situ computing

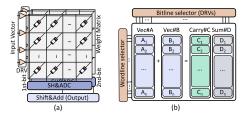


Figure 6: (a) Analog in-situ computing of ReRAM array, (b) Digital in-situ computing of ReRAM array

- Motivations

- **Observation#1:** Diagonal locality is prevalent in both static and dynamic sparse attention
- Observation#2: Current PIM-based sparse attention accelerators have high on-chip communication overhead

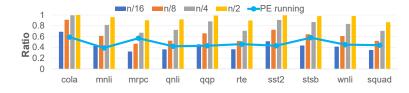


Figure 7: (a) The distribution of non-zeros in Sanger [5] with various ω (four bars), (b) The ratio of on-chip PE runtime to overall PIM chip runtime (broken lines)

Our Goals from the Observations

Background

- Opportunity from Observation#1: Current accelerators convert diagonal locality into row/column locality because the lack of DIA-based computation paradigm, e.g., Sanger [5] and SPRINT [6]
- Goal#1: Designing a new matrix multiplication computation paradigm to efficiently support the DIA format

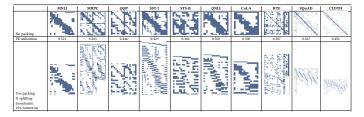


Figure 8: (a) The sparse plots obtained from Sanger [5]



Our Goals from the Observations

Background

- Opportunity from Observation#2: Utilizing row/column wise SpMM/SDDMM computation paradigm to PUM platforms will introduce many zeros, greatly decreasing PE utilization (Quantitative analysis in the paper)
- Goal#2: Designing DIA-based SpMM/SDDMM computation paradigm for PUM platforms to increase PE utilization

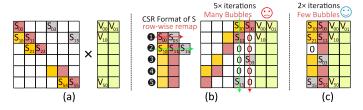


Figure 9: (a) SpMM between S and V, (b) In-situ computing with CSR format of S, (c) In-situ computing with DIA format of S

Our Goals from the Observations

- **Opportunity from Observation#2:** Utilizing row/column wise SpMM/SDDMM computation paradigm to PUM platforms will introduce many zeros, greatly decreasing PE utilization (Quantitative analysis in the paper)
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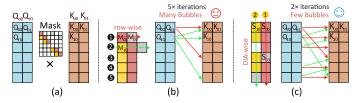


Figure 10: (a) SDDMM between Q and K^T , (b) In-situ computing with CSR format of M, (c) In-situ computing with DIA format of M

- 3 DIA-based PUM

Novel Compression Format

- Classic bubble-free DIA: Diagonal with all non-zeros, like Longformer [3], which has perfect diagonal locality
- Advantages of DIA: Each diagonal at least has $n \frac{\omega}{2}$ non-zeros while each row has up to ω non-zeros. Assuming $\omega = \frac{n}{8}$, one diagonal has 7.5× non-zeros than one row

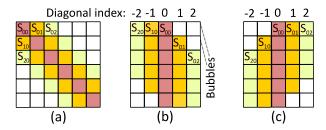


Figure 11: (a) Sparse S matrix ($\omega = 5$ and n = 6) without bubbles, (b) Bubble-free DIA compression, (c) Decompressed DIA format

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• Enhance diagonal locality: Move non-zeros in other region to the bubbles of ω region, maintaining column coordinates

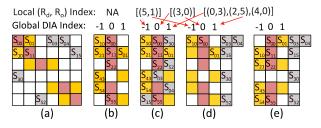


Figure 12: (a) Sparse *S* matrix with bubbles, (b) Bubble-free DIA compression, (c) Bubble-containing DIA compression, (d) Decompress non-central diagonals, (e) Decompress central diagonals

Novel Compression Format

Background

• How to select ω : We refer to the central ω diagonal region as ω region while referring the rest as other region. After calculation, we choose $\frac{n}{8}$ as the default configuration of ω

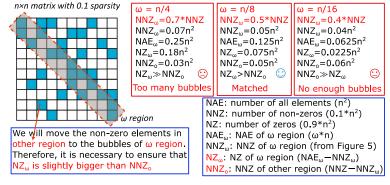


Figure 13: Details to calculate NZ_{ω} and NNZ_{o}



Before We Start

 See a simple example first: Assuming we only have one diagonal, then what should we do

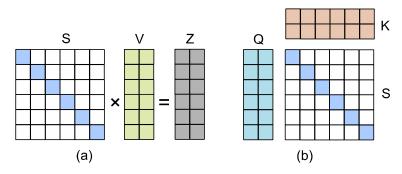


Figure 14: (a) SpMM between S and V, (b) SDDMM between Qand $K^{\mathcal{T}}$



 Details of computation paradigm: The following Figure presents a visualization version of our method, the pseudo-code and detailed description are in the paper

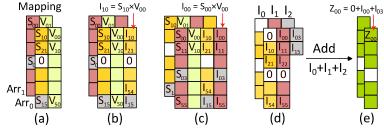


Figure 15: (a) Mapping matrices S and V to two ReRAM arrays,

- (b) Intermediate results of the first iteration of vector-vector multiplication, (c) Intermediate results of the second iteration of vector-vector multiplication, (d) Decompressed intermediate results,
- (e) Output Z matrix



In-situ $Q \times K^{\mathcal{T}}$

Background

 Details of computation paradigm: The following Figure presents a visualization version of our method, the pseudo-code and detailed description are in the paper

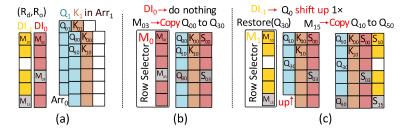


Figure 16: (a) Matrices Q and K in two ReRAM arrays, (b) Vector-vector multiplication of DI_0 , (c) Vector-vector multiplication of DI_{-1}



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Evaluation

 Details of computation paradigm: The following Figure presents a visualization version of our method, the pseudo-code and detailed description are in the paper

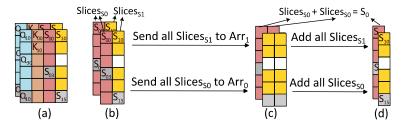


Figure 17: (a) Two slices of $Q_0 \times K_0$ and $Q_1 \times K_1$, (b) We refer the slices of DI₀ as $Slices_{S0}$ and DI₋₁ to $Slices_{S1}$, (c) All $Slices_{S0}$ and $Slices_{S1}$ are transferred to the same ReRAM array, (d) Results of DIA-based S matrix

<u>In-sit</u>u Linear Layer

Details of computation paradigm: The following Figure presents a visualization version of our method. $Q = I \times W_O$

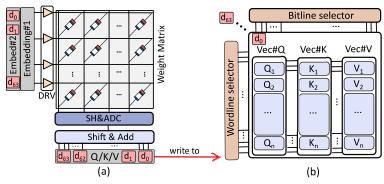


Figure 18: (a) Linear layer computation, (b) The data mapping of matrices Q, K, and V



In-situ Softmax

Background

 Details of computation paradigm: The following Figure presents a visualization version of 2^x . Since $e^x = 2^{x \log_2 e}$. we can perform in-situ vector-vector multiplication $y = x \log_2 e$ to get vector y, followed by 2^y to obtain e^x .

$$softmax(s_i) = \frac{e^{s_i - s_{max}}}{\sum_{c=1}^n e^{s_c - s_{max}}}$$

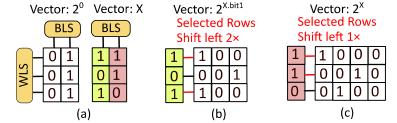


Figure 19: (a) Vector 2^0 and vector x, (b) Shift operation of bit1, (c) Shift operation of bit0

- Architecture and Dataflow

Overall Architecture

 Details of architecture: ASADI contains multiple En-PEs and De-PEs; Each En/De-PE contains two analog modules and one digital module.

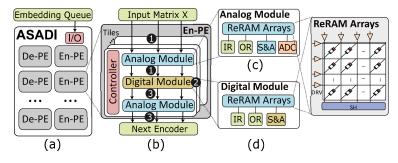
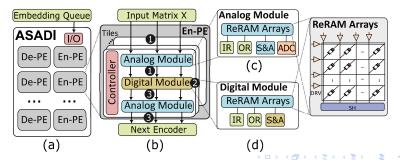


Figure 20: (a) Overall ASADI architecture, (b) Details of one En-PE, (c) Details of the analog module, (d) Details of the digital module

Dataflow

- Inter-PE dataflow: One En/De-PE for one Encoder/Decoder layer; we use pipeline to achieve parallelism between PEs
- Intra-PE dataflow: The generation of matrices Q, K, and V (**1**). The digital module performs the in-situ $Q \times K^T$. $S \times V$. and softmax operations ($\mathbf{\Theta}$). The matrix Z is sequentially read and sent to the second analog module (3).



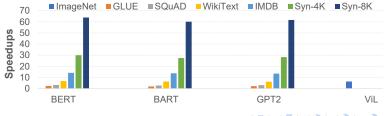
- Evaluation



- Models: BERT, BART, GPT-2, and Vil.
- Datasets: GLUE, SQuAD v1.1, WikeText-2, IMDB, ImageNet-1K, Syn-4K, and Syn-8K
- Baseline: The PIM baseline employs Samsung's novel function-in-memory DRAM (FIMDRAM). We use Ramulator-PIM to obtain latency and energy consumption.
- Other platforms: NVIDIA RTX A6000, SPRINT, and CPSAA
- Configuration of ASADI: Table 1 of the paper
- Pre-processing: Our code is modified from the GitHub project of Sanger [5]. All models and datasets are obtained from Hugging Face's models library [2] and datasets library.



- ASADI vs. PIM baseline
- Results: ViL: $6.4 \times$ speedup; BERT: $2.3 \times$ to $63.7 \times$ on GLUE, SQuAD, WikeText, IMDB, Syn-4K, and Syn-8k datasets. BART: $1.9 \times$ to $60.1 \times$ speedups; GPT2: $2.1 \times$ to $61.7 \times$.
- Reasons: Reducing on-chip random access; The PIM baseline uses near-memory computation, where the on-chip logic units need to random access many cross-bank data.



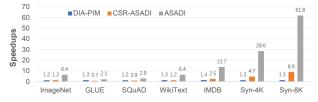
Overall Energy Saving and Analysis

- ASADI vs. PIM baseline
- **Results:** ViL: $1.8\times$; BERT, BART, GPT-2: $2.3\times$ to $63.7\times$ across all datasets.
- **Reasons:** The reduced data transfers between on-chip memory and PEs. With increasing sequence length, ASADI is capable of reducing more on-chip transfers, which results in more energy savings.





- **DIA-PIM:** DIA format involves both compression and decompression phases. While DIA-PIM benefits from the compression phase, it does not gain any advantage from the decompression phase, as it requires the same number of cross-bank transfers as the CSR format.
- CSR-ASADI: The CSR-based SDDMM and SpMM computation paradigms involve many bubbles in PUM platform and severely impact the overall parallelism.





Latency and Energy Breakdown

Background



Figure 21: Latency breakdown. OCT and CTRL: less than 4%; Softmax: 5%; QK and SV: more than 80%.



Figure 22: Energy breakdown. Digital module: more than 98%; Linear layer: 1%; CTRL: less than 1%



otivations DIA-based PUM Architecture and Dataflow **Evaluation**

Sensitivity Analysis

Background

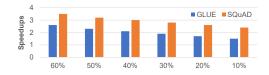


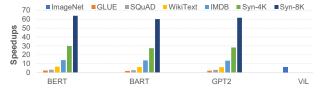
Figure 23: Impact of diagonal locality. Performance degradation as diagonal locality decreases. Lower diagonal locality leads to more bubbles in the DIA format and reduces parallelism in the ReRAM arrays.



Figure 24: Impact of sparsity. Performance degradation as sparsity (τ) increases. More bubbles will increase the ratio of invalid computations, which in turn decreases ASADI's performance.



- **Results:** ASADI achieves linearly increased speedups compared to the baseline when processing longer sequences.
- Analysis: ASADI's latency grows linearly while baseline's latency grows quadratically with sequence length. The overall latency (OL) is related to the latency of one iteration (LOI) and the number of iterations (NI), i.e., $OL = LOI \times NI$. For the PIM baseline, both the NI and LOI increase as sequence length increase, indicating quadratic increasing.





- Observations: 1) We observe the prevalence of diagonal locality in various sparse attention mechanisms; 2) We observe the high on-chip communication overhead in PIM solutions
- Opportunities: Current solutions convert diagonal locality to row/column locality. How to directly support diagonal locality
- Contributions: i) a new compression method to further enhance the diagonal locality; ii) we propose DIA-based sparse matrix computation paradigm and conduct quantitative comparisons with the CSR computing paradigm; iii) we present architecture and dataflow utilizing in-situ computing, which we refer to as ASADI
- Evaluations: The results indicate that ASADI exhibits superior performance and energy efficiency.



Thanks!

- [1] Ashish Vaswani et al.
 - Attention is all you need.

In *Advances in neural information processing systems*, pages 5998–6008, 2017.

- [2] Thomas Wolf et al.
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- [3] Iz Beltagy et al.
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[4] Zheng Qu et al.

Background

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