ELEN E4215 Instructor: T. Dickson
Fall 2020
Programmable Anti-Aliasing Filter Design (v1.1)
Due Date: Tuesday December 15, 2020

1 Project Background

You are to design a digitally programmable low-pass or bandpass anti-aliasing filter (AAF). The continuous-time filter runs off of dual power supplies of +/- 1V, and should be designed using an op-amp RC topology with as low-power solution as possible.

A table of specifications is listed below. The filter has 3b control, to program the response (low-pass or bandpass), passband response (Butterworth or Chebyshev), and the cutoff (3dB) frequency (150kHz or 300kHz). Closed loop

Parameter	Specification	Description
Filter response	Lowpass or bandpass	Programmable
Passband response	Butterworth or Chebyshev	Programmable passband characteristic
Cutoff frequency / center frequency	150 or 300kHz	Filter 3dB frequency (low-pass mode) or center frequency (bandpass mode)
DC or center-frequency gain	0 dB	
Filter order	6^{th} order	
Maximum input amplitude	500mV	Peak signal amplitude
Average (dc) input level	0V	

同学的
Q= 1.93 (3rd section)
Q = .707 (2nd section)
Q = 0.518 (1st section)

Input range: 500mv input amplitude

How to order sections?

High q (at 1st ? - no)—>
So lower q sectons first,

Chebyshev would have higher q than butterworth
Power consumption: 3 s-k lowest power
but q hard to design

Akerberg compared to t-t:

2nd integrator has lower loss, preferable

2 Subcomponents

2.1 Op-amps – You will need to develop op-amp models for your opamp-RC filter, based on the 2-stage op-amp model discussed in class. Determine any required op-amp specifications such as gain, bandwidth, slew rate, and output swing. For the first stage transconductor, the maximum output current and transconductance must adhere to the following relationship: Iomax/gm = 200mV. The output stage of the op-amp can provide no more than +/- 800mV output swing. The simple approximation for op-amp power consumption described in class is sufficient for determining the static power consumption of your op-amp.

2.2 'Analog multiplexers' – You can make use of the 'analog_mux' element in the ahdlLib component library provided in the Cadence Virtuoso design environment. This element selects one of two analog input signals to pass through to the output, depending on the voltage applied to the digital select voltage 'vsel'. This 'vsel' signal should be expected to take on digital logic values of +1V (logic high) or -1V (logic low), with a selection threshold of 0V (in other words, any voltage greater than the threshold will be interpreted as logic high, and any voltage lower than the threshold will be interpreted as logic low). While this 'analog_mux' element is ideal, we should consider the impact of parasitics associated with this switch on the filter performance. Therefore, on each input of the analog_mux, you must add a 100-ohm resistor in series with the input. in series iwth input mux

2.3 Capacitor limits – no capacitors smaller than 50pF should be used.

3 Assessment:

3.1 A report will be submitted from each design group (maximum of 2 students per group, but you can work individually if you prefer – there will be no difference in assessment). Quality of the written report will be assessed, including clarity and organization. The report should be no more than 10 pages, including figures. The IEEE template for transactions articles should be followed:

https://ieeeauthorcenter.ieee.org/create-your-ieee-article/use-authoring-tools-and-ieee-article-templates/ieee-article-templates/templates-for-transactions/

References to the textbook (Schaumann) or the instructor's lecture notes are not required. Any other books or scholarly articles that may have inspired your design should be properly cited.

3.2 You are free to include any information you feel relevant to describing your design into your report. Here are some recommendations of what could be included in a successful report:

- 3.2.1 Filter transfer function – clearly derive the required AAF transfer function. MATLAB plots of the transfer function frequency response are encouraged to verify that the transfer function meets the specifications.
- 3.2.2 Describe the procedure for implementing the transfer function.
- 3.2.3 Subcomponents – clearly determine the op-amp requirements. Relevant simulations of subcomponent performance (bandwidth, transfer characteristic, output resistance, etc) can be included.
- 3.2.4 Schematics – clearly show all filter and/or sub-section designs, including resistor/capacitor values and how they are determined.
- 3.2.5 Simulation Results – show relevant simulation results for your filter, including:
  - 3.2.5.1 Frequency response
  - 3.2.5.2 Transient simulations to show adequate slew rate, etc.
  - 3.2.5.3 Power consumption (this can be estimated as the three times the product of the supply voltage and the maximum output current of the 1st stage transconductor)
  - 3.2.5.4 Any other sims you feel are relevant to demonstrating your filter performance