



sim -Default

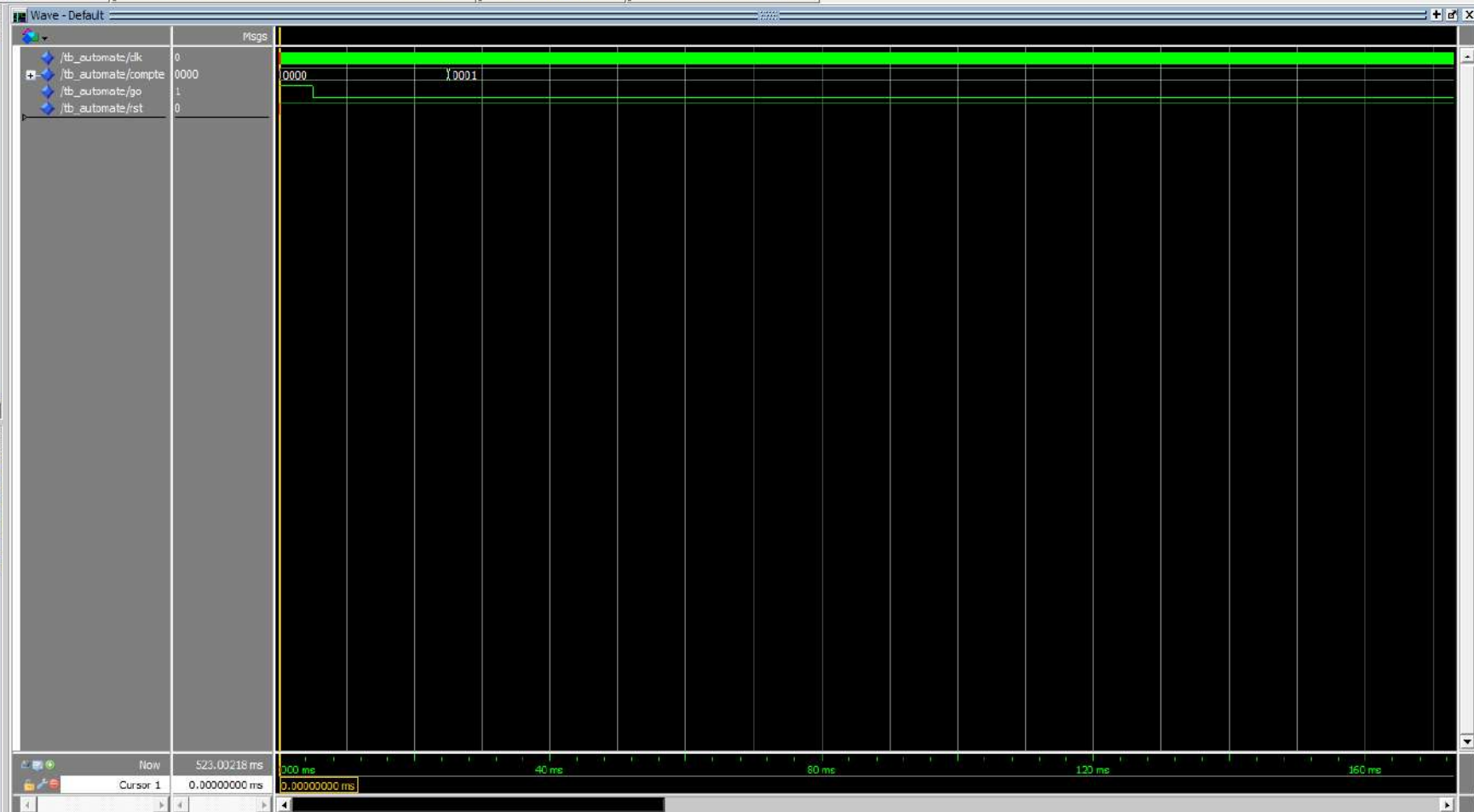
Instance	Design unit	Des
tb_automate	tb_automate...	And
i1	automate(...	And
stim_proc	tb_automate...	Proc
line_38	tb_automate...	Proc
standard	standard	Pac
textio	textio	Pac
std_logic_1164	std_logic_1...	Pac
std_logic_arith	std_logic_a...	Pac
std_logic_unsigned	std_logic_u...	Pac

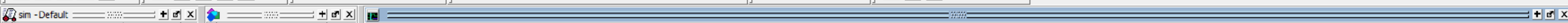
Objects

Name	Value
clk	0
compte	0000
go	1
rst	0

Processes (Active)

Name	Type (f)
stim_proc	VHDL P
line_38	VHDL P
p5	VHDL P
p4	VHDL P
p3	VHDL P
p2	VHDL P
p1	VHDL P





Instance	Design unit	Des
tb_automate	tb_automate...	Ard
i1	automate(...	Ard
stim_proc	tb_automate...	Pro
line_38	tb_automate...	Pro
standard	standard	Pac
textio	textio	Pac
std_logic_1164	std_logic_1...	Pac
std_logic_arith	std_logic_a...	Pac
std_logic_unsigned	std_logic_u...	Pac

Name	Value
clk	0
rst	0
go	1
compte	0000
cp	IDLE
es	IDLE
enable	0
go_compte	0
fin	0

Name	Value
/tb_automate/clk	0
/tb_automate/rst	0
/tb_automate/go	1
/tb_automate/compte	0000
/tb_automate/i1/ep	IDLE
/tb_automate/i1/es	IDLE
/tb_automate/i1/enable	0
/tb_automate/i1/go_compte	0
/tb_automate/i1/fin	0
/tb_automate/i1/clk	0
/tb_automate/i1/rst	0
/tb_automate/i1/go	1
/tb_automate/i1/compte	0000

Processes (Active)

Name	Type (t)

