

An Automated Design Flow from Synchronous RTL to Optimized Layout using Commercial  
EDA Tools for Multi-Threshold NULL Convention Logic Circuits

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Cole Harrington Sherrill  
University of Arkansas  
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University of Arkansas  
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University of Arkansas

This dissertation is approved for recommendation to the Graduate Council.

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Jia Di, Ph.D.  
Dissertation Director

---

Alexander Nelson, Ph.D.  
Committee Member

---

David Andrews, Ph.D.  
Committee Member

---

Zhong Chen, Ph.D.  
Committee Member

## ABSTRACT

This work presents the first automated design flow from synchronous RTL to highly optimized layout for Multi-Threshold NULL Convention Logic (MTNCL) circuits. The developed synthesis flow overcomes many of the drawbacks of existing attempts and leverages the advanced optimization features provided by modern synthesis tools. The remaining timing race conditions native to the MTNCL architecture have been identified and thoroughly explored. Two sets of novel timing constraints were devised: the first responds to these race conditions, yielding highly reliable MTNCL circuits; the second directly targets the critical paths within MTNCL circuits, allowing the designer to optimize the target circuit for high performance, low power, or some tradeoff between the two. To demonstrate the advantages of the proposed flow and timing constraints, a large set of circuits—including 64-bit adders, 32×32 Montgomery modular multipliers, and AES-256 cores—was developed in the TSMC 65nm technology. Following physical implementation and R+C parasitic extraction, each circuit was simulated at transistor level to provide the highest accuracy evaluations possible. Results range from 140% higher throughput for *high-performance* circuits to 28.6% less active energy per operation, 42.9% less static power consumption, and 29.6% less area for circuits targeting *low-power* operation. The circuits developed with the proposed design flow are arguably the most reliable and highest quality MTNCL circuits to date. These results indicate that when MTNCL designs leverage the same tools ubiquitous to synchronous circuit design, they can simultaneously achieve significantly higher performance, greater active energy efficiency, lower static power consumption, and smaller design area compared to previous attempts.

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