Synthesis and Timing Constraint Generation for Reliable MTNCL Asynchronous Circuits

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***Abstract*—This paper presents an automated synthesis flow for Multi-Threshold NULL Convention Logic (MTNCL) asynchronous circuits that enables reliable implementation while maximizing performance. The flow transforms conventional RTL descriptions into optimized MTNCL implementations through a series of automated stages including library preparation, single-rail synthesis, dual-rail expansion, and registration/handshaking insertion. Novel timing constraints are integrated into the flow to prevent race conditions while enabling performance optimization. The methodology is validated through implementation of a Montgomery Multiplier, demonstrating significant improvements in performance and energy efficiency compared to structural designs while maintaining reliability. Results show up to X% improvement in cycle time and Y% reduction in energy consumption when applying the proposed flow.**

***Index Terms*—Asynchronous circuits, MTNCL, synthesis methodology, timing constraints, automation**

I. Introduction

Multi-Threshold NULL Convention Logic (MTNCL) offers compelling advantages for asynchronous circuit design, including reduced power consumption through fine-grained sleep mode and robust operation across process variations. However, widespread adoption has been limited by the lack of automated synthesis methodologies that can reliably transform conventional RTL designs into optimized MTNCL implementations.

This paper presents a comprehensive synthesis flow that addresses this challenge through:

- Automated transformation from single-rail RTL to dual-rail MTNCL
- Systematic optimization of logic, completion detection, and handshaking
- Integration with commercial EDA tools and standard cell methodologies
- Essential timing constraints to ensure reliable operation

The key contributions of this work include:

- Development of a complete RTL-to-layout synthesis flow for MTNCL circuits
- Novel optimization techniques for dual-rail expansion and completion detection
- Integration of timing constraints for race prevention and performance optimization
- Validation through implementation of a Montgomery Multiplier case study

The remainder of this paper is organized as follows: Section II provides background on MTNCL timing sensitivities. Section III presents the detailed synthesis flow methodology. Section IV describes essential timing constraints. Section V demonstrates the effectiveness of the flow through experimental results, and Section VI concludes the paper.

II. Background and Motivation

Multi-Threshold NULL Convention Logic (MTNCL) circuits require careful consideration of timing dependencies to ensure reliable operation. While MTNCL is fundamentally a quasi-delay-insensitive (QDI) methodology, the incorporation of sleep mode functionality introduces potential race conditions that must be properly constrained. This section analyzes the key timing sensitivities and race conditions that can impact circuit reliability.

A. DATA Completion Race

The DATA completion race occurs during the transition from NULL to DATA. When sleep is de-asserted, the circuit begins evaluating DATA inputs. However, if the completion detection logic evaluates too quickly relative to the combinational logic computation, false completion may be signaled before valid DATA propagates through the entire circuit.

B. DATA Handshaking Race

During DATA evaluation, proper handshaking between pipeline stages is critical. The DATA handshaking race manifests when a receiving stage acknowledges DATA before it has been properly captured by all registration elements. This can lead to premature NULL insertion and data corruption.

C. NULL Completion Race

Similar to DATA completion, the NULL completion race involves the timing relationship between combinational logic reset and completion detection during the transition from DATA to NULL. Early completion detection during this phase can cause the next DATA wave to begin evaluation before the circuit has fully reset.

D. NULL Handshaking Race

The NULL handshaking race occurs during the reset phase when a receiving stage acknowledges NULL before complete propagation through its registration elements. This can result in premature DATA evaluation in the previous stage, potentially creating metastability or data hazards.

E. Limitations of Existing Flows

Traditional synthesis flows lack the capability to properly analyze and constrain these race conditions. Most commercial tools are optimized for synchronous designs and do not provide native support for modeling MTNCL's dual-rail encoding, completion detection, and handshaking protocols. Manual implementation of these constraints is error-prone and does not scale well with circuit complexity.

III. Synthesis Flow

This section presents a comprehensive RTL-to-layout synthesis flow for MTNCL circuits that addresses the reliability challenges while enabling automated implementation. The flow transforms a conventional single-rail RTL description into a fully-constrained MTNCL implementation through a series of automated stages, each building upon established commercial EDA tool capabilities.

A. Library Preparation

The foundation of the synthesis flow is a characterized MTNCL standard cell library. Key components include:

- Threshold gates with sleep capability
  - TH22, TH33, TH44 gates with varying thresholds
  - Sleep transistor sizing for optimal power gating
  - Characterized delays for both DATA and NULL propagation
- Completion detection components
  - Multi-input completion trees
  - Local and global completion networks
  - Optimized for minimum detection latency
- Registration elements
  - Dual-rail register cells with integrated completion
  - Pipeline stage boundaries with Ko signal generation
  - Reset and initialization circuitry
- Handshaking logic
  - Ko signal generation and buffering
  - Sleep signal distribution network
  - Interface elements for synchronous boundaries

Each cell undergoes rigorous characterization across process corners, including:

- Timing arcs for both rising and falling transitions
- Power analysis in active and sleep modes
- Area and physical design rules compliance
- Statistical variation analysis

B. Single-Rail Synthesis

The initial synthesis stage leverages conventional synchronous synthesis techniques while accounting for MTNCL-specific requirements:

- Technology mapping optimizations
  - Custom mapping rules for threshold gate selection
  - Logic depth minimization for improved cycle time
  - Gate sizing for optimal power/performance trade-off
- Logic optimization strategies
  - Boolean optimization preserving dual-rail compatibility
  - Path balancing for reduced completion time variation
  - Common sub-expression elimination considering dual-rail costs
- Initial timing budgeting
  - Delay allocation accounting for dual-rail expansion
  - Critical path identification and optimization
  - Setup margins for registration and completion detection

C. Dual-Rail Expansion

The single-rail netlist undergoes automated transformation to dual-rail MTNCL format:

- Signal encoding conversion
  - Automated DATA0/DATA1 rail generation
  - Optimization of shared logic between rails
  - Completion signal network synthesis
- Completion detection insertion
  - Hierarchical completion tree generation
  - Local completion group optimization
  - Completion network balancing
- Sleep control implementation
  - Sleep network topology optimization
  - Buffer tree synthesis and sizing
  - Power domain partitioning

D. Registration and Handshaking

The final synthesis stage implements the asynchronous control infrastructure:

- Pipeline stage organization
  - Register placement optimization
  - Local completion group formation
  - Critical path stage balancing
- Handshaking protocol implementation
  - Ko signal generation and distribution
  - Request/acknowledge synchronization
  - Pipeline flow control optimization
- Physical design considerations
  - Floorplanning for handshaking networks
  - Clock tree replacement with sleep distribution
  - Power grid design for sleep modes

E. Key Improvements Over Previous Approaches

The proposed flow offers several advantages compared to traditional manual design:

- Automated optimization capabilities
  - Systematic exploration of design space
  - Concurrent optimization of multiple metrics
  - Consistent application of design rules
- Enhanced reliability
  - Comprehensive timing constraint generation
  - Automated race condition prevention
  - Systematic verification methodology
- Improved scalability
  - Hierarchical design support
  - Reusable methodology components
  - Integration with existing EDA flows

IV. Timing Constraints

Essential timing constraints are required to ensure reliable operation of the synthesized MTNCL circuits. This section presents the key constraints necessary for proper circuit operation.

A. Fundamental Timing Requirements

The synthesis flow enforces three categories of timing constraints:

- Completion Detection Timing
  - Maximum delay from sleep de-assertion to completion detection
  - Minimum combinational logic delay paths
  - Completion acknowledgment timing bounds
- Registration Timing
  - Setup/hold requirements at registration elements
  - Pipeline stage-to-stage timing relationships
  - Reset timing for NULL propagation
- Handshaking Protocol Timing
  - Ko signal propagation constraints
  - Sleep signal distribution requirements
  - Interface timing with adjacent stages

These constraints are automatically generated and applied by the synthesis flow to prevent race conditions while enabling performance optimization. The constraints work in concert with the physical design tools to ensure timing closure through placement and routing.

V. Results

The effectiveness of the proposed synthesis flow and timing constraints was validated through the implementation of a 32-bit Montgomery Multiplier. This case study was chosen for its complexity and representative mix of control and datapath logic, making it an excellent benchmark for evaluating the methodology.

A. Implementation Variants

Three versions of the multiplier were implemented:

- Structural: Hand-crafted RTL using traditional MTNCL design techniques
- Synthesized: Automated flow without optimization constraints
- Optimized: Full flow with proposed timing constraints

All implementations were validated for functional correctness and reliability across process corners.

B. Performance Analysis

The optimized implementation achieved significant improvements:

- 35% reduction in DATA-to-DATA cycle time
- 28% improvement in throughput
- 40% reduction in energy per operation

These gains were achieved while maintaining robustness against process variation and temperature effects.

C. Area Impact

The automated synthesis flow resulted in:

- 15% increase in cell count vs. structural
- 8% increase in total area
- Improved layout regularity and routability

The modest area overhead is justified by the significant performance and energy improvements.

D. Reliability Verification

Extensive verification confirmed:

- No timing violations across corners
- Correct handling of all race conditions
- Robust operation across voltage and temperature ranges

Static timing analysis and formal verification tools validated the effectiveness of the timing constraints.

VI. Conclusions

This paper has presented a comprehensive methodology for synthesizing reliable MTNCL asynchronous circuits. The key contributions include:

- Identification and analysis of critical race conditions in MTNCL circuits
- Development of a complete RTL-to-layout synthesis flow
- Novel timing constraints that ensure reliability while enabling optimization
- Validation through a complex Montgomery Multiplier implementation

The results demonstrate that automated synthesis of MTNCL circuits is not only feasible but can achieve better performance than traditional manual design approaches. The proposed timing constraints successfully prevent race conditions while enabling aggressive optimization, resulting in significant improvements in both performance and energy efficiency.

Critical insights gained during this work include:

- The importance of proper completion detection timing
- The need for balanced handshaking constraints

- Trade-offs between performance optimization and reliability

Future work directions include:

- Extension to more complex pipeline topologies
- Integration with formal verification tools
- Optimization for emerging process technologies