APPROACHES (SCIENTIFIC METHOD)

ANALYTICAL FOUNDATIONS

1. POWER ATTRIBUTION PRINCIPLE

- 1.011 (a) GUEST VEs: DYNAMIC POWER ONLY (b) HOST/ROOT VM: STATIC ONLY
- 1.012 (a) DATA PLANE (b) VIRTUAL IO (c) NETWORK FUNCTION
- 1.013 (a) IDLE POWER (b) W/L POWER EXCL. TEMP-DEPENDENT EFFECTS (c) TEMP.-DEPENDENT ADDITIONAL POWER

1.01 DECOMPOSITION

- 1.02 ATTRIBUTION OF BOTH STATIC AND DYNAMIC POWER TO GUEST VEs
- 1.03 DIRECT ENERGY ACCOUNTING TO EACH I/O REQUEST: DISK STATE, POWER CONS. IN DISK STATE, TRANSFER RATE, REQUEST SIZE.

2. MODELLING BIAS

- 2.01 LINEAR REGRESSION
- 2.02 POLYNOMIAL REGRESSION
- 2.03 SUB-LINEAR REGRESSION
- 2.04 GAUSSIAN MIXTURE MODELLING
- 2.05 SUPPORT VECTOR REGRESSION
- 2.06 CLASSIFICATION OF DATA
- 2.07 PRINCIPAL COMPONENT ANALYSIS
- 2.08 HYPOTHESIS: POWER AS QUADRATIC(EFF. FREQ.)
- 2.09 HYPOTHESIS: POWER AS QUADRATIC(TEMP.)
- 2.10 METAHEURISTICS
- 2.11 PROCESSOR MODELLED AS A SINGLE QUEUE, SINGLE SERVER WITH VACATION & SETUP TIME
- 2.12 PACKET TRAFFIC ARRIVAL IS BMAP
- 2.13 MULTI-LAYER PERCEPTRON
- 2.14 DECISION TREE REGRESSION

3. GREEN OPERATING PRINCIPLES

- 3.01 RUN-TO-COMPLETION AUGMENTED BY LPI AND ADAPTATION OF POWER STATE ON RESUMPTION
- 3.02 RUN-TO-COMPLETION
- 3.03 RUN-TO-COMPLETION AUGMENTED BY LPI
- 3.04 USE LOW-POWER INSTRUCTION INSTEAD OF LOW-POWER IDLE AND USE PROCESSOR-UTILIZATION-DRIVEN ADAPTATION OF P-STATE

4. PHYSICAL ANALYSIS

- 4.01 PROCESSOR SUBUNIT PHYSICAL ANALYSIS, INCL. (IMPLICIT) USE OF DENNARD'S LAW & SWITCHING FREQUENCY
- 4.02 PHYSICAL ANALYSIS OF CAUSES OF MOS POWER CONSUMPTION

5. IDENTIFICATION OF METRIC OF ENERGY EFFICIENCY

- 5.01 J/Web interaction
- 5.02 hash/J
- 5.03 GFLOP/W
- 5.04 J/bit

EXPERIMENT DESIGN

RESOURCE PROVISION

6. MANAGED (AT SETUP TIME)

- 6.01 MANUAL FREQUENCY SCALING
- 6.02 USE TIME-BASED INTERRUPT COALESCENCE ON NIC
- 6.03 HARDWARE THREADS
- 6.04 NIC DATA RATE CAPACITY or UTILIZATION
- 6.051 BIND vCPU TO HARDWARE THREAD
- 6.052 BIND vCPU TO PHYSICAL CORE
- 6.053 BIND DPDK TO PHYSICAL CORE
- 6.054 APPLY NUMA CONSTRAINT
- 6.055 BIND CORE TO NETWORK PORT
- 6.056 BIND VM TO PHYSICAL CORE
- 6.057 BIND INTERRUPT HANDLING TO A PHYSICAL CORE

6.05 AFFINITY TECHNIQUES

- 6.061 USE A MENU OF VM RESOURCE CONFIGS
- 6.062 USE A MENU OF NETWORK IO PLATFORMS

6.06 USE A SET OF RESOURCE CONFIGURATIONS

- 6.07 FORCE IDLE
- 6.08 USE SOFTWARE NETWORK SWITCH.

7. OPERATING TIME

- 7.01 ADJUST P-STATE & LOW-POWER-INSTRUCTION TIME ACCORDING TO PROC. UTIL. THRESHOLD OBTAINED USING Q-ING MODEL
- 7.02 ADJUST P-STATE & C-STATE ACCORDING TO PAST LOAD SAMPLE
- 7.03 AUTOMATED FREQUENCY ADJUSTMENT
- 7.04 AUTOMATED ADJUSTMENT OF #THREADS

WORKLOAD SELECTION

8. RESOURCE SPECIFIC

- 8.01 Processor-intensive W/L
- 8.02 Memory-intensive W/L
- 8.03 Network-intensive W/L
- 8.04 Mass-storage-intensive W/L
- 8.05 CPU CORE SPECIFIC W/L
- 8.06 MEM-HIER.-LEVEL SPECIFIC W/L
- 8.07 MULTI-CORE, CORE-SPECIFIC, PROGRESSIVE UTILIZATION

9. REPRESENTATIVE OF REAL USE

- 9.01 TPC-W / Web Search
- 9.02 FILE TRANSFER
- 9.03 MULTIPLE, CONCURRENT HTTP DOWNLOADS
- 9.04 Representative processor-intensive (CPU2006, CPU2000, BYTEmark, SPECpower_ssj2008)
- 9.05 STRESS-NG
- 9.06 NASA PARALLEL BENCHMARKS
- 9.07 GCC
- 9.08 PARSEC
- 9.09 MISC SMALL PROGS.
- 9.10 MULTIMEDIA TRAFFIC
- 9.11 REAL-WORLD TRAFFIC TRACE
- 9.12 BMAP TRAFFIC STREAM
- 9.13 TRANSCODING TO HEVC STREAM
- 9.14 AUTOMATED IMAGE CLASSIFICATION

DATA COLLECTION

10. COMPUTING RESOURCE CONSUMPTION METRIC (predictor)

- 10.011 µ-ARCH EVENT INSTRUMENTATION
- 10.012 µ-ARCH POWER INSTRUMENTATION
- 10.013 VIRTUAL MSRs FOR EVENT INSTRUM.

10.01 IN MICROARCHITECTURE

- 10.021 PROCESSOR UTILIZATION
- 10.022 CONTAINER UTILIZATION
- 10.023 HDD IOPS/DATA RATE/ACTIVE TIME
- 10.024 INSTRUMENTATION INSIDE CUSTOM I/O DEVICE EMULATOR
- 10.025 MEMORY USAGE
- 10.026 INSTRUMENTATION INSIDE TRAFFIC SINK TOOL (e.g. iperf)

10.02 ABSTRACTED BY SYSTEM SOFTWARE

11. WORKLOAD METRIC (predictor)

- 11.01 N/W TX DATA RATE
- 11.02 NUMBER OF PROCESSES
- 11.03 NUMBER OF THREADS
- 11.04 WEB INTERACTIONS/S
- 11.05 N/W PACKET RATE
- 11.06 PACKET MTU
- 11.07 FRAMES PER SECOND
- 11.08 INFERENCES PER SECOND
- 11.09 MIPS

DIRECT POWER MEASUREMENT

- 12.01 SYSTEM POWER METER
- 12.02 POWER SUPPLY OUTPUT

HARDWARE INSTRUMENTATION OF PREDICTORS

- 13.01 CPU PACKAGE TEMP.
- 13.02 FAN SPEED
- 13.03 PACKET TIMESTAMP ON NIC

MODEL VALIDATION

14. SIMULATION

- 14.01 USING DISCRETE-EVENT DRIVEN PROGRAM

15. USE TEST DATA IN POST-TRAINING PHASE

16. CORROBORATION THROUGH EXPERIMENTATION

17. MODEL ADAPTATION TECHNIQUE

- 17.01 MODELLING ON DEMAND: TRAIN A NEW POWER MODEL FOR UNKNOWN {WORKLOAD/ RESOURCE-CONFIGURATION/HOST}
- 17.02 EXTEND THE SET OF COUNTERS WHEN POWER CONSUMPTION UNDER A WORKLOAD DOES NOT FIT THE MODEL
- 17.03 DIVIDE RESOURCE UTIL RANGE & OFFLINE MODEL EACH SUB-RANGE TO CAPTURE UNIQUE SUB-RANGE BEHAVIOUR
- .1 EVENTS OCCURRING IN A VE'S OP-TIME
- .2 EVENTS ARISING OUT OF ACTIVITIES OF EMULATING DRIVERS ON BEHALF OF VE
- .3 EVENTS OCCURRING IN A THREAD'S OP-TIME
- .4 DECOMPOSITION OF SYSTEM POWER INTO VE POWER THROUGH CPU-UTIL.

17.04 MULTIPLE CONCURRENT VEs: TDM