



ua

**Universidade de Aveiro**  
**Mestrado Integrado em Engenharia de Computadores e Telemática**  
**Arquitectura de Computadores Avançada**

**Memory**

Academic year 2019/2020

---

1. Assume a memory subsystem with 23 address lines.
  - 1.1. How many bytes, half-words, words and double-words can be stored in it?
  - 1.2. Give examples of addresses (in hexadecimal form) for bytes, half-words, words and double-words stored in the last quarter of its addressing space.
  - 1.3. Which of the following addresses are classified as *misaligned* if one intends to reference a byte, a half-word, a word and a double-word:  $14902_{10}$ ,  $3710_{10}$ ,  $5555_{10}$ ,  $764_{10}$  and  $2760_{10}$ ? Convert them first to hexadecimal form before giving your answer.
  - 1.4. Can the address  $11899675_{10}$  express a valid byte reference for the memory subsystem?
2. Consider a 128Mbit SDRAM chip organized in 8 banks of 4096 rows x 1024 columns of 4 bits.
  - 2.1. How many address lines are there? Justify clearly your answer.
  - 2.2. How many chips are needed to build a 64-bit data wide memory subsystem? Justify clearly your answer.
  - 2.3. What is the storage capacity of such subsystem? Justify clearly your answer.
  - 2.4. Sketch how the external address bus are mapped internally to make data access as efficient as possible. What is the main concern to be taken into account?