

MPSoC Ultron

Rev 1.3A

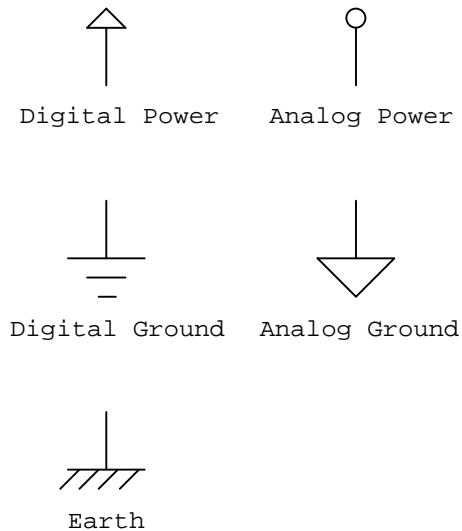
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< Reference Define >

U : Unit (Device)
PU : Power Unit
LD : Discrete LED
D : Diode
H : Header pin (male)
BH : Box Header pin (male)
HS : Header Socket (Female)
SW : Switch
F : Fuse, Filter
CN : Connector
R : Resistor
RA : Array Resistor
EC : Electrolytic Capacitors
CC : Ceramic Capacitors
TC : Tantalum Capacitors
PC : Poymer-Tantalum Capacitors
L : Inductor
FB : Ferrite Bead
Y : Crystal
OSC : Oscillator
Q : Transistor
P : External Port
SPK : Speaker
MIC : Mic
TP : Test Point
BAT : Battery
BZ : Buzzer
JP : Jack
PS : Poly Switch
B : EMI Filter


< Power Symbol >



전원표기 방법
Digital +3.3V => VCC_3P3V
Analog +3.3V => AVCC_3P3V


* PCB Ordering Note
1. PCB width 2.4T.
2. Pin is Gold coating.
3. Layer is 22th.
4. PSR is Green

Passive 소자 표기 방법
3.3K옴 1608Size 저항 => 3.3K_1608
0.1uF 1608Size 커패시터(내압표기 없을경우) => 0.1uF_1608
100uF 7343Size 커패시터(내압표기 있을경우) => 100uF/10V_7343

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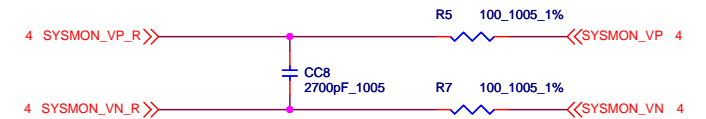
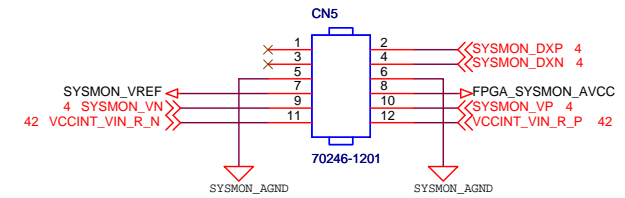
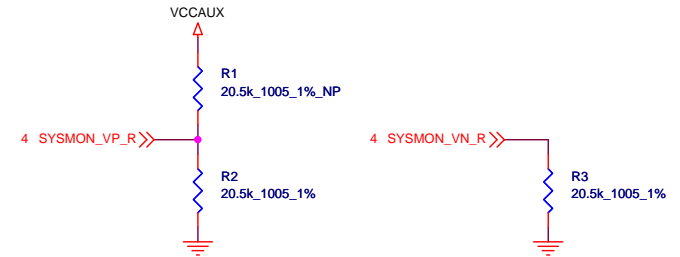
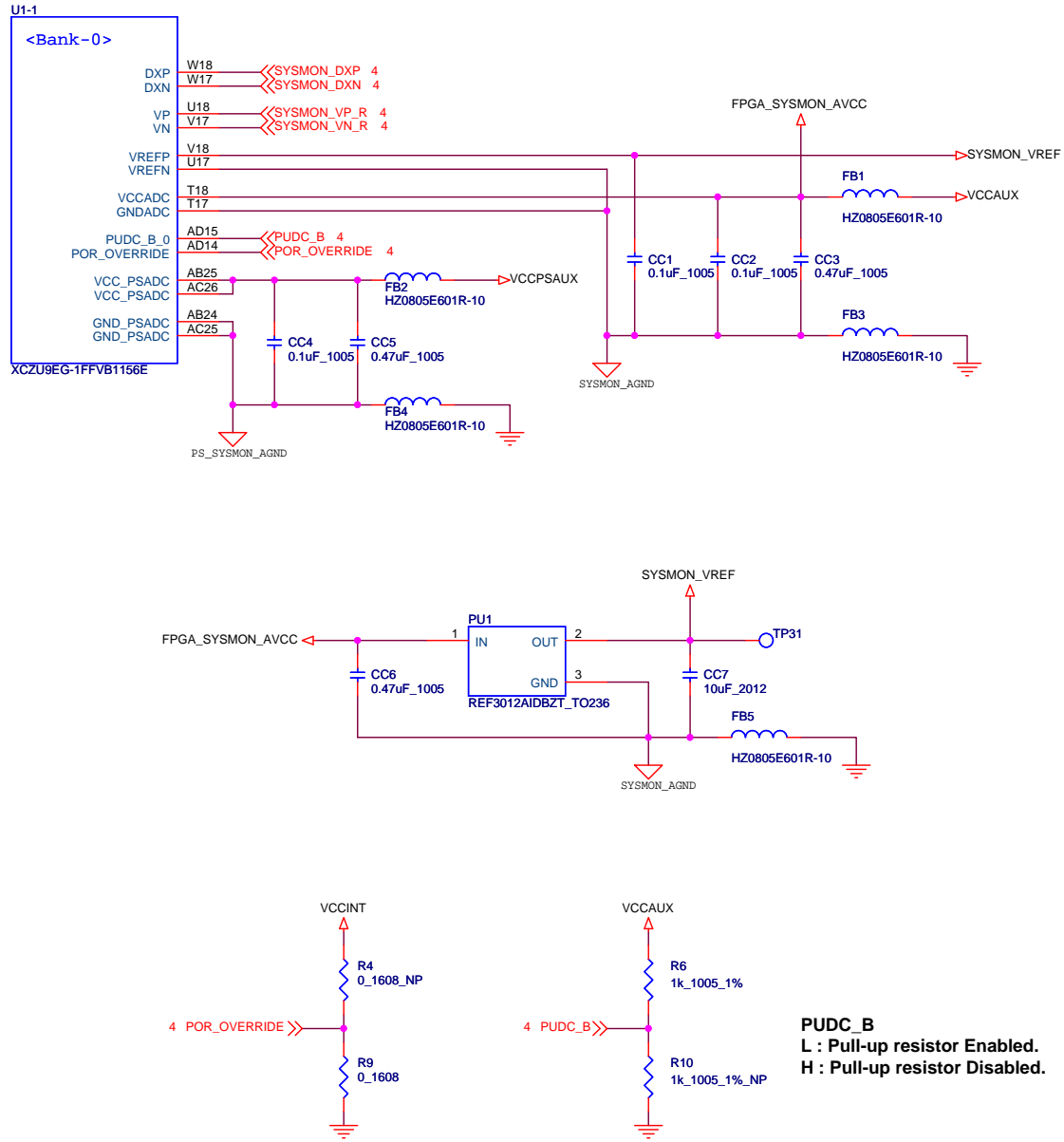
* Revision History

Rev	Date	Descriptions	Director
V1.0A	2017/01/13	1. Initial release	Kim Ki Heon
V1.0F	2017/02/10	1. Product release	Kim Ki Heon
V1.1A	2017/05/10	1. Revision release	Kim Ki Heon
V1.1B	2017/05/17	1. 2nd release	Kim Ki Heon
V1.1C	2017/05/26	1. 3rd release	Kim Ki Heon
V1.1D	2017/05/30	1. 4th release	Kim Ki Heon
V1.1E	2017/06/08	1. 5th release	Kim Ki Heon
V1.2A	2017/07/20	1. Revision release	Kim Ki Heon
V1.3A	2017/12/06	1. Revision release	Kim Ki Heon



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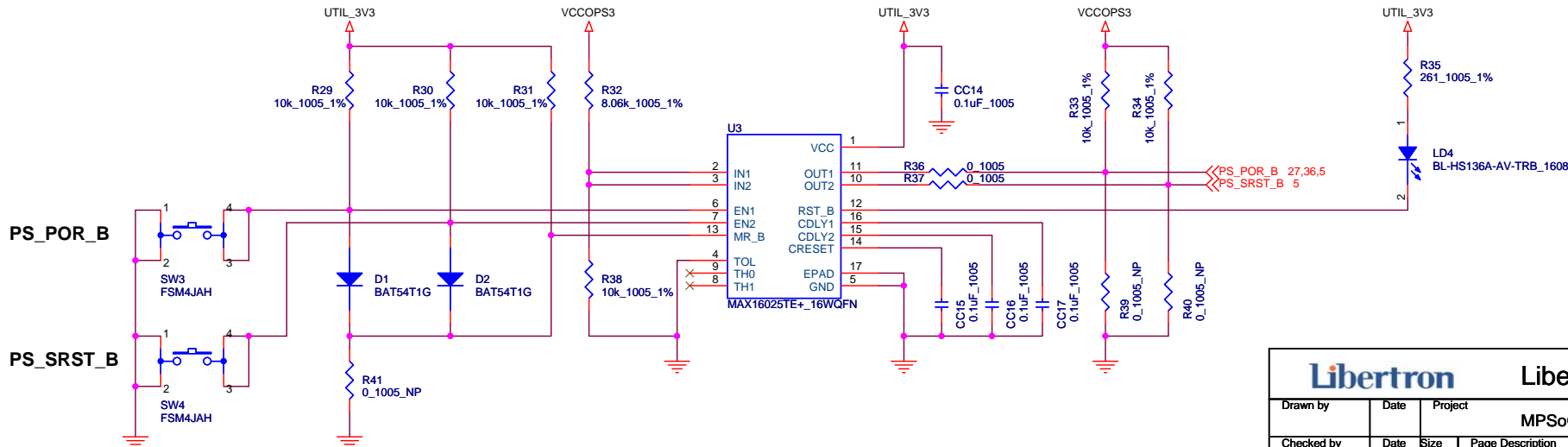
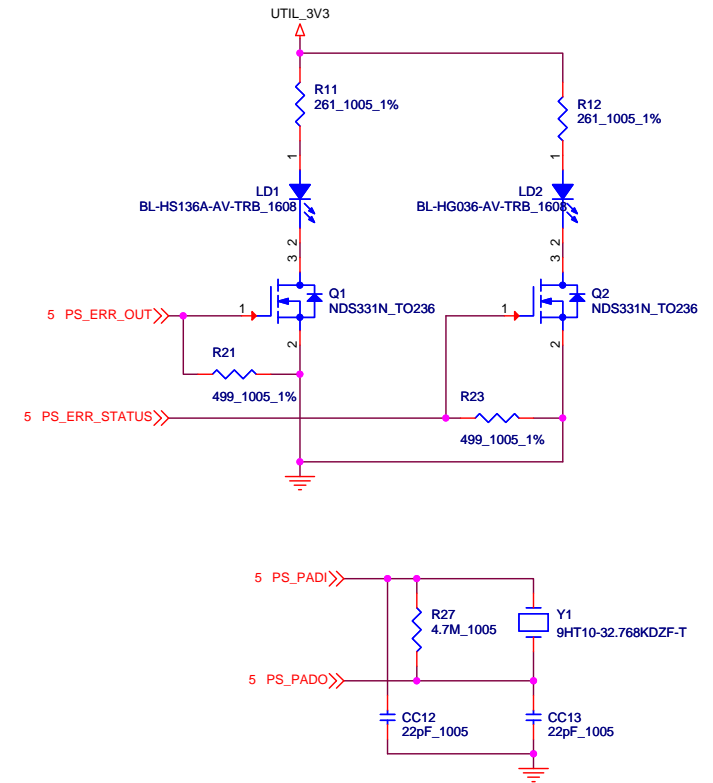
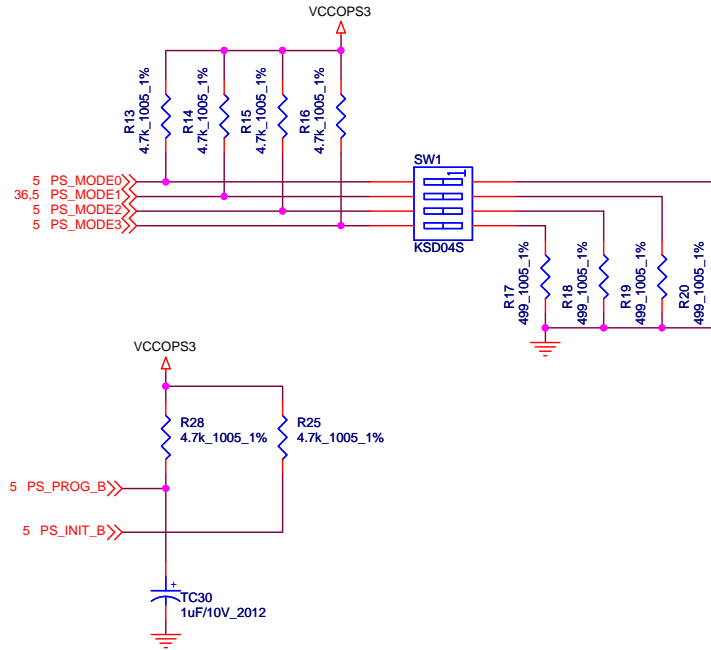
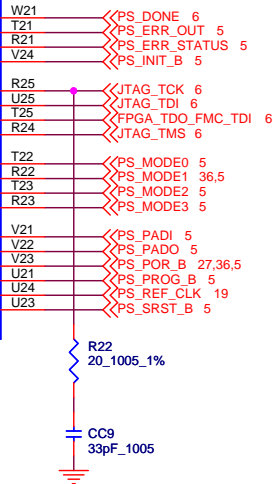
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<PS Configuration>

PS_DONE 6
PS_ERROR_OUT 5
PS_ERROR_STATUS 5
PS_INIT_B 5
PS_JTAG_TCK 6
PS_JTAG_TDI 6
PS_JTAG_TDO 6
PS_JTAG_TMS 6
PS_MODE0 5
PS_MODE1 36,5
PS_MODE2 5
PS_MODE3 5
PS_PADI 5
PS_PADO 5
PS_POR_B 27,36,5
PS_PROG_B 5
PS_REF_CLK 19
PS_SRST_B 5

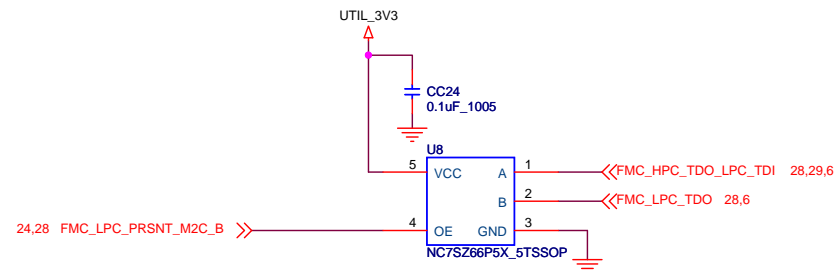
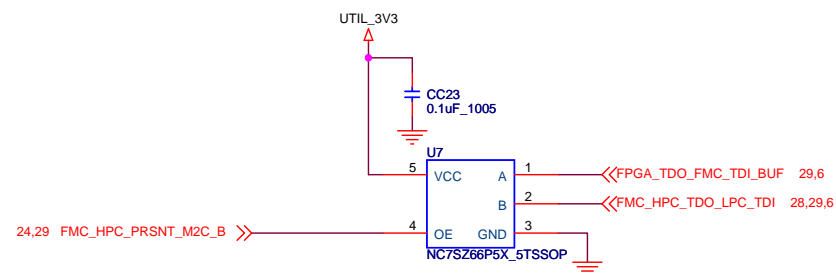
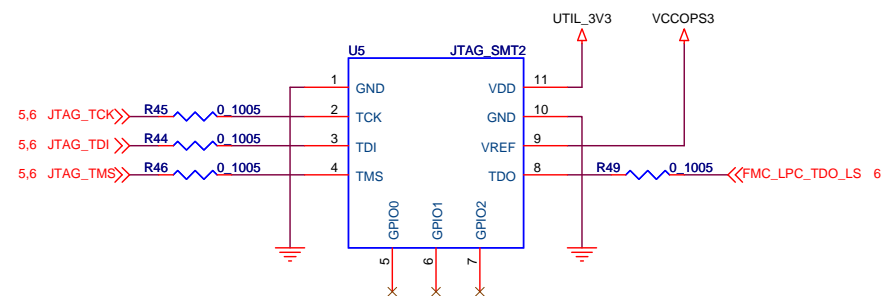
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U1-2

<Bank-44>

IO_L1P_AD11P_44	AN14	<<FPGA_IO_P_44	AN14	29
IO_L1N_AD11N_44	AP14	<<FPGA_IO_N_44	AP14	29
IO_L2P_AD10P_44	AM14	<<FPGA_IO_P_44	AM14	29
IO_L2N_AD10N_44	AN13	<<FPGA_IO_N_44	AN13	29
IO_L3P_AD9P_44	AN12	<<FPGA_IO_P_44	AN12	29
IO_L3N_AD9N_44	AP12	<<FPGA_IO_N_44	AP12	29
IO_L4P_AD8P_44	AL13	<<FPGA_IO_P_44	AL13	29
IO_L4N_AD8N_44	AK15	<<FPGA_IO_N_44	AM13	29
IO_L5P_HDGC_AD7P_44	AK15	<<CLK_74_25_P	19,7	
IO_L5N_HDGC_AD7N_44	AK13	<<CLK_74_25_N	19,7	
IO_L6P_HDGC_AD6P_44	AL12	<<FPGA_IO_GC_P_44	AK13	29
IO_L6N_HDGC_AD6N_44	AH14	<<FPGA_IO_GC_N_44	AL12	29
IO_L7P_HDGC_AD5P_44	AH13	<<FPGA_IO_GC_P_44	AH14	29
IO_L7N_HDGC_AD5N_44	AJ15	<<FPGA_IO_GC_N_44	AH13	29
IO_L8P_HDGC_AD4P_44	AJ14	<<FPGA_IO_GC_P_44	AJ15	29
IO_L8N_HDGC_AD4N_44	AE13	<<FPGA_IO_GC_N_44	AJ14	29
IO_L9P_AD3P_44	AF13	<<FPGA_IO_P_44	AE13	29
IO_L9N_AD3N_44	AG14	<<FPGA_IO_N_44	AF13	29
IO_L10P_AD2P_44	AG13	<<FPGA_IO_P_44	AG14	29
IO_L10N_AD2N_44	AF15	<<FPGA_IO_N_44	AG13	29
IO_L11P_AD1P_44	AG15	<<FPGA_IO_P_44	AF15	29
IO_L11N_AD1N_44	AE15	<<FPGA_IO_N_44	AG15	29
IO_L12P_AD0P_44	AE14	<<FPGA_IO_P_44	AE15	29
IO_L12N_AD0N_44		<<FPGA_IO_N_44	AE14	29

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U1-3

<Bank-47>

IO_L1P_AD11P_47	L20	<<FPGA_IO_P_47	L20	29
IO_L1N_AD11N_47	K20	<<FPGA_IO_N_47	K20	29
IO_L2P_AD10P_47	L19	<<FPGA_IO_P_47	L19	29
IO_L2N_AD10N_47	K19	<<FPGA_IO_N_47	K19	29
IO_L3P_AD9P_47	J21	<<FPGA_IO_P_47	J21	29
IO_L3N_AD9N_47	H21	<<FPGA_IO_N_47	H21	29
IO_L4P_AD8P_47	J19	<<FPGA_IO_P_47	J19	29
IO_L4N_AD8N_47	J20	<<FPGA_IO_N_47	J20	29
IO_L5P_HDGC_AD7P_47	G21	<<CLK_125_P	19,7	
IO_L5N_HDGC_AD7N_47	F21	<<CLK_125_N	19,7	
IO_L6P_HDGC_AD6P_47	G20	<<FPGA_IO_GC_P_47	G20	29
IO_L6N_HDGC_AD6N_47	F20	<<FPGA_IO_GC_N_47	F20	29
IO_L7P_HDGC_AD5P_47	E22	<<FPGA_IO_GC_P_47	E22	29
IO_L7N_HDGC_AD5N_47	D22	<<FPGA_IO_GC_N_47	D22	29
IO_L8P_HDGC_AD4P_47	E20	<<FPGA_IO_GC_P_47	E20	29
IO_L8N_HDGC_AD4N_47	D20	<<FPGA_IO_GC_N_47	D20	29
IO_L9P_AD3P_47	D21	<<FPGA_IO_P_47	D21	29
IO_L9N_AD3N_47	C22	<<FPGA_IO_N_47	C22	29
IO_L10P_AD2P_47	C21	<<FPGA_IO_P_47	C21	29
IO_L10N_AD2N_47	B21	<<FPGA_IO_N_47	B21	29
IO_L11P_AD1P_47	A21	<<FPGA_IO_P_47	A21	29
IO_L11N_AD1N_47	A22	<<FPGA_IO_N_47	A22	29
IO_L12P_AD0P_47	B20	<<FPGA_IO_P_47	B20	29
IO_L12N_AD0N_47	A20	<<FPGA_IO_N_47	A20	29

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<Bank-48>

IO_L1P_AD15P_48	H18	<<FPGA_IO_P_48	H18	29
IO_L1N_AD15N_48	H19	<<FPGA_IO_N_48	H19	29
IO_L2P_AD14P_48	J17	<<FPGA_IO_P_48	J17	29
IO_L2N_AD14N_48	H17	<<FPGA_IO_N_48	H17	29
IO_L3P_AD13P_48	L18	<<FPGA_IO_P_48	L18	29
IO_L3N_AD13N_48	K18	<<FPGA_IO_N_48	K18	29
IO_L4P_AD12P_48	L17	<<FPGA_IO_P_48	L17	29
IO_L4N_AD12N_48	K17	<<FPGA_IO_N_48	K17	29
IO_L5P_HDGC_48	G18	<<FPGA_IO_GC_P_48	G18	29
IO_L5N_HDGC_48	F17	<<FPGA_IO_GC_N_48	F17	29
IO_L6P_HDGC_48	F18	<<FPGA_IO_GC_P_48	F18	29
IO_L6N_HDGC_48	E19	<<FPGA_IO_GC_N_48	E19	29
IO_L7P_HDGC_48	D19	<<FPGA_IO_GC_P_48	D19	29
IO_L7N_HDGC_48	E17	<<FPGA_IO_GC_N_48	E17	29
IO_L8P_HDGC_48	E18	<<FPGA_IO_GC_P_48	E18	29
IO_L8N_HDGC_48	D17	<<FPGA_IO_GC_N_48	D17	29
IO_L9P_AD11P_48	C17	<<FPGA_IO_P_48	C17	29
IO_L9N_AD11N_48	B18	<<FPGA_IO_N_48	B18	29
IO_L10P_AD10P_48	B19	<<FPGA_IO_P_48	B19	29
IO_L10N_AD10N_48	C18	<<FPGA_IO_N_48	C18	29
IO_L11P_AD9P_48	C19	<<FPGA_IO_P_48	C19	29
IO_L11N_AD9N_48	A17	<<FPGA_IO_N_48	A17	29
IO_L12P_AD8P_48	A18	<<FPGA_IO_P_48	A18	29
IO_L12N_AD8N_48		<<FPGA_IO_N_48	A18	29

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<Bank-49>

IO_L1P_AD15P_49	F16	<<FPGA_IO_P_49	F16	29
IO_L1N_AD15N_49	F15	<<FPGA_IO_N_49	F15	29
IO_L2P_AD14P_49	D16	<<FPGA_IO_P_49	D16	29
IO_L2N_AD14N_49	C16	<<FPGA_IO_N_49	C16	29
IO_L3P_AD13P_49	B16	<<FPGA_IO_P_49	B16	29
IO_L3N_AD13N_49	A16	<<FPGA_IO_N_49	A16	29
IO_L4P_AD12P_49	B15	<<FPGA_IO_P_49	B15	29
IO_L4N_AD12N_49	A15	<<FPGA_IO_N_49	A15	29
IO_L5P_HDGC_49	D15	<<FPGA_IO_GC_P_49	D15	29
IO_L5N_HDGC_49	E14	<<FPGA_IO_GC_N_49	E14	29
IO_L6P_HDGC_49	D14	<<FPGA_IO_GC_P_49	D14	29
IO_L6N_HDGC_49	C14	<<FPGA_IO_GC_N_49	C14	29
IO_L7P_HDGC_49	B14	<<FPGA_IO_GC_P_49	B14	29
IO_L7N_HDGC_49	C13	<<FPGA_IO_GC_N_49	C13	29
IO_L8P_HDGC_49	B13	<<FPGA_IO_GC_P_49	B13	29
IO_L8N_HDGC_49	A13	<<FPGA_IO_GC_N_49	A13	29
IO_L9P_AD11P_49	A12	<<FPGA_IO_P_49	A12	29
IO_L9N_AD11N_49	C12	<<FPGA_IO_N_49	C12	29
IO_L10P_AD10P_49	B12	<<FPGA_IO_P_49	B12	29
IO_L10N_AD10N_49	D12	<<FPGA_IO_N_49	D12	29
IO_L11P_AD9P_49	F13	<<FPGA_IO_P_49	F13	29
IO_L11N_AD9N_49	E13	<<FPGA_IO_N_49	E13	29
IO_L12P_AD8P_49		<<FPGA_IO_P_49	F13	29
IO_L12N_AD8N_49		<<FPGA_IO_N_49	E13	29

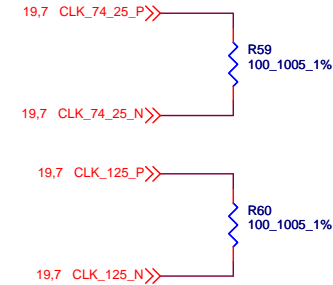
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<Bank-50>

IO_L1P_AD15P_50	J11	<<PMOD_A0	31	
IO_L1N_AD15N_50	J10	<<PMOD_A1	31	
IO_L2P_AD14P_50	H10	<<PMOD_A2	31	
IO_L2N_AD14N_50	G10	<<PMOD_A3	31	
IO_L3P_AD13P_50	F10	<<PMOD_A4	31	
IO_L3N_AD13N_50	E10	<<PMOD_A5	31	
IO_L4P_AD12P_50	D11	<<PMOD_A6	31	
IO_L4N_AD12N_50	H11	<<PL_DPAUX_OUT	33	
IO_L5P_HDGC_50	G11	<<PL_DP_HPDP	33	
IO_L5N_HDGC_50	F12	<<PL_DP_OE	33	
IO_L6P_HDGC_50	F11	<<PL_DPAUX_IN	33	
IO_L6N_HDGC_50	J12	<<PMOD_A7	31	
IO_L7P_HDGC_50	H12	<<UART_RXD_FPGA_TXD	25	
IO_L7N_HDGC_50	H13	<<UART_TXD_FPGA_RXD	25	
IO_L8P_HDGC_50	G13	<<FPGA_PL_RS232_TXD	31	
IO_L8N_HDGC_50	G15	<<FPGA_PL_RS232_RXD	31	
IO_L9P_AD11P_50	G14	<<PMOD_B0	31	
IO_L9N_AD11N_50	J14	<<PMOD_B1	31	
IO_L10P_AD10P_50	H14	<<PMOD_B2	31	
IO_L10N_AD10N_50	G16	<<PMOD_B3	31	
IO_L11P_AD9P_50	J16	<<PMOD_B4	31	
IO_L11N_AD9N_50	J15	<<PMOD_B5	31	
IO_L12P_AD8P_50		<<PMOD_B6	31	
IO_L12N_AD8N_50		<<PMOD_B7	31	

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<Bank-64>

IO_L1P_T0L_N0_DBC_64 AJ12 <<DDR4_BA1 16
 IO_L1N_T0L_N1_DBC_64 AK12 <<DDR4_BA0 16
 IO_L2P_T0L_N2_64 AL11 <<DDR4_A13 16
 IO_L2N_T0L_N3_64 AM11 <<DDR4_A12 16
 IO_L3P_T0L_N4_AD15P_64 AL10 <<DDR4_A11 16
 IO_L3N_T0L_N5_AD15N_64 AM10 <<DDR4_A10 16
 IO_L4P_T0U_N6_DBC_AD7P_64 AP11 <<DDR4_A9 16
 IO_L4N_T0U_N7_DBC_AD7N_64 AP10 <<DDR4_A8 16
 IO_L5P_T0U_N8_AD14P_64 AN9 <<DDR4_A7 16
 IO_L5N_T0U_N9_AD14N_64 AP9 <<DDR4_A6 16
 IO_L6P_T0U_N10_AD6P_64 AJ10 <<DDR4_A5 16
 IO_L6N_T0U_N11_AD6N_64 AK10 <<DDR4_A4 16
 IO_T0U_N12_VRP_64 AN11 <<VRP_64 8
 IO_T1U_N12_64 AJ7 <<DDR4_A14_WE_B 16
 IO_L7P_T1L_N0_QBC_AD13P_64 AN8 <<DDR4_A3 16
 IO_L7N_T1L_N1_QBC_AD13N_64 AP8 <<DDR4_A2 16
 IO_L8P_T1L_N2_AD5P_64 AM9 <<DDR4_A1 16
 IO_L8N_T1L_N3_AD5N_64 AM8 <<DDR4_A0 16
 IO_L9P_T1L_N4_AD12P_64 AJ9 <<DDR4_A16_RAS_B 16
 IO_L9N_T1L_N5_AD12N_64 AK9 <<DDR4_ODT 16
 IO_L10P_T1U_N6_QBC_AD4P_64 AN7 <<DDR4_CK_T 16
 IO_L10N_T1U_N7_QBC_AD4N_64 AP7 <<DDR4_CK_C 16
 IO_L11P_T1U_N8_GC_64 AK8 <<DDR4_ACT_B 16
 IO_L11N_T1U_N9_GC_64 AL7 <<DDR4_BG0 16
 IO_L12P_T1U_N10_GC_64 AL8 <<DDR4_CLK_P 21,8
 IO_L12N_T1U_N11_GC_64 AL7 <<DDR4_CLK_N 21,8
 IO_L13P_T2L_N0_GC_QBC_64 AL6 <<DDR4_DM0 16
 IO_L13N_T2L_N1_GC_QBC_64 AL5 <<DDR4_A15_CAS_B 16
 IO_L14P_T2L_N2_GC_64 AM6 <<DDR4_DQ7 16
 IO_L14N_T2L_N3_GC_64 AP5 <<DDR4_DQ6 16
 IO_L15P_T2L_N4_AD11P_64 AP4 <<DDR4_DQ5 16
 IO_L15N_T2L_N5_AD11N_64 AN6 <<DDR4_DQ4 16
 IO_L16P_T2U_N6_QBC_AD3P_64 AP6 <<DDR4_DQS0_T 16
 IO_L16N_T2U_N7_QBC_AD3N_64 AM4 <<DDR4_DQS0_C 16
 IO_L17P_T2U_N8_AD10P_64 AN4 <<DDR4_DQ2 16
 IO_L17N_T2U_N9_AD10N_64 AK5 <<DDR4_DQ1 16
 IO_L18P_T2U_N10_AD2P_64 AK4 <<DDR4_DQ0 16
 IO_L18N_T2U_N11_AD2N_64 AM3 <<DDR4_CKE 16
 IO_T2U_N12_64 AP1 <<DDR4_PAR 16
 IO_T3U_N12_64 AN2 <<DDR4_DM1 16
 IO_L19P_T3L_N0_DBC_AD9P_64 AP2 <<DDR4_CS_B 16
 IO_L19N_T3L_N1_DBC_AD9N_64 AN3 <<DDR4_DQ15 16
 IO_L20P_T3L_N2_AD1P_64 AP3 <<DDR4_DQ14 16
 IO_L20N_T3L_N3_AD1N_64 AM1 <<DDR4_DQ13 16
 IO_L21P_T3L_N4_AD8P_64 AN1 <<DDR4_DQ12 16
 IO_L21N_T3L_N5_AD8N_64 AL3 <<DDR4_DQS1_T 16
 IO_L22P_T3U_N6_DBC_AD0P_64 AL2 <<DDR4_DQS1_C 16
 IO_L22N_T3U_N7_DBC_AD0N_64 AK1 <<DDR4_DQ11 16
 IO_L23P_T3U_N8_64 AL1 <<DDR4_DQ10 16
 IO_L23N_T3U_N9_64 AK3 <<DDR4_DQ9 16
 IO_L24P_T3U_N10_64 AK2 <<DDR4_DQ8 16
 IO_L24N_T3U_N11_64 AJ11 <<DDR4_DQ8 16
 VREF_64

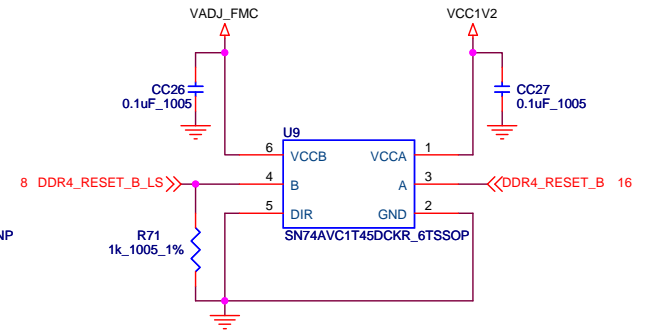
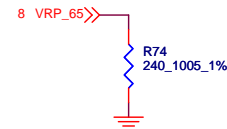
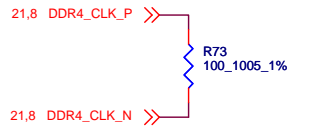
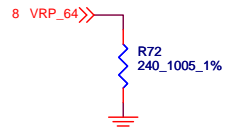
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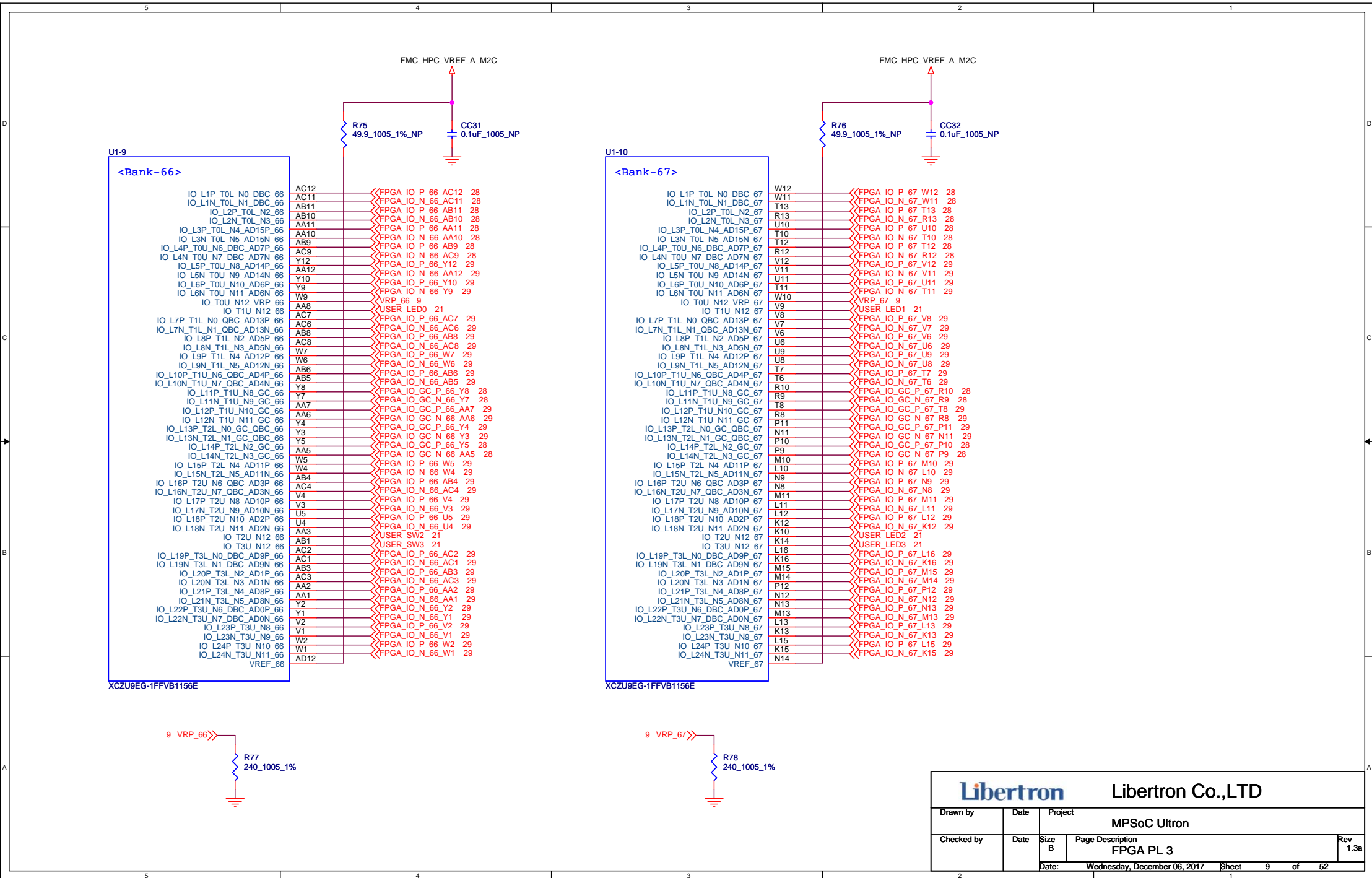
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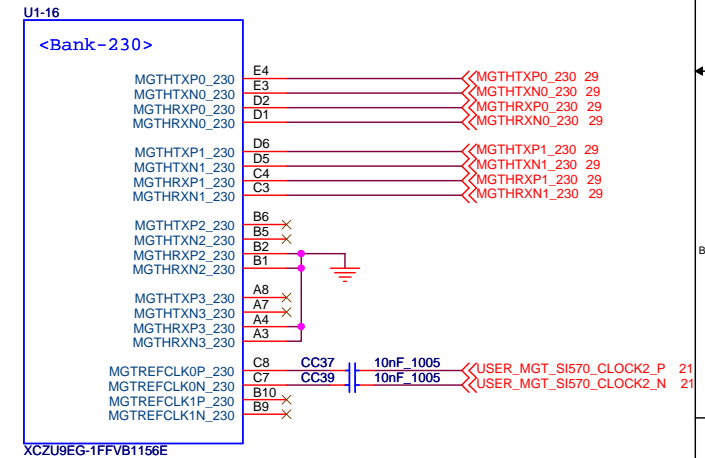
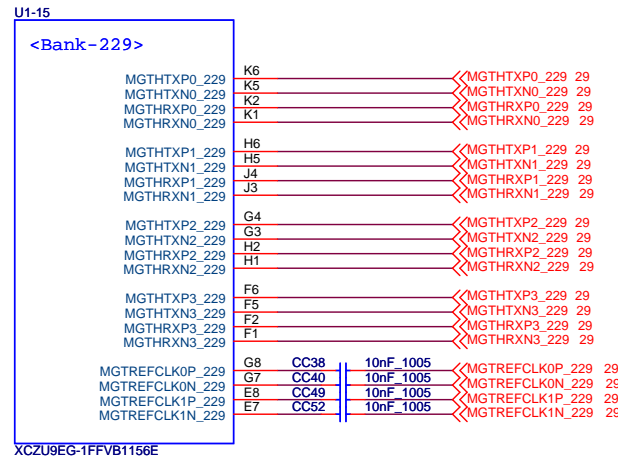
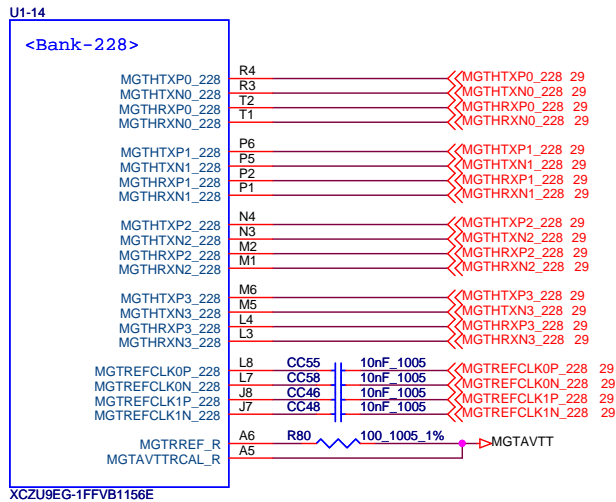
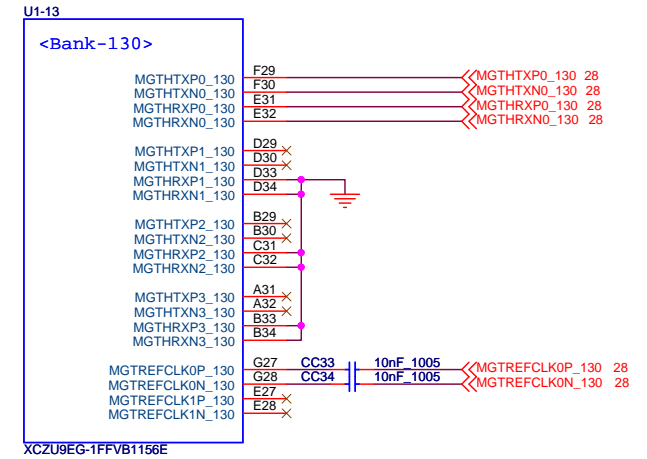
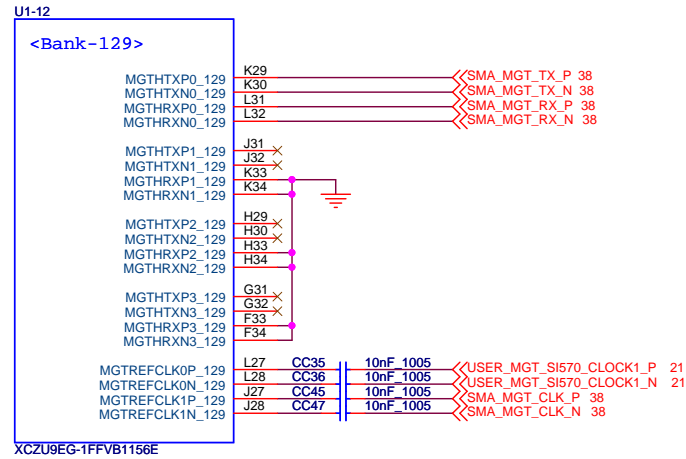
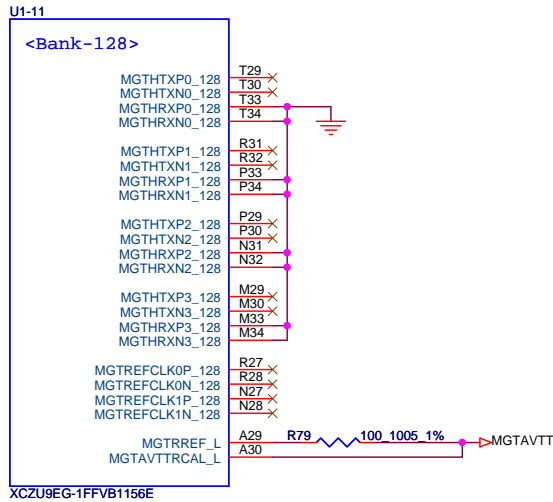
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 IO_L1N_T0L_N1_DBC_65 AF10 <<FPGA_IO_N_65_AF10 28
 IO_L2P_T0L_N2_65 AH12 <<FPGA_IO_P_65_AH12 28
 IO_L2N_T0L_N3_65 AH11 <<FPGA_IO_N_65_AH11 28
 IO_L3P_T0L_N4_AD15P_65 AE12 <<FPGA_IO_P_65_AE12 28
 IO_L3N_T0L_N5_AD15N_65 AF12 <<FPGA_IO_N_65_AF12 28
 IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65 AF11 <<FPGA_IO_P_65_AF11 28
 IO_L4N_T0U_N7_DBC_AD7N_65 AG11 <<FPGA_IO_N_65_AG11 28
 IO_L5P_T0U_N8_AD14P_65 AG9 <<FPGA_IO_P_65_AG10 28
 IO_L5N_T0U_N9_AD14N_65 AD10 <<FPGA_IO_N_65_AD10 28
 IO_L6P_T0U_N10_AD6P_65 AE9 <<FPGA_IO_N_65_AE9 28
 IO_L6N_T0U_N11_AD6N_65 AD9 <<VRP_65 8
 IO_T0U_N12_VRP_65 AH9 <<DDR4_RESET_B_LS 8
 IO_T1U_N12_65 AH7 <<FPGA_IO_P_65_AH7 28
 IO_L7P_T1L_N0_QBC_AD13P_65 AH6 <<FPGA_IO_N_65_AH6 28
 IO_L7N_T1L_N1_QBC_AD13N_65 AG8 <<FPGA_IO_P_65_AG8 28
 IO_L8P_T1L_N2_AD5P_65 AH8 <<FPGA_IO_N_65_AH8 28
 IO_L8N_T1L_N3_AD5N_65 AD7 <<FPGA_IO_P_65_AD7 28
 IO_L9P_T1L_N4_AD12P_65 AD6 <<FPGA_IO_N_65_AD6 28
 IO_L9N_T1L_N5_AD12N_65 AE8 <<FPGA_IO_P_65_AE8 28
 IO_L10P_T1U_N6_QBC_AD4P_65 AF8 <<FPGA_IO_N_65_AF8 28
 IO_L10N_T1U_N7_QBC_AD4N_65 AF6 <<FPGA_IO_GC_P_65_AF6 28
 IO_L11P_T1U_N8_GC_65 AG6 <<FPGA_IO_GC_N_65_AG6 28
 IO_L11N_T1U_N9_GC_65 AE7 <<FPGA_IO_GC_P_65_AE7 28
 IO_L12P_T1U_N10_GC_65 AF7 <<FPGA_IO_GC_N_65_AF7 28
 IO_L12N_T1U_N11_GC_65 AE5 <<FPGA_IO_GC_P_65_AE5 28
 IO_L13P_T2L_N0_GC_QBC_65 AF5 <<FPGA_IO_GC_N_65_AF5 28
 IO_L13N_T2L_N1_GC_QBC_65 AG5 <<FPGA_IO_GC_P_65_AG5 28
 IO_L14P_T2L_N2_GC_65 AG4 <<FPGA_IO_GC_N_65_AG4 28
 IO_L14N_T2L_N3_GC_65 AH4 <<FPGA_IO_P_65_AH4 28
 IO_L15P_T2L_N4_AD11P_65 AJ4 <<FPGA_IO_N_65_AJ4 28
 IO_L15N_T2L_N5_AD11N_65 AJ6 <<FPGA_IO_P_65_AJ6 28
 IO_L16P_T2U_N6_QBC_AD3P_65 AJ5 <<FPGA_IO_N_65_AJ5 28
 IO_L16N_T2U_N7_QBC_AD3N_65 AE3 <<FPGA_IO_P_65_AE3 28
 IO_L17P_T2U_N8_AD10P_65 AF3 <<FPGA_IO_N_65_AF3 28
 IO_L17N_T2U_N9_AD10N_65 AD4 <<FPGA_IO_P_65_AD4 28
 IO_L18P_T2U_N10_AD2P_65 AE4 <<FPGA_IO_N_65_AE4 28
 IO_L18N_T2U_N11_AD2N_65 AD5 <<USER_SW0 21
 IO_T2U_N12_65 AG1 <<USER_SW1 21
 IO_T3U_N12_65 AH2 <<FPGA_IO_P_65_AH2 28
 IO_L19P_T3L_N0_DBC_AD9P_65 AJ2 <<FPGA_IO_N_65_AJ2 28
 IO_L19N_T3L_N1_DBC_AD9N_65 AG3 <<FPGA_IO_P_65_AG3 28
 IO_L20P_T3L_N2_AD1P_65 AH3 <<FPGA_IO_N_65_AH3 28
 IO_L20N_T3L_N3_AD1N_65 AF2 <<FPGA_IO_P_65_AF2 28
 IO_L21P_T3L_N4_AD8P_65 AF1 <<FPGA_IO_N_65_AF1 28
 IO_L21N_T3L_N5_AD8N_65 AH1 <<FPGA_IO_P_65_AH1 28
 IO_L22P_T3U_N6_DBC_AD0P_65 AJ1 <<FPGA_IO_N_65_AJ1 28
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 IO_L23P_T3U_N8_I2C_SCLK_65 AD1 <<FPGA_IO_N_65_AD1 28
 IO_L23N_T3U_N9_65 AE2 <<FPGA_IO_P_65_AE2 28
 IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65 AE1 <<FPGA_IO_N_65_AE1 28
 IO_L24N_T3U_N11_PERSTN0_65 AD11 <<FPGA_IO_N_65_AE1 28
 VREF_65

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<Bank-500>

PS_MIO0	AF16	<<MIO0_QSPI_LWR_CLK	20
PS_MIO1	AJ16	<<MIO1_QSPI_LWR_DQ1	20
PS_MIO2	AD16	<<MIO2_QSPI_LWR_DQ2	20
PS_MIO3	AG16	<<MIO3_QSPI_LWR_DQ3	20
PS_MIO4	AH16	<<MIO4_QSPI_LWR_CS_B	20
PS_MIO5	AM15	<<MIO5_QSPI_LWR_CS_B	20
PS_MIO6	AL15	<<MIO6_QSPI_LWR_CS_B	20
PS_MIO7	AD17	<<MIO7_QSPI_UPR_CS_B	20
PS_MIO8	AE17	<<MIO8_QSPI_UPR_DQ0	20
PS_MIO9	AP15	<<MIO9_QSPI_UPR_DQ1	20
PS_MIO10	AH17	<<MIO10_QSPI_UPR_DQ2	20
PS_MIO11	AF17	<<MIO11_QSPI_UPR_DQ3	20
PS_MIO12	AJ17	<<MIO12_QSPI_UPR_CLK	20
PS_MIO13	AK17	<<MIO13_PS_GPIO2	26
PS_MIO14	AL16	<<MIO14_I2C0_SCL	22
PS_MIO15	AN16	<<MIO15_I2C0_SDA	22
PS_MIO16	AM16	<<MIO16_I2C1_SCL	23
PS_MIO17	AP16	<<MIO17_I2C1_SDA	23
PS_MIO18	AE18	<<MIO18_UART0_RXD	25
PS_MIO19	AL17	<<MIO19_UART0_TXD	25
PS_MIO20	AD18	<<MIO20_38	
PS_MIO21	AF18	<<MIO21_38	
PS_MIO22	AD20	<<MIO22_38	
PS_MIO23	AD19	<<MIO23_38	
PS_MIO24	AE20	<<MIO24_CAN_TX	38
PS_MIO25	AE19	<<MIO25_CAN_RX	38

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<Bank-501>

PS_MIO26	P21	<<MIO26_PMU_INPUT	22
PS_MIO27	M21	<<MIO27_DP_AUX_OUT	33
PS_MIO28	N21	<<MIO28_DP_HP0	33
PS_MIO29	K22	<<MIO29_DP_OE	33
PS_MIO30	L21	<<MIO30_DP_AUX_IN	33
PS_MIO31	J22	<<MIO31_PCIE_RESET_N	34
PS_MIO32	H22	<<MIO32_PMU_GPO0	26
PS_MIO33	L23	<<MIO33_PMU_GPO1	26
PS_MIO34	L22	<<MIO34_PMU_GPO2	26
PS_MIO35	P22	<<MIO35_PMU_GPO3	26
PS_MIO36	K23	<<MIO36_PMU_GPO4	26
PS_MIO37	N22	<<MIO37_PMU_GPO5	26
PS_MIO38	L23	<<MIO38_PS_GPIO1	26
PS_MIO39	N23	<<MIO39_PS_GPIO2	26
PS_MIO40	M23	<<MIO40_PS_GPIO3	26
PS_MIO41	J24	<<MIO41_PS_GPIO4	26
PS_MIO42	M24	<<MIO42_PS_GPIO5	26
PS_MIO43	K24	<<MIO43_PS_GPIO6	26
PS_MIO44	N24	<<MIO44_SDIO_PROTECT	20
PS_MIO45	P24	<<MIO45_SDIO_DETECT	20
PS_MIO46	R48	<<MIO46_SDIO_DAT0	20
PS_MIO47	R50	<<MIO47_SDIO_DAT1	20
PS_MIO48	M25	<<MIO48_SDIO_DAT2	20
PS_MIO49	K25	<<MIO49_SDIO_DAT3	20
PS_MIO50	P25	<<MIO50_SDIO_CMD	20
PS_MIO51	N25	<<MIO51_SDIO_CLK	20

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<Bank-502>

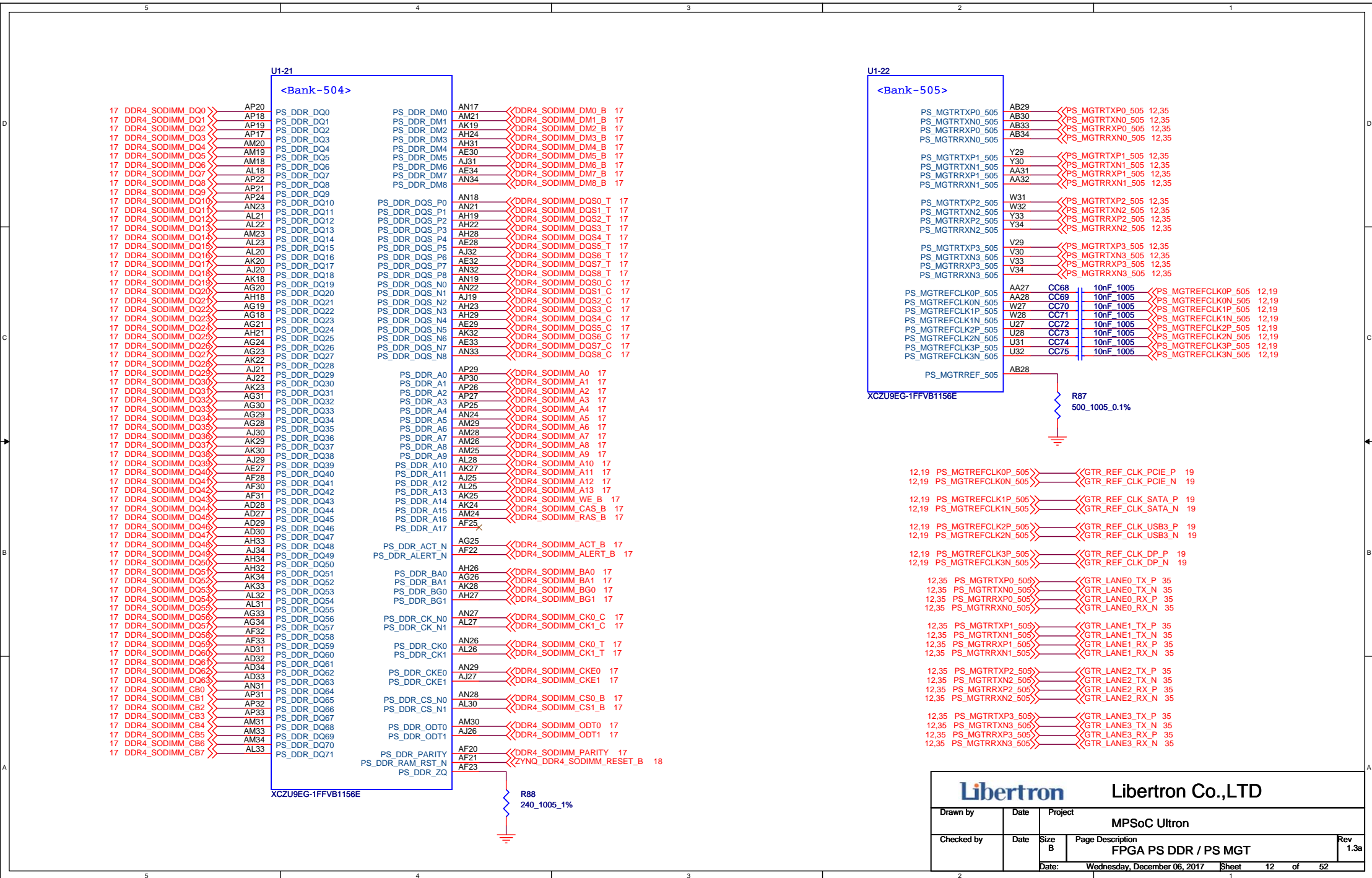
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PS_MIO53	E23	<<MIO53_USB_DIR	36
PS_MIO54	F23	<<MIO54_USB_DATA2	36
PS_MIO55	B23	<<MIO55_USB_NXT	36
PS_MIO56	C23	<<MIO56_USB_DATA0	36
PS_MIO57	A23	<<MIO57_USB_DATA1	36
PS_MIO58	G23	<<MIO58_USB_STP	36
PS_MIO59	B24	<<MIO59_USB_DATA3	36
PS_MIO60	E24	<<MIO60_USB_DATA4	36
PS_MIO61	C24	<<MIO61_USB_DATA5	36
PS_MIO62	G24	<<MIO62_USB_DATA6	36
PS_MIO63	D24	<<MIO63_USB_DATA7	36
PS_MIO64	A25	<<MIO64_ENET_TX_CLK	27
PS_MIO65	A26	<<MIO65_ENET_TX_D0	27
PS_MIO66	A27	<<MIO66_ENET_TX_D1	27
PS_MIO67	B25	<<MIO67_ENET_TX_D2	27
PS_MIO68	B26	<<MIO68_ENET_TX_D3	27
PS_MIO69	B27	<<MIO69_ENET_TX_CTRL	27
PS_MIO70	C26	<<MIO70_ENET_RX_CLK	27
PS_MIO71	C27	<<MIO71_ENET_RX_D0	27
PS_MIO72	E25	<<MIO72_ENET_RX_D1	27
PS_MIO73	H24	<<MIO73_ENET_RX_D2	27
PS_MIO74	G25	<<MIO74_ENET_RX_D3	27
PS_MIO75	D25	<<MIO75_ENET_RX_CTRL	27
PS_MIO76	H25	<<MIO76_ENET_MDC	27
PS_MIO77	F25	<<MIO77_ENET_MDIO	27

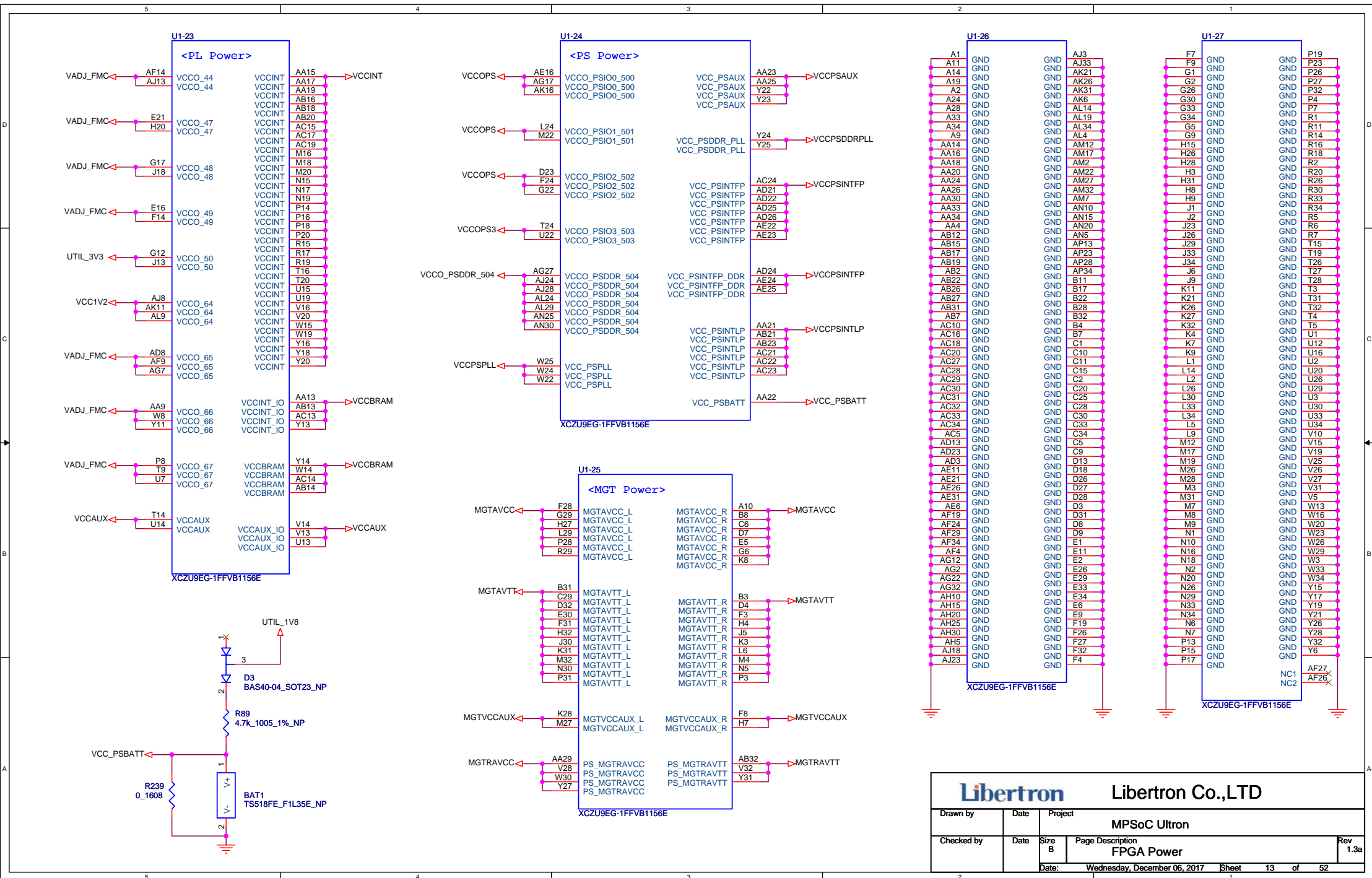
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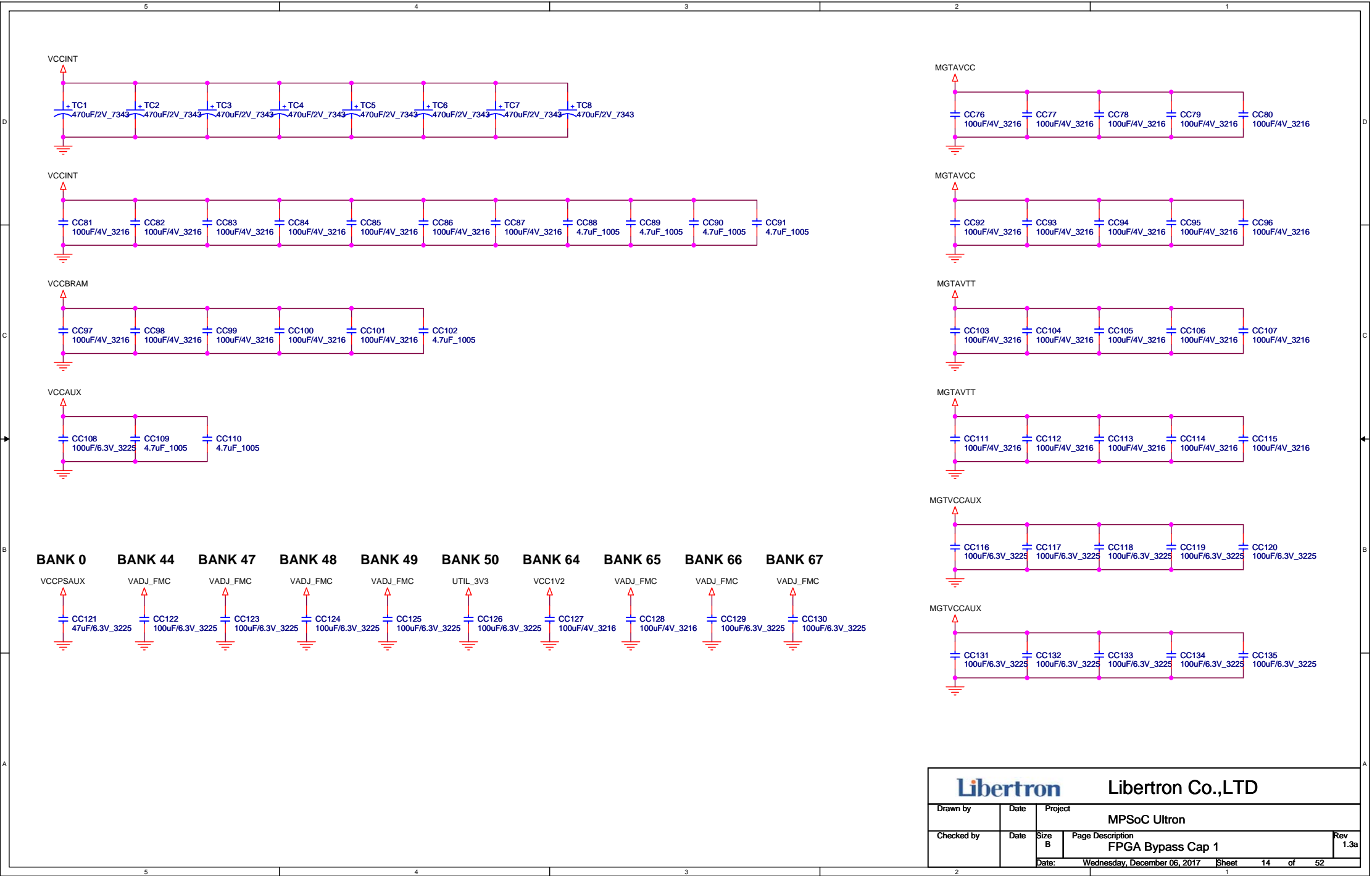
Libertron

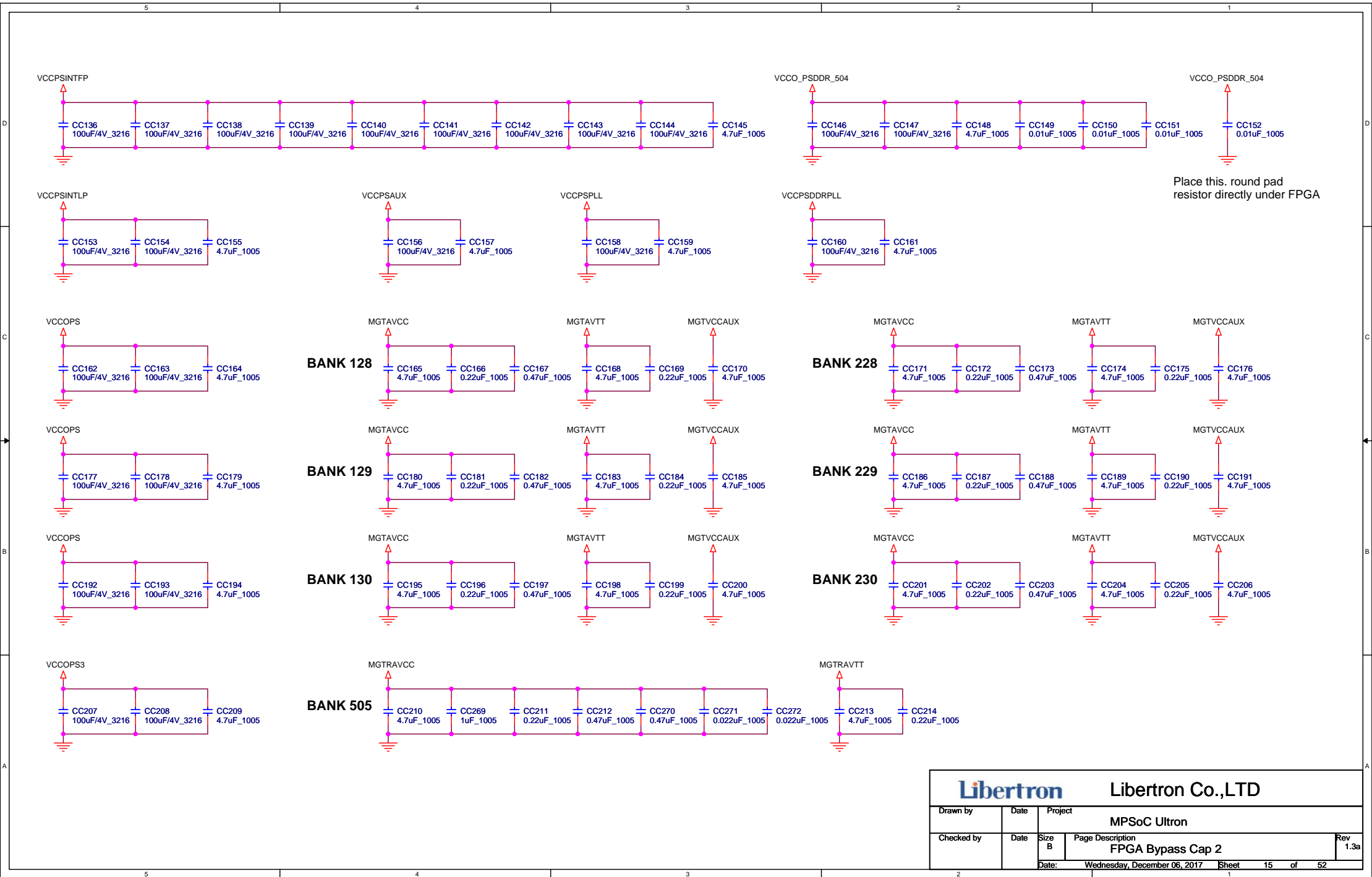
Libertron Co.,LTD

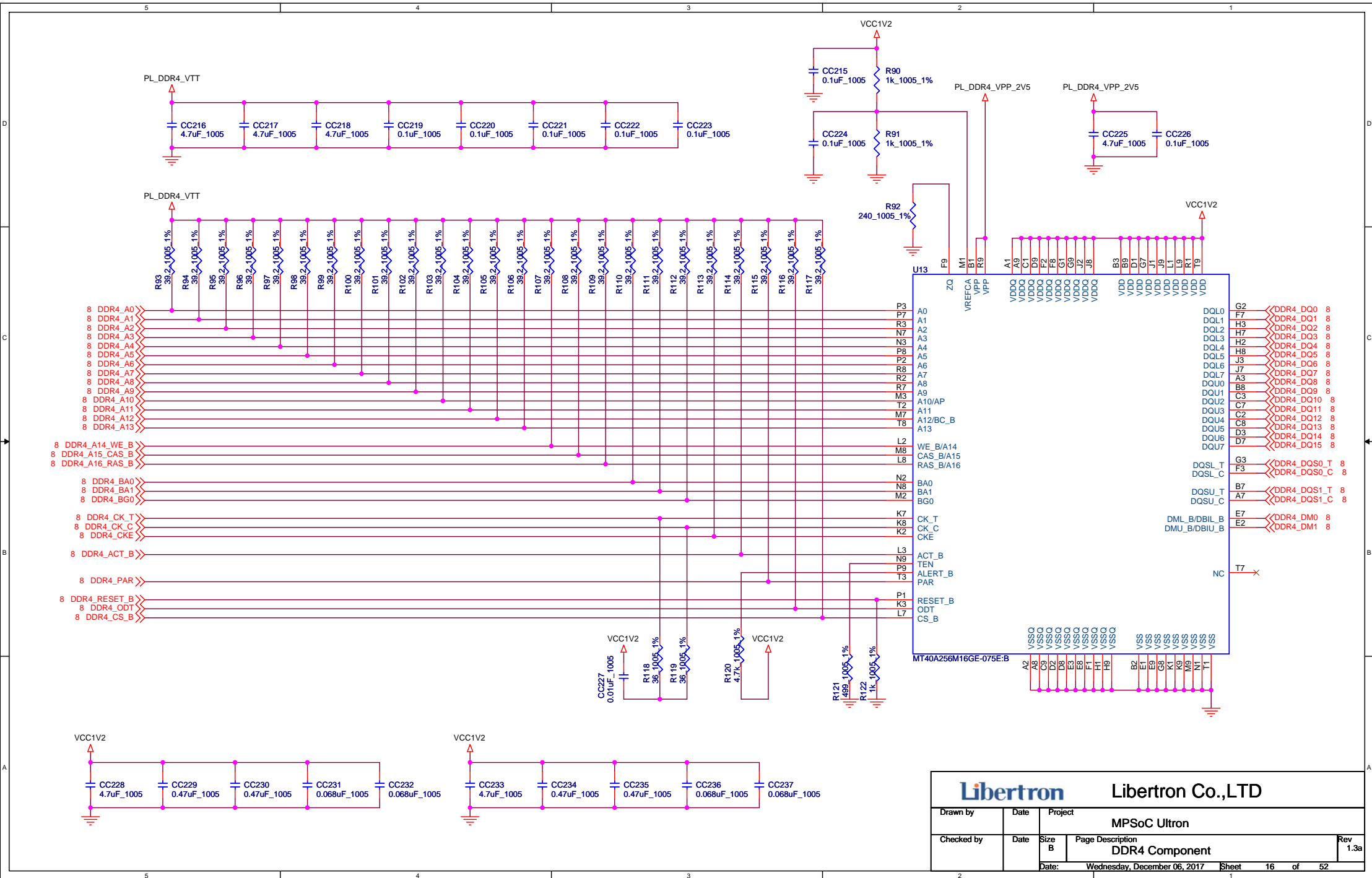
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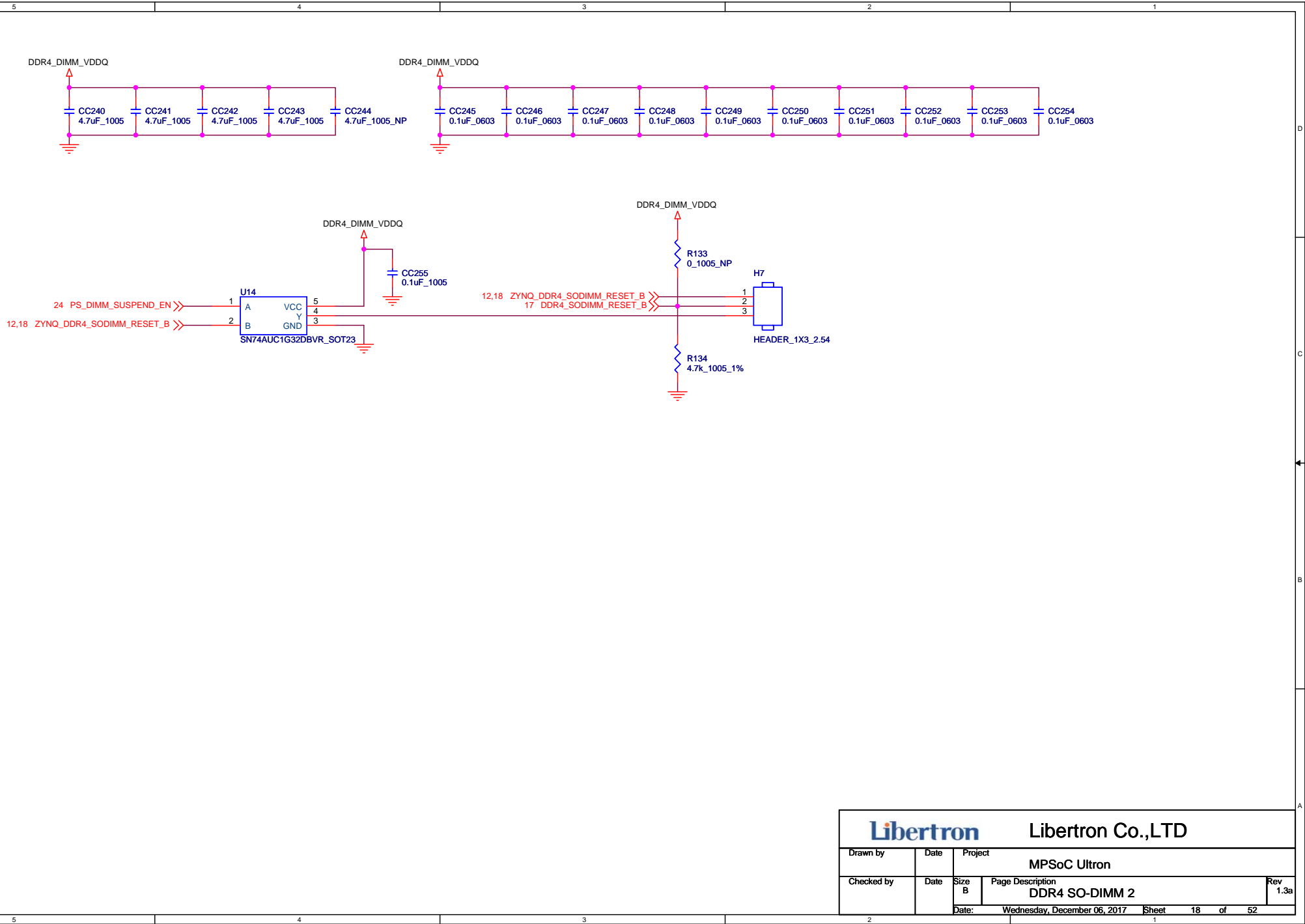


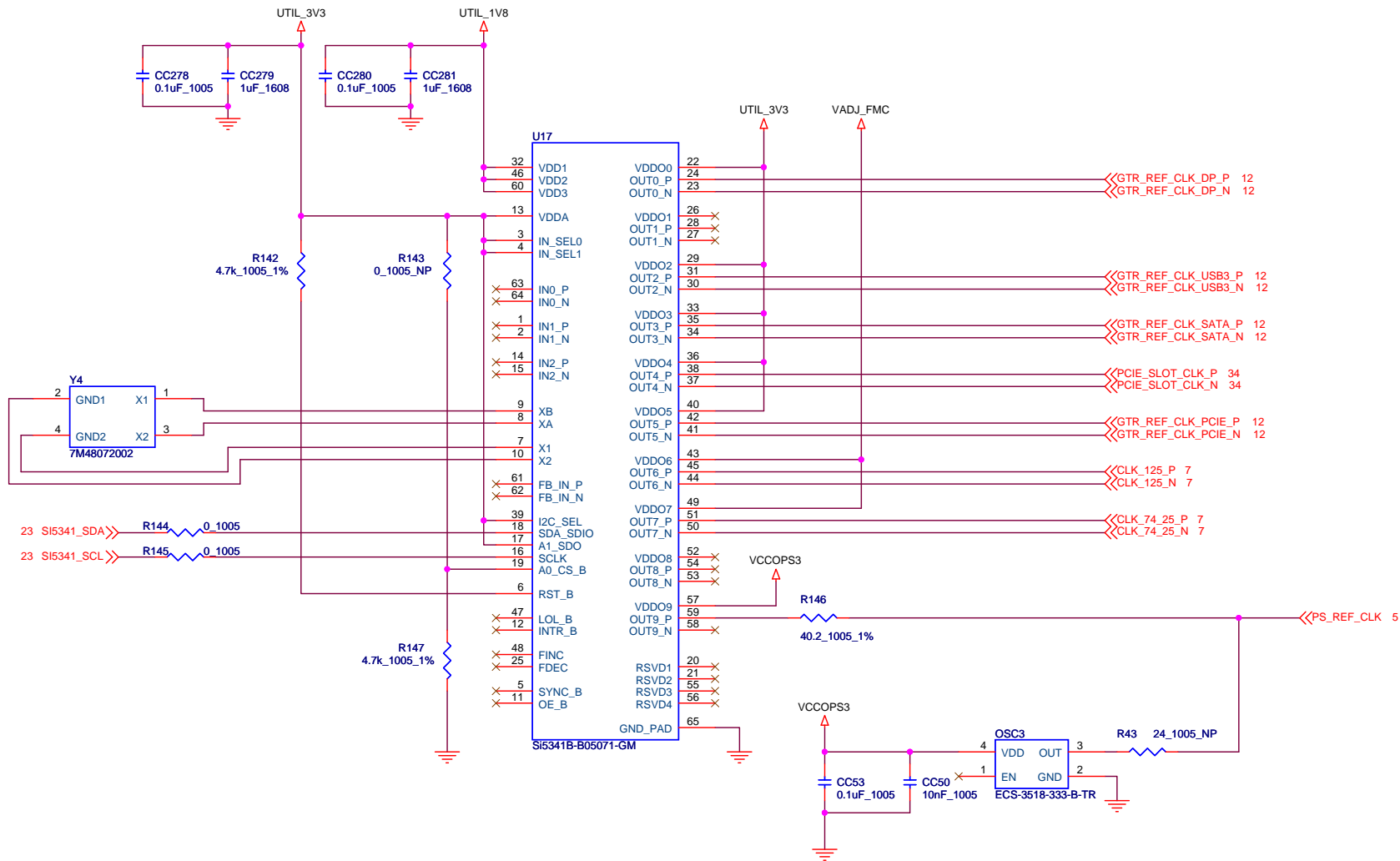




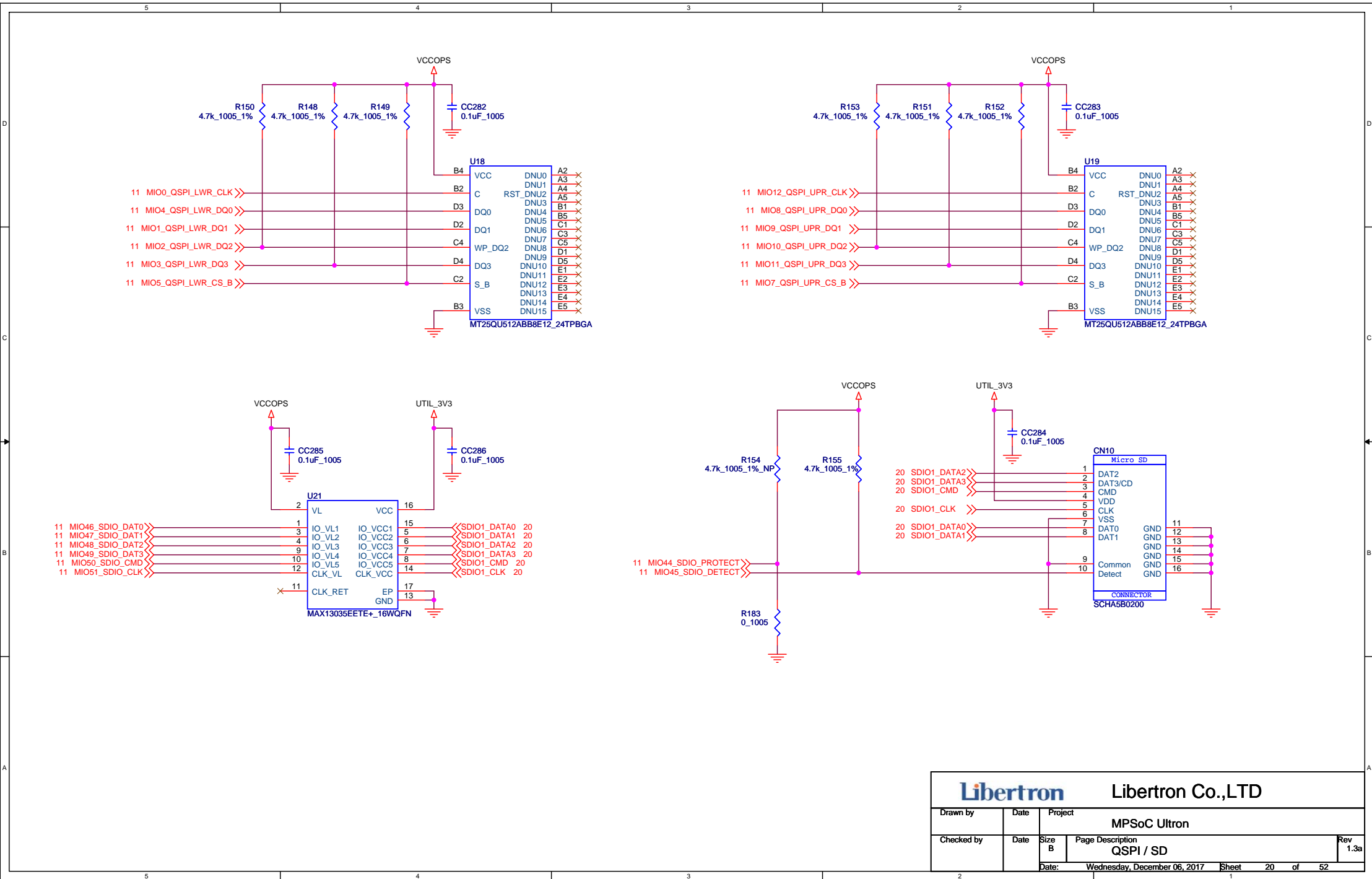


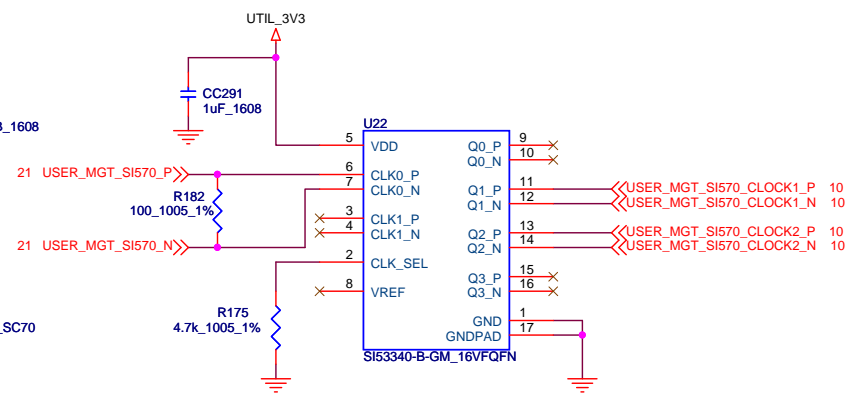
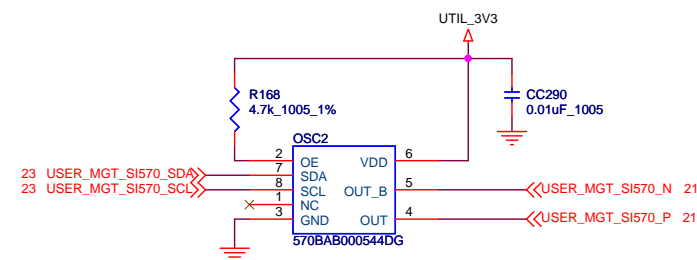
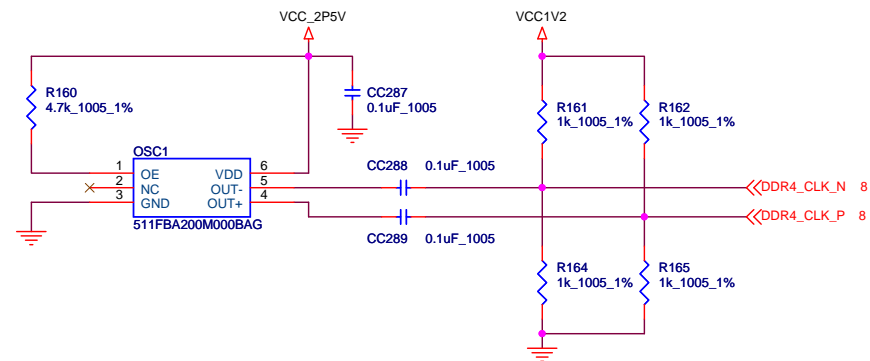
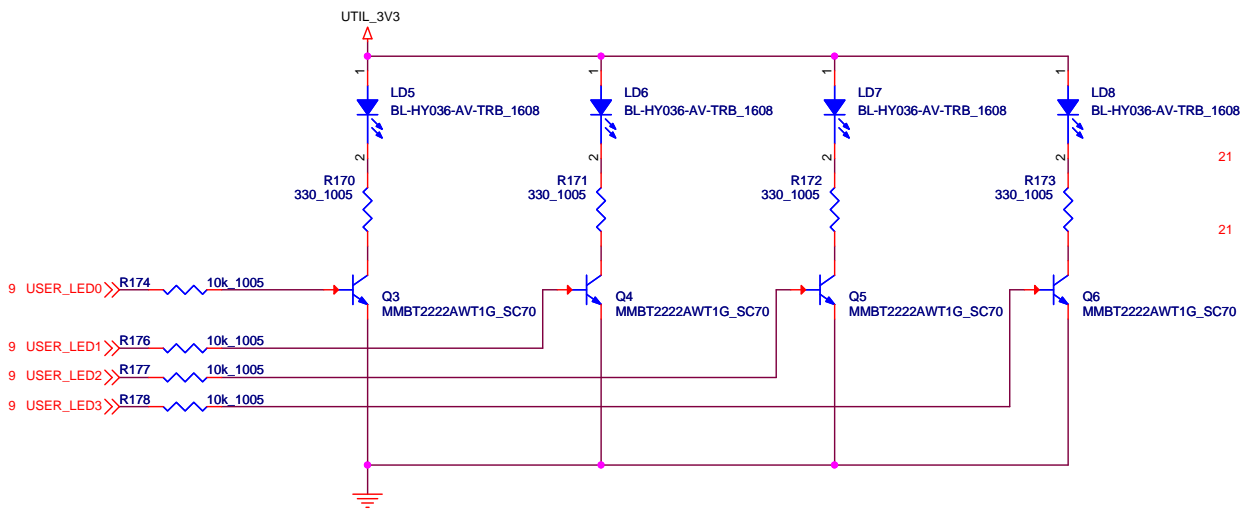
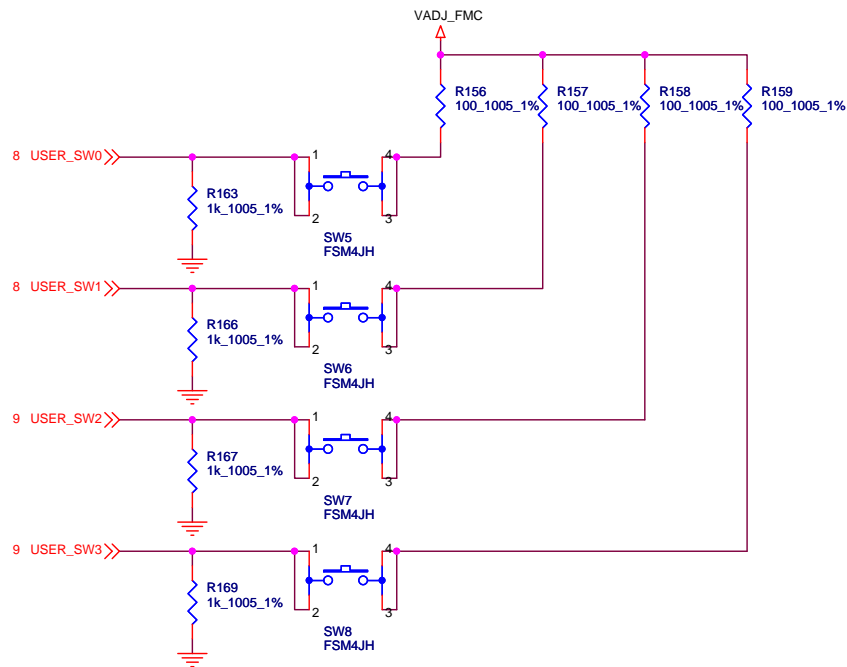




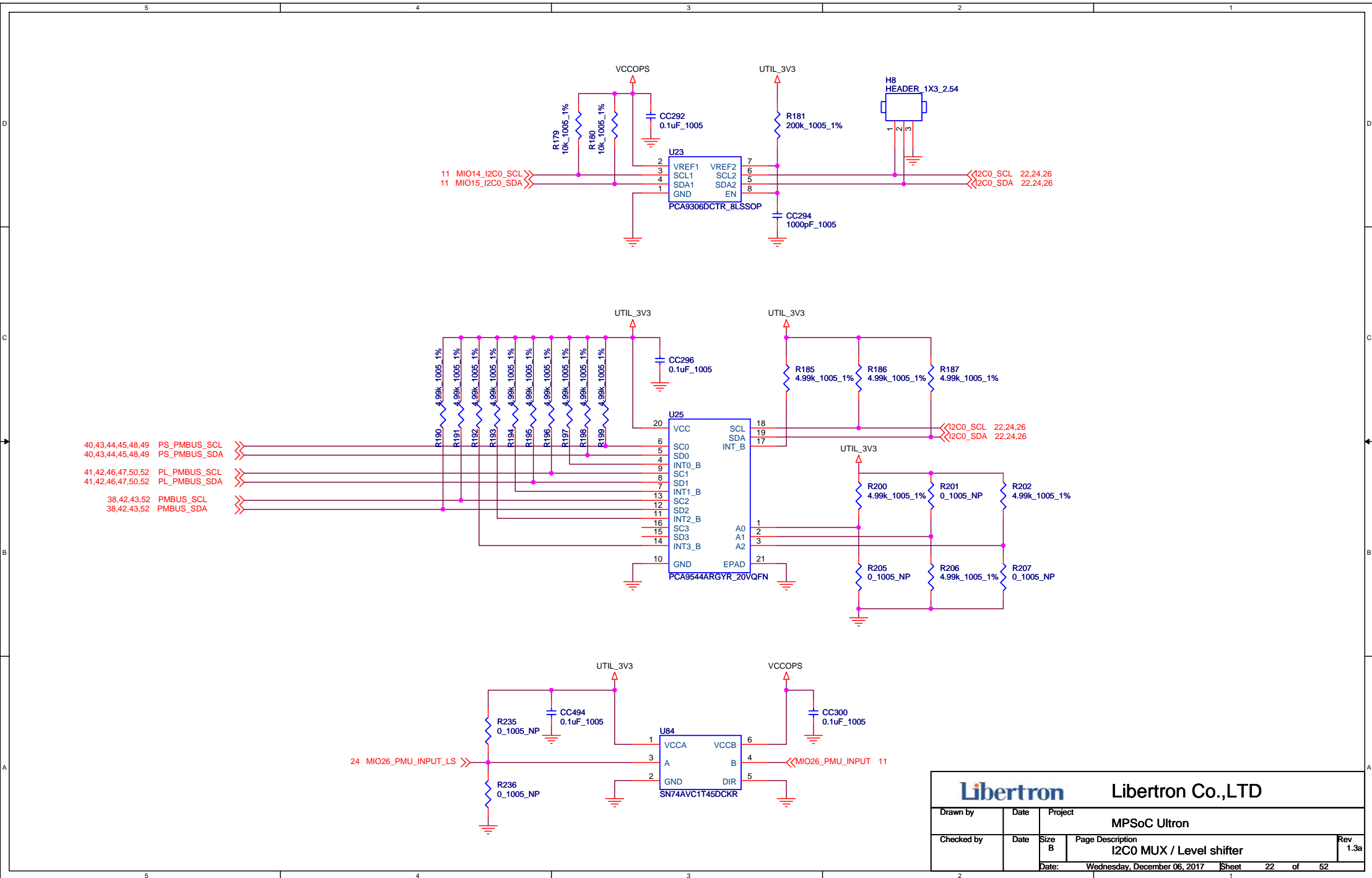


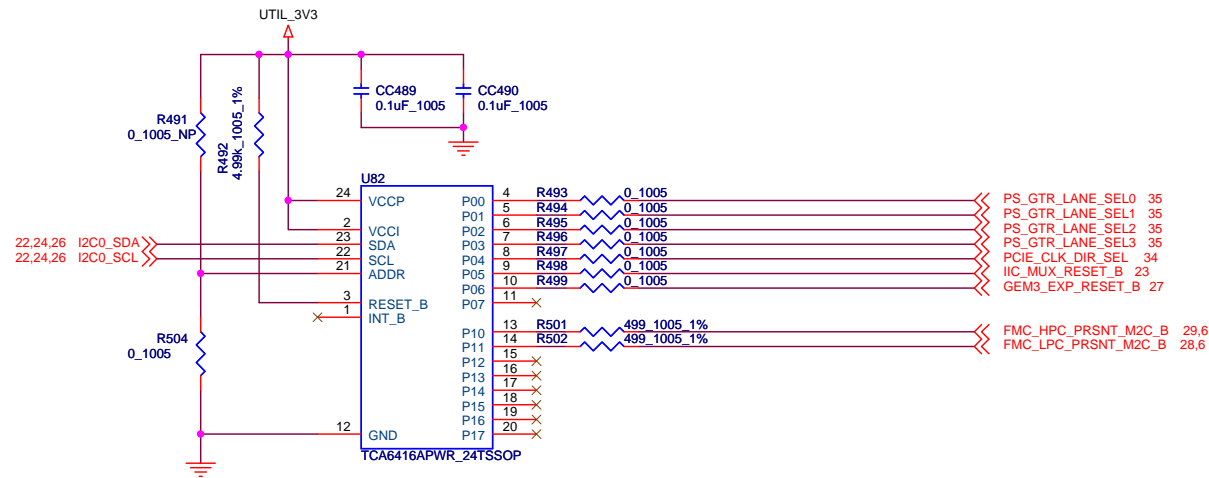
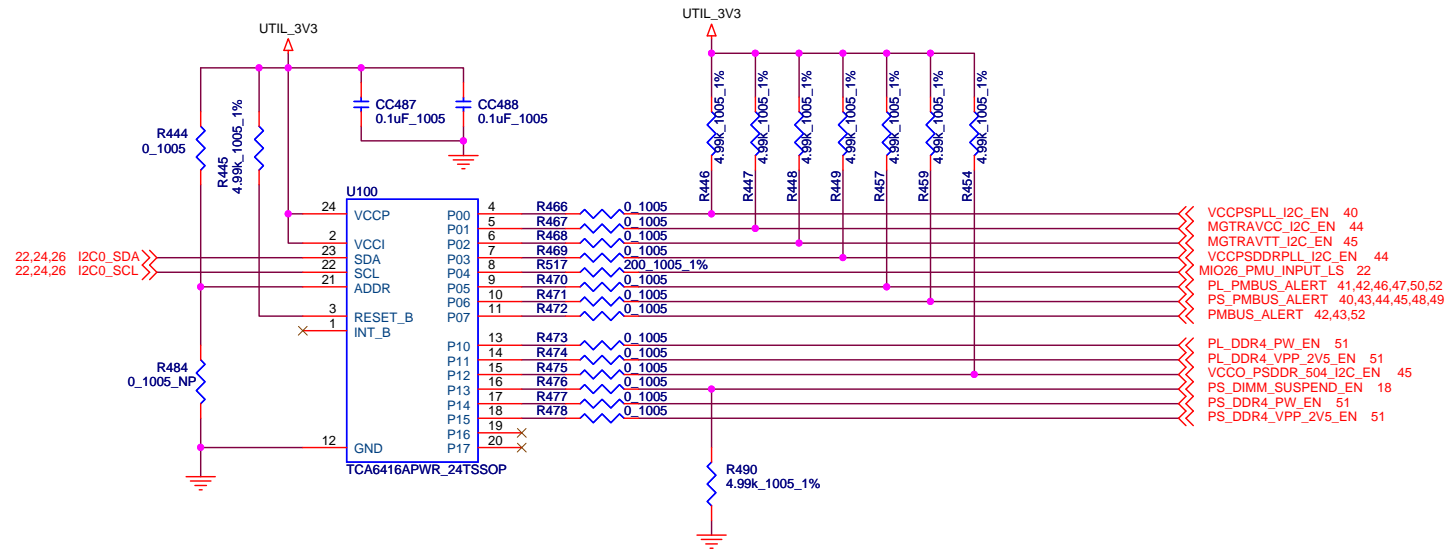
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		MPSoC Ultron		
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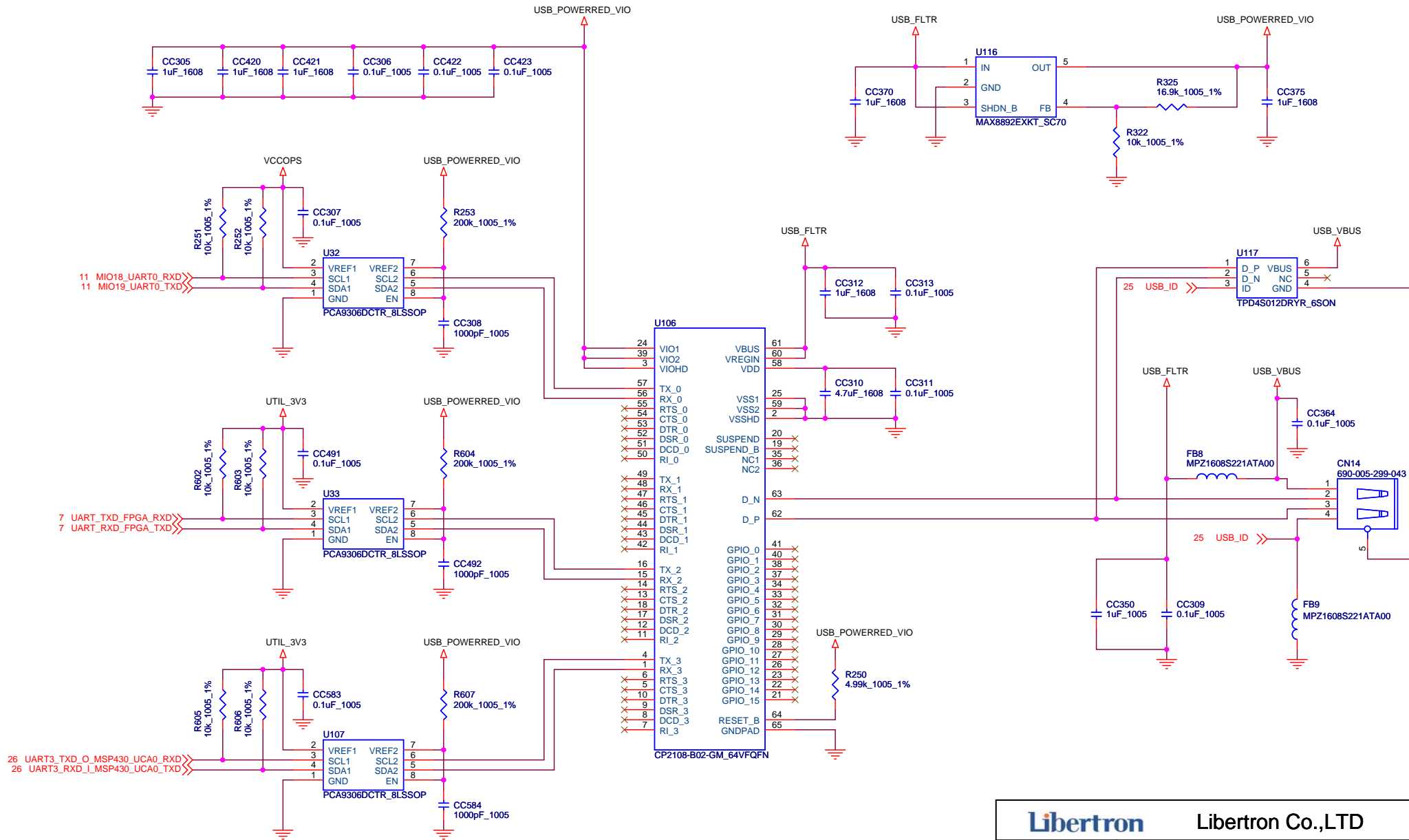




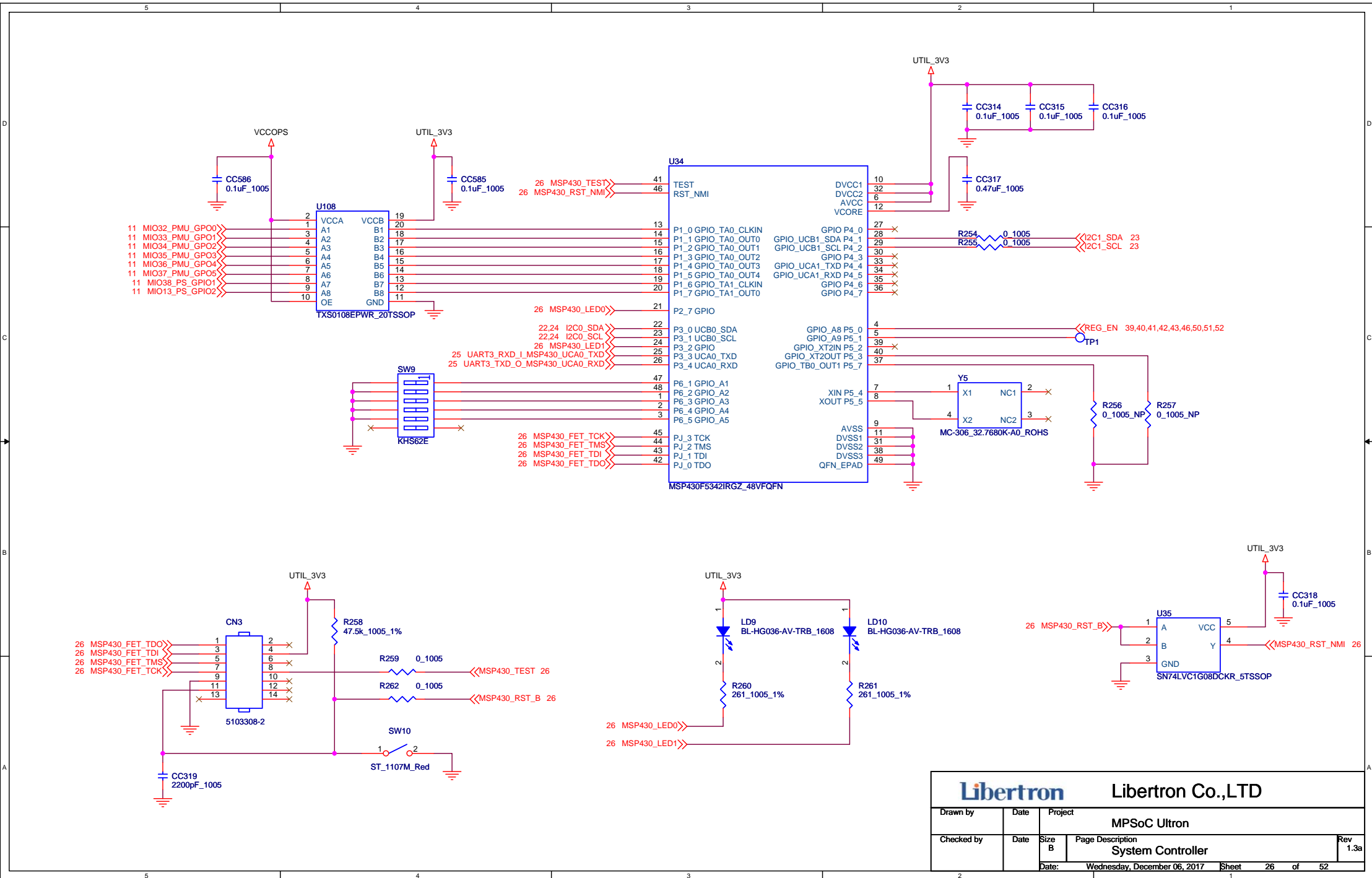
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		MPSoC Ultron	
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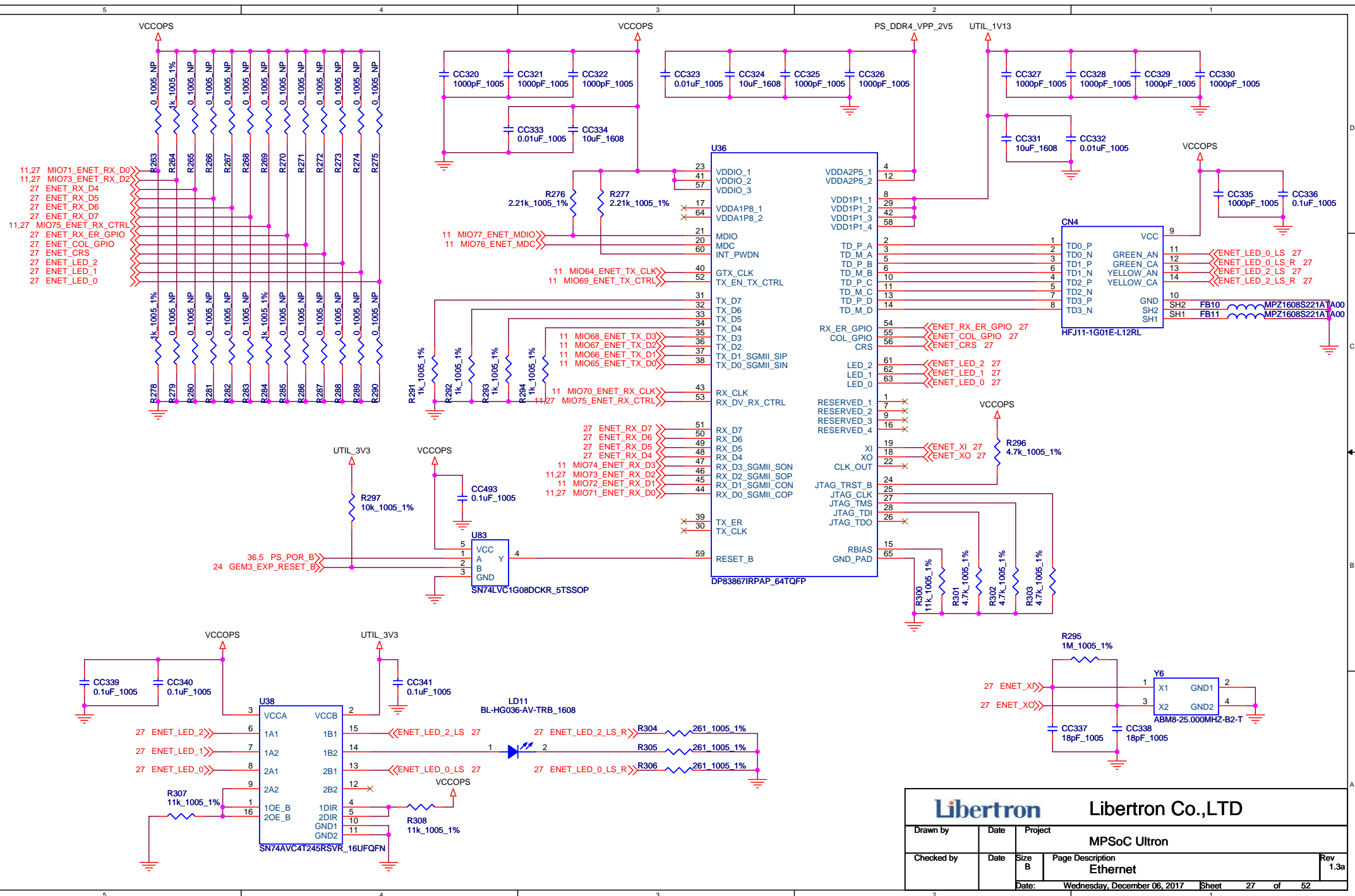


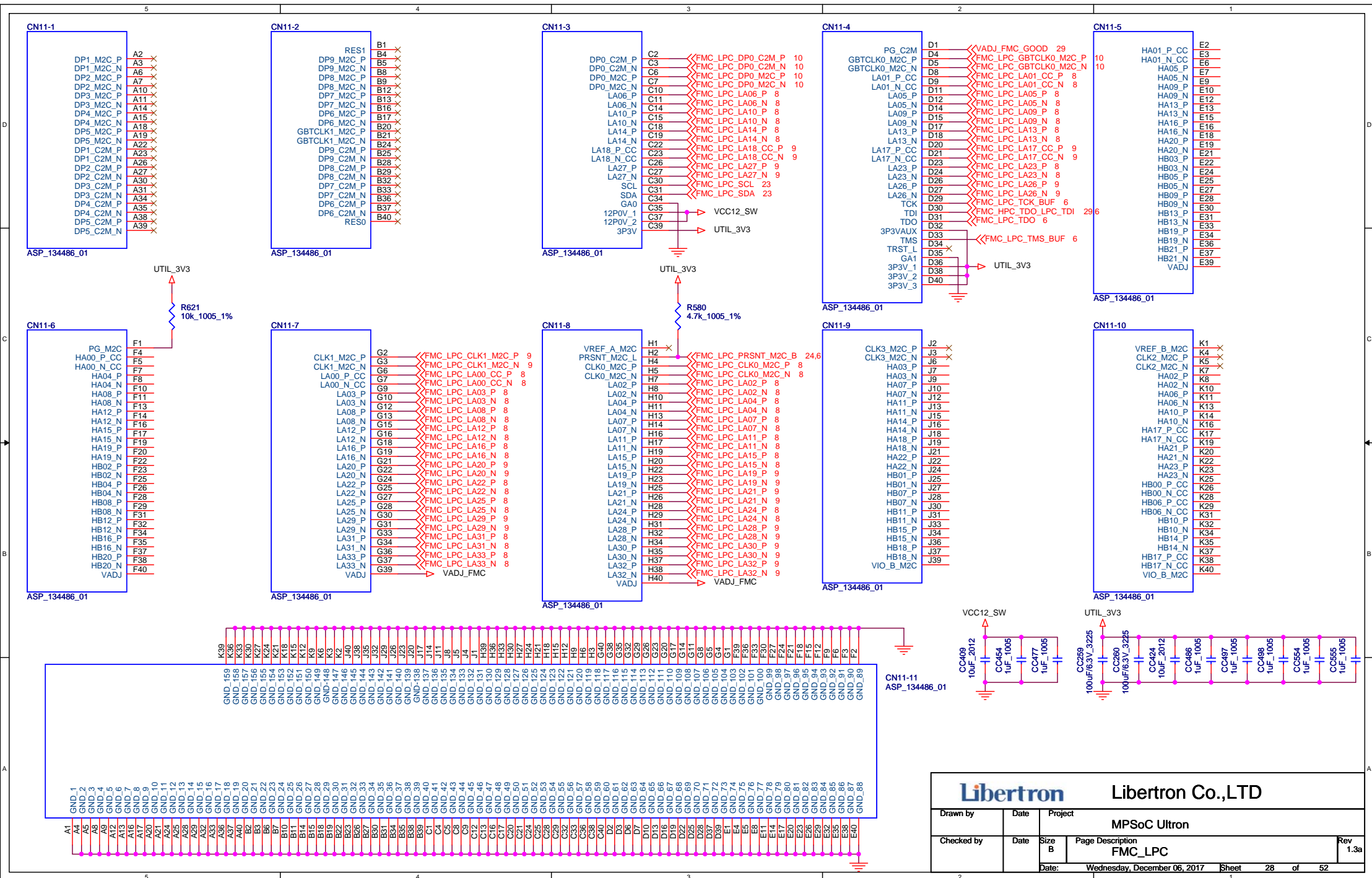


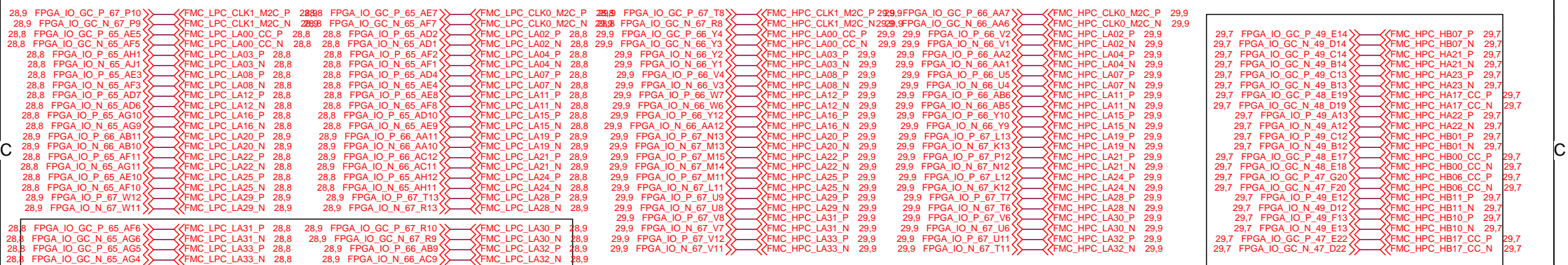
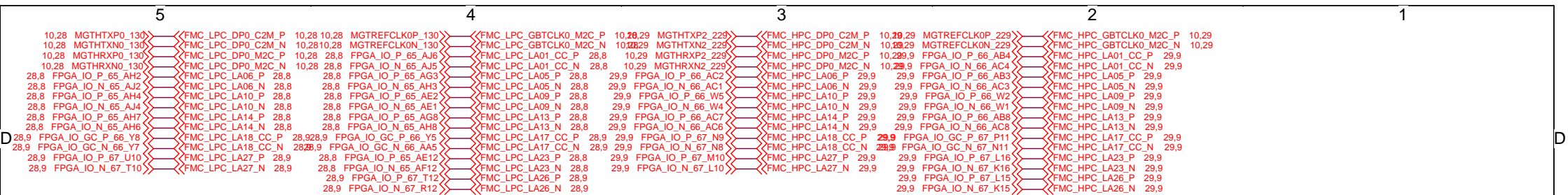


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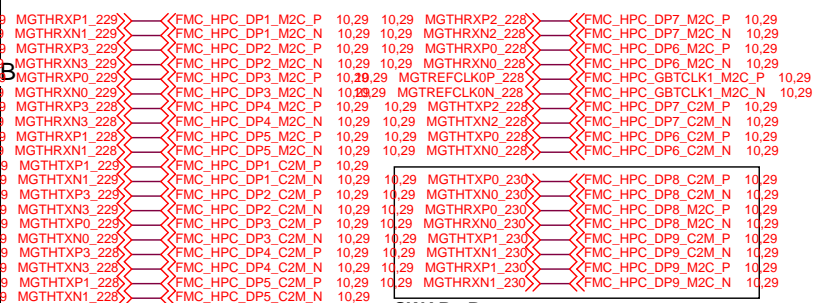




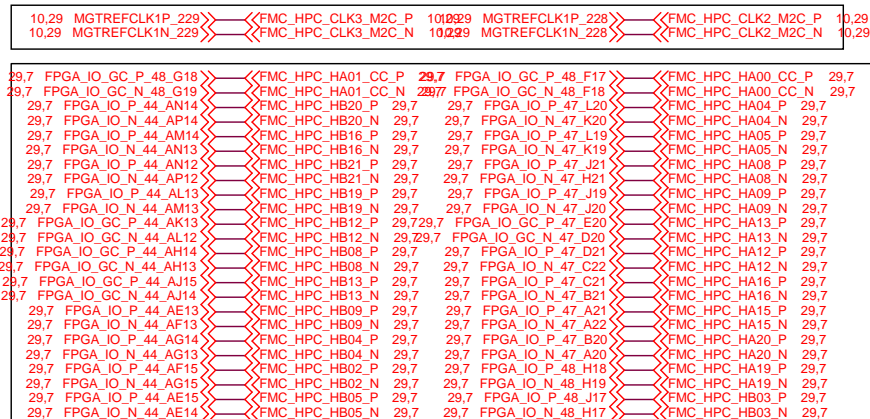




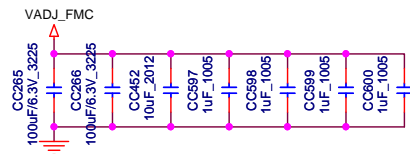
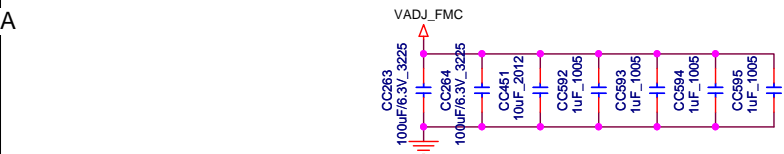
SWAP - A




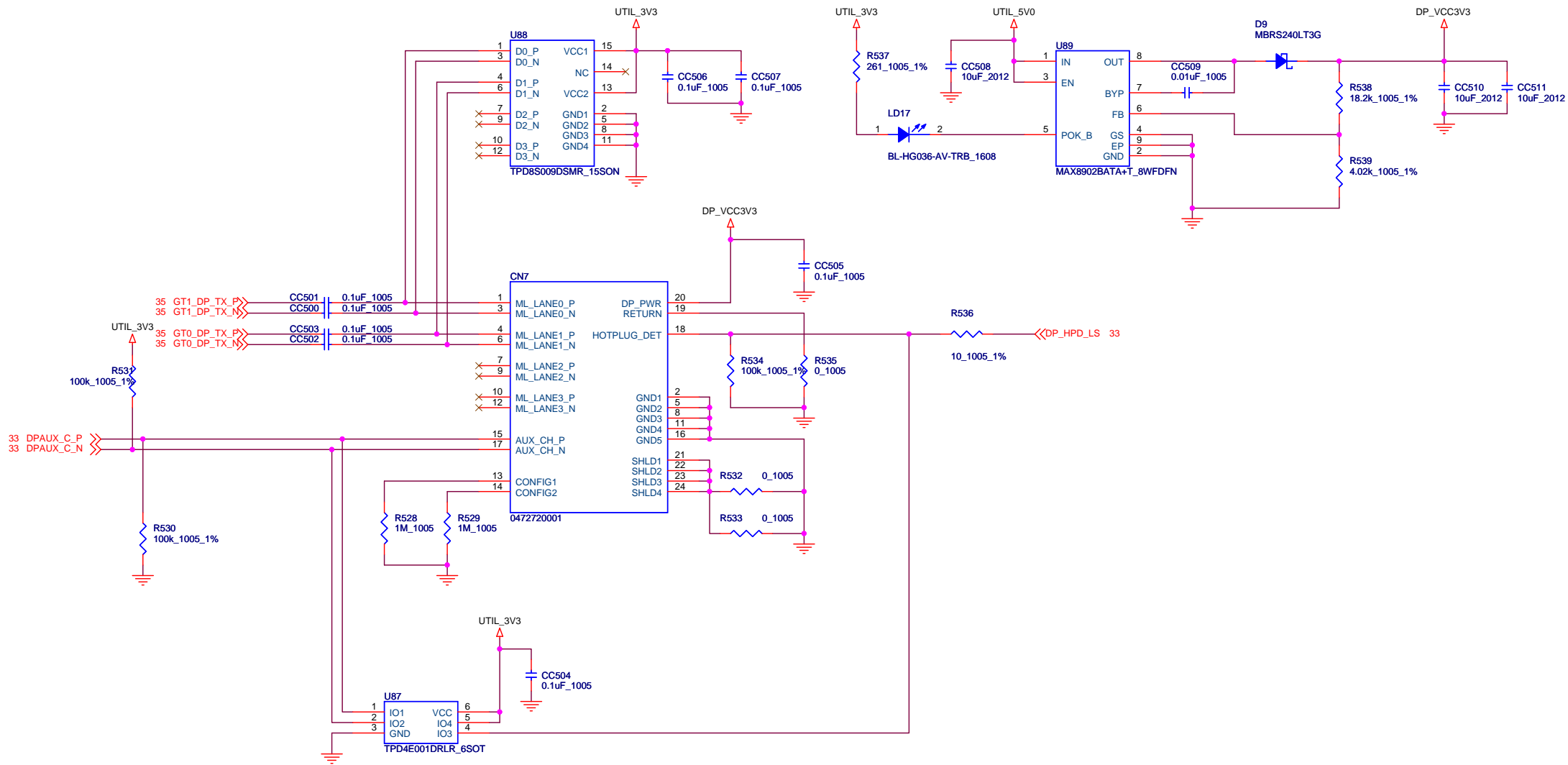
SWAP - B



SWAP - D



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11 MIO29_DP_OE
11 MIO30_DP_AUX_IN
11 MIO28_DP_HPDP

7 PL_DP_HPDP
7 PL_DPAUX_IN
7 PL_DP_OE
7 PL_DPAUX_OUT

R544
0_1005

R545
0_1005

R542
0_1005

R543
0_1005

R547
0_1005_NP

R546
0_1005_NP

R549
0_1005_NP

R548
0_1005_NP

UTIL_3V3
R540
0_1005
CC512
0.1uF_1005

VCCOPS
R541
0_1005_NP

UTIL_3V3
CC513
0.1uF_1005

U90
VCCA VCCB
1A1 1B1
1A2 1B2
2A1 2B1
2A2 2B2
1OE_B 1DIR
2OE_B 2DIR
GND1
GND2
SN74AVC4T245RSVR_16UFQFN

U91
DE VCC
DIN DOUT_P
RE_B DOUT_N
ROUT RIN_P
RIN_N
NC1
NC2
NC3
NC4
FIN1019MTC_14TSSOP

UTIL_3V3
R553
2.49k_1005_1%
R552
1.5k_1005_1%

UTIL_3V3
CC514
0.1uF_1005

CC516
0.1uF_1005
DPAUX_C_P 32

R550
49.9_1005_1%

R551
49.9_1005_1%

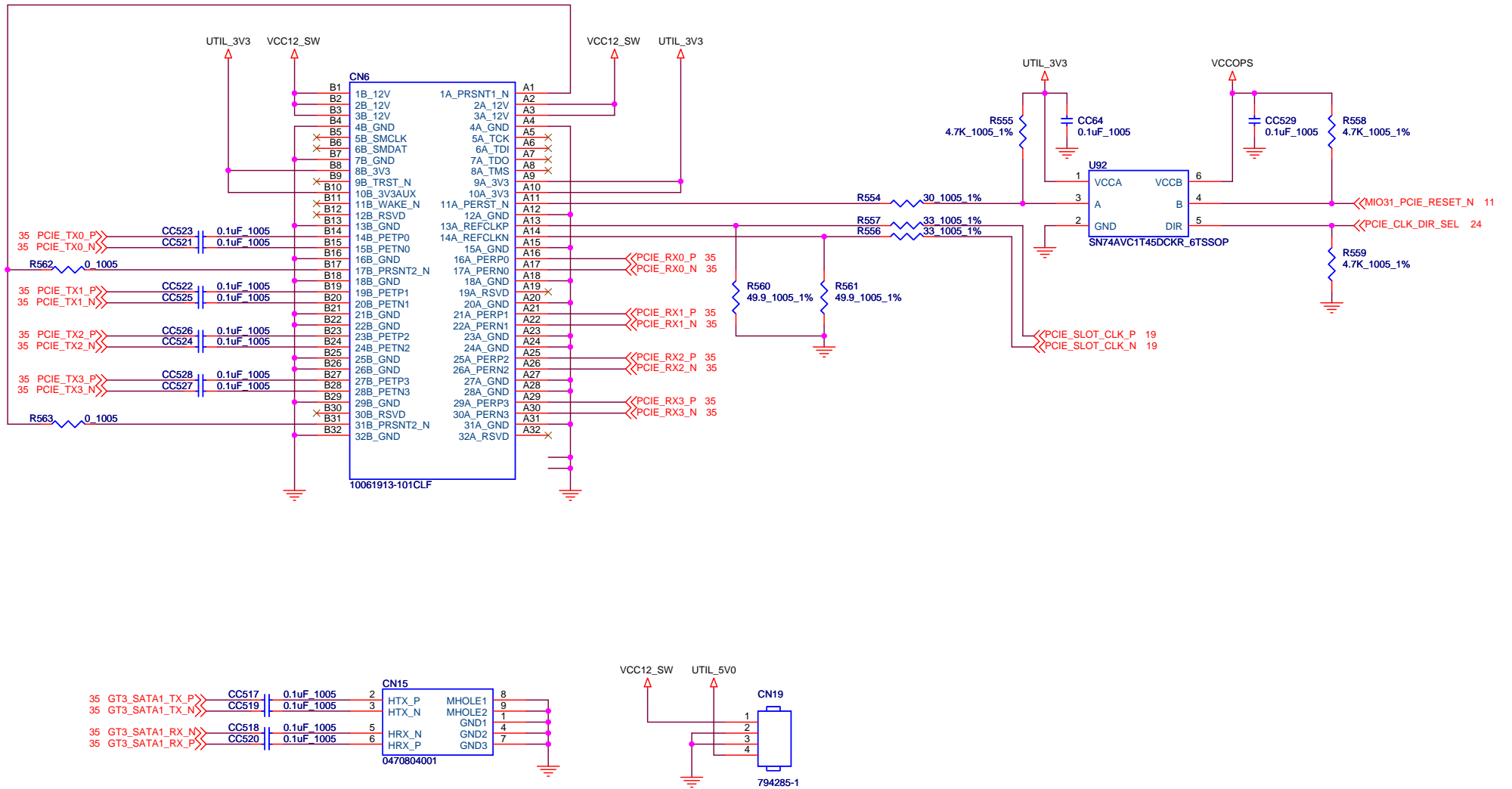
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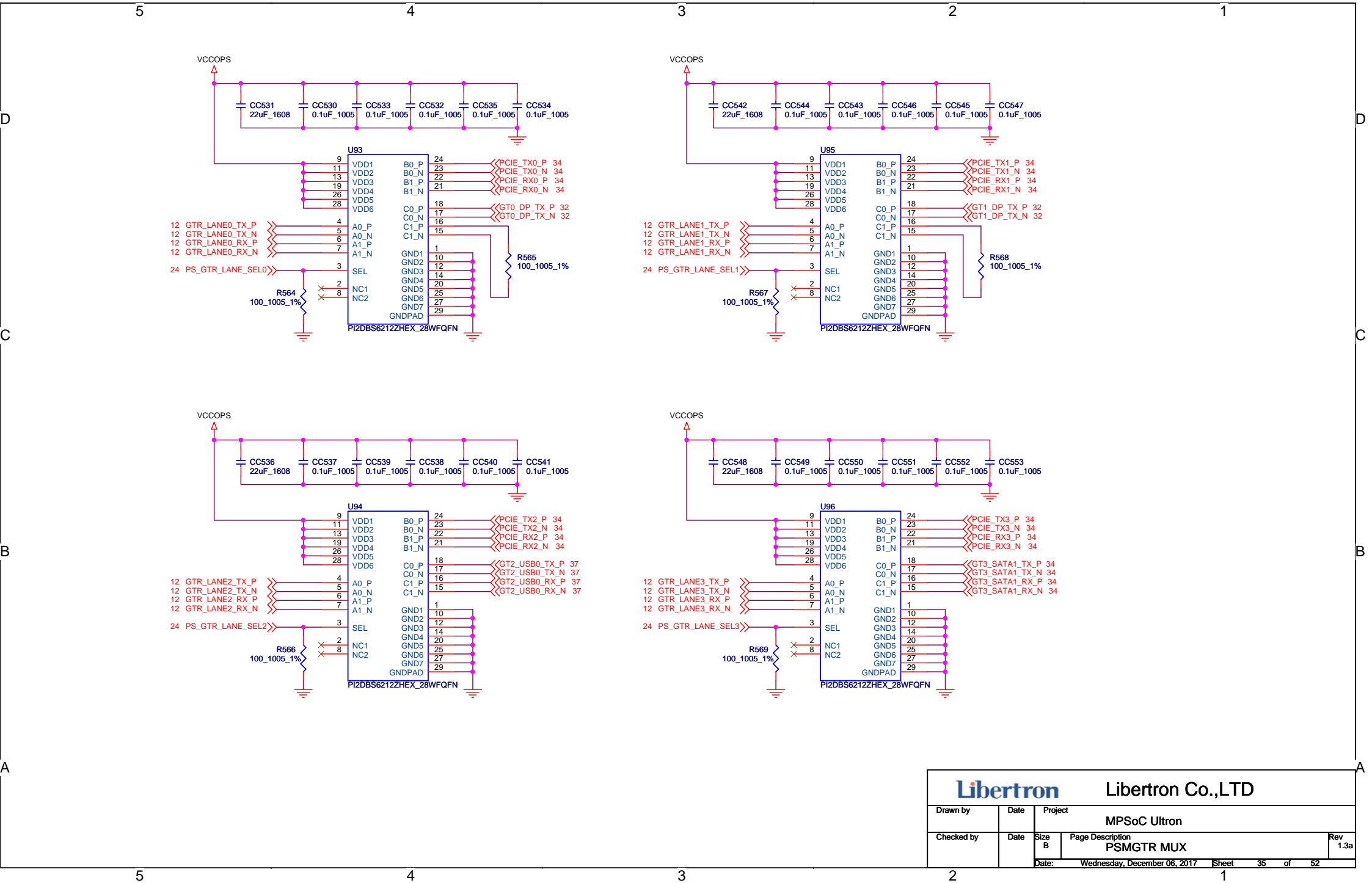
DPAUX_LS 32

Libertron

Libertron Co.,LTD

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Checked by	Date	Size	Page Description	Rev
		B	Display Port 2	1.3a
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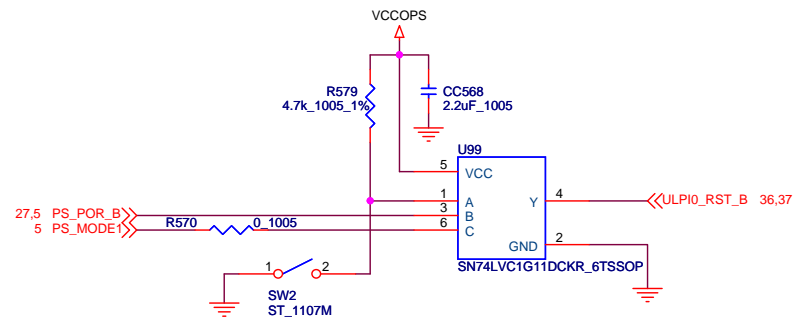
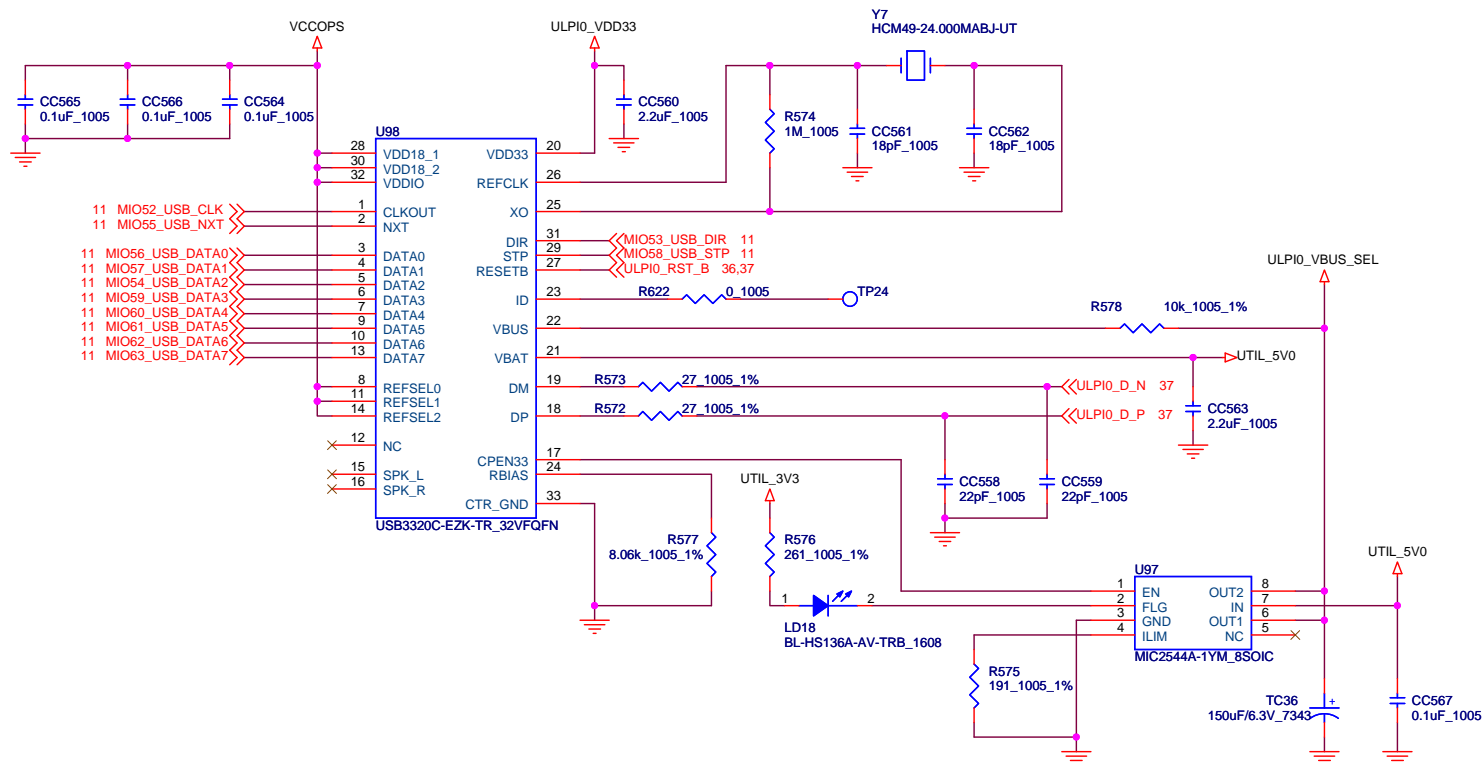




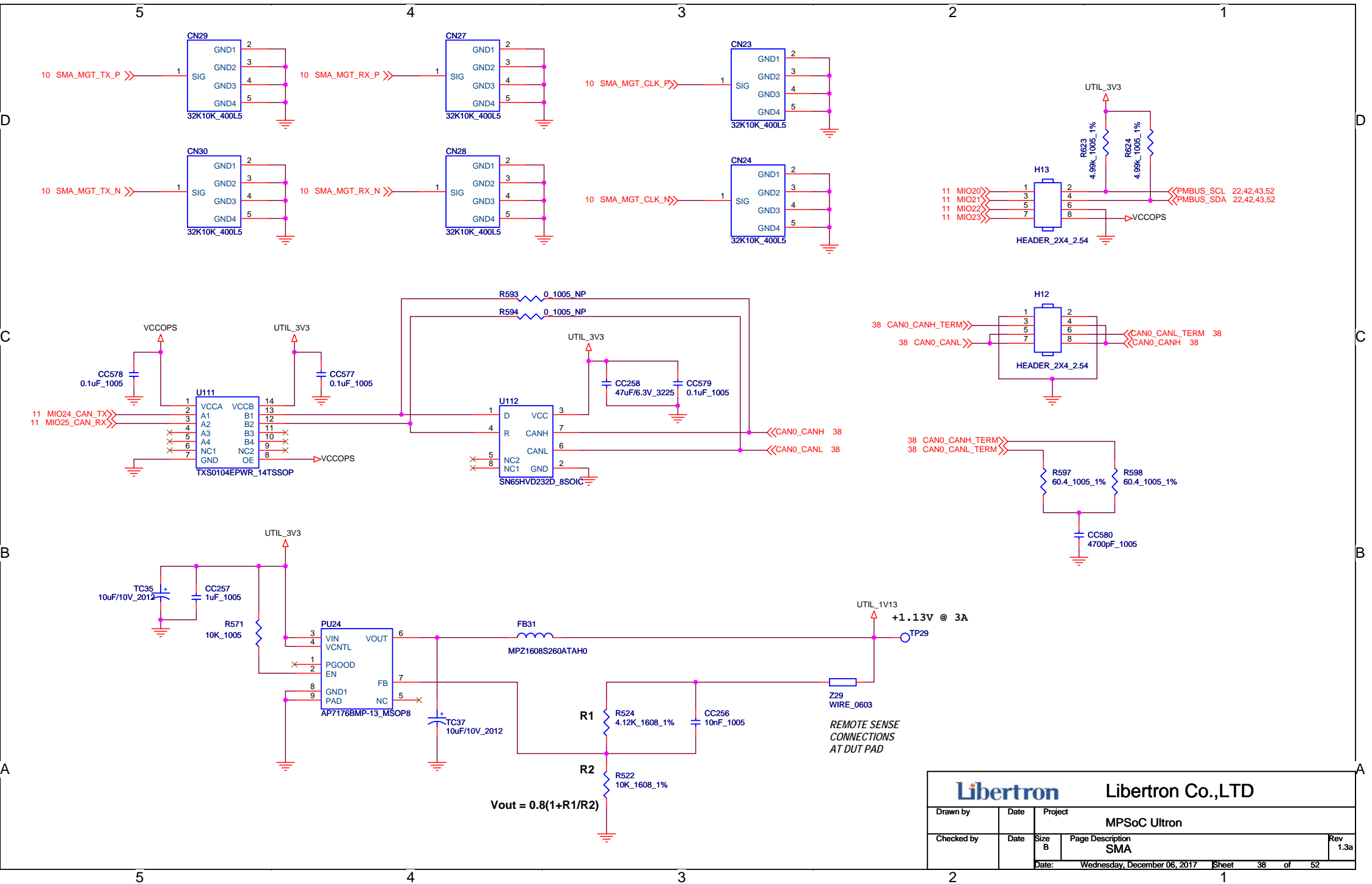
Libertron

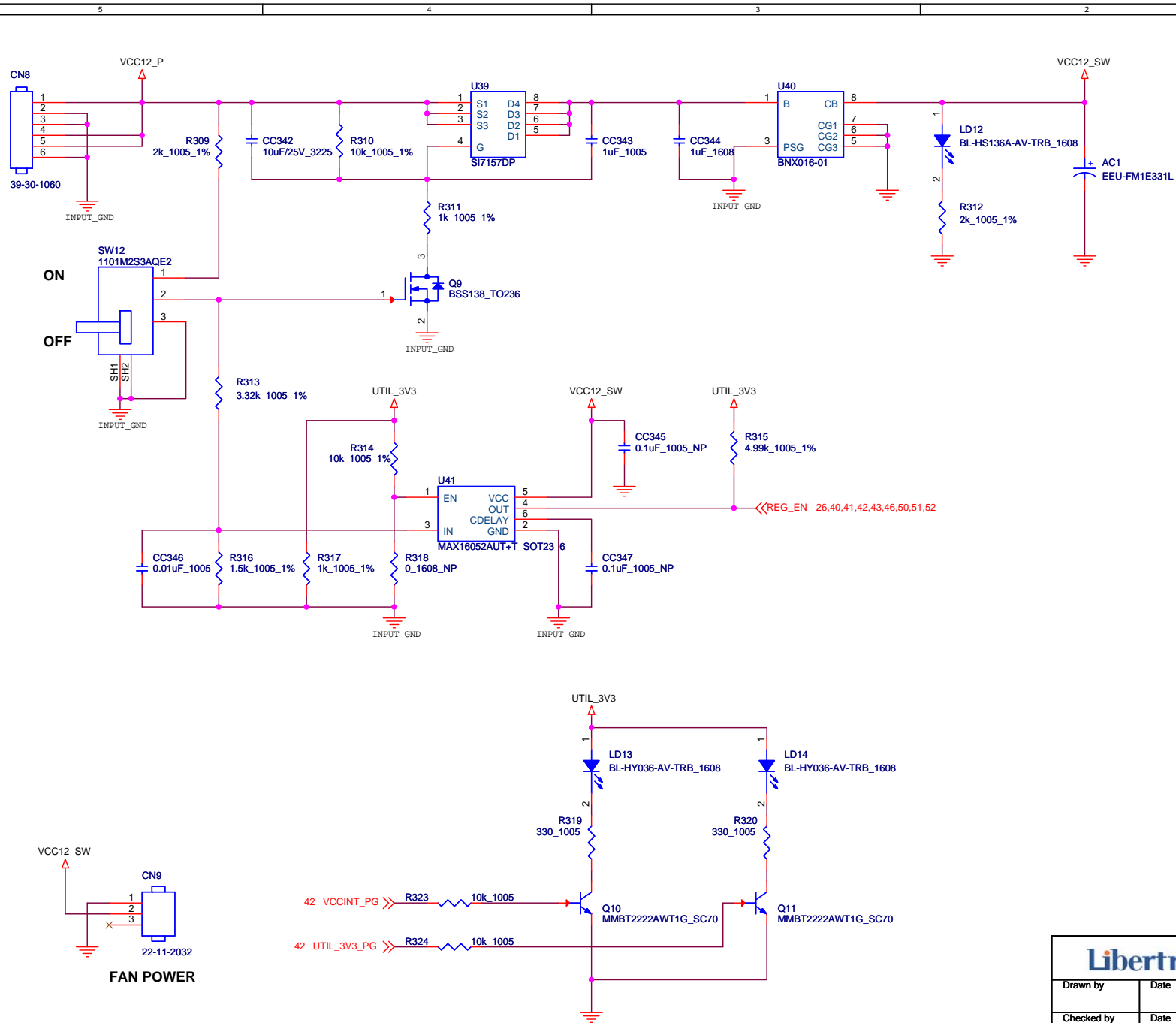
Libertron Co.,LTD

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Checked by	Date	Size	Page Description	Rev
		B	PSMGTR MUX	1.3a
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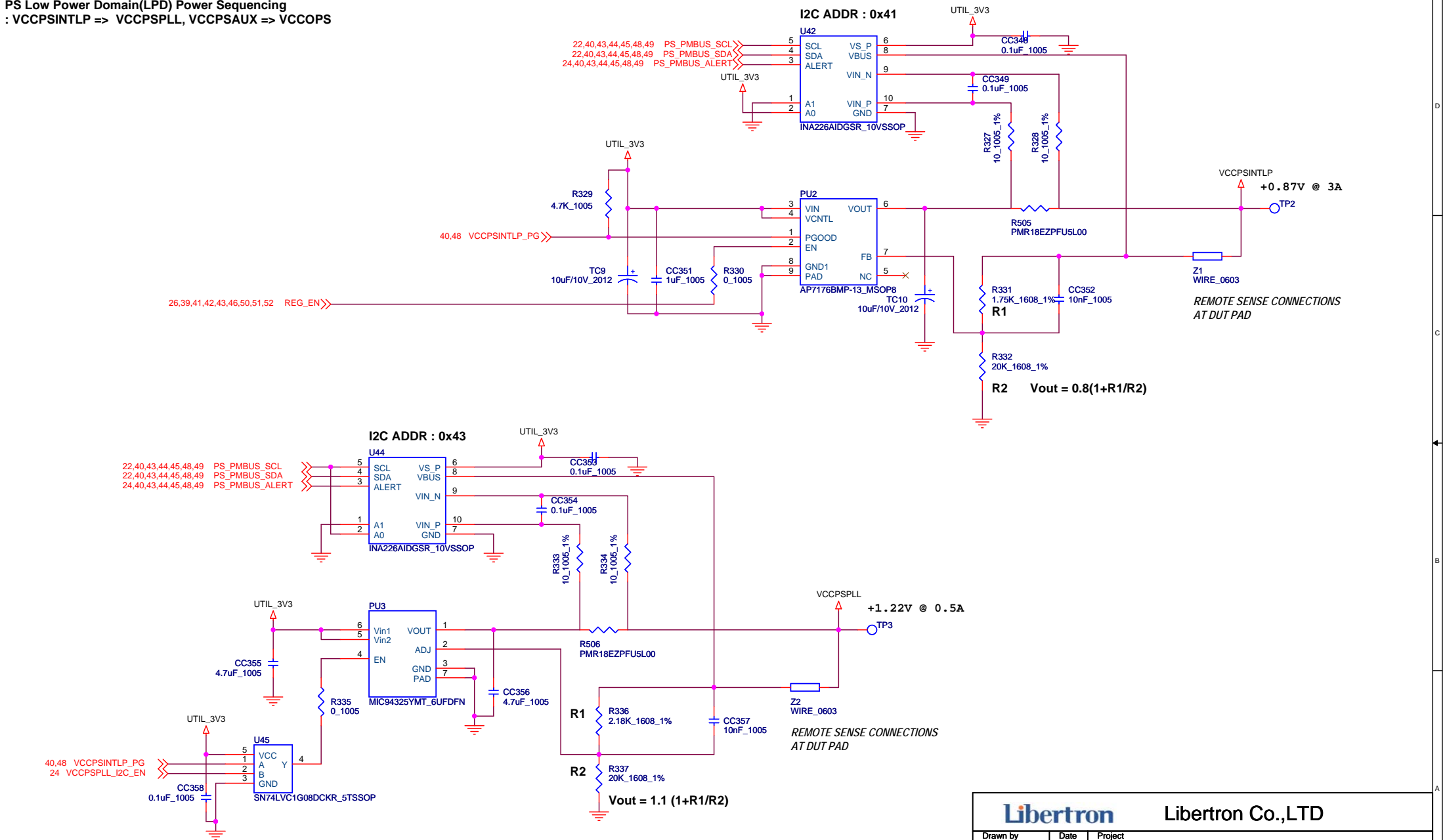
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Drawn by	Date	Project	
Checked by	Date	MPSoC Ultron	
Size B	Page Description	USB Transceiver	
Date:	Wednesday, December 06, 2017	Sheet	36 of 52
		Rev	1.3a



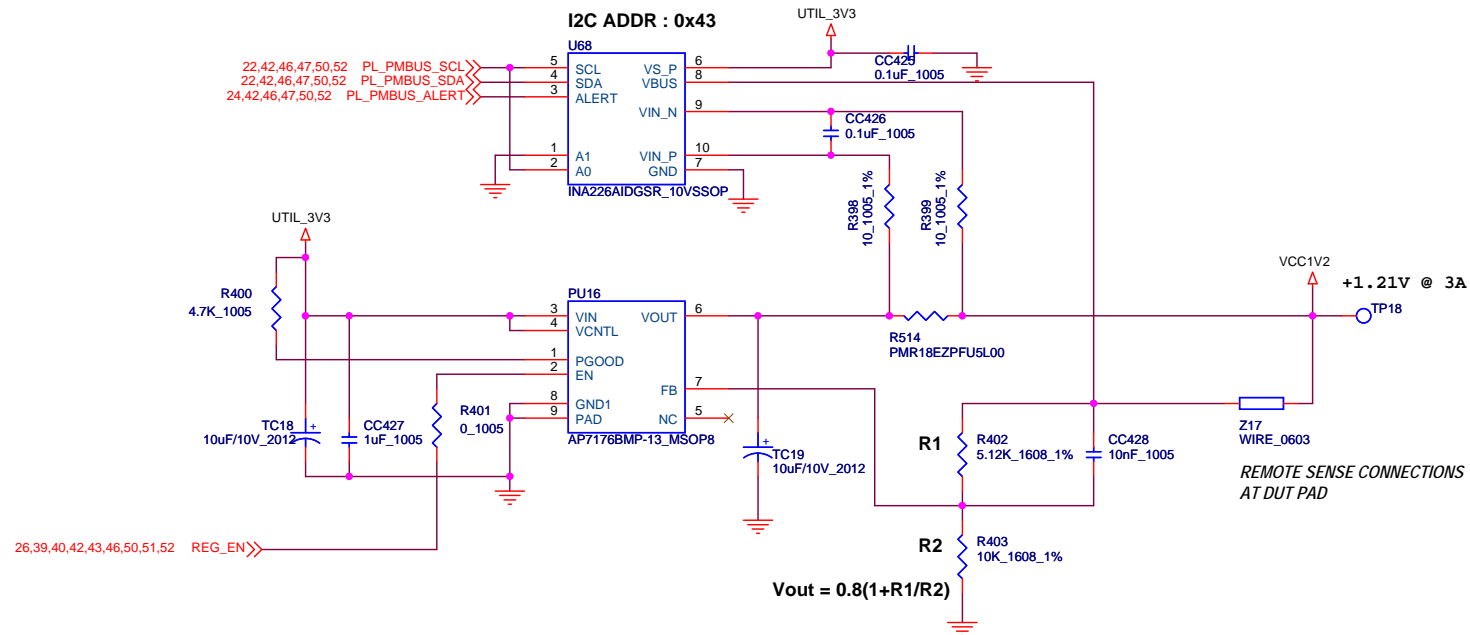


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Drawn by	Date	Project		
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Checked by	Date	Size	Page Description	Rev
		B	Power Input	1.3a
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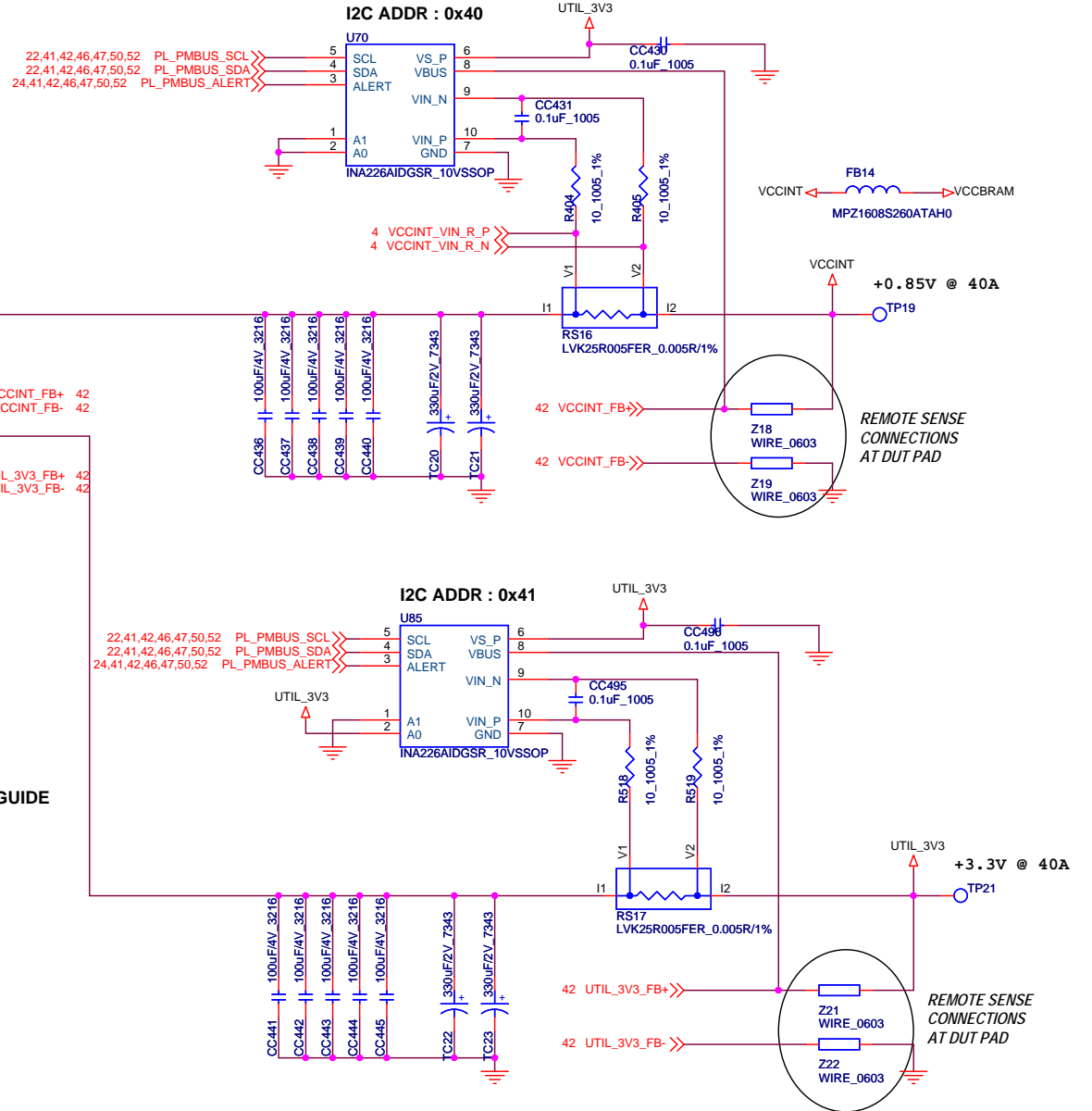
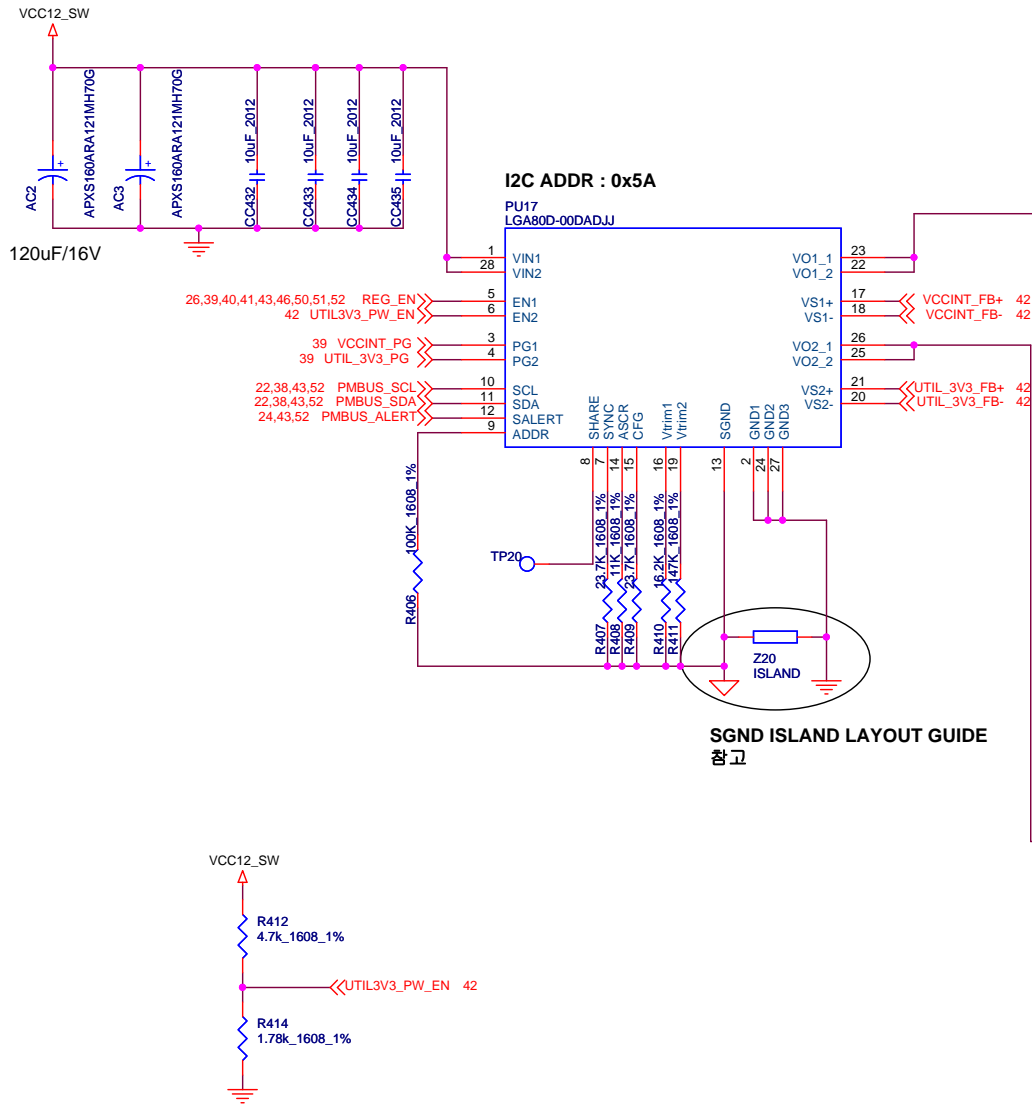
PS Low Power Domain(LPD) Power Sequencing
: VCCPSINTLP => VCCPSPLL, VCCPSAUX => VCCOPS



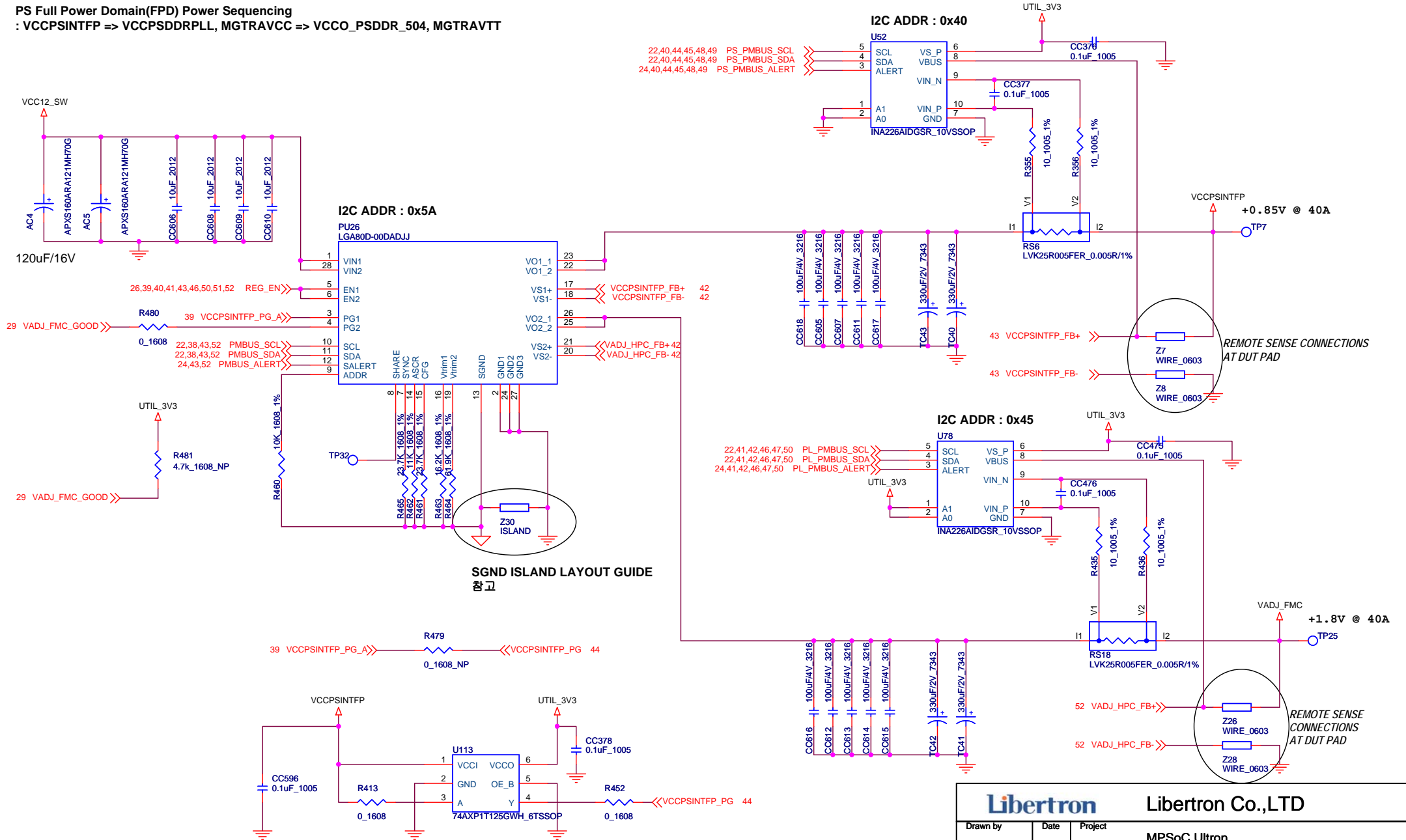
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Drawn by	Date	Project	
		MPSoc Ultron	
Checked by	Date	Size	Page Description
		B	VCCPSINTLP / VCCPSPLL
		Date:	Wednesday, December 06, 2017
		Sheet	40 of 52
		Rev	1.3a

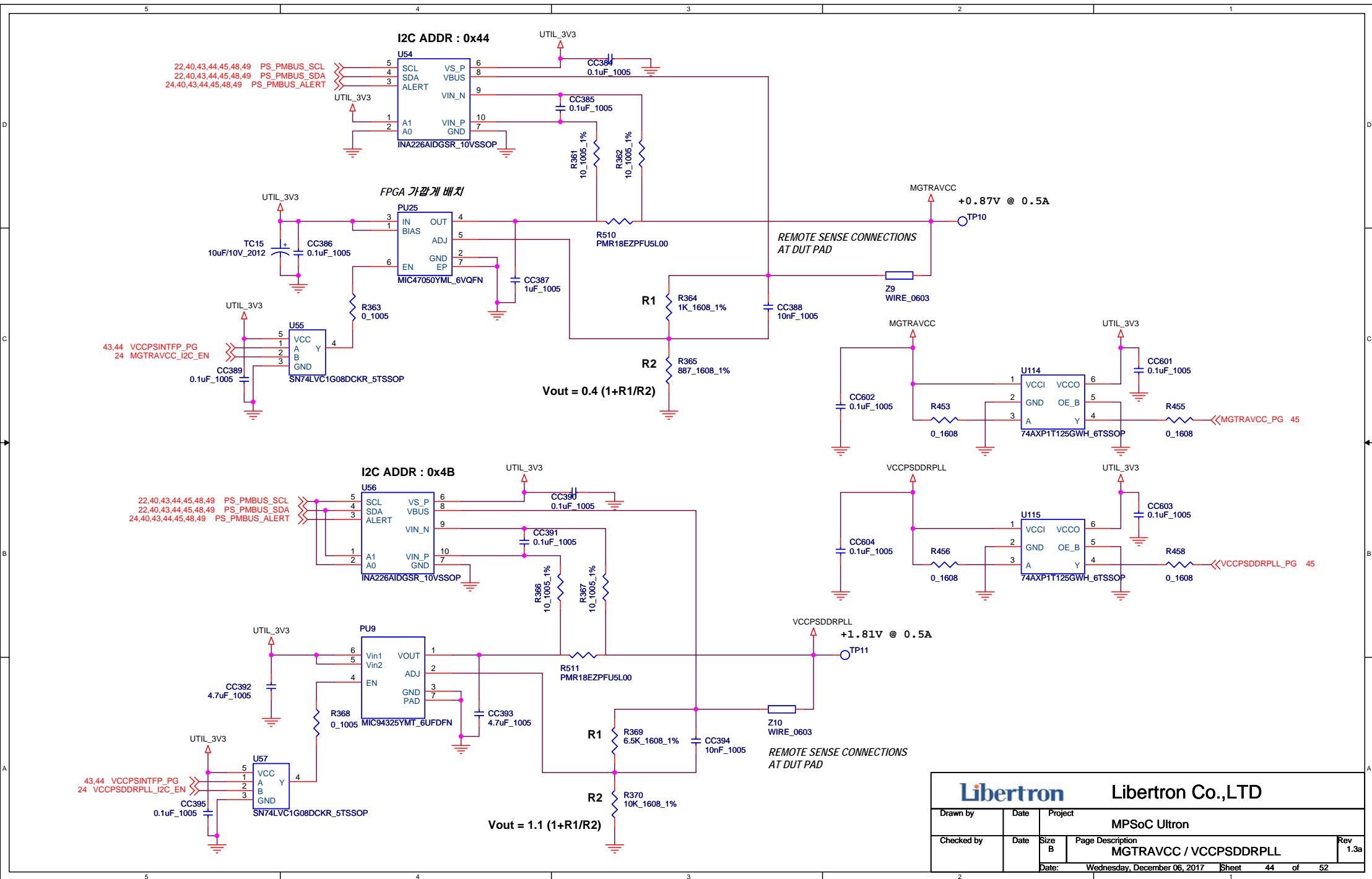


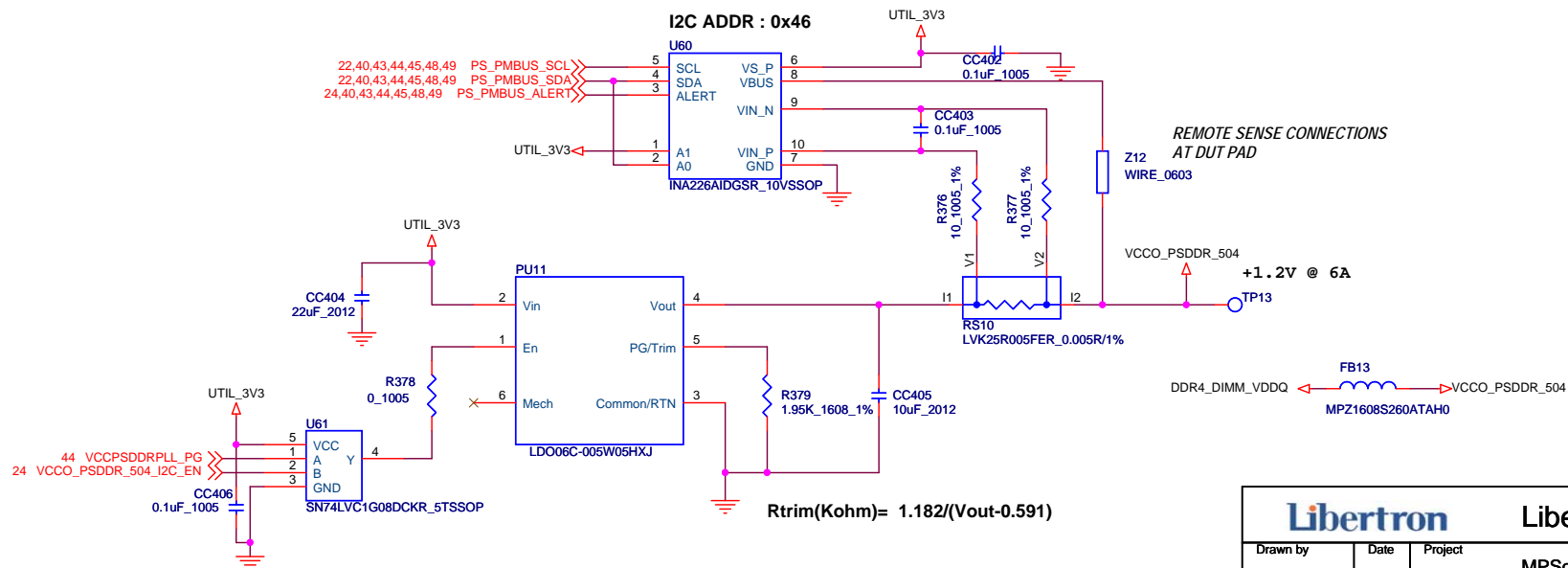
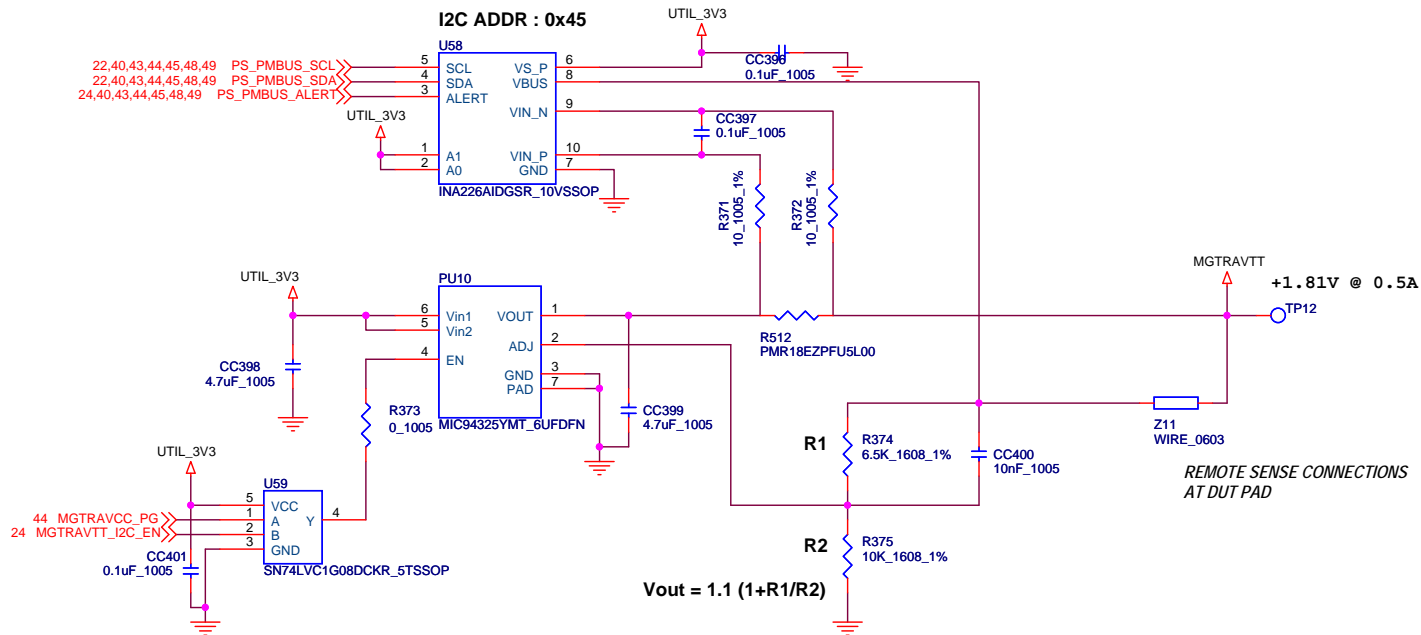
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Drawn by	Date	Project		
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Checked by	Date	Size	Page Description	Rev
		B	VCC3V3 / VCC1V2	1.3a
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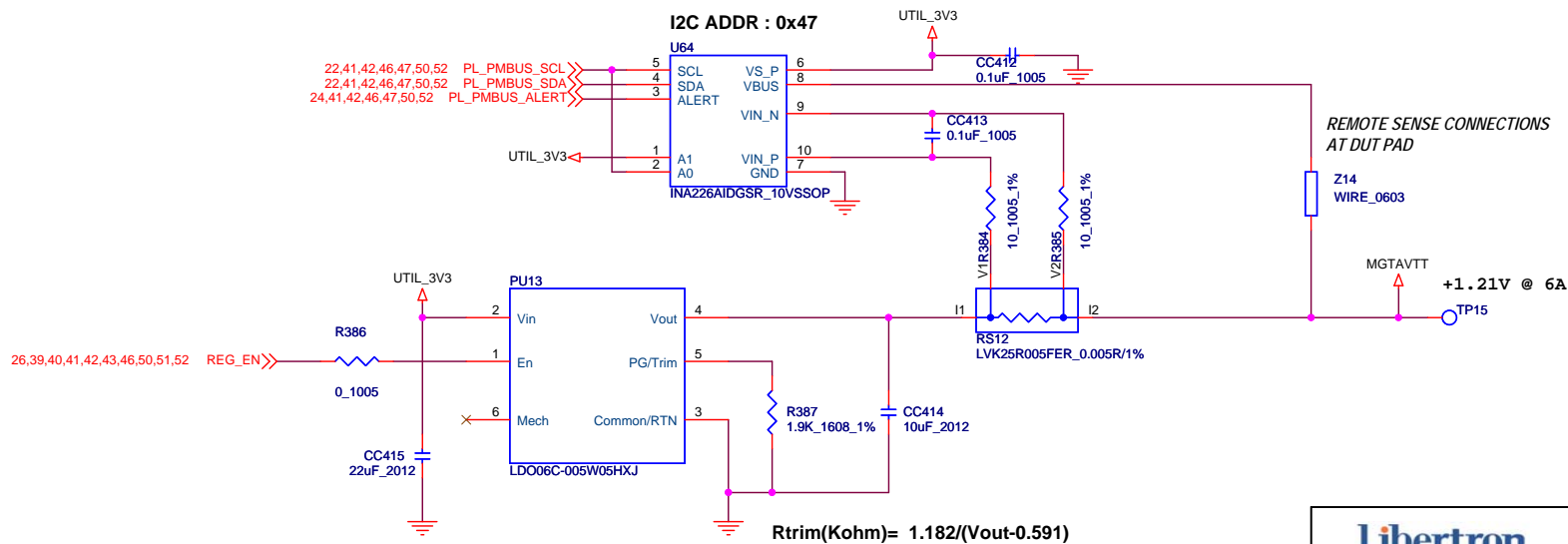
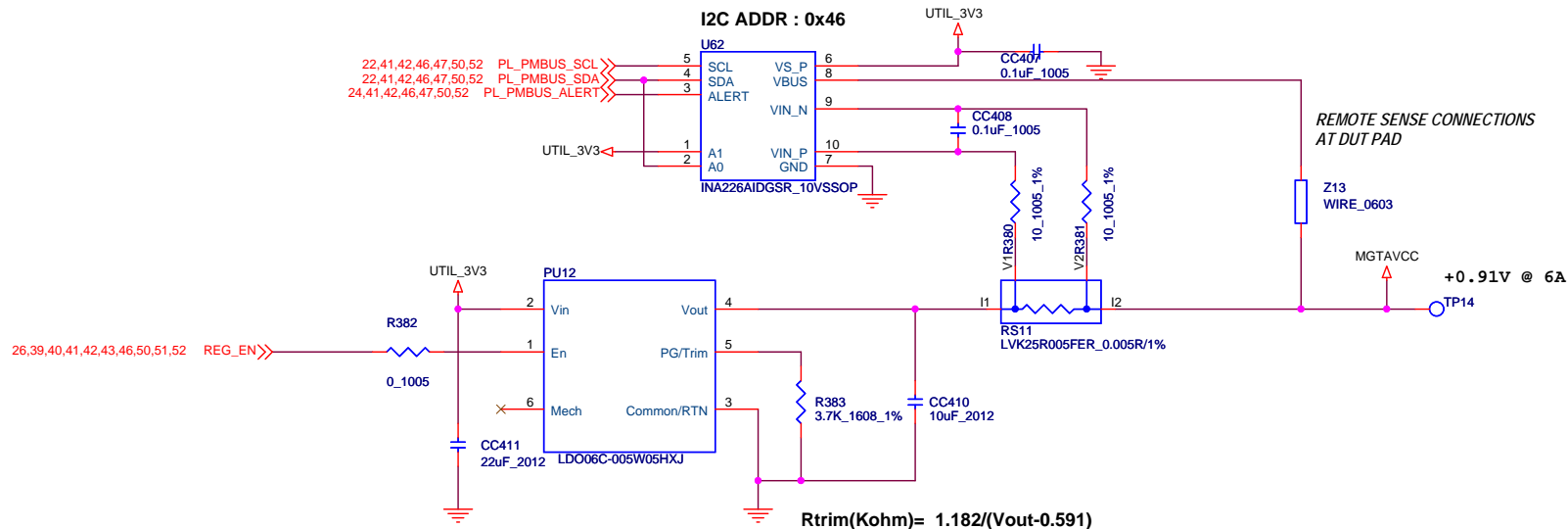
: VCCPSINTFP => VCCPSDDRPLL, MGTRAVCC => VCCO_PSDDR_504, MGTRAVTT



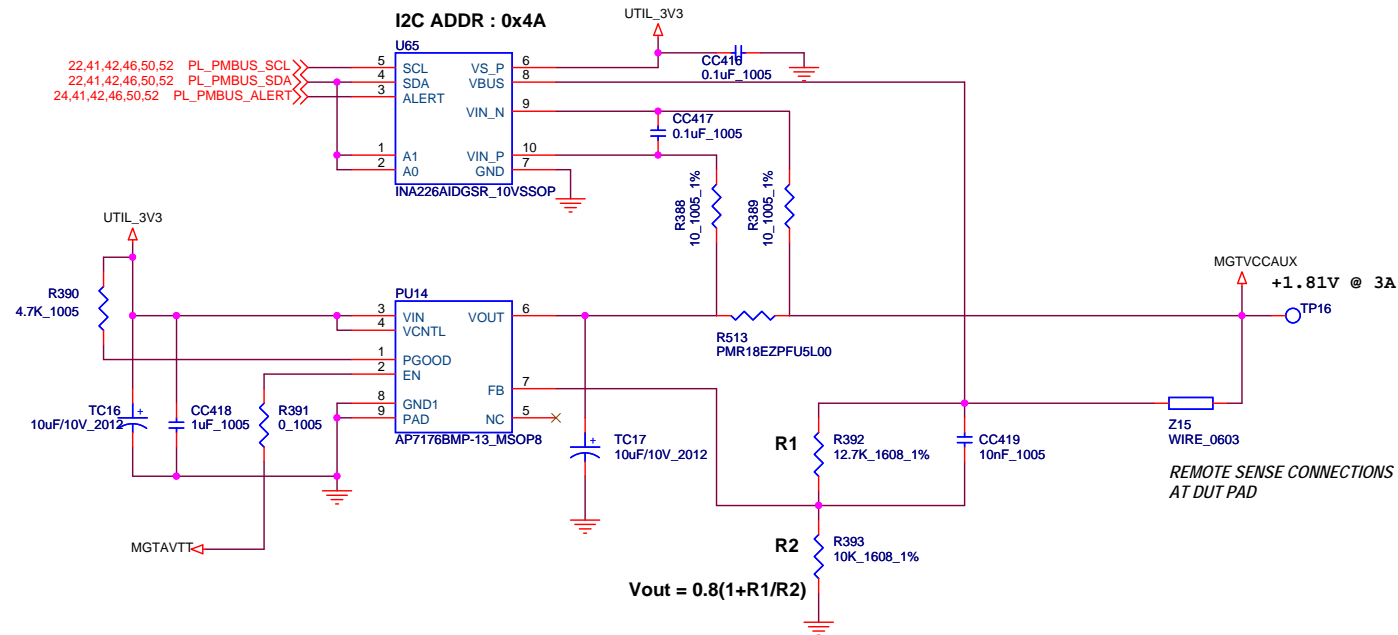




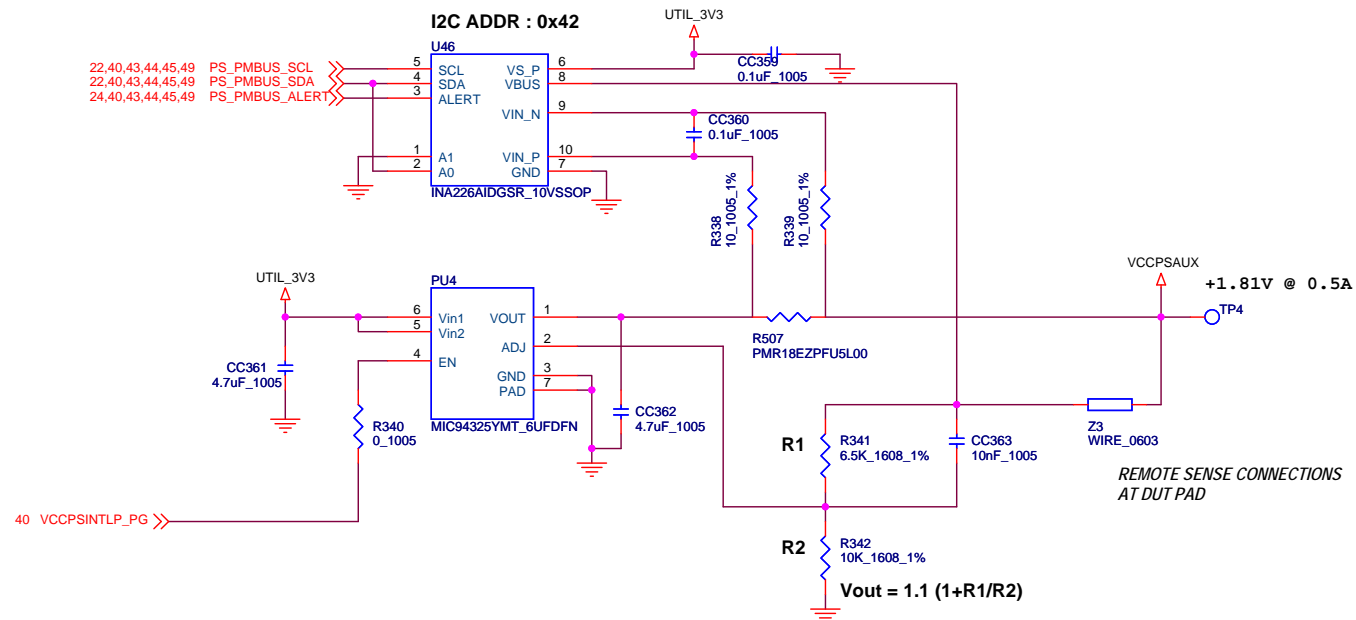
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Drawn by	Date	Project	
		MPSoc Ultron	
Checked by	Date	Size	Page Description
		B	MGTRAVTT / VCCO_PSDDR_504
		Rev	1.3a
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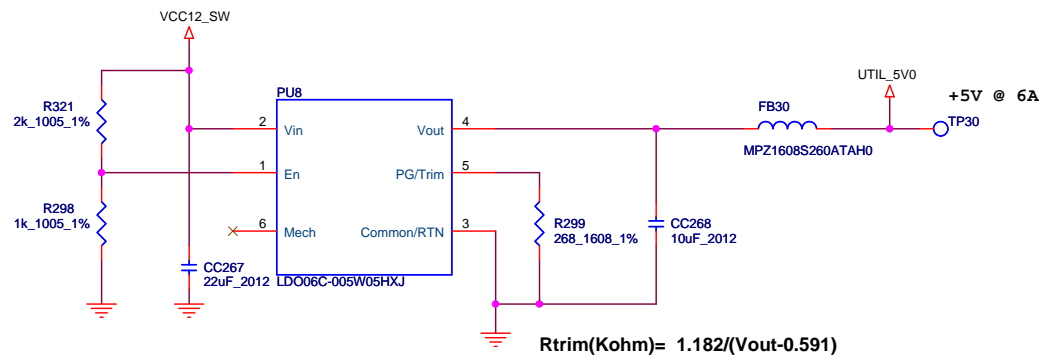
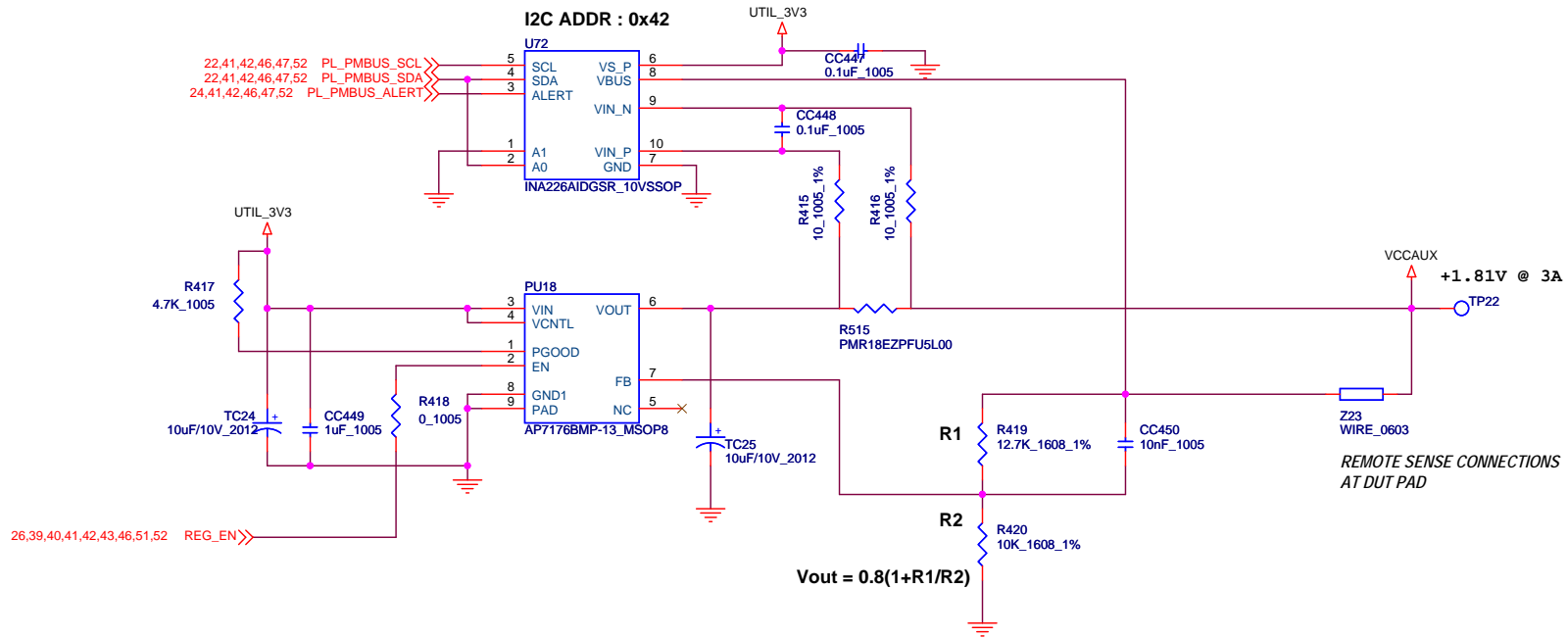
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Drawn by	Date	Project		
		MPSoC Ultron		
Checked by	Date	Size	Page Description	Rev
		B	MGTAVCC / MGTAVTT	1.3a
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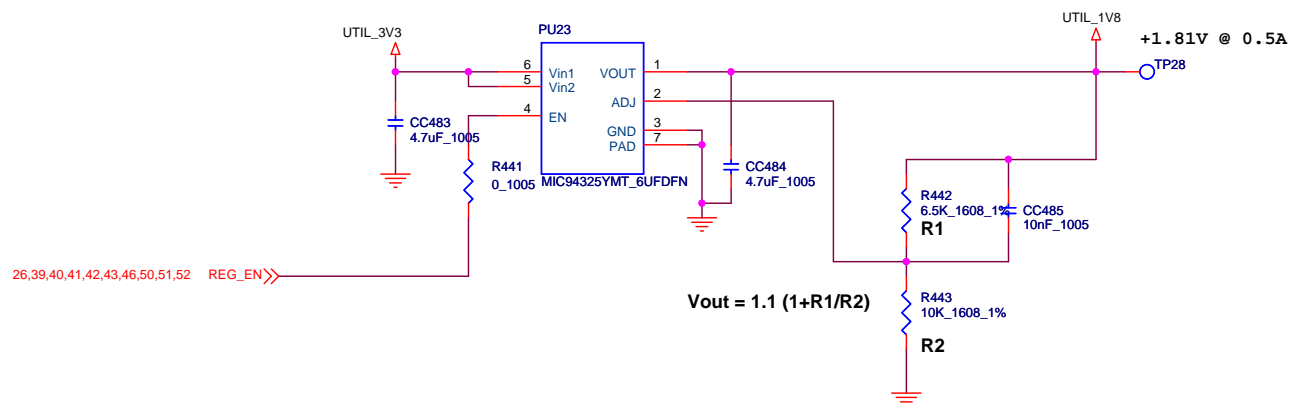
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Checked by	Date	Size	Page Description	Rev
		B	MGTVCCAUX	1.3a
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Libertron		Libertron Co.,LTD		
Drawn by	Date	Project		
		MPSoC Ultron		
Checked by	Date	Size	Page Description	Rev
		B	VCCPSAUX	1.3a
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		Sheet	48	of 52



Libertron		Libertron Co.,LTD		
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		MPSoC Ultron		
Checked by	Date	Size	Page Description	Rev
		B	VCCAUX	1.3a
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Libertron		Libertron Co.,LTD		
Drawn by	Date	Project		
		MPSoC Ultron		
Checked by	Date	Size	Page Description	Rev
		B	VADJ_HPC / UTIL_1V8	1.3a
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