ULTRON Board
User Manual

Libertron Co., Ltd

◆ Contents

✓ Revision History

Ver	Date	Revision
1.0	2017-03-23	1st Initial Version.
1.1	2017-09-01	2nd Revision Version.

1. ULTRON Board 개요 및 특징

1.1. 개요

- ULTRON Board는 Xilinx 社의 최신 FPGA인 Zynq UltraScale+ 를 적용한 Board 로써 PMOD 및 FMC Connector를 제공하여 다른 Board와의 확장이 용이하며, DDR4 Memory, Ethernet, PCI Express, USB, SATA, DisplayPort 등 외부 Interface 를 제공하여 다양한 개발 환경에 사용할 수 있습니다.

1.2. 제품 특징

- Xilinx 社의 Zynq UltraScale+ FPGA사용
- FPGA Configuration : JTAG Module, JTAG Header, MicroSD, QSPI 지원
- 다양한 Memory 지원 : DDR4 SO-DIMM, DDR4 Component(4Gb)
- FMC (FPGA Mezzanine Card) HPC, LPC 지원
  - ✓ LPC : 사용자 I/O 72핀, 고속 Transceiver 1-Channel 제공
  - ✓ HPC : 사용자 I/O 164핀, 고속 Transceiver 10-Channel 제공
- USB2.0 1-Port, USB3.0 1-Port 지원 (Host Only)
- DisplayPort (V1.2) 1-Port 지원 (Source Only)
- SATA (V3.1) 1-Port 지원
- PCI Express (V2.1) Gen2 x 4Lane 지원 (Root Only)
- SMA 고속 Transceiver 1-Channel 지원
- CAN Bus Transceiver 지원
- UART (Mini USB, RS-232) 지원
- Xilinx SYSMON 지원
- Power Monitoring 지원
- 사용자 Programmable Clock Generator 지원
- Ethernet, UART Interface를 통한 Debugging 환경 제공

2. 제품 구성

구성	수량	제품사진
MPSoC ULTRON Board	**1**	
DC Adaptor (12V/7.5A)	**1**	
Micro USB Cable	**1**	
Mini USB Cable	**1**	
Ethernet Cable	**1**	

3. Specification

Item	Part	Spec	Note
FPGA	Zynq UltraScale+ XCZU9EG-1FFVB1156E	- Quad-Core ARM Cortex-A53 - ARM Mali-400MP2 GPU - 600K Logic Cells - 32Mb BRAM	
FPGA Configuration	JTAG	- Digilent USB to JTAG Module - JTAG Header 6-pin	
	QSPI	- Dual QSPI (512Mb x 2)	
	SD	- Micro SD Card Slot	
Memory	DDR4 SO-DIMM	- 64bit SODIMM Socket with ECC (For PS)	
	DDR4 Component	- 4Gb Density, 16bit Data width (For PL)	
External I/F	FMC	- HPC 1EA (I/O : 164pin, MGT : 10-Ch) - LPC 1EA (I/O : 72pin, MGT : 1-Ch)	
	USB	- USB 2.0 1-Port (Host Only) - USB 3.0 1-Port (Host Only)	
	DisplayPort	- V1.2 (Source-only, Up to 4k x 2k)	
	SATA	- SATA 3.1 specification	
	PCI Express	- V2.1 Root Only (Gen2 x 4Lane)	
	Ethernet	- 10/100/1000 Mb/s, 1-Port (RJ-45)	
	PMOD	- PMOD Connector 2EA	
	SMA	- MGT 고속 Transceiver 1-Ch	
	CAN	- CAN 2.0A/B Standards.	
	UART	- Mini USB Connector - RS232 DSUB 9-pin Connector	
Etc	Status LED	- PS Error Status LED 2EA - PS Reset Status LED 1EA - User LED 4EA	
	Switch	- PS Reset Switch 1EA - PS POR Reset Switch 1EA - User Push Switch 4EA	
	Clock	- Programmable Clock Generator	
Power	DC Power Input	- DC +12V/7.5A Power Input	
PCB Layer	PCB spec	- Layer : 22L / 2.6T / FR-4	
Size	가로 x 세로	- 260mm x 165mm	

4. ULTRON Board Description

4.1. Block-Diagram

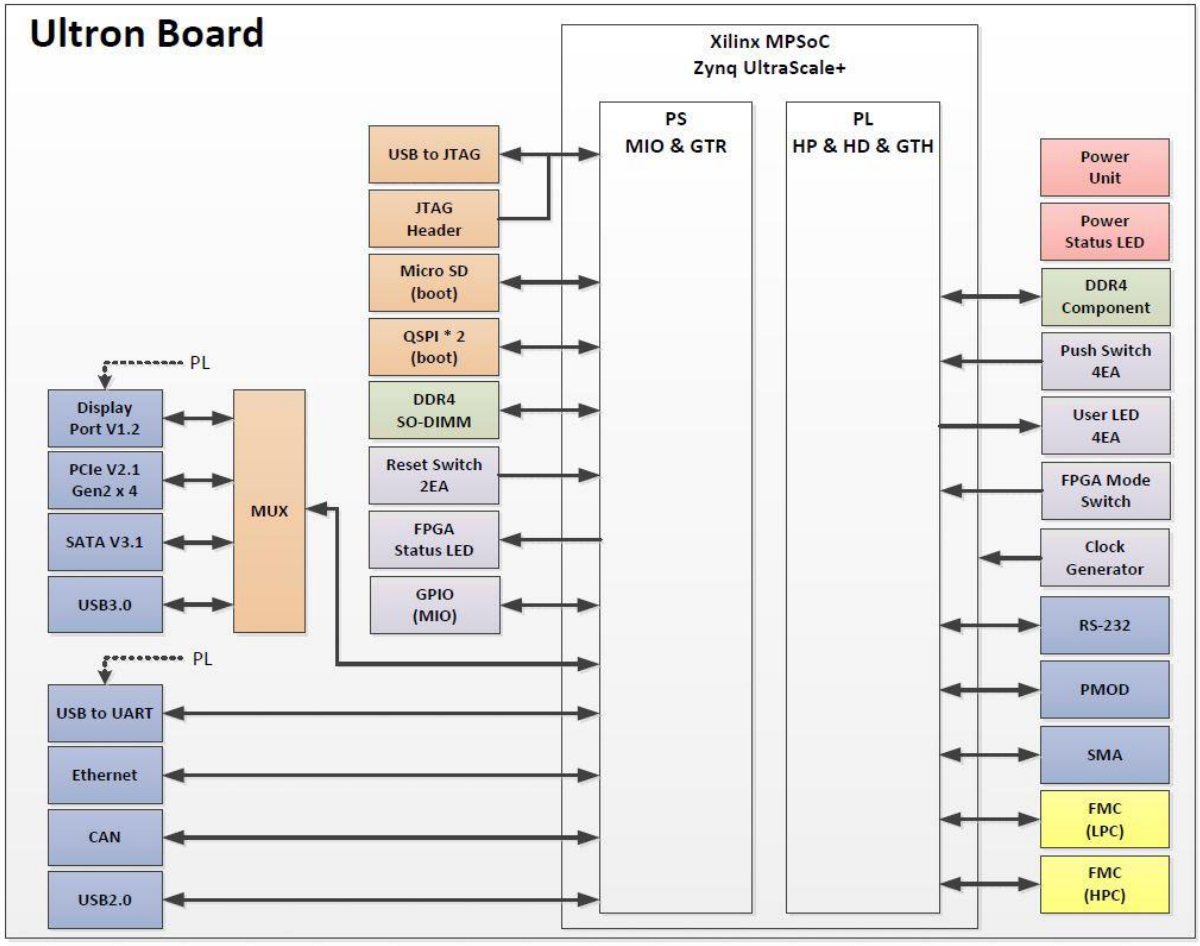
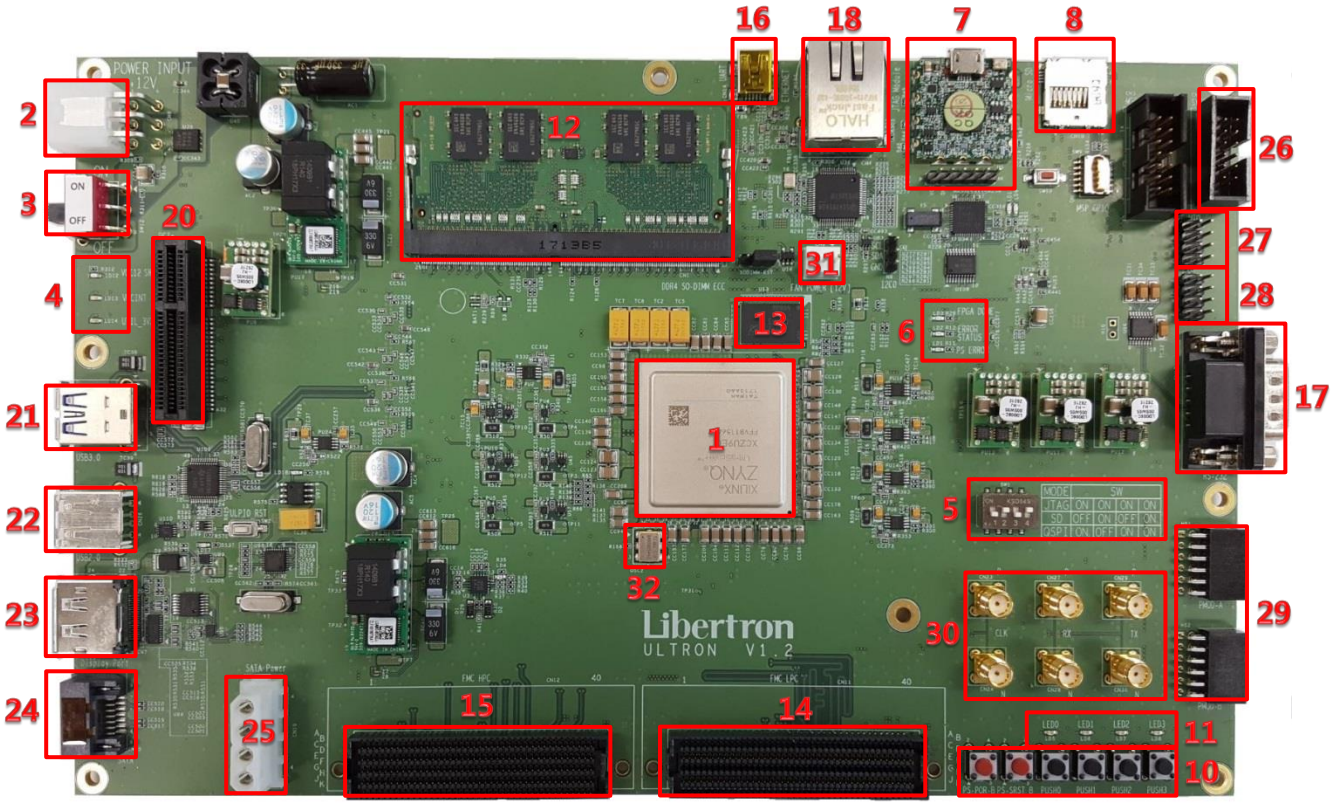
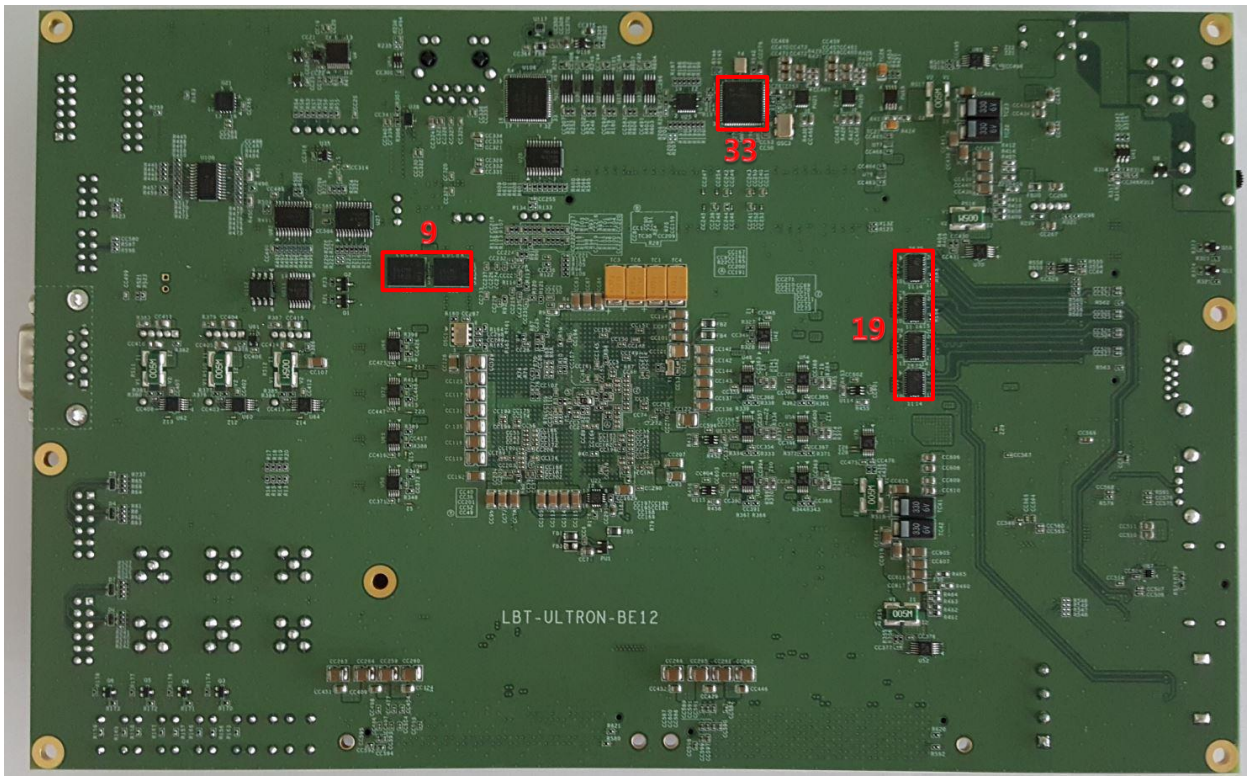


그림 1. Board Block Diagram

4.2. ULTRON Board Description



<Top View>



<Bottom View>

1. MPSoC Zynq UltraScale+
2. Power Input Connector
3. Power ON/OFF Switch
4. Power Status LED
5. FPGA Configuration Mode Switch
6. FPGA Status LED
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15. FMC HPC
16. Mini USB (UART) Connector
17. DSUB (RS-232) Connector
18. Ethernet RJ-45 Connector
19. FPGA PS GTR MUX
20. PCI Express x 4Lane Connector
21. USB3.0 A-Type Connector
22. USB2.0 A-Type Connector
23. DisplayPort Connector
24. SATA Connector
25. SATA Power Connector
26. FPGA SYSMON Connector
27. FPGA PS-MIO Connector
28. CAN Connector
29. PMOD Connector
30. SMA Connector
31. FAN Connector
32. Programmable OSC
33. Fixed Clock Generator

4.2.1. MPSoC Zynq UltraScale+

- ULTRON Board는 Xilinx 社의 최신 Device인 Zynq UltraScale+ MPSoC (XCZU9EG-1FFVB1156E)을 장착하였다. Application Processing Unit으로는 ARM Cortex-A53 Quad-Core를 기반으로 하며, Real-Time Processing Unit으로는 ARM Cortex-R5 Dual-Core를 지원 한다. 이밖에 Programmable Logic으로는 600K Logic Cells를 지원하며, ARM Mali-400를 기반으로 하는 GPU 등의 다양한 Interface를 제공한다.
- ULTRON Board의 PS MIO 구성은 아래와 같다.

<PS MIO Peripheral mapping>

MIO[0:25]	BANK 0	MIO[26:51]	BANK 1	MIO[52:77]	BANK 2
0	QSPI	26	PMU IN	52	USB0
1	QSPI	27	DPAUX	53	USB0
2	QSPI	28	DPAUX	54	USB0
3	QSPI	29	DPAUX	55	USB0
4	QSPI	30	DPAUX	56	USB0
5	QSPI	31	PCIe	57	USB0
6	QSPI	32	PMU OUT	58	USB0
7	QSPI	33	PMU OUT	59	USB0
8	QSPI	34	PMU OUT	60	USB0
9	QSPI	35	PMU OUT	61	USB0
10	QSPI	36	PMU OUT	62	USB0
11	QSPI	37	PMU OUT	63	USB0
12	QSPI	38	GPIO	64	GEM3
13	GPIO	39	SD1	65	GEM3
14	I2C0	40	SD1	66	GEM3
15	I2C0	41	SD1	67	GEM3
16	I2C1	42	SD1	68	GEM3
17	I2C1	43	SD1	69	GEM3
18	UART0	44	SD1	70	GEM3
19	UART0	45	SD1	71	GEM3
20	GPIO	46	SD1	72	GEM3
21	GPIO	47	SD1	73	GEM3
22	GPIO	48	SD1	74	GEM3
23	GPIO	49	SD1	75	GEM3
24	CAN1	50	SD1	76	MDIO3
25	CAN1	51	SD1	77	MDIO3

<Processor Performance>

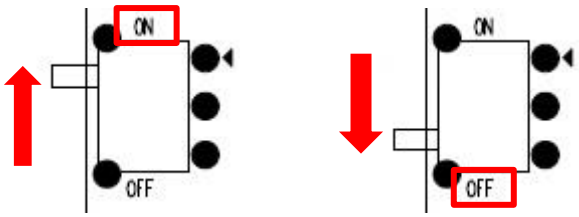
Processor	Description	Frequency	Unit
APU	Maximum APU clock frequency.	1200	MHz
RPU	Maximum RPU clock frequency.	500	MHz
GPU	Maximum GPU clock frequency.	600	MHz

4.2.2. Power Input Connector

- 전원을 공급하는 Connector로 Molex 社의 "39-30-1060"을 적용하였으며, 공급전원은 DC +12V / 7.5A 를 사용한다.
- **주의사항 : PCIe Power (Desktop ATX Power) 를 사용하지 않도록 한다.**

4.2.3. Power ON/OFF Switch

- 전원을 ON/OFF 하는 Switch로 C&K 社의 "1101M2S3AQE2"를 적용하였으며, ON/OFF 조작은 아래와 같다.



< ON > < OFF >

4.2.4. Power Status LED

- Board의 Power Status를 확인할 수 있는 LED를 제공하며, 각 LED의 Description은 아래와 같다.

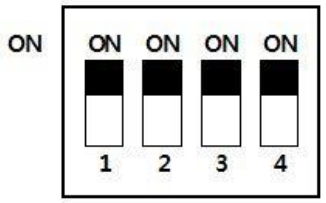
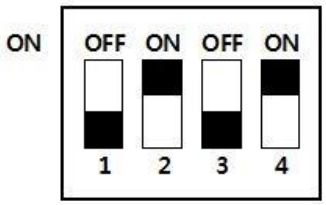
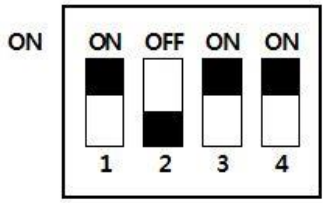
<Power Status LED Description>

LED	Description
Board 전원 ON LED (LD12)	Board의 전원이 ON 되면, LED 점등 (Red)
VCCINT 전원 LED (LD13)	FPGA VCCINT Core 전원 Status LED (Red)
UTIL_3V3 전원 LED (LD14)	Board +3.3V 전원 Status LED (Red)

4.2.5. FPGA Configuration Mode Switch

- FPGA Configuration Mode를 선택하는 스위치이며, Description은 아래와 같다.

<FPGA Mode Switch Description>

Boot Mode	Mode Switch (SW1)	Description
JTAG		JTAG Module 혹은 Xilinx JTAG 케이블을 사용하여 Configuration할 경우 사용하는 Mode
Micro SD		Micro SD를 통해 Configuration할 경우 사용하는 Mode
QSPI		QSPI를 통해 Configuration할 경우 사용하는 Mode

4.2.6. FPGA Status LED

- FPGA의 Status 확인을 위한 LED를 제공하며, 각 LED의 Description은 아래와 같다.

<FPGA Status LED Description>

LED	Description
FPGA Done (LD3)	FPGA Configuration Status LED로 Configuration 이 완료 되면 LED 점등 (Green)
PS Error (LD1) (1)	Platform management Unit의 전원 이상이 있을 경우, LED 점등 (Red)
PS Error status (LD2) (1)	Secure lockdown state일 경우 LED 점등 (Green)

Notes:

1. PS Error, PS Error status에 대한 자세한 설명은 Xilinx "Zynq UltraScale+ MPSoC Technical Reference Manual (UG1085)를 참고한다.

4.2.7. USB to JTAG Module & JTAG Header

- FPGA의 JTAG Mode Configuration을 위해 Micro USB Connector를 지원하는 Digilent 社의 "JTAG-SMT2" 및 6-pin JTAG Header (H4)를 적용 하였으며, Pin Description은 아래와 같다.

<JTAG Pin Description>

Pin Number	Description
1-pin	VCC : JTAG Cable에 공급되는 전원 핀
2-pin	GND : JTAG Cable에 공급되는 전원 핀
3-pin	TCK : JTAG Clock 입력 핀
4-pin	TDO : JTAG Data 출력 핀
5-pin	TDI : JTAG Data 입력 핀
6-pin	TMS : JTAG Mode 선택 입력 핀

4.2.8. Micro SD Connector

- FPGA의 SD Mode Configuration을 위해 ALPS 社의 "SCHA5B0200" Micro SD Connector를 적용하였다.

<Micro SD Interface Description>

Signal Name	FPGA Pin	Description
MIO44_SDIO_PROTECT	N24	SD Interface Write Protect
MIO45_SDIO_DETECT	P24	SD Interface Card Detect
MIO46_SDIO_DAT0	J25	SD Interface Data 0
MIO47_SDIO_DAT1	L25	SD Interface Data 1
MIO48_SDIO_DAT2	M25	SD Interface Data 2
MIO49_SDIO_DAT3	K25	SD Interface Data 3
MIO50_SDIO_CMD	P25	SD Interface Command
MIO51_SDIO_CLK	N25	SD Interface Clock

4.2.9. QSPI

- FPGA의 QSPI Mode Configuration을 위해 Micron 社의 "MT25QU512ABB8E12" 2개를 적용하였다.

<QSPI Interface Description>

Signal Name	FPGA Pin	Description
MIO0_QSPI_LWR_CLK	AF16	Lower QSPI Clock output
MIO1_QSPI_LWR_DQ1	AJ16	Lower QSPI Data 1
MIO2_QSPI_LWR_DQ2	AD16	Lower QSPI Data 2
MIO3_QSPI_LWR_DQ3	AG16	Lower QSPI Data 3
MIO4_QSPI_LWR_DQ0	AH16	Lower QSPI Data 0
MIO5_QSPI_LWR_CS_B	AM15	Lower QSPI Chip Select
MIO7_QSPI_UPR_CS_B	AD17	Upper QSPI Chip Select
MIO8_QSPI_UPR_DQ0	AE17	Upper QSPI Data 0
MIO9_QSPI_UPR_DQ1	AP15	Upper QSPI Data 1
MIO10_QSPI_UPR_DQ2	AH17	Upper QSPI Data 2
MIO11_QSPI_UPR_DQ3	AF17	Upper QSPI Data 3
MIO12_QSPI_UPR_CLK	AJ17	Upper QSPI Clock output

4.2.10. FPGA Reset & User Push Switch

- FPGA의 PS Reset Switch로 각 Switch의 Description은 아래와 같다.

<FPGA PS Reset Switch Description>

Switch	Description
PS-POR Reset (SW3)	FPGA Power On Reset (Active Low)
PS SRST (SW4)	FPGA System Reset (Active Low)

- 사용자 Push Switch로 Switch를 누를 때마다 FPGA에 High 신호를 인가 하며, Description은 아래와 같다.

<User Push Switch Description>

Switch	Signal Name	FPGA Pin	I/O Standard	Description
PUSH0 (SW5)	USER_SW0	AD5	LVCMOS18	User Push Switch [3:0] (Active High)
PUSH1 (SW6)	USER_SW1	AG1		
PUSH2 (SW7)	USER_SW2	AA3		
PUSH3 (SW8)	USER_SW3	AB1		

4.2.11. User LED

- 사용자 LED로 High 신호를 인가하면 LED가 ON 되며, Description은 아래와 같다.

<User LED Description>

LED	Signal Name	FPGA Pin	I/O Standard	Description
LED0 (LD5)	USER_LED0	AA8	LVCMOS18	User LED [3:0] Active High
LED1 (LD6)	USER_LED1	V9		
LED2 (LD7)	USER_LED2	K10		
LED3 (LD8)	USER_LED3	K14		

4.2.12. DDR4 SO-DIMM(PS)

- ULTRON Board는 대용량 Data 처리를 위한 DDR4 SO-DIMM을 지원한다.
- DDR4 SO-DIMM의 Density는 최대 32GB까지 지원하며, Data rate는 최대 2400Mb/s 까지 지원한다. (기본 구성은 4GB를 제공 한다.)

- **ULTRON Board의 PS 영역에서 사용하는 DDR4 메모리는 상기의 내용과 같이 SO-DIMM을 지원하는데, 당사에서는 DDR4 SO-DIMM 메모리 수급 영향에 따라서 M471A5143EB0-CPB 의 Dual Rank(양면) 타입과 M471A5244BB0-CPB의 Single Rank(단면) 타입을 지원한다.**
  Ultron 보드를 확인하여 M471A5143EB0-CPB 의 dual rank(양면) 타입의 SO-DIMM 이 달려 있으면 ZCU102 보드로 Preset 또는 다음의 첫 번째 그림과 같이 셋팅하여 사용하면 M471A5143EB0-CPB 의 dual rank(양면) 타입으로 셋팅 되어 PS영역의 DDR4 메모리를 사용할 수 있고, 만약 M471A5244BB0-CPB의 single rank(단면) 타입이 달려 있으면 다음의 두 번째 그림과 같이 셋팅하여 PS영역의 DDR4 메모리를 사용해야 한다.

◆ **M471A5143EB0-CPB 의 Dual Rank(양면) 타입(GA0, 1 둘 다 사용)**

DDR Configuration

Memory Inteface Device Frequency (MHz) 1067 (Actual Interface :1066.656006)

DDR Controller Options

Memory Type	DDR 4	Effective DRAM Bus Width	64 Bit
Components	UDIMM	ECC	Disabled

DDR Memory Options

Speed Bin (use tooltip)	DDR4 2133P	DRAM IC Bus Width	8 Bits
Cas Latency (cycles)	15	DRAM Device Capacity (per die)	4096 MBits
RAS to CAS Delay (cycles)	15	Bank Group Address Count (Bits)	2
Precharge Time (cycles)	15	Bank Address Count (Bits)	2
Cas Write Latency (cycles)	14	Row Address Count (Bits)	15
tRC (ns)	47.06	Column Address Count (Bits)	10
tRASmin (ns)	33	Dual Rank	
tFAW (ns)	30.0		
Additive Latency (cycles)	0	DDR Size (in Hexa)	0xFFFFFFFF (4GB)

<PS DDR4 Dual Rank SO-DIMM 윗면(좌) 과 아랫면(우)>

◆ **M471A5244BB0-CPB의 Single Rank(단면) 타입(GA0 만 사용)**

DDR Configuration

Clocking Options

Memory Inteface Device Frequency (MHz) 1067 (Actual Interface :1066.656006)

DDR Controller Options

Memory Type	DDR 4	Effective DRAM Bus Width	64 Bit
Components	UDIMM	ECC	Disabled

DDR Memory Options

Speed Bin (use tooltip)	DDR4 2133P	DRAM IC Bus Width	16 Bits
Cas Latency (cycles)	15	DRAM Device Capacity (per die)	8192 MBits
RAS to CAS Delay (cycles)	15	Bank Group Address Count (Bits)	1
Precharge Time (cycles)	15	Bank Address Count (Bits)	2
Cas Write Latency (cycles)	14	Row Address Count (Bits)	16
tRC (ns)	47.06	Column Address Count (Bits)	10
tRASmin (ns)	33	Dual Rank	
tFAW (ns)	30.0		
Additive Latency (cycles)	0	DDR Size (in Hexa)	0xFFFFFFFF (4GB)

<PS DDR4 Single Rank SO-DIMM 윗면(좌) 과 아랫면(우)>

4.2.13. DDR4 Component(PL)

- 대용량 Data 처리를 위한 Micron 社의 DDR4 Component "MT40A256M16GE-075E:B"를 적용하였다.
- DDR4 Component의 Density는 4Gb까지 지원하며, Data rate는 2666MT/s까지 지원한다.

4.2.14. FMC LPC

- 다른 외부 Board와의 확장을 위하여 Samtec 社의 FMC LPC "ASP-134603-01"을 적용하였으며, Description은 아래와 같다.

<FMC LPC Description>

LPC Pin	Signal Name	FPGA Pin	I/O Standard
C2	FMC_LPC_DP0_C2M_P	F29	
C3	FMC_LPC_DP0_C2M_N	F30	
C6	FMC_LPC_DP0_M2C_P	E31	
C7	FMC_LPC_DP0_M2C_N	E32	
C10	FMC_LPC_LA06_P	AH2	LVDS
C11	FMC_LPC_LA06_N	AJ2	LVDS
C14	FMC_LPC_LA10_P	AH4	LVDS
C15	FMC_LPC_LA10_N	AJ4	LVDS
C18	FMC_LPC_LA14_P	AH7	LVDS
C19	FMC_LPC_LA14_N	AH6	LVDS
C22	FMC_LPC_LA18_CC_P	Y8	LVDS
C23	FMC_LPC_LA18_CC_N	Y7	LVDS
C26	FMC_LPC_LA27_P	U10	LVDS
C27	FMC_LPC_LA27_N	T10	LVDS
C30	FMC_LPC_SCL		
C31	FMC_LPC_SDA		
C34	GND		
C35	VCC12_SW		
C37	VCC12_SW		
C39	UTIL_3V3		
D4	FMC_LPC_GBTCLK0_M2C_P	G27	
D5	FMC_LPC_GBTCLK0_M2C_N	G28	
D8	FMC_LPC_LA01_CC_P	AJ6	LVDS
D9	FMC_LPC_LA01_CC_N	AJ5	LVDS
D11	FMC_LPC_LA05_P	AG3	LVDS
D12	FMC_LPC_LA05_N	AH3	LVDS
D14	FMC_LPC_LA09_P	AE2	LVDS

D15	FMC_LPC_LA09_N	AE1	LVDS
D17	FMC_LPC_LA13_P	AG8	LVDS
D18	FMC_LPC_LA13_N	AH8	LVDS
D20	FMC_LPC_LA17_CC_P	Y5	LVDS
D21	FMC_LPC_LA17_CC_N	AA5	LVDS
D23	FMC_LPC_LA23_P	AE12	LVDS
D24	FMC_LPC_LA23_N	AF12	LVDS
D26	FMC_LPC_LA26_P	T12	LVDS
D27	FMC_LPC_LA26_N	R12	LVDS
D29	FMC_LPC_TCK_BUF		
D30	FMC_HPC_TDO_LPC_TDI		
D31	FMC_LPC_TDO		
D32	UTIL_3V3		
D33	FMC_LPC_TMS_BUF		
D34	NC		
D35	GND		
D36	UTIL_3V3		
D38	UTIL_3V3		
D40	UTIL_3V3		
G2	FMC_LPC_CLK1_M2C_P	P10	LVDS
G3	FMC_LPC_CLK1_M2C_N	P9	LVDS
G6	FMC_LPC_LA00_CC_P	AE5	LVDS
G7	FMC_LPC_LA00_CC_N	AF5	LVDS
G9	FMC_LPC_LA03_P	AH1	LVDS
G10	FMC_LPC_LA03_N	AJ1	LVDS
G12	FMC_LPC_LA08_P	AE3	LVDS
G13	FMC_LPC_LA08_N	AF3	LVDS
G15	FMC_LPC_LA12_P	AD7	LVDS
G16	FMC_LPC_LA12_N	AD6	LVDS
G18	FMC_LPC_LA16_P	AG10	LVDS
G19	FMC_LPC_LA16_N	AG9	LVDS
G21	FMC_LPC_LA20_P	AB11	LVDS
G22	FMC_LPC_LA20_N	AB10	LVDS
G24	FMC_LPC_LA22_P	AF11	LVDS
G25	FMC_LPC_LA22_N	AG11	LVDS
G27	FMC_LPC_LA25_P	AE10	LVDS
G28	FMC_LPC_LA25_N	AF10	LVDS
G30	FMC_LPC_LA29_P	W12	LVDS

G31	FMC_LPC_LA29_N	W11	LVDS
G33	FMC_LPC_LA31_P	AF6	LVDS
G34	FMC_LPC_LA31_N	AG6	LVDS
G36	FMC_LPC_LA33_P	AG5	LVDS
G37	FMC_LPC_LA33_N	AG4	LVDS
G39	VADJ_FMC		1.8V
H1	NC		
H2	FMC_LPC_PRSNT_M2C_B		
H4	FMC_LPC_CLK0_M2C_P	AE7	LVDS
H5	FMC_LPC_CLK0_M2C_N	AF7	LVDS
H7	FMC_LPC_LA02_P	AD2	LVDS
H8	FMC_LPC_LA02_N	AD1	LVDS
H10	FMC_LPC_LA04_P	AF2	LVDS
H11	FMC_LPC_LA04_N	AF1	LVDS
H13	FMC_LPC_LA07_P	AD4	LVDS
H14	FMC_LPC_LA07_N	AE4	LVDS
H16	FMC_LPC_LA11_P	AE8	LVDS
H17	FMC_LPC_LA11_N	AF8	LVDS
H19	FMC_LPC_LA15_P	AD10	LVDS
H20	FMC_LPC_LA15_N	AE9	LVDS
H22	FMC_LPC_LA19_P	AA11	LVDS
H23	FMC_LPC_LA19_N	AA10	LVDS
H25	FMC_LPC_LA21_P	AC12	LVDS
H26	FMC_LPC_LA21_N	AC11	LVDS
H28	FMC_LPC_LA24_P	AH12	LVDS
H29	FMC_LPC_LA24_N	AH11	LVDS
H31	FMC_LPC_LA28_P	T13	LVDS
H32	FMC_LPC_LA28_N	R13	LVDS
H34	FMC_LPC_LA30_P	R10	LVDS
H35	FMC_LPC_LA30_N	R9	LVDS
H37	FMC_LPC_LA32_P	AB9	LVDS
H38	FMC_LPC_LA32_N	AC9	LVDS
H40	VADJ_FMC		1.8V

4.2.15. FMC HPC

- 다른 외부 Board와의 확장을 위하여 Samtec 社의 FMC HPC "ASP-134486-01"을 적용하였으며, Description은 아래와 같다.

  <FMC HPC Description>

HPC Pin	Signal Name	FPGA Pin	I/O Standard
A2	FMC_HPC_DP1_M2C_P	J4	
A3	FMC_HPC_DP1_M2C_N	J3	
A6	FMC_HPC_DP2_M2C_P	F2	
A7	FMC_HPC_DP2_M2C_N	F1	
A10	FMC_HPC_DP3_M2C_P	K2	
A11	FMC_HPC_DP3_M2C_N	K1	
A14	FMC_HPC_DP4_M2C_P	L4	
A15	FMC_HPC_DP4_M2C_N	L3	
A18	FMC_HPC_DP5_M2C_P	P2	
A19	FMC_HPC_DP5_M2C_N	P1	
A22	FMC_HPC_DP1_C2M_P	H6	
A23	FMC_HPC_DP1_C2M_N	H5	
A26	FMC_HPC_DP2_C2M_P	F6	
A27	FMC_HPC_DP2_C2M_N	F5	
A30	FMC_HPC_DP3_C2M_P	K6	
A31	FMC_HPC_DP3_C2M_N	K5	
A34	FMC_HPC_DP4_C2M_P	M6	
A35	FMC_HPC_DP4_C2M_N	M5	
A38	FMC_HPC_DP5_C2M_P	P6	
A39	FMC_HPC_DP5_C2M_N	P5	
B1	NC		
B4	FMC_HPC_DP9_M2C_P	C4	
B5	FMC_HPC_DP9_M2C_N	C3	
B8	FMC_HPC_DP8_M2C_P	D2	
B9	FMC_HPC_DP8_M2C_N	D1	
B12	FMC_HPC_DP7_M2C_P	M2	
B13	FMC_HPC_DP7_M2C_N	M1	
B16	FMC_HPC_DP6_M2C_P	T2	
B17	FMC_HPC_DP6_M2C_N	T1	
B20	FMC_HPC_GBTCLK1_M2C_P	L8	
B21	FMC_HPC_GBTCLK1_M2C_N	L7	
B24	FMC_HPC_DP9_C2M_P	D6	
B25	FMC_HPC_DP9_C2M_N	D5	
B28	FMC_HPC_DP8_C2M_P	E4	
B29	FMC_HPC_DP8_C2M_N	E3	
B32	FMC_HPC_DP7_C2M_P	N4	
B33	FMC_HPC_DP7_C2M_N	N3	

B36	FMC_HPC_DP6_C2M_P	R4	
B37	FMC_HPC_DP6_C2M_N	R3	
B40	NC		
C2	FMC_HPC_DP0_C2M_P	G4	
C3	FMC_HPC_DP0_C2M_N	G3	
C6	FMC_HPC_DP0_M2C_P	H2	
C7	FMC_HPC_DP0_M2C_N	H1	
C10	FMC_HPC_LA06_P	AC2	LVDS
C11	FMC_HPC_LA06_N	AC1	LVDS
C14	FMC_HPC_LA10_P	W5	LVDS
C15	FMC_HPC_LA10_N	W4	LVDS
C18	FMC_HPC_LA14_P	AC7	LVDS
C19	FMC_HPC_LA14_N	AC6	LVDS
C22	FMC_HPC_LA18_CC_P	N9	LVDS
C23	FMC_HPC_LA18_CC_N	N8	LVDS
C26	FMC_HPC_LA27_P	M10	LVDS
C27	FMC_HPC_LA27_N	L10	LVDS
C30	FMC_HPC_SCL		
C31	FMC_HPC_SDA		
C34	GND		
C35	VCC12_SW		
C37	VCC12_SW		
C39	UTIL_3V3		
D4	FMC_HPC_GBTCLK0_M2C_P	G8	
D5	FMC_HPC_GBTCLK0_M2C_N	G7	
D8	FMC_HPC_LA01_CC_P	AB4	LVDS
D9	FMC_HPC_LA01_CC_N	AC4	LVDS
D11	FMC_HPC_LA05_P	AB3	LVDS
D12	FMC_HPC_LA05_N	AC3	LVDS
D14	FMC_HPC_LA09_P	W2	LVDS
D15	FMC_HPC_LA09_N	W1	LVDS
D17	FMC_HPC_LA13_P	AB8	LVDS
D18	FMC_HPC_LA13_N	AC8	LVDS
D20	FMC_HPC_LA17_CC_P	P11	LVDS
D21	FMC_HPC_LA17_CC_N	N11	LVDS
D23	FMC_HPC_LA23_P	L16	LVDS
D24	FMC_HPC_LA23_N	K16	LVDS
D26	FMC_HPC_LA26_P	L15	LVDS

D27	FMC_HPC_LA26_N	K15	LVDS
D29	FMC_HPC_TCK_BUF		
D30	FPGA_TDO_FMC_TDI_BUF		
D31	FMC_HPC_TDO_LPC_TDI		
D32	UTIL_3V3		
D33	FMC_HPC_TMS_BUF		
D34	NC		
D35	GND		
D36	UTIL_3V3		
D38	UTIL_3V3		
D40	UTIL_3V3		
E2	FMC_HPC_HA01_CC_P	G18	LVDS
E3	FMC_HPC_HA01_CC_N	G19	LVDS
E6	FMC_HPC_HA05_P	L19	LVDS
E7	FMC_HPC_HA05_N	K19	LVDS
E9	FMC_HPC_HA09_P	J19	LVDS
E10	FMC_HPC_HA09_N	J20	LVDS
E12	FMC_HPC_HA13_P	E20	LVDS
E13	FMC_HPC_HA13_N	D20	LVDS
E15	FMC_HPC_HA16_P	C21	LVDS
E16	FMC_HPC_HA16_N	B21	LVDS
E18	FMC_HPC_HA20_P	B20	LVDS
E19	FMC_HPC_HA20_N	A20	LVDS
E21	FMC_HPC_HB03_P	J17	LVDS
E22	FMC_HPC_HB03_N	H17	LVDS
E24	FMC_HPC_HB05_P	AE15	LVDS
E25	FMC_HPC_HB05_N	AE14	LVDS
E27	FMC_HPC_HB09_P	AE13	LVDS
E28	FMC_HPC_HB09_N	AF13	LVDS
E30	FMC_HPC_HB13_P	AJ15	LVDS
E31	FMC_HPC_HB13_N	AJ14	LVDS
E33	FMC_HPC_HB19_P	AL13	LVDS
E34	FMC_HPC_HB19_N	AM13	LVDS
E36	FMC_HPC_HB21_P	AN12	LVDS
E37	FMC_HPC_HB21_N	AP12	LVDS
E39	VADJ_FMC		1.8V
F4	FMC_HPC_HA00_CC_P	F17	LVDS
F5	FMC_HPC_HA00_CC_N	F18	LVDS

F7	FMC_HPC_HA04_P	L20	LVDS
F8	FMC_HPC_HA04_N	K20	LVDS
F10	FMC_HPC_HA08_P	J21	LVDS
F11	FMC_HPC_HA08_N	H21	LVDS
F13	FMC_HPC_HA12_P	D21	LVDS
F14	FMC_HPC_HA12_N	C22	LVDS
F16	FMC_HPC_HA15_P	A21	LVDS
F17	FMC_HPC_HA15_N	A22	LVDS
F19	FMC_HPC_HA19_P	H18	LVDS
F20	FMC_HPC_HA19_N	H19	LVDS
F22	FMC_HPC_HB02_P	AF15	LVDS
F23	FMC_HPC_HB02_N	AG15	LVDS
F25	FMC_HPC_HB04_P	AG14	LVDS
F26	FMC_HPC_HB04_N	AG13	LVDS
F28	FMC_HPC_HB08_P	AH14	LVDS
F29	FMC_HPC_HB08_N	AH13	LVDS
F31	FMC_HPC_HB12_P	AK13	LVDS
F32	FMC_HPC_HB12_N	AL12	LVDS
F34	FMC_HPC_HB16_P	AM14	LVDS
F35	FMC_HPC_HB16_N	AN13	LVDS
F37	FMC_HPC_HB20_P	AN14	LVDS
F38	FMC_HPC_HB20_N	AP14	LVDS
F40	VADJ_FMC		1.8V
G2	FMC_HPC_CLK1_M2C_P	T8	LVDS
G3	FMC_HPC_CLK1_M2C_N	R8	LVDS
G6	FMC_HPC_LA00_CC_P	Y4	LVDS
G7	FMC_HPC_LA00_CC_N	Y3	LVDS
G9	FMC_HPC_LA03_P	Y2	LVDS
G10	FMC_HPC_LA03_N	Y1	LVDS
G12	FMC_HPC_LA08_P	V4	LVDS
G13	FMC_HPC_LA08_N	V3	LVDS
G15	FMC_HPC_LA12_P	W7	LVDS
G16	FMC_HPC_LA12_N	W6	LVDS
G18	FMC_HPC_LA16_P	Y12	LVDS
G19	FMC_HPC_LA16_N	AA12	LVDS
G21	FMC_HPC_LA20_P	N13	LVDS
G22	FMC_HPC_LA20_N	M13	LVDS
G24	FMC_HPC_LA22_P	M15	LVDS

G25	FMC_HPC_LA22_N	M14	LVDS
G27	FMC_HPC_LA25_P	M11	LVDS
G28	FMC_HPC_LA25_N	L11	LVDS
G30	FMC_HPC_LA29_P	U9	LVDS
G31	FMC_HPC_LA29_N	U8	LVDS
G33	FMC_HPC_LA31_P	V8	LVDS
G34	FMC_HPC_LA31_N	V7	LVDS
G36	FMC_HPC_LA33_P	V12	LVDS
G37	FMC_HPC_LA33_N	V11	LVDS
G39	VADJ_FMC		1.8V
H1	NC		
H2	FMC_HPC_PRSNT_M2C_B		
H4	FMC_HPC_CLK0_M2C_P	AA7	LVDS
H5	FMC_HPC_CLK0_M2C_N	AA6	LVDS
H7	FMC_HPC_LA02_P	V2	LVDS
H8	FMC_HPC_LA02_N	V1	LVDS
H10	FMC_HPC_LA04_P	AA2	LVDS
H11	FMC_HPC_LA04_N	AA1	LVDS
H13	FMC_HPC_LA07_P	U5	LVDS
H14	FMC_HPC_LA07_N	U4	LVDS
H16	FMC_HPC_LA11_P	AB6	LVDS
H17	FMC_HPC_LA11_N	AB5	LVDS
H19	FMC_HPC_LA15_P	Y10	LVDS
H20	FMC_HPC_LA15_N	Y9	LVDS
H22	FMC_HPC_LA19_P	L13	LVDS
H23	FMC_HPC_LA19_N	K13	LVDS
H25	FMC_HPC_LA21_P	P12	LVDS
H26	FMC_HPC_LA21_N	N12	LVDS
H28	FMC_HPC_LA24_P	L12	LVDS
H29	FMC_HPC_LA24_N	K12	LVDS
H31	FMC_HPC_LA28_P	T7	LVDS
H32	FMC_HPC_LA28_N	T6	LVDS
H34	FMC_HPC_LA30_P	V6	LVDS
H35	FMC_HPC_LA30_N	U6	LVDS
H37	FMC_HPC_LA32_P	U11	LVDS
H38	FMC_HPC_LA32_N	T11	LVDS
H40	VADJ_FMC		1.8V
J2	FMC_HPC_CLK3_M2C_P	E8	

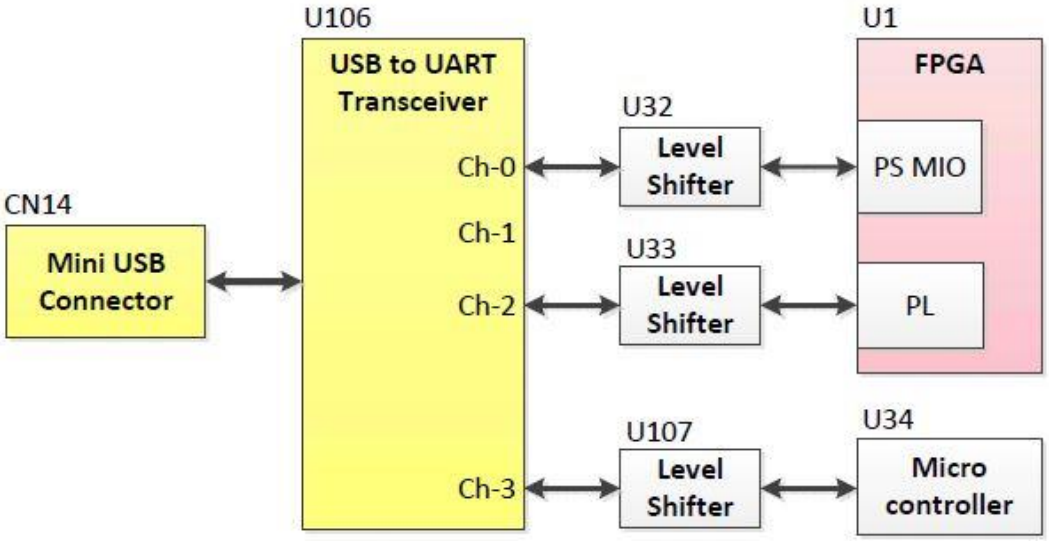
J3	FMC_HPC_CLK3_M2C_N	E7	
J6	FMC_HPC_HA03_P	L18	LVDS
J7	FMC_HPC_HA03_N	K18	LVDS
J9	FMC_HPC_HA07_P	L17	LVDS
J10	FMC_HPC_HA07_N	K17	LVDS
J12	FMC_HPC_HA11_P	A17	LVDS
J13	FMC_HPC_HA11_N	A18	LVDS
J15	FMC_HPC_HA14_P	B16	LVDS
J16	FMC_HPC_HA14_N	A16	LVDS
J18	FMC_HPC_HA18_P	B15	LVDS
J19	FMC_HPC_HA18_N	A15	LVDS
J21	FMC_HPC_HA22_P	A13	LVDS
J22	FMC_HPC_HA22_N	A12	LVDS
J24	FMC_HPC_HB01_P	C12	LVDS
J25	FMC_HPC_HB01_N	B12	LVDS
J27	FMC_HPC_HB07_P	E14	LVDS
J28	FMC_HPC_HB07_N	D14	LVDS
J30	FMC_HPC_HB11_P	E12	LVDS
J31	FMC_HPC_HB11_N	D12	LVDS
J33	FMC_HPC_HB15_P	D16	LVDS
J34	FMC_HPC_HB15_N	C16	LVDS
J36	FMC_HPC_HB18_P	E15	LVDS
J37	FMC_HPC_HB18_N	D15	LVDS
J39	NC		
K1	NC		
K4	FMC_HPC_CLK2_M2C_P	J8	
K5	FMC_HPC_CLK2_M2C_N	J7	
K7	FMC_HPC_HA02_P	C18	LVDS
K8	FMC_HPC_HA02_N	C19	LVDS
K10	FMC_HPC_HA06_P	B18	LVDS
K11	FMC_HPC_HA06_N	B19	LVDS
K13	FMC_HPC_HA10_P	D17	LVDS
K14	FMC_HPC_HA10_N	C17	LVDS
K16	FMC_HPC_HA17_CC_P	E19	LVDS
K17	FMC_HPC_HA17_CC_N	D19	LVDS
K19	FMC_HPC_HA21_P	C14	LVDS
K20	FMC_HPC_HA21_N	B14	LVDS
K22	FMC_HPC_HA23_P	C13	LVDS

K23	FMC_HPC_HA23_N	B13	LVDS
K25	FMC_HPC_HB00_CC_P	E17	LVDS
K26	FMC_HPC_HB00_CC_N	E18	LVDS
K28	FMC_HPC_HB06_CC_P	G20	LVDS
K29	FMC_HPC_HB06_CC_N	F20	LVDS
K31	FMC_HPC_HB10_P	F13	LVDS
K32	FMC_HPC_HB10_N	E13	LVDS
K34	FMC_HPC_HB14_P	F16	LVDS
K35	FMC_HPC_HB14_N	F15	LVDS
K37	FMC_HPC_HB17_CC_P	E22	LVDS
K38	FMC_HPC_HB17_CC_N	D22	LVDS
K40	NC		

4.2.16. Mini USB (UART) Connector

- UART Interface를 위해 EDAC 사의 "690-005-299-043" Mini USB Connector를 적용하였으며, Block-Diagram 및 Description은 아래와 같다.

<UART Interface Block-Diagram>



<UART Interface Description>

UART	Signal Name	FPGA Pin	I/O Standard
FGPA PS	MIO18_UART0_RXD	AE18	-
	MIO19_UART0_TXD	AL17	-
FPGA PL	UART_TXD_FPGA_RXD	J12	LVCMOS33
	UART_RXD_FPGA_TXD	H12	
Micro Controller	UART3_TXD_O_MSP430_UCA0_RXD	U34-26pin	-
	UART3_RXD_I_MSP430_UCA0_TXD	U34-25pin	-

4.2.17. DSUB (RS-232) Connector

- RS-232 통신을 위한 DSUB 9-pin (Male) Connector를 적용하였으며, Description은 아래와 같다.

<RS-232 Interface Description>

Signal Name	FPGA Pin	I/O Standard	Description
FPGA_PL_RS232_TXD	H13	LVCMOS33	RS-232 Transmit Data
FPGA_PL_RS232_RXD	G13		RS-232 Receive Data

4.2.18. Ethernet RJ-45 Connector

- Ethernet Connector 1-Port를 제공하며 HALO 社의 "HFJ11-1G01E-L12RL"을 적용하였으며, Ethernet Interface를 위한 Description은 아래와 같다.

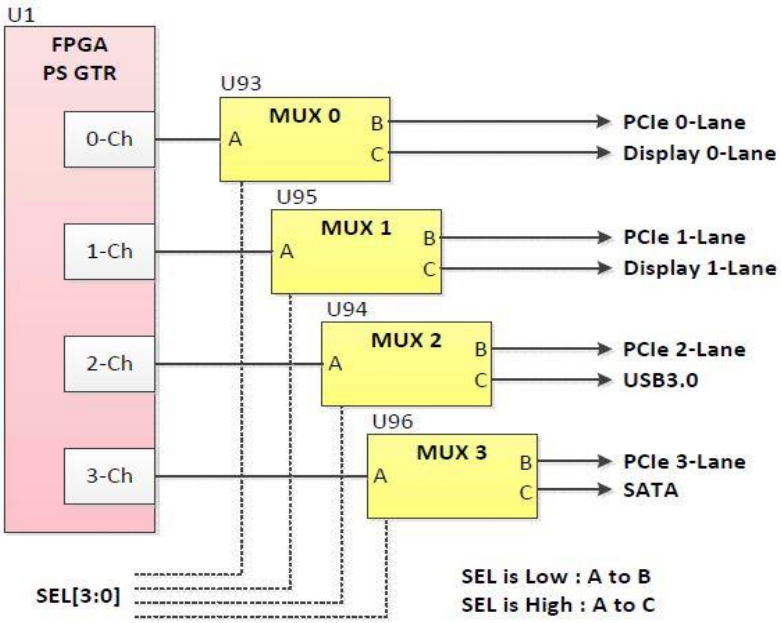
<Ethernet Interface Description>

PS MIO	FPGA Pin	Signal Name	Description
MIO 64	A25	MIO64_ENET_TX_CLK	Ethernet transmit Clock
MIO 65	A26	MIO65_ENET_TX_D0	Ethernet transmit Data 0
MIO 66	A27	MIO66_ENET_TX_D1	Ethernet transmit Data 1
MIO 67	B25	MIO67_ENET_TX_D2	Ethernet transmit Data 2
MIO 68	B26	MIO68_ENET_TX_D3	Ethernet transmit Data 3
MIO 69	B27	MIO69_ENET_TX_CTRL	Ethernet transmit Control
MIO 70	C26	MIO70_ENET_RX_CLK	Ethernet Received Clock
MIO 71	C27	MIO71_ENET_RX_D0	Ethernet Received Data 0
MIO 72	E25	MIO72_ENET_RX_D1	Ethernet Received Data 1
MIO 73	H24	MIO73_ENET_RX_D2	Ethernet Received Data 2
MIO 74	G25	MIO74_ENET_RX_D3	Ethernet Received Data 3
MIO 75	D25	MIO75_ENET_RX_CTRL	Ethernet Received Control
MIO 76	H25	MIO76_ENET_MDC	Management Data Clock
MIO 77	F25	MIO77_ENET_MDIO	Management Data I/O

4.2.19. FPGA PS GTR MUX

- PS GTR Transceiver에 MUX를 적용하여 PCI Express, DisplayPort, USB3.0 및 SATA Interface를 선택적으로 사용할 수 있도록 설계하였으며, PS GTR Block-Diagram 및 MUX에 대한 Description은 아래와 같다.

<PS GTR Block-Diagram>



<PS GTR Description>

Channel	FPGA Pin	Signal Name	비고
0-Ch	AB29	GTR_LANE0_TX_P	MUX0
	AB30	GTR_LANE0_TX_N	
	AB33	GTR_LANE0_RX_P	
	AB34	GTR_LANE0_RX_N	
1-Ch	Y29	GTR_LANE1_TX_P	MUX1
	Y30	GTR_LANE1_TX_N	
	AA31	GTR_LANE1_RX_P	
	AA32	GTR_LANE1_RX_N	
2-Ch	W31	GTR_LANE2_TX_P	MUX2
	W32	GTR_LANE2_TX_N	
	Y33	GTR_LANE2_RX_P	
	Y34	GTR_LANE2_RX_N	
3-Ch	V29	GTR_LANE3_TX_P	MUX3
	V30	GTR_LANE3_TX_N	
	V33	GTR_LANE3_RX_P	
	V34	GTR_LANE3_RX_N	
RefClk0	AA27	GTR_REF_CLK_PCIE_P	100MHz

	AA28	GTR_REF_CLK_PCIE_N	
RefClk1	W27	GTR_REF_CLK_SATA_P	125MHz
	W28	GTR_REF_CLK_SATA_N	
RefClk2	U27	GTR_REF_CLK_USB3_P	24MHz
	U28	GTR_REF_CLK_USB3_N	
RefClk3	U31	GTR_REF_CLK_DP_P	27MHz
	U32	GTR_REF_CLK_DP_N	

<PS GTR Connector Functionality>

SEL[3:0]	PCIe Connector	DP Connector	USB Connector	SATA Connector
0000	PCIe Gen2 x 4	NC	NC	NC
1111	NC	DP0, DP1	USB	SATA1
1100	PCIe Gen2 x 2	NC	USB	SATA1
1110	PCIe Gen2 x 1	DP0	USB	SATA1

4.2.20. PCI Express x 4Lane Connector

- PCIe Interface를 위해 4-Lane Connector를 제공하며, Amphenol 社의 "10061913-101CLF"를 적용하였으며, Description은 아래와 같다.
- PCIe Interface를 사용하기 위해서는 PS GTR MUX를 Control 해야 하며 자세한 사항은 4.2.19 항목을 참고한다.

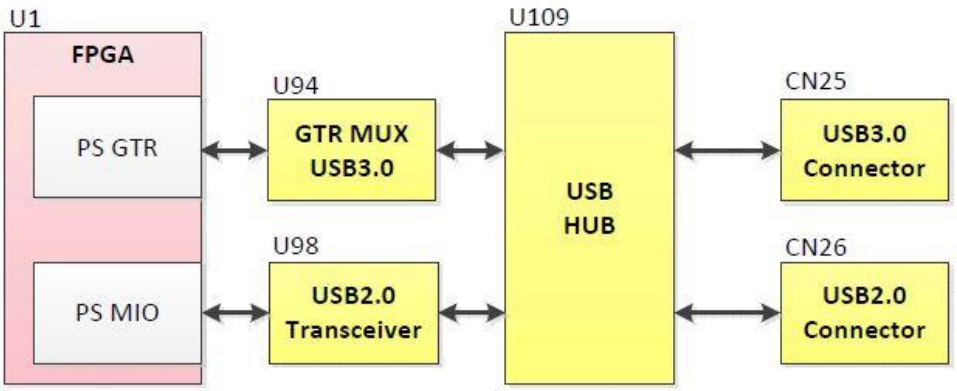
<PCI Express Interface Description>

PS	FPGA Pin	Signal Name		Description
0-Ch	AB29	GTR_LANE0_TX_P	PCIE_TX0_P	PCIe 0-Lane Data
	AB30	GTR_LANE0_TX_N	PCIE_TX0_N	
	AB33	GTR_LANE0_RX_P	PCIE_RX0_P	
	AB34	GTR_LANE0_RX_N	PCIE_RX0_N	
1-Ch	Y29	GTR_LANE1_TX_P	PCIE_TX1_P	PCIe 1-Lane Data
	Y30	GTR_LANE1_TX_N	PCIE_TX1_N	
	AA31	GTR_LANE1_RX_P	PCIE_RX1_P	
	AA32	GTR_LANE1_RX_N	PCIE_RX1_N	
2-Ch	W31	GTR_LANE2_TX_P	PCIE_TX2_P	PCIe 2-Lane Data
	W32	GTR_LANE2_TX_N	PCIE_TX2_N	
	Y33	GTR_LANE2_RX_P	PCIE_RX2_P	
	Y34	GTR_LANE2_RX_N	PCIE_RX2_N	
3-Ch	V29	GTR_LANE3_TX_P	PCIE_TX3_P	PCIe 3-Lane Data
	V30	GTR_LANE3_TX_N	PCIE_TX3_N	
	V33	GTR_LANE3_RX_P	PCIE_RX3_P	
	V34	GTR_LANE3_RX_N	PCIE_RX3_N	
MIO31	J22	MIO31_PCIE_RESET_N		PCIe Reset (Active Low)
-	-	PCIE_SLOT_CLK_P		PCIe Reference Clock
-	-	PCIE_SLOT_CLK_N		PCIe Reference Clock
-	-	PCIE_CLK_DIR_SEL		PCIe Clock Direction

4.2.21. USB3.0 A-Type Connector

- USB3.0 Interface를 위해 A-Type Connector 1-port를 제공하며, Amphenol 社의 "10117835-002LF"를 적용하였다.
- USB Interface의 Block-Diagram은 아래와 같으며, PS GTR MUX는 4.2.19 항목을 참고한다.

<USB Interface Block-Diagram>



<USB3.0 Interface Description>

PS GTR	FPGA Pin	Signal Name		Description
2-Ch	W31	GTR_LANE2_TX_P	GT2_USB0_TX_P	USB3.0 Data
	W32	GTR_LANE2_TX_N	GT2_USB0_TX_N	
	Y33	GTR_LANE2_RX_P	GT2_USB0_RX_P	
	Y34	GTR_LANE2_RX_N	GT2_USB0_RX_N	

4.2.22. USB2.0 A-Type Connector

- USB2.0 Interface를 위해 A-Type Connector 1-port를 제공하며, Amphenol 社의 "87520-0010BLF"를 적용하였으며, Description은 아래와 같다.

<USB2.0 Interface Description>

PS MIO	FPGA Pin	Signal Name	Description
MIO 52	F22	MIO52_USB_CLK	USB Interface Clock
MIO 53	E23	MIO53_USB_DIR	USB Interface Direction
MIO 54	F23	MIO54_USB_DATA2	USB Interface Data 2
MIO 55	B23	MIO55_USB_NXT	USB Interface transceiver asserts
MIO 56	C23	MIO56_USB_DATA0	USB Interface Data 0
MIO 57	A23	MIO57_USB_DATA1	USB Interface Data 1
MIO 58	G23	MIO58_USB_STP	USB Interface Link asserts
MIO 59	B24	MIO59_USB_DATA3	USB Interface Data 3
MIO 60	E24	MIO60_USB_DATA4	USB Interface Data 3
MIO 61	C24	MIO61_USB_DATA5	USB Interface Data 5
MIO 62	G24	MIO62_USB_DATA6	USB Interface Data 6
MIO 63	D24	MIO63_USB_DATA7	USB Interface Data 7

4.2.23. DisplayPort Connector

- DisplayPort Output Connector 1-port를 제공하며 Molex 社의 "0472720001"을 적용하였으며, Display Interface를 위한 Description은 아래와 같다.
- DisplayPort Interface를 사용하기 위해서는 PS GTR MUX를 Control 해야 하며 자세한 사항은 4.2.19 항목을 참고한다.

<DisplayPort Interface Description>

PS	FPGA Pin	Signal Name		Description
0-Ch	AB29	GTR_LANE0_TX_P	GT0_DP_TX_P	DisplayPort 0-Lane Data
	AB30	GTR_LANE0_TX_N	GT0_DP_TX_N	
1-Ch	Y29	GTR_LANE1_TX_P	GT1_DP_TX_P	DisplayPort 1-Lane Data
	Y30	GTR_LANE1_TX_N	GT1_DP_TX_N	

<DisplayPort AUX Description>

Signal Name	FPGA Pin	I/O Standard	Description
PL_DP_HPD	H11	LVCMOS33	Hot Plug Detect
PL_DPAUX_IN	F12		Aux Data Input
PL_DP_OE	G11		Aux Data Enable
PL_DPAUX_OUT	D10		Aux Data Output
MIO27_DP_AUX_OUT	M21	-	Aux Data Output
MIO28_DP_HPD	N21	-	Hot Plug Detect
MIO29_DP_OE	K22	-	Aux Data Enable
MIO30_DP_AUX_IN	L21	-	Aux Data Input

4.2.24. SATA Connector

- SATA Connector 1-port를 제공하며 Molex 社의 "67800-5005"을 적용하였으며, SATA Interface를 위한 Description은 아래와 같다.
- SATA Interface를 사용하기 위해서는 PS GTR MUX를 Control 해야 하며 자세한 사항은 4.2.19 항목을 참고한다.

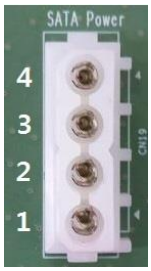
<SATA Interface Description>

PS	FPGA Pin	Signal Name		Description
3-Ch	V29	GTR_LANE3_TX_P	GT3_SATA1_TX_P	SATA Transmit Data
	V30	GTR_LANE3_TX_N	GT3_SATA1_TX_N	
	V33	GTR_LANE3_RX_P	GT3_SATA1_RX_P	SATA Receive Data
	V34	GTR_LANE3_RX_N	GT3_SATA1_RX_N	

4.2.25. SATA Power Connector

- SATA Power Connector 1-port를 제공하며 TE Connectivity 社의 "794285-1"를 적용하였으며, Connector Pin Description은 아래와 같다.

<SATA Power Connector Description>

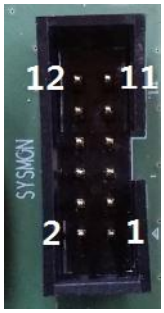


Pin Number	Description
1	+12V
2	GND
3	GND
4	+5V

4.2.26. FPGA SYSMON Connector

- FPGA SYSMON Connector 1-port를 제공하며 Molex 社의 "70246-1201"을 적용하였으며, SYSMON Interface를 위한 Description은 아래와 같다.

<SYSMON Interface Description>



Pin Number	Signal Name	Description
1	NC	No Connect
2	SYSMON_DXP	Temperature sensing Anode
3	NC	No Connect
4	SYSMON_DXN	Temperature sensing Cathode
5	GND	Ground
6	GND	Ground
7	SYSMON_VREF	SYSMON Reference Voltage
8	FPGA_SYSMON_AVCC	SYSMON AVCC Voltage
9	SYSMON_VN	Analog Input (Positive)
10	SYSMON_VP	Analog Input (Negative)
11	VCCINT_VIN_R_N	VCCINT Shunt Voltage
12	VCCINT_VIN_R_P	VCCINT Shunt Voltage

4.2.27. FPGA PS-MIO Connector

- 다른 외부 Board와의 PS MIO 확장을 위한 2.54mm 2x4 Header pin을 제공하며 Description은 아래와 같다.

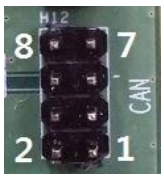
<PS-MIO Connector Description>

Pin Number	Signal Name	FPGA Pin	Description
1	MIO20	AD18	PS MIO20
2	PMBUS_SCL	-	PMBUS I2C Clock
3	MIO21	AF18	PS MIO21
4	PMBUS_SDA	-	PMBUS I2C Data
5	MIO22	AD20	PS MIO22
6	GND	-	Ground
7	MIO23	AD19	PS MIO23
8	VCCOPS	-	1.8V - PS MIO 전원

4.2.28. CAN Connector

- CAN Bus를 위한 2.54mm 2x4 Header pin을 제공하며 Description은 아래와 같다.

<CAN Interface Description>

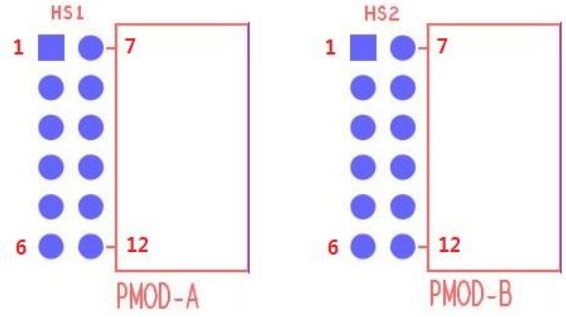


Pin Number	Signal Name	Description
1	GND	Ground
2	GND	Ground
3	CAN0_CANH_TERM	CAN Termination Resistor
4	CAN0_CANH	CAN_H Bus Line
5	CAN0_CANL	CAN_L Bus Line
6	CAN0_CANL_TERM	CAN Termination Resistor
7	CAN0_CANL	CAN_L Bus Line
8	CAN0_CANH	CAN_H Bus Line

4.2.29. PMOD (Peripheral Module Interface) Connector

- PMOD Connector 2-Port를 제공하며 SULLINS 社의 "PPTC062LJBN-RC" 를 적용하였으며, PMOD Interface를 위한 Description은 아래와 같다.

<PMOD Connector Pin Description>



<PMOD Connector Description>

PMOD	Pin Number	Signal Name	FPGA Pin	I/O Standard
PMOD-A	1	PMOD_A0	J11	LVCMOS33
	2	PMOD_A1	J10	
	3	PMOD_A2	H10	
	4	PMOD_A3	G10	
	5	GND	-	-
	6	UTIL_3V3	-	-
	7	PMOD_A4	F10	LVCMOS33
	8	PMOD_A5	E10	
	9	PMOD_A6	D11	
	10	PMOD_A7	F11	
	11	GND	-	-
	12	UTIL_3V3	-	-
PMOD-B	1	PMOD_B0	G15	LVCMOS33
	2	PMOD_B1	G14	
	3	PMOD_B2	J14	
	4	PMOD_B3	H14	
	5	GND	-	-
	6	UTIL_3V3	-	-
	7	PMOD_B4	H16	LVCMOS33
	8	PMOD_B5	G16	
	9	PMOD_B6	J16	
	10	PMOD_B7	J15	
	11	GND	-	-
	12	UTIL_3V3	-	-

4.2.30. SMA Connector

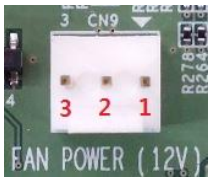
- MGT 고속 Transceiver를 위해 SMA Connector 1-Channel을 제공하며, SMA 고속 Transceiver Interface를 위한 Description은 아래와 같다.

<SMA Interface Description>

SMA	Signal Name	FPGA Pin	I/O Standard
CN23	SMA_MGT_CLK_P	J27	SMA Receive Reference Clock (Positive)
CN24	SMA_MGT_CLK_N	J28	SMA Receive Reference Clock (Negative)
CN27	SMA_MGT_RX_P	L31	SMA Receive Data (Positive)
CN26	SMA_MGT_RX_N	L32	SMA Receive Data (Negative)
CN29	SMA_MGT_TX_P	K29	SMA Transmit Data (Positive)
CN30	SMA_MGT_TX_N	K30	SMA Transmit Data (Negative)

4.2.31. FAN Connector

- FPGA의 방열을 위해 DC +12V FAN Power Connector를 지원한다.

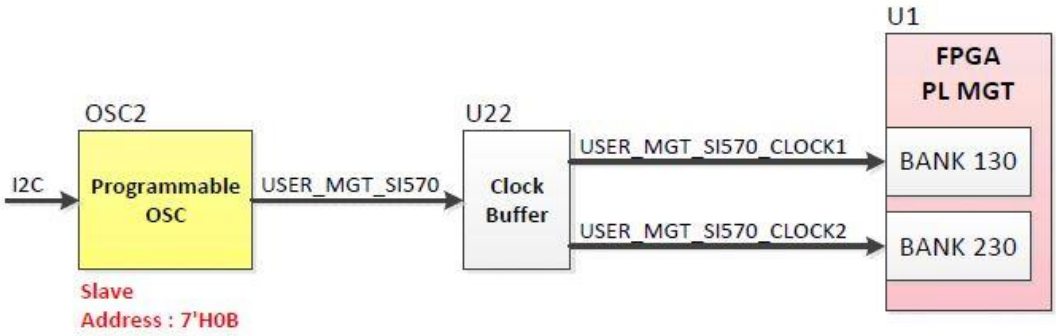


Pin Number	Description
1	GND
2	DC +12V
3	NC

4.2.32. Programmable OSC

- MGT 고속 Transceiver의 Reference Clock 공급을 위해 Programmable OSC를 제공하며, Silicon Labs 社의 "598BCA001134DG"(1)을 적용하였으며, Block-Diagram 및 Description은 아래와 같다.

<Programmable OSC Block-Diagram>



<Programmable OSC Description>

Signal Name	FPGA Pin	Description
USER_MGT_SI570_SCL	-	Programmable OSC I2C Clock
USER_MGT_SI570_SDA	-	Programmable OSC I2C Data
USER_MGT_SI570_CLOCK1_P	L27	Reference Clock (Default : 156.25MHz)
USER_MGT_SI570_CLOCK1_N	L28	
USER_MGT_SI570_CLOCK2_P	C8	Reference Clock (Default : 156.25MHz)
USER_MGT_SI570_CLOCK2_N	C7	

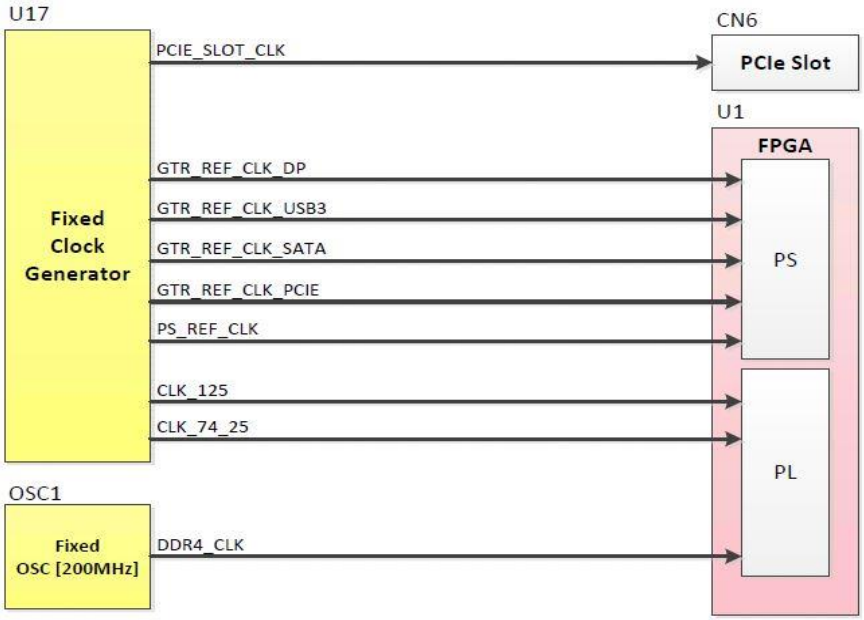
Notes:

1. 598BCA001134DG에 대한 자세한 설명은 Silicon Labs Datasheet "598BCA001134DG" 를 참고한다.

4.2.33. Fixed Clock Generator

- FPGA Clock 공급을 위해 Fixed Clock Generator를 제공하며, Silicon Labs 社의 "Si5341B-B05071-GM"(1)을 적용하였으며, Block-Diagram및 Description은 아래와 같다.

<Fixed Clock Generator Block-Diagram>



<Fixed Clock Generator Description>

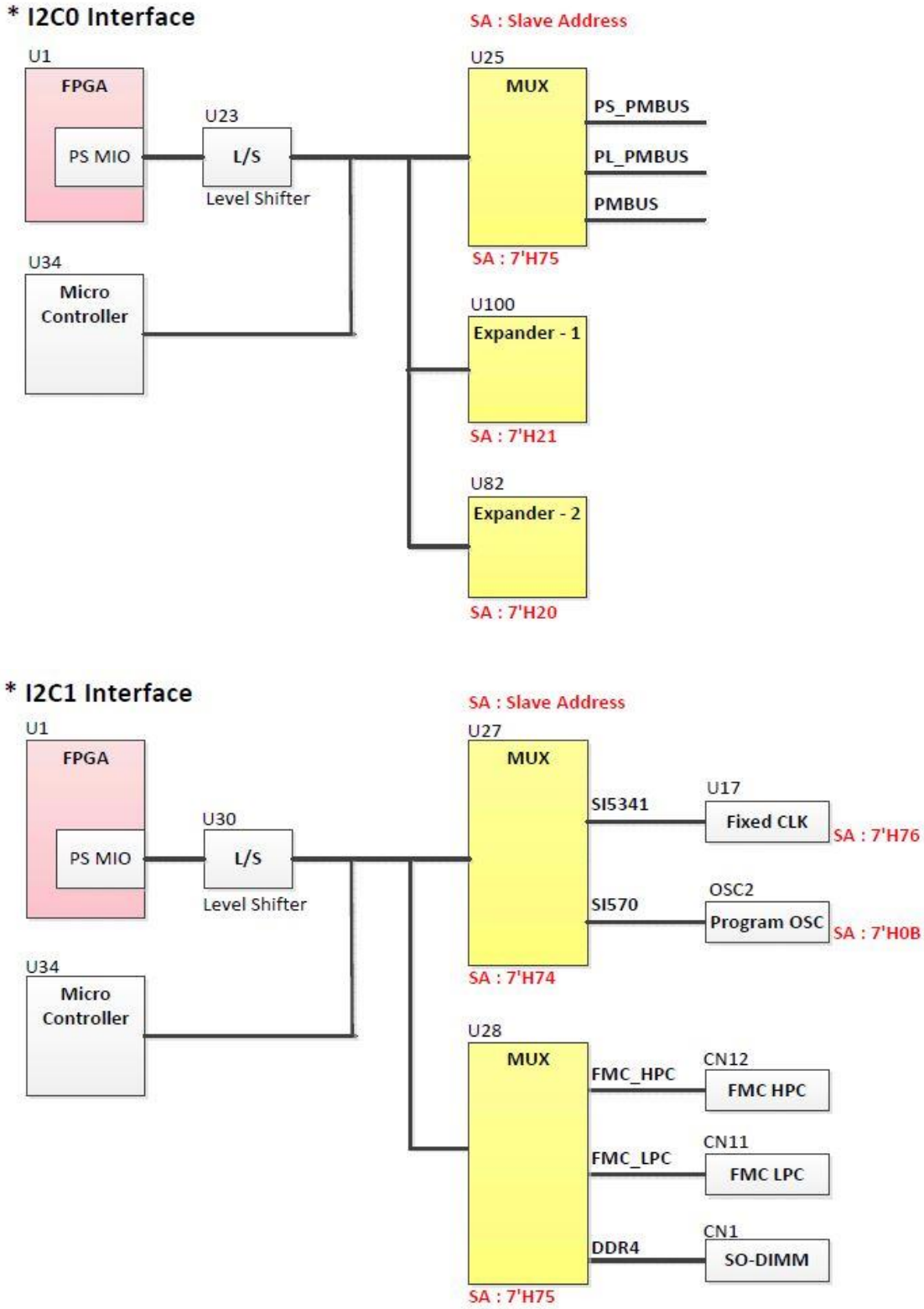
Signal Name	FPGA Pin	Frequency	Description
PCIE_SLOT_CLK_P	-	100MHz	PCIe Slot Clock
PCIE_SLOT_CLK_N	-		
GTR_REF_CLK_DP_P	U31	27MHz	PS GTR DP Reference Clock
GTR_REF_CLK_DP_N	U32		
GTR_REF_CLK_USB3_P	U27	24MHz	PS GTR USB3.0 Reference Clock
GTR_REF_CLK_USB3_N	U28		
GTR_REF_CLK_SATA_P	W27	125MHz	PS GTR SATA Reference Clock
GTR_REF_CLK_SATA_N	W28		
GTR_REF_CLK_PCIE_P	AA27	100MHz	PS GTR PCIe Reference Clock
GTR_REF_CLK_PCIE_N	AA28		
PS_REF_CLK	U24	33MHz	PS Reference Clock
CLK_125_P	G21	125MHz	PL Clock
CLK_125_N	F21		
CLK_74_25_P	AK15	74.25MHz	PL Clock
CLK_74_25_N	AK14		
DDR4_CLK_P	AL8	200MHz	PL DDR4 Component Clock
DDR4_CLK_N	AL7		

Notes:

1. Si5341B-B05071-GM에 대한 자세한 설명은 Silicon Labs Datasheet "Si5341B-B05071-GM" 를 참고한다.

4.3. MPSoC Main Module I2C Interface

4.3.1. I2C Interface Block-Diagram



4.3.2. I2C0 Interface Description

- Multiplexer는 TI 社의 "PCA9544ARGYR"[(1)]를 적용하였으며, Description은 아래와 같다.

<I2C0 Multiplexer U25 Description – 7'H75>

Pin name	I2C BUS Name	Register	Description
SC0 / SD0	PS_PMBUS	8'H04	I2C0 to PS_PMBUS
SC1 / SD1	PL_PMBUS	8'H05	I2C0 to PL_PMBUS
SC2 / SD2	PMBUS	8'H06	I2C0 to PMBUS

- PS_PMBUS는 PS 공급 전원을 모니터링 하는 I2C Interface로 TI 社의 "INA226AIDGSR"[(2)]을 적용하였으며, Description은 아래와 같다.

<PS_PMBUS Description>

I2C BUS Name	Reference Designation	Slave Address	Power Source	Voltage Level
PS_PMBUS	U42	7'H41	VCCPSINTLP	0.85V
	U44	7'H43	VCCPSPLL	1.20V
	U46	7'H42	VCCPSAUX	1.80V
	U48	7'H4A	VCCOPS3	1.80V
	U50	7'H47	VCCOPS	1.80V
	U52	7'H40	VCCPSINTFP	0.85V
	U54	7'H44	MGTRAVCC	0.85V
	U56	7'H4B	VCCPSDDRPLL	1.80V
	U58	7'H45	MGTRAVTT	1.80V
	U60	7'H46	VCCO_PSDDR_504	1.20V

- PL_PMBUS는 PL 공급 전원을 모니터링 하는 I2C Interface로 TI 社의 "INA226AIDGSR"[(2)]을 적용하였으며, Description은 아래와 같다.

<PL_PMBUS Description>

I2C BUS Name	Reference Designation	Slave Address	Power Source	Voltage Level
PL_PMBUS	U62	7'H46	MGTAVCC	0.90V
	U64	7'H47	MGTAVTT	1.20V
	U65	7'H4A	MGTVCCAUX	1.80V
	U68	7'H43	VCC1V2	1.20V
	U70	7'H40	VCCINT	0.85V
	U85	7'H41	UTIL_3V3	3.30V
	U72	7'H42	VCCAUX	1.80V
	U78	7'H45	VADJ_FMC	1.80V

- PMBUS는 Board 주요 공급 전원을 컨트롤 하는 I2C Interface로 Description은 아래와 같다.

<PMBUS Description>

I2C BUS Name	Reference Designation	Slave Address	Power Unit	Vendor
PMBUS	PU7	7'H50	ZL9010MAIRZ	Intersil
	PU22	7'H51	ZL9010MAIRZ	Intersil
	PU17	7'H5A	LGA80D-00DADJJ	Artesyn
	PU26	7'H41	LGA80D-00DADJJ	Artesyn

- Expander–1은 TI 社의 "TCA6416APWR"[(3)]를 적용하였으며, Description은 아래와 같다.

<I2C0 Expander -1 (U100) Description – 7'H21>

Pin name	Pin number	Signal Name	Description
P00	4	VCCPSPLL_I2C_EN	VCCPSPLL Enable
P01	5	MGTRAVCC_I2C_EN	MGTRAVCC Enable
P02	6	MGTRAVTT_I2C_EN	MGTRAVTT Enable
P03	7	VCCPSDDRPLL_I2C_EN	VCCPSDDRPLL Enable
P04	8	MIO26_PMU_INPUT_LS	PMU Input signal
P05	9	PL_PMBUS_ALERT	PL_PMBUS Alert Indicate
P06	10	PS_PMBUS_ALERT	PS_PMBUS Alert Indicate
P07	11	PMBUS_ALERT	PMBUS Alert Indicate
P10	13	PL_DDR4_PW_EN	PL_DDR4_VTT Enable
P11	14	PL_DDR4_VPP_2V5_EN	PL_DDR4_VPP Enable
P12	15	VCCO_PSDDR_504_I2C_EN	VCCO_PSDDR_504 Enable
P13	16	PS_DIMM_SUSPEND_EN	SO-DIMM Suspend Enable
P14	17	PS_DDR4_PW_EN	PS_DDR4_VTT Enable
P15	18	PS_DDR4_VPP_2V5_EN	PS_DDR4_VPP Enable
P16	19	NC	-
P17	20	NC	-

- Expander–2은 TI 社의 "TCA6416APWR"[3]를 적용하였으며, Description은 아래와 같다.

<I2C0 Expander -2 (U82) Description – 7'H20>

Pin name	Pin number	Signal Name	Description
P00	4	PS_GTR_LANE_SEL0	PS GTR Lane Selection (4.2.19 항목 참고)
P01	5	PS_GTR_LANE_SEL1	
P02	6	PS_GTR_LANE_SEL2	
P03	7	PS_GTR_LANE_SEL3	
P04	8	PCIE_CLK_DIR_SEL	PCIE Clock Direction select
P05	9	IIC_MUX_RESET_B	I2C MUX Reset (Active Low)
P06	10	GEM3_EXP_RESET_B	Ethernet Reset (Active Low)
P07	11	NC	-
P10	13	FMC_HPC_PRSNT_M2C_B	FMC HPC Detect
P11	14	FMC_LPC_PRSNT_M2C_B	FMC LPC Detect
P12	15	NC	-
P13	16	NC	-
P14	17	NC	-
P15	18	NC	-
P16	19	NC	-
P17	20	NC	-

Notes:

1. PCA9544ARGYR 에 대한 자세한 설명은 Texas Instruments Datasheet "PCA9544ARGYR" 를 참고한다.
2. INA226AIDGSR 에 대한 자세한 설명은 Texas Instruments Datasheet "INA226AIDGSR" 를 참고한다.
3. TCA6416APWR 에 대한 자세한 설명은 Texas Instruments Datasheet "TCA6416APWR" 를 참고한다.

4.3.3. I2C1 Interface Description

- Multiplexer는 TI 社의 "TCA9548APWR"(1)를 적용하였으며, Description은 아래와 같다.

<I2C1 Multiplexer U27 Description – 7'H74>

Pin name	I2C BUS Name	Register	Description
SC0 / SD0	No Connection	8'H01	
SC1 / SD1	SI5341_SDA/SCL	8'H02	Fixed Clock I2C I/F
SC2 / SD2	No Connection	8'H04	
SC3 / SD3	USER_MGT_SI570_SDA/SCL	8'H08	Programmable OSC I2C I/F
SC4 / SD4	No Connection	8'H10	
SC5 / SD5	No Connection	8'H20	
SC6 / SD6	No Connection	8'H40	
SC7 / SD7	No Connection	8'H80	

<I2C1 Multiplexer U28 Description – 7'H75>

Pin name	I2C BUS Name	Register	Description
SC0 / SD0	FMC_HPC_SDA/SCL	8'H01	FMC HPC I2C I/F
SC1 / SD1	FMC_LPC_SDA/SCL	8'H02	FMC LPC I2C I/F
SC2 / SD2	No Connection	8'H04	
SC3 / SD3	DDR4_SODIMM_SDA/SCL	8'H08	SO-DIMM I2C I/F
SC4 / SD4	No Connection	8'H10	
SC5 / SD5	No Connection	8'H20	
SC6 / SD6	No Connection	8'H40	
SC7 / SD7	No Connection	8'H80	

Notes:

1. TCA9548APWR 에 대한 자세한 설명은 Texas Instruments Datasheet "TCA9548APWR" 를 참고한다.

5. 참고 자료

- MPSoC Zynq UltraScale+와 관련된 최신 정보는 아래 Xilinx Web site에서 이용 가능합니다.
  http://www.xilinx.com/products/silicon-devices/soc.html

- 아래의 Xilinx 문서는 ULTRON User Manual에 유용한 보충 자료를 제공합니다.
  1. UltraScale Architecture and Product Overview (DS890)
  2. Zynq UltraScale+ MPSoC Technical Reference Manual (UG1085)
  3. UltraScale Architecture PCB Design Guide (UG583)
  4. UltraScale Architecture FPGAs Memory Interface Solution LogiCORE IP Product Guide (PG150)
  5. UltraScale Architecture GTH Transceivers User Guide (UG576)
  6. UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide (PG156)
  7. Silicon Labs CP210X USB-to-UART Installation Guide (UG1033)
  8. Tera Term Terminal Emulator Installation Guide (UG1036)
  9. Vivado Design Suite User Guide:Using Constraints User Guide (UG903)
  10. UltraScale Architecture System Monitor User Guide (UG580)

- 아래의 Website는 ULTRON User Manual에 유용한 보충 자료를 제공합니다.
  1. Micron Technology : www.micron.com
     (Datasheet : MT40A256M16GE-075E:B, MT25QU512ABB8E12)
  2. Standard Microsystems Corporation (SMSC):
     www.microchip.com/redirect-notifications/smsc
     (Datasheet : USB3320C-EZK-TR)
  3. Silicon Labs : www.silabs.com/Pages/default.aspx
     (Datasheet : 598BCA001134DG, Si5341B-B05071-GM)
  4. Texas Instruments : http://www.ti.com
     (Datasheet : PCA9544ARGYR, INA226AIDGSR, TCA6416APWR, TCA9548APWR)
  5. PCI website : https://pcisig.com/specifications
  6. Pericom : https://www.pericom.com
     (Datasheet : PI2DBS6212ZHEX)
  7. VITA FMC Marketing Alliance website : http://www.vita.com/fmc