Final Project Team21

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***Abstract* - These instructions give you the basic guidelines for preparing papers for IEEE conference proceedings.**

Index Terms - List key index terms here. No mare than 5.

I. INTRODUCTION

Our goal is design a 64 bits ROM marco with access time smaller than 5ns. We design the 6 to 64 bits decoder,3 to 8 decoder, timing control, mux and SA respectively. Then, we compare its performance in different corners. We also drew the layout by ourselves and compared the pre-sim and post-sim performance. In this report, we show how we design the ROM macro and evaluate its performance in different kind of conditions. Besides, we will also explain how we design the components and how it operates..

II. DESIGN

A. Waveform OF 5 CORNER

We have input A<8:0>, A<2:0> is responsible for the control of 3 to 8 decoder and A<8:3> for the control of 6 to 64 decoder. Besides, we also use the clock(100MHz) as input. SAEN , pre_b and WL_EN is signal generated by timing control. We will also show our timing control later. The output signals are Dout<1:0>, which is from SA. In our waveform, when A<2:0> is 0 and A<8:3> is 0 , the ROM macro will read 1.While A<2:0> is 0 and A<7:3> is 63, it will read 0. In the beginning , the waveform is 1.8(V), because we have a precharge to keep it high. However, as it read 0, the nmos in ROM array will release it and it will become low. Our waveform of five corner(TT25°C, SS25°C, FF25°C, SF25°C, FS25°C) can be seen in Figure1. From these waveform, we can find that the corner significantly affect the performance of our model (see table 1). It seems that in SS, it has the highest power consumption and the largest access time while in FF, it has the smallest access time. By the waveform, we can sees that in some corner such as SS, the Dout<0:1> will spend more time to change as the input clk become high. However, our model can perform as expected in all of the conditions. It seems that our model work in the these extreme conditions. But it still not work very well in situation such as SS. We have check the components and we think that the components that significantly perform not well in some corner are 6 to 64 decoder and timing control. It may because these two components are very complicated and with many mosfets. The different corners may lead to different rising and falling time of signals. It affects the performance of each mosfets. For components pass so many mosfets, even if a subtle change in the performance of nmos and pmos may make the waveform become abnormal.

TABLE I
ACCESS TIME AND POWER CONSUMPTION FOR FIVE CORNERS AND POST-SIM

	access time(ns)	Power(um^2)
TT25℃	2.13	944.6
TT25℃	1.73	620.6
SS25℃	4.37	701.3
FF25℃	1.47	654.2
SF25℃	2.74	648.9
FS25℃	1.76	618.9

B. LAYOUT OF ROM MACRO

Figure 2 is our layout, and Figure 3 shows that we pass the lvs and drc. Our area is

$$Area = w * L = 132.91um * 79.055um$$
$$=> 10500.55um^2$$

We spend very large space for our decoders and timing control. To reduce the area of the ROM macro, it may be important to design decoders and timing control well to make them occupied smaller space.

C. POST-SIM WAVEFORM AND PRE-SIM WAVEFORM

The waveform of post-sim has much higher access time than post-sim(Table1).Besides post-sim also consume more power. It seems that post-sim seriously affects the signal generated to control our components. It may due to the fact that parasitic capacitance and resistance will make the rising time or falling time of our control signal different. In our waveform, the post-sim has very serious delay. We can see that it need longer time to change the output value. And it needs longer time for decoder to output result. Therefore, to make our design work, the WL_EN and SAEN should generate properly. We delay SAEN to make sure the decoder has operate successfully before the SA start to operate. If they do not generate in the right order or time, it may make our ROM macro output abnormal signal because they may read the wrong signal. In the waveform, we have control our component in the right order, so it can still output as expected.

D. DESIGN OF EACH BLOCK

1) 3 to 8 Decoder: In the decoder(Figure 4), we use the input signals with the nands gate.It can generate eight kind of different output. The output correspond to the input value will be low. In our design, all of our pmos is 1.5um/0.18um and nmos is 0.5um/0.18um. The reason of why we. Choose this size is that it can output right result and occupied small area. Besides it also consume little power.

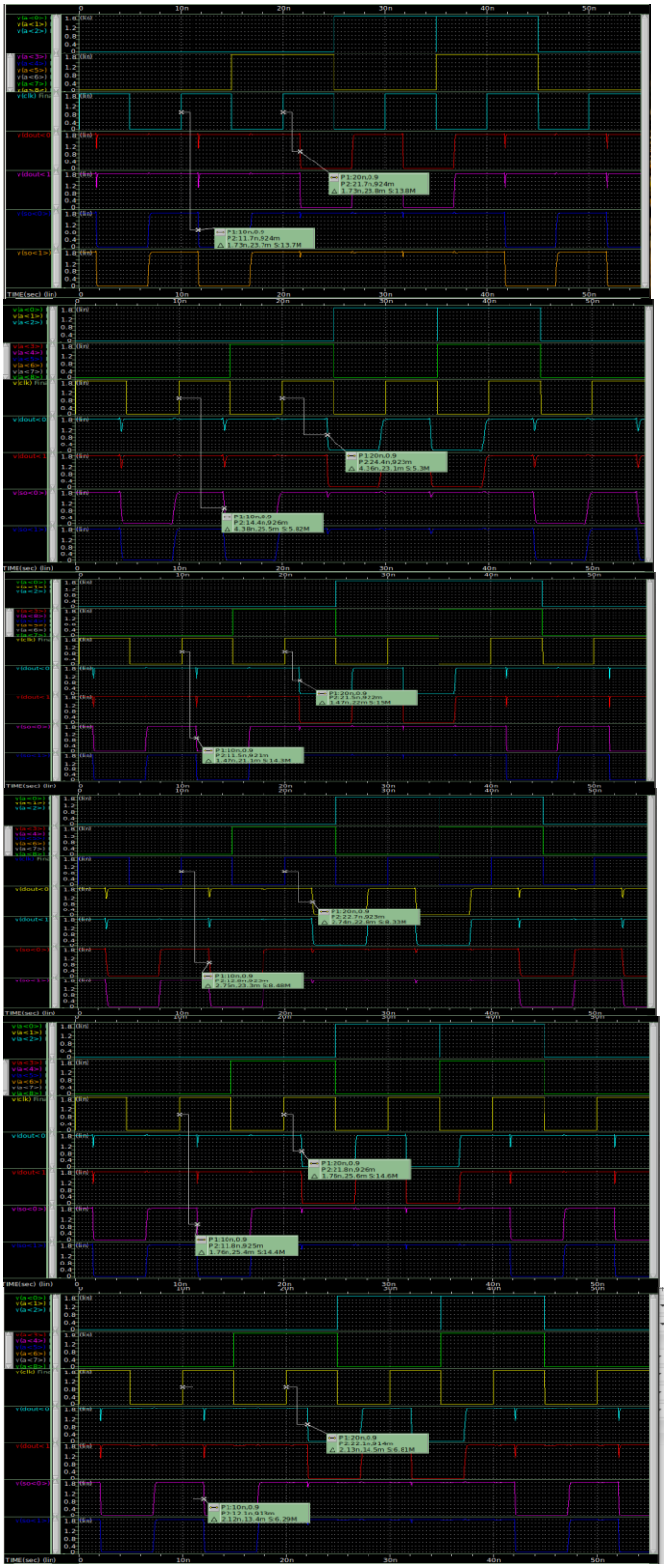

Fig. 1 .the pre-sim and waveform of five corner and post-sim waveform of TT25°C.(the first is TT25°C, the second is FS25°C, the third is SF25°C , the fourth is FF25°C, the fifth is SS25°C)

2) 6 To 64 Decoder: We use two 3 to 8 decoder and 64 nor gate to design this decoder.(Figure 5). The size of 3to 8 decoder is the same as the as in Figure 4. And the nor pmos use for nor gate is 1.5um/0.18um, while the nmos is 0.5um/0.18um.Because this decoder occupied extremely large area with 64 nor gate.Therefore we do not choose the size that will occupied too much space for our nor gate and also we want to make it consume less power, so we use the size with small width.

3) 8 to 1 MUX: We simply use 8 transmission gate and connect its output together(Figure 6).Size of all the pmos is 1.5um/0.18um and nmos is 0.5um/0.18um.The only reason we choose the size is that it takes small space.

4) Sense amplifier: We design the Sense amplifier with the size as Figure 7.We choose this size because that we want to make its sensing time as small as possible when occupying not too much space. So we only choose M9 to have larger width, because it can make our sensing amplifier obviously have lower sensing time. It can reduce our access time which is very important. The signals WLEN and SAEN can control the order of components. First ,we use the buffer to generate a signal which has the same waveform as clk but delay for a while. Different control signals needs delay of different time. To make our control signal stable, we need many buffers. Different signals use different numbers of buffer. All of our buffer are composed of two inverters and all of our inverter are composed of pmos 1.5um/0.18um and nmos 0.5um/0.18um. We choose such kind of size because it can generate stable signal and occupied smaller space. We need many buffers,so we cannot choose too large size. Besides our input A<8:0> will pass the d flip flop, so we also need nine d flip flop for our timing control.

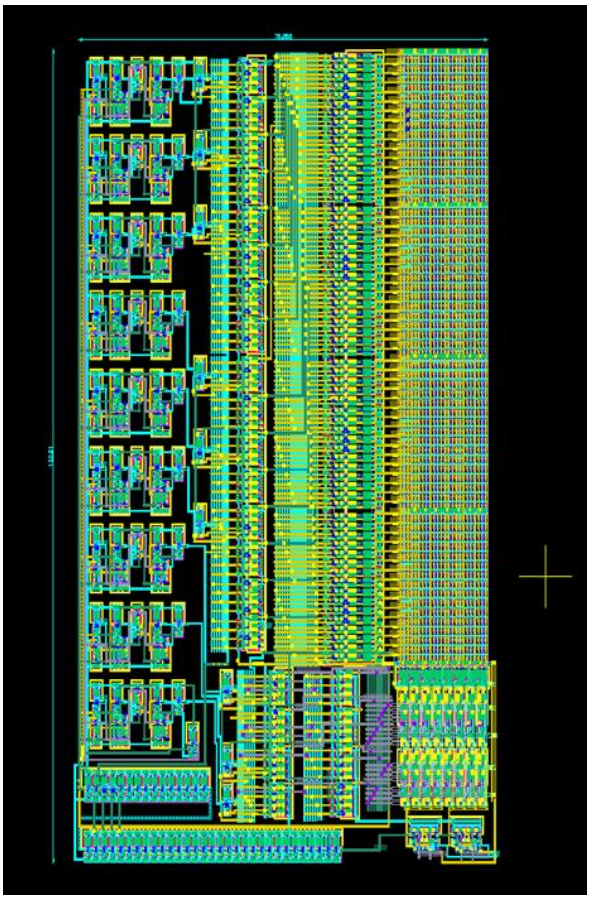

Fig. 2 the layout of ROM macro

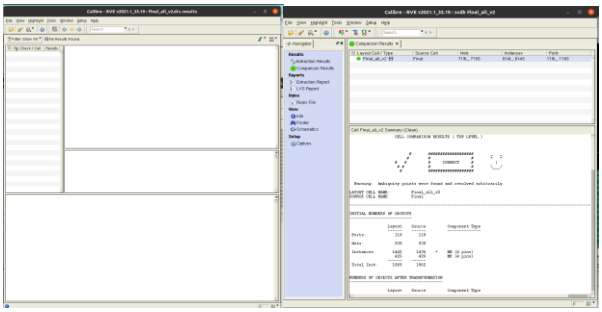

Fig. 3 the drc and lvs

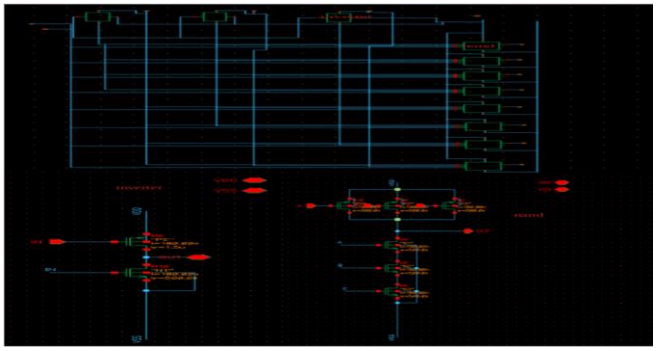

Fig. 4 3 to 8 decode

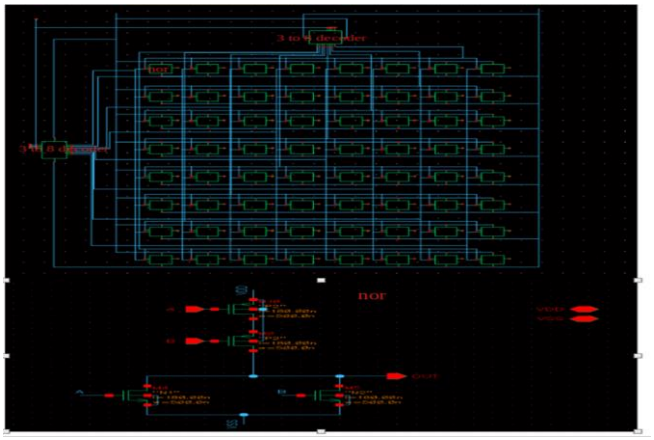

Fig. 5 6 to 64 decoder

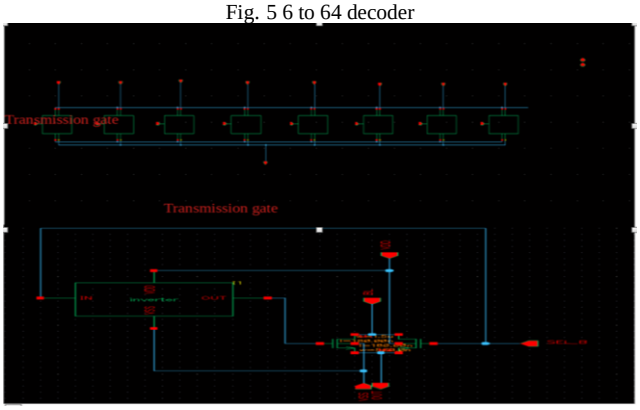

Fig. 6 8 to 1 MUX

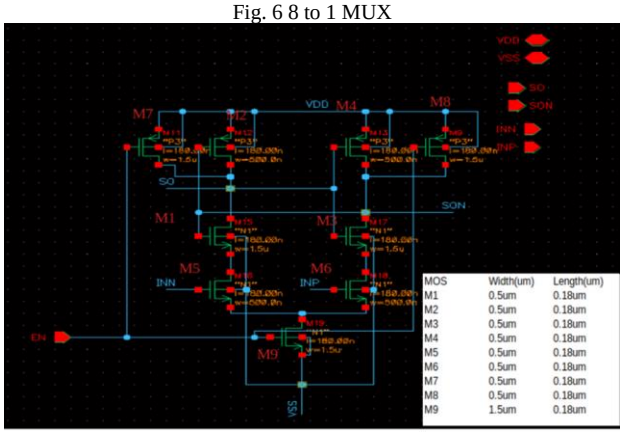

Fig. 7 sense amplifier

E. THE WAY ROM MACRO WORK

In our design, first of all, we will pass A<8:0>, Vref, and CLK to the timing control. Timing control will use the input to generate all signals we need. As the timing control receive the inputs, it will pass the A<8:0> to our decoders. Our 6 to 64 decoder will output the result as the clk and WL_EN is high. And then the output of 6 to 64 decoder will make some bits of precharged ROM array become low. Finally the timing Finally the output will come to SA. If SAEN is high, SAEN will output our final output(Dout<1:0>).

TABLE2I
FOM

FOM	access time(ns)	Power(um^2)	area(um^2)
44832047.8	2.16	944.6	10500.6

III. Result

According to our data and waveform, we can know that the parasitic capacitance and resistance will make our design perform worse. Besides, post-sim will increase our power consumption. To make our design well, we cannot ignore the effect of parasitic capacitance and resistance. We also need to consider about the performance of different corner. We can see that it affects the performance of each mosfets. It may not only affect the power consumption but also the access time. From waveform, we know that the SS25°C and SF25°C need longer access time. If we do not think about the effect of corners, our timing control may not control our components in right order because some components may need much longer time to operate in certain corners.

IV. Conclusion

Although our design perform significantly worse after post-sim. But it seems that it can still work as expected.
If we want to improve our design, we may try to improve our decoder and timing control first. Because we find that the waveforms of our timing control and decoder may not be very stable sometimes. As for our timing control, we use too much buffer to generate the signals. To reduce delay and save space, it may be better to use less buffer or other kind of combinational circuit to generate the impulse signal. Besides our layout may still not arrange very well, so we may not take advantage of all the space , and the way we connect the components are too complicated. And only evaluate the components respectively when we design, so we do not consider the performance when all of them operate together.