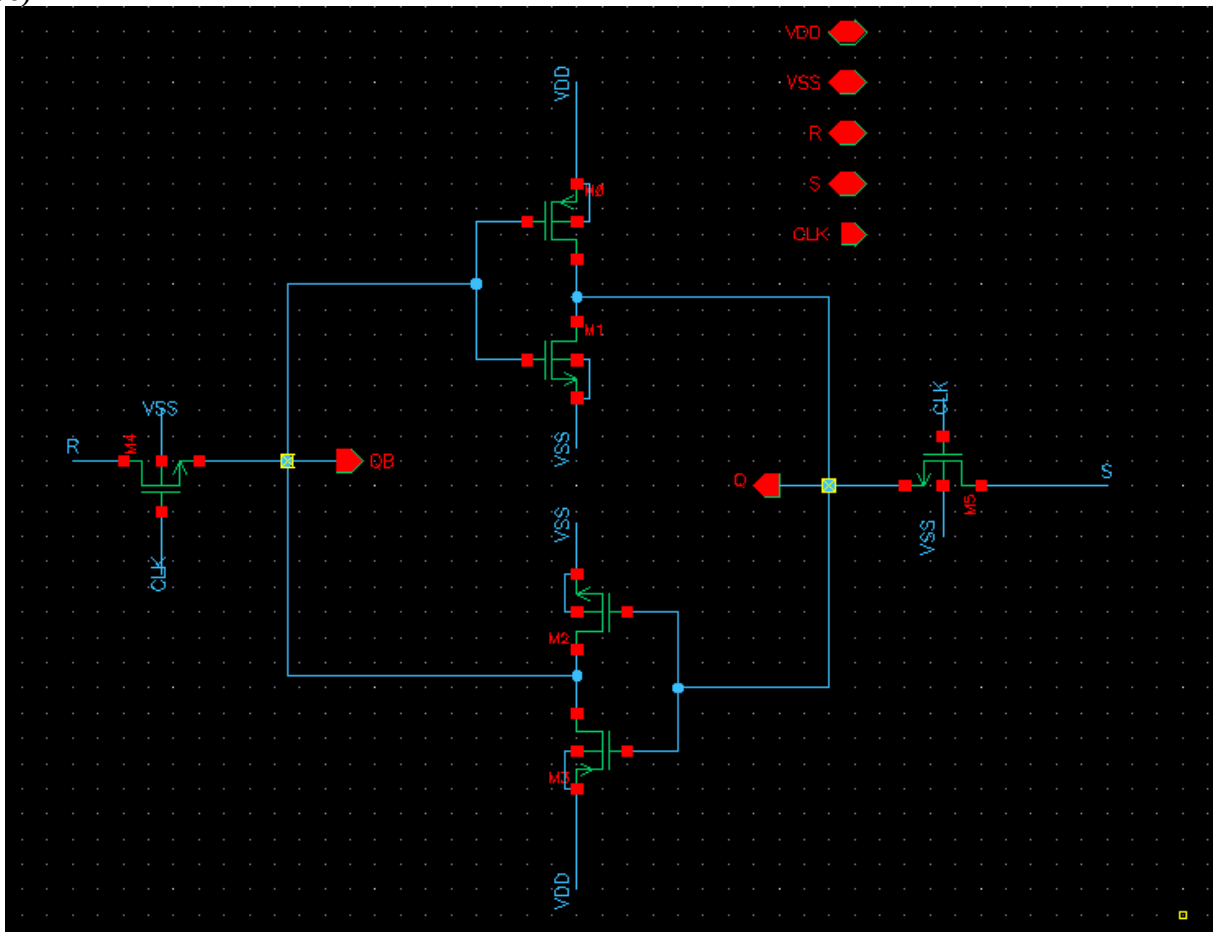


108061217 鍾永桓

Part I (42%)

1. Design a SR latch as shown in Fig. 1. Assume CLK=100MHz with $t_r=t_f=10\text{ps}$, duty cycle=50%. (7%)

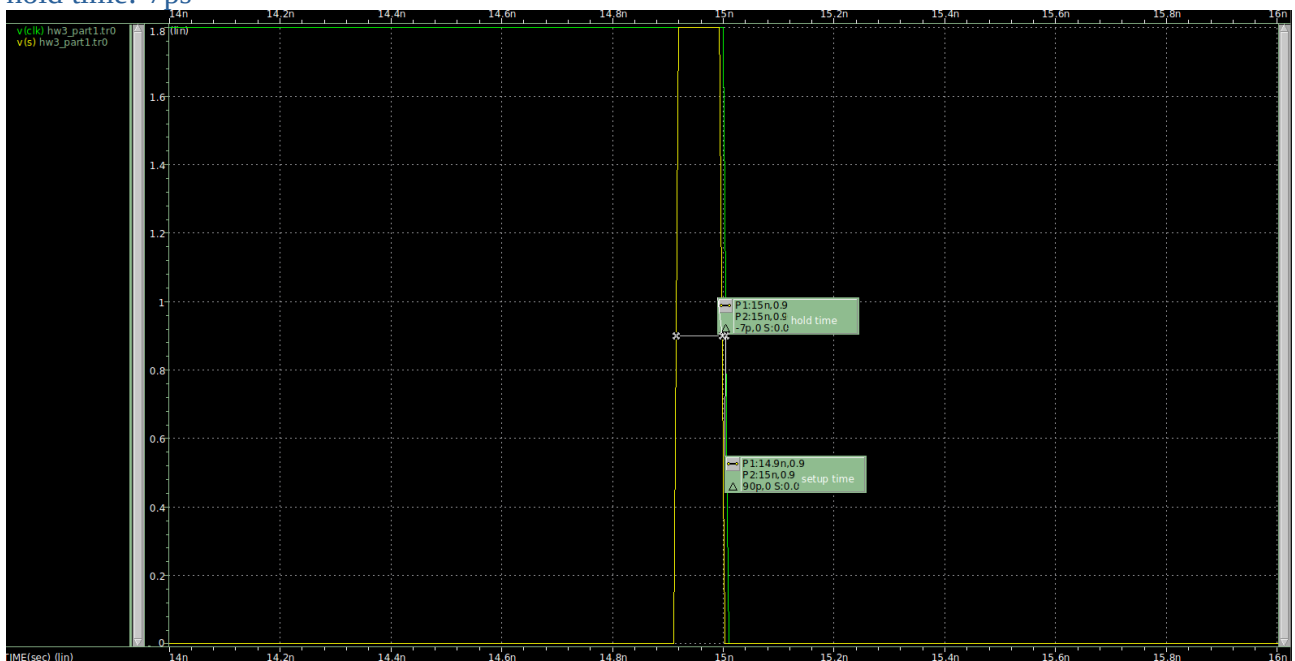


2. Simulate and find the setup time of this latch. (7%)

setup time: 90ps

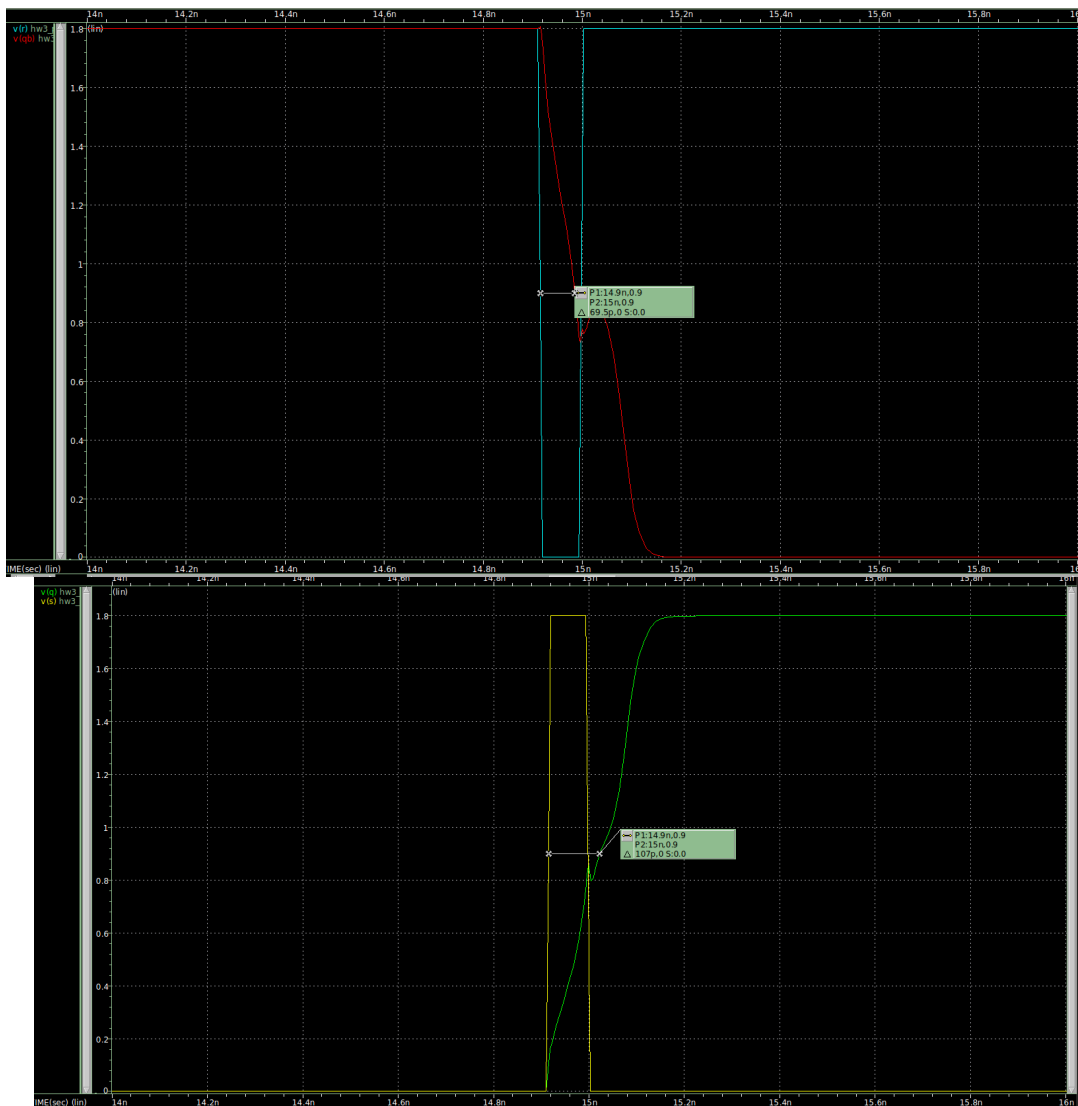
3. Same as above, simulate and find the hold time of this latch. (7%)

hold time: 7ps



4. Simulate the S to Q delay tpsq and R to QB delay tprqb. (7%)

tpsq:107.1ps tprqb:69.47ps

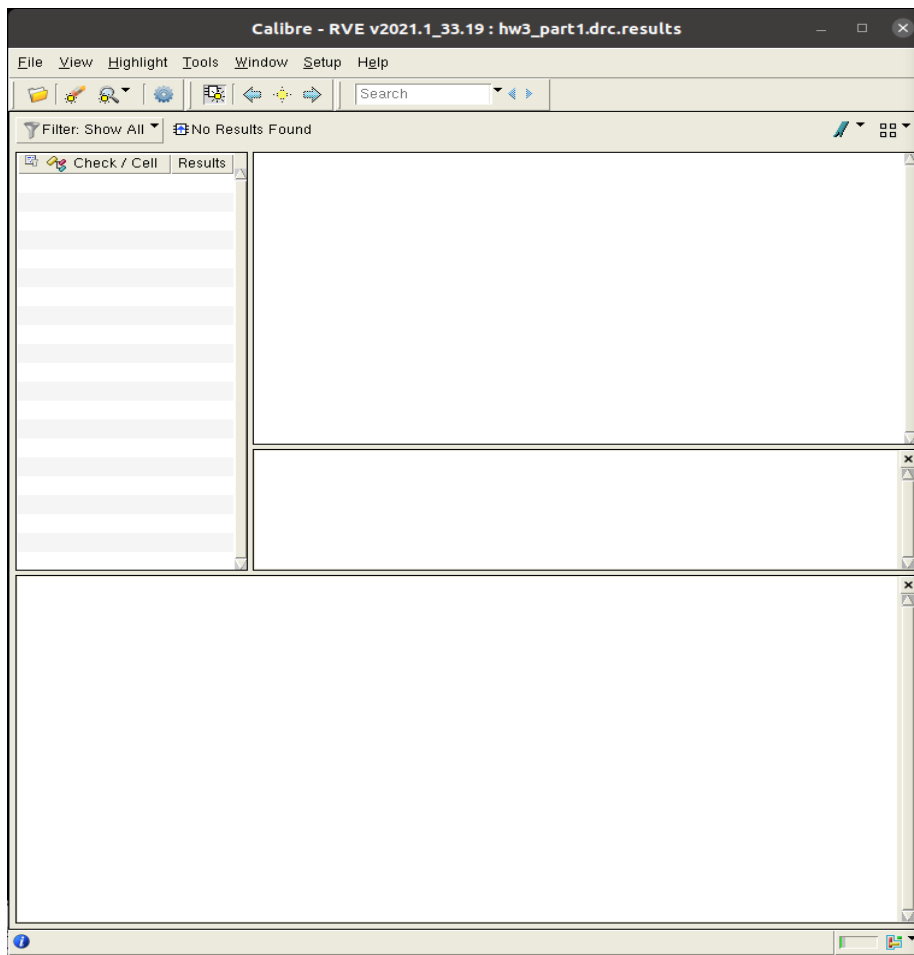
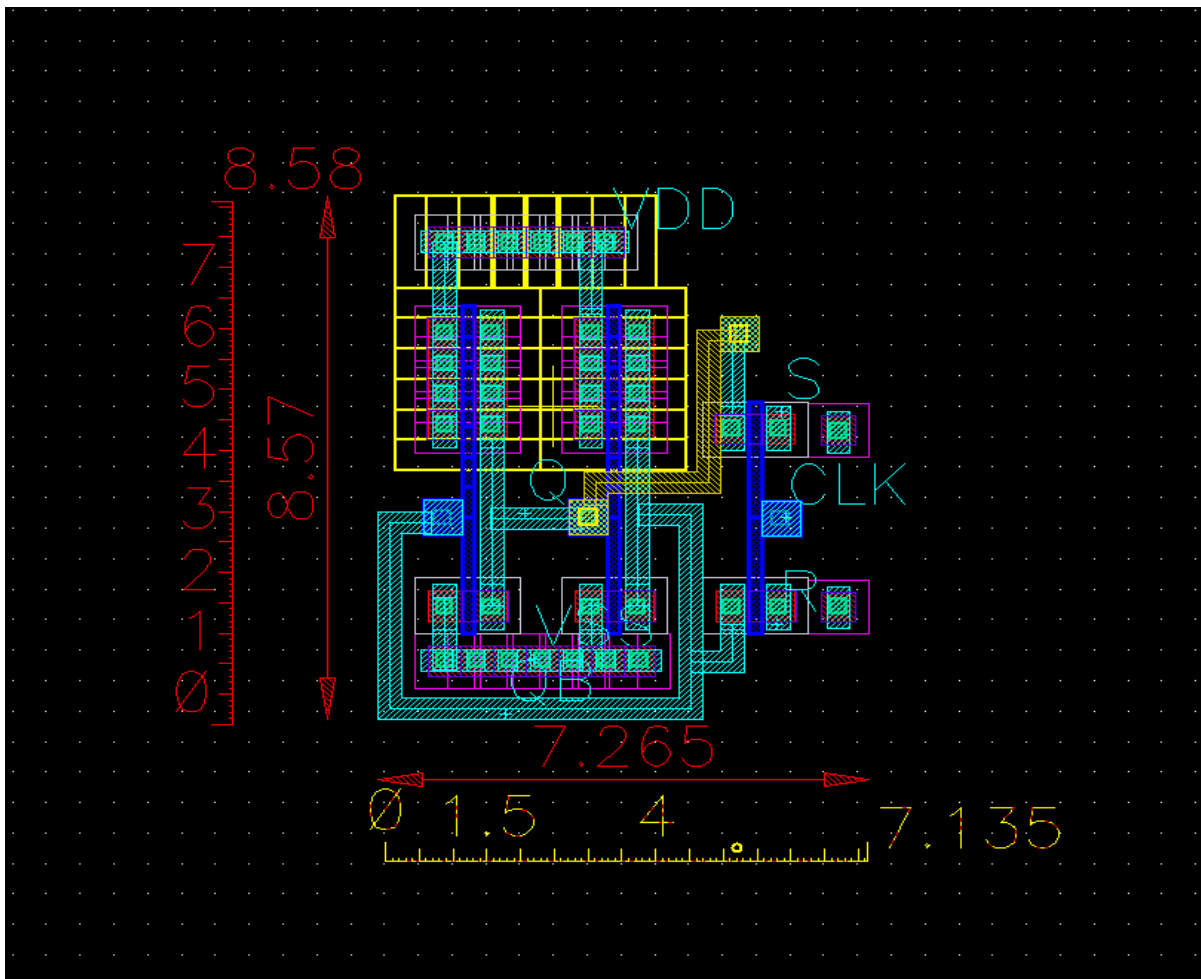


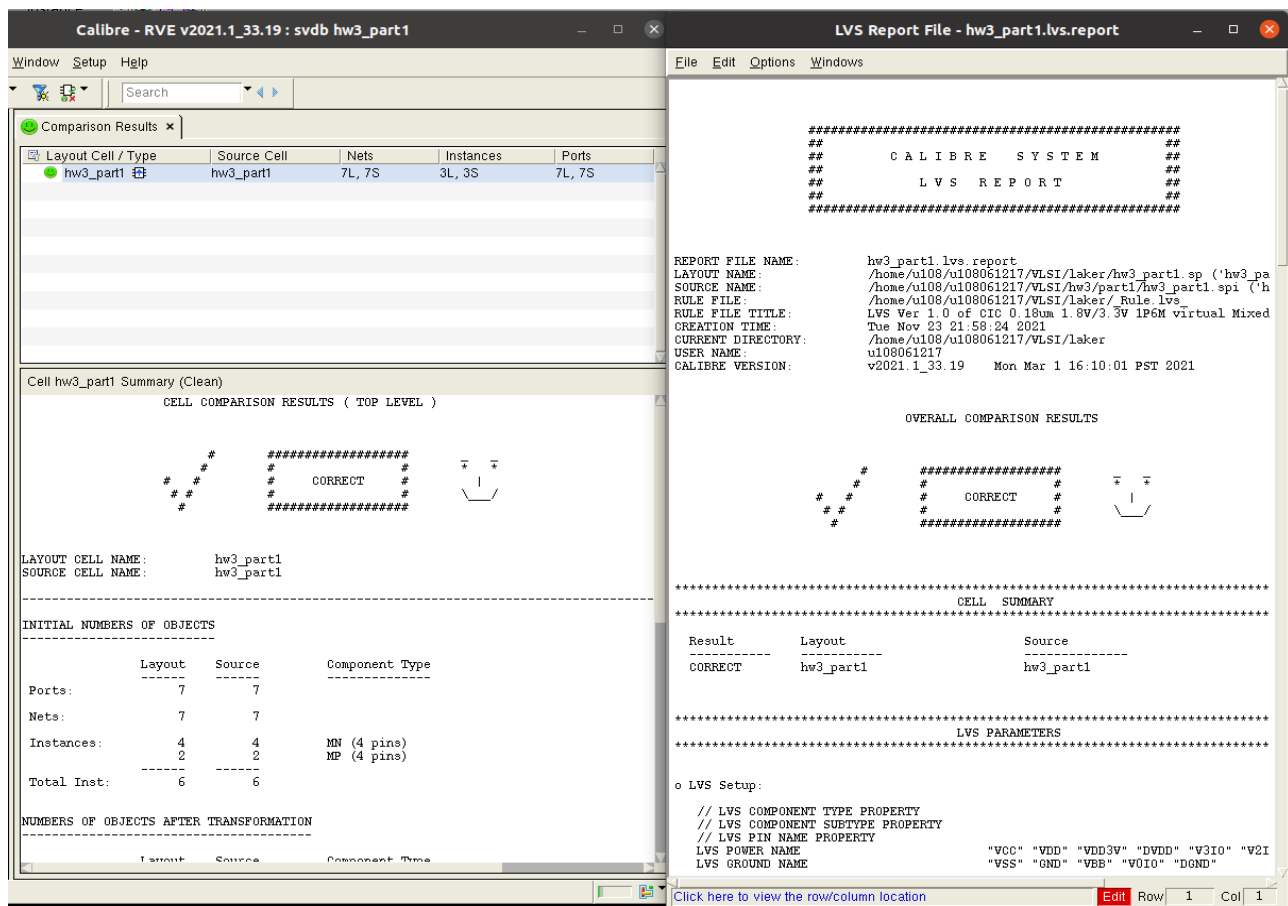
5. Sweep Vdd and find the operation voltage of this latch.

operation voltage:1.772

6. Complete the layout of this design. The layout should measure the area. (8%) Note: Area of the layout is the area of the minimum single rectangle that can cover all circuits.

Area:62.26105(um^2)





7. Run the post-layout simulation (post-sim) and compare it with pre-simulation(2., 3., 4. and 5.) (pre-sim) (7%)

pre-sim:

setup time:90ps

hold time:-7ps

tps:107.1ps tprqb:69.47ps

operation voltage:1.772v

post-sim:

setup time:300ps

hold time:18ps

tps:102.9ps tprqb:85.36ps

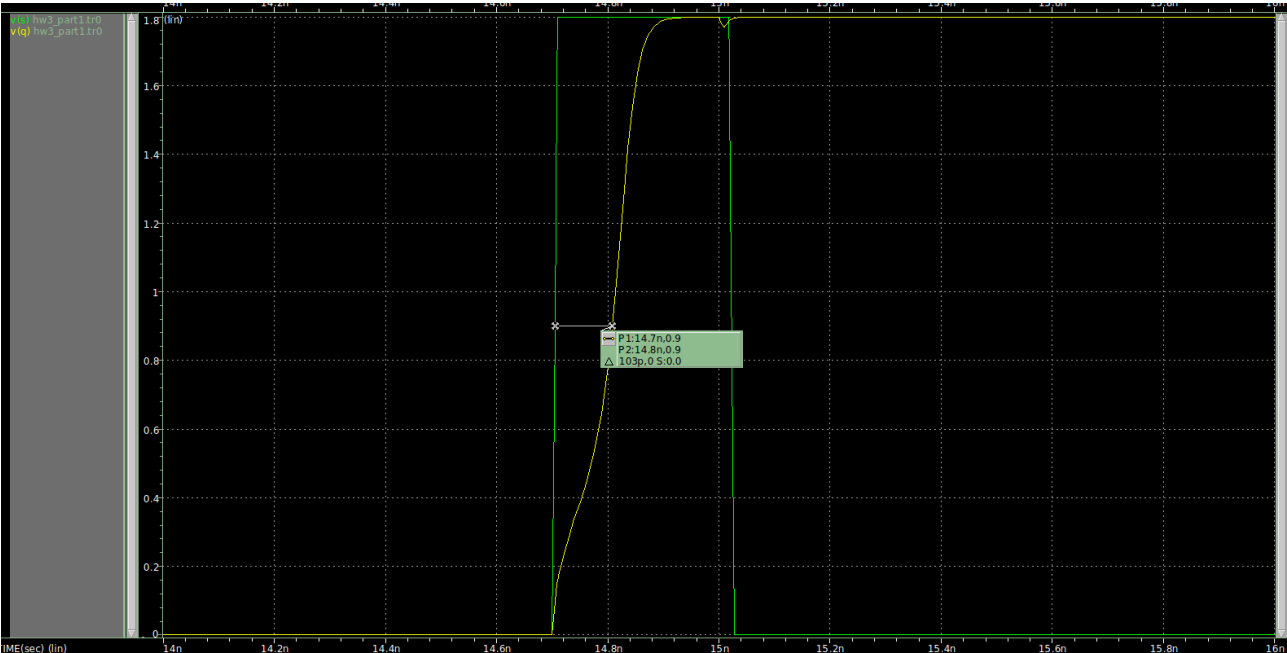
operation voltage:0.7v

由結果來看 setup time 和 hold time 都有增加，而且 tprqb 也有變大，尤其 setup time 變化蠻大的，這應該也是因為 post-sim 考量到了寄生電阻和電容才導致 setup 的速度慢很多，需要更長的 setup time。

setup time and hold time(post-sim)

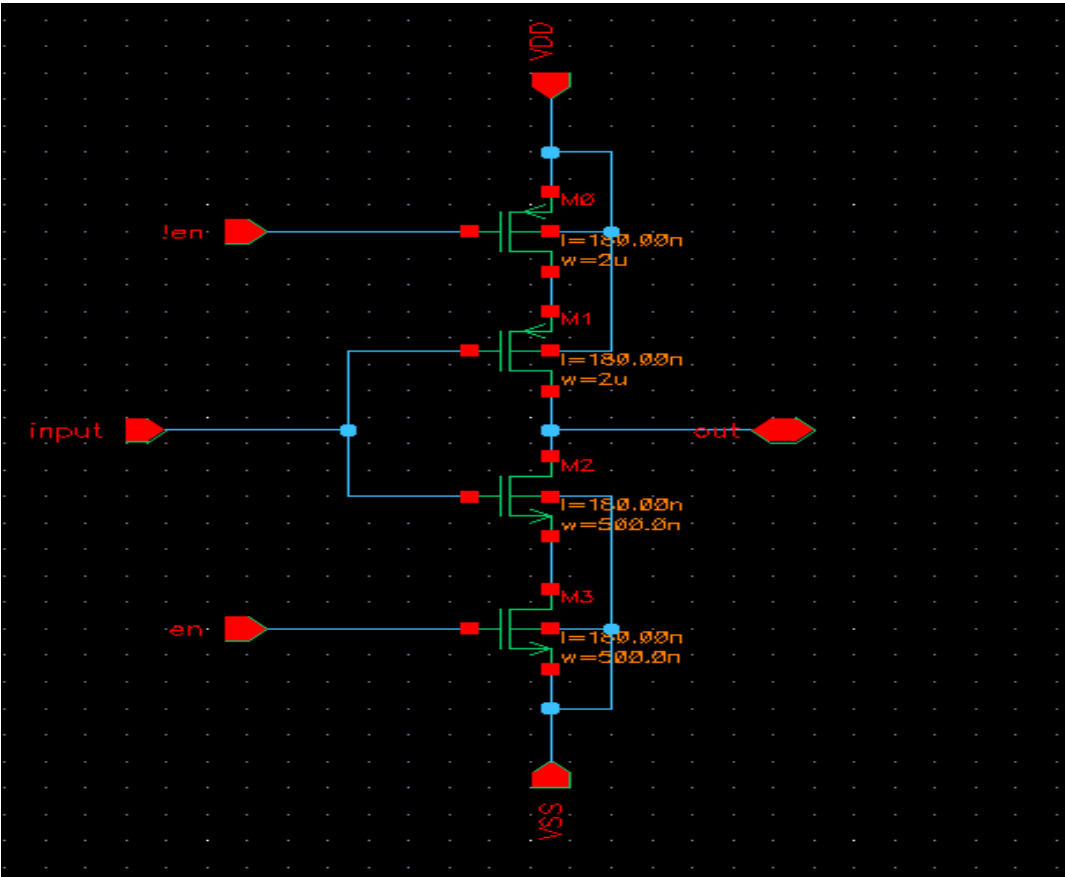


tpsq(post-sim):

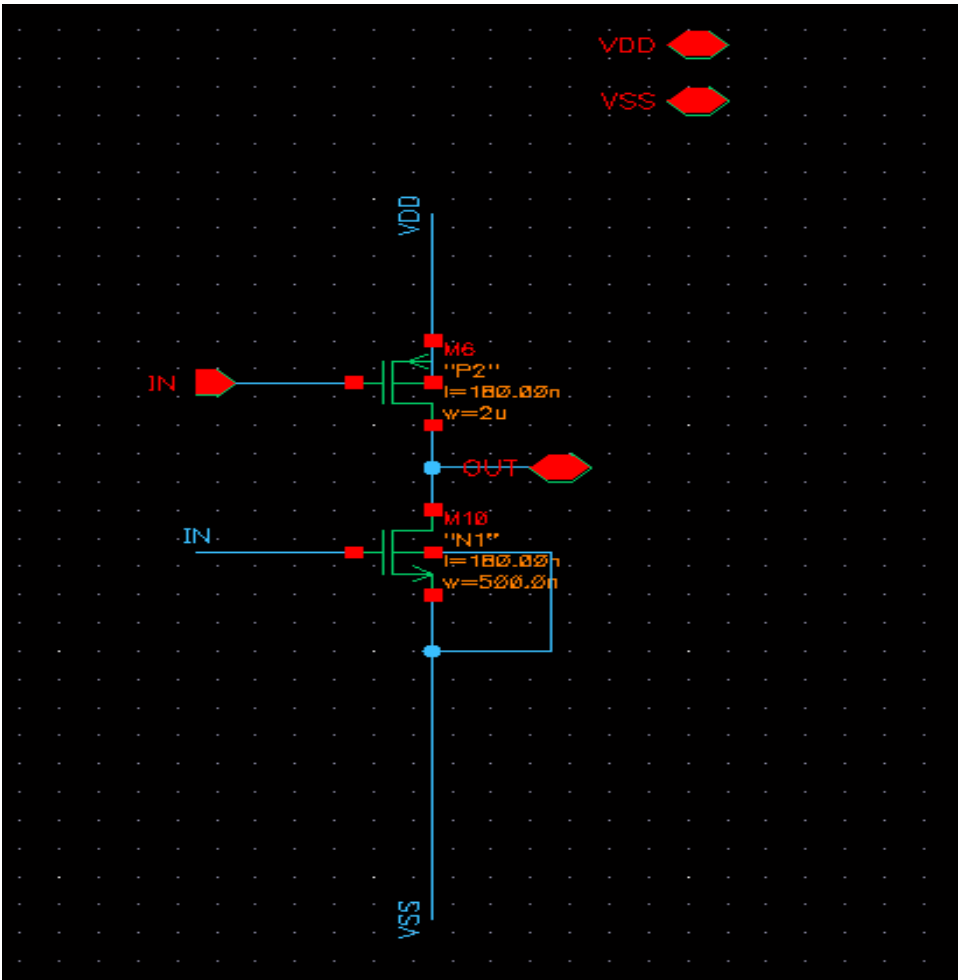


tprqb(post-sim)

tri_state



inverter:

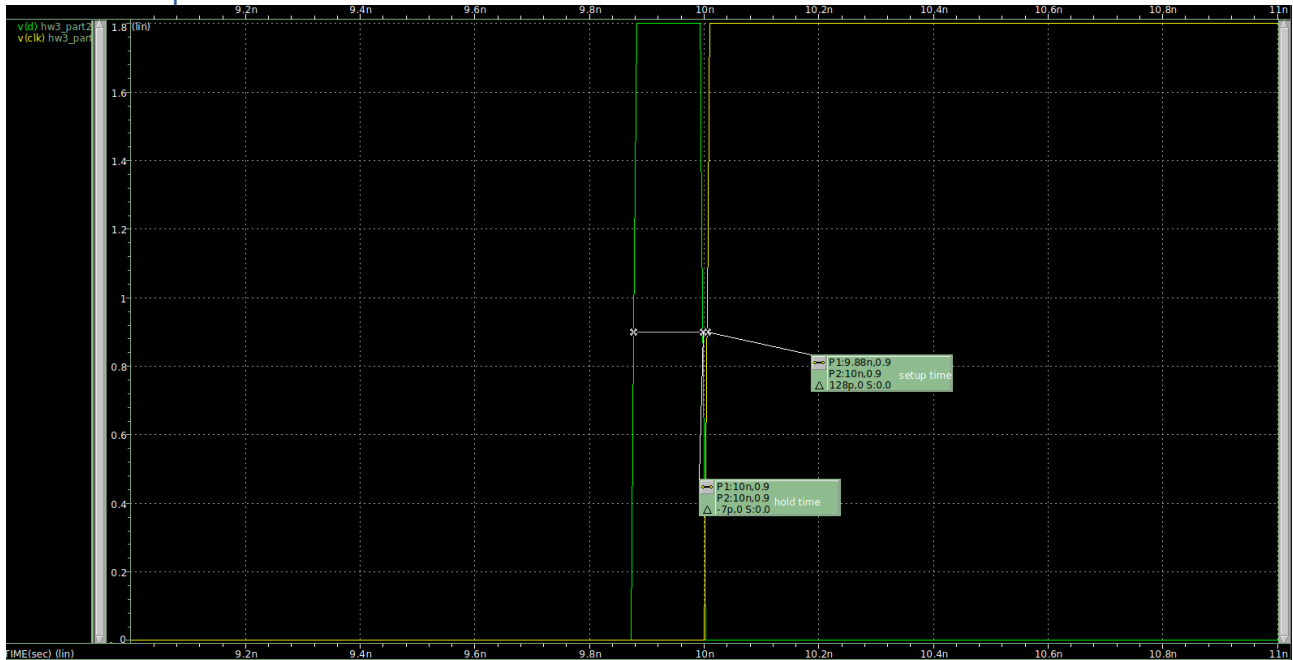


2. Simulate and find the setup time of this flip-flop. (7%)

setup time: 128ps

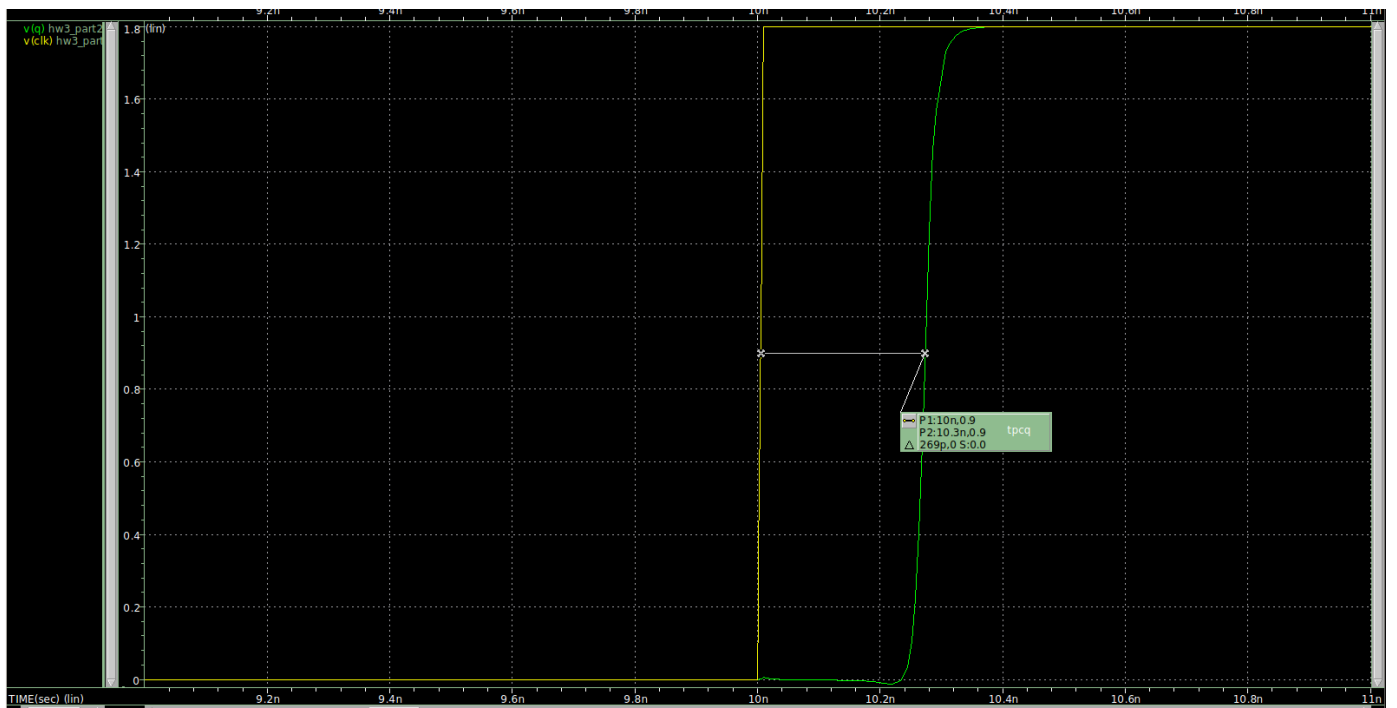
3. Simulate and find the hold time of this flip-flop. (7%)

hold time: -7ps

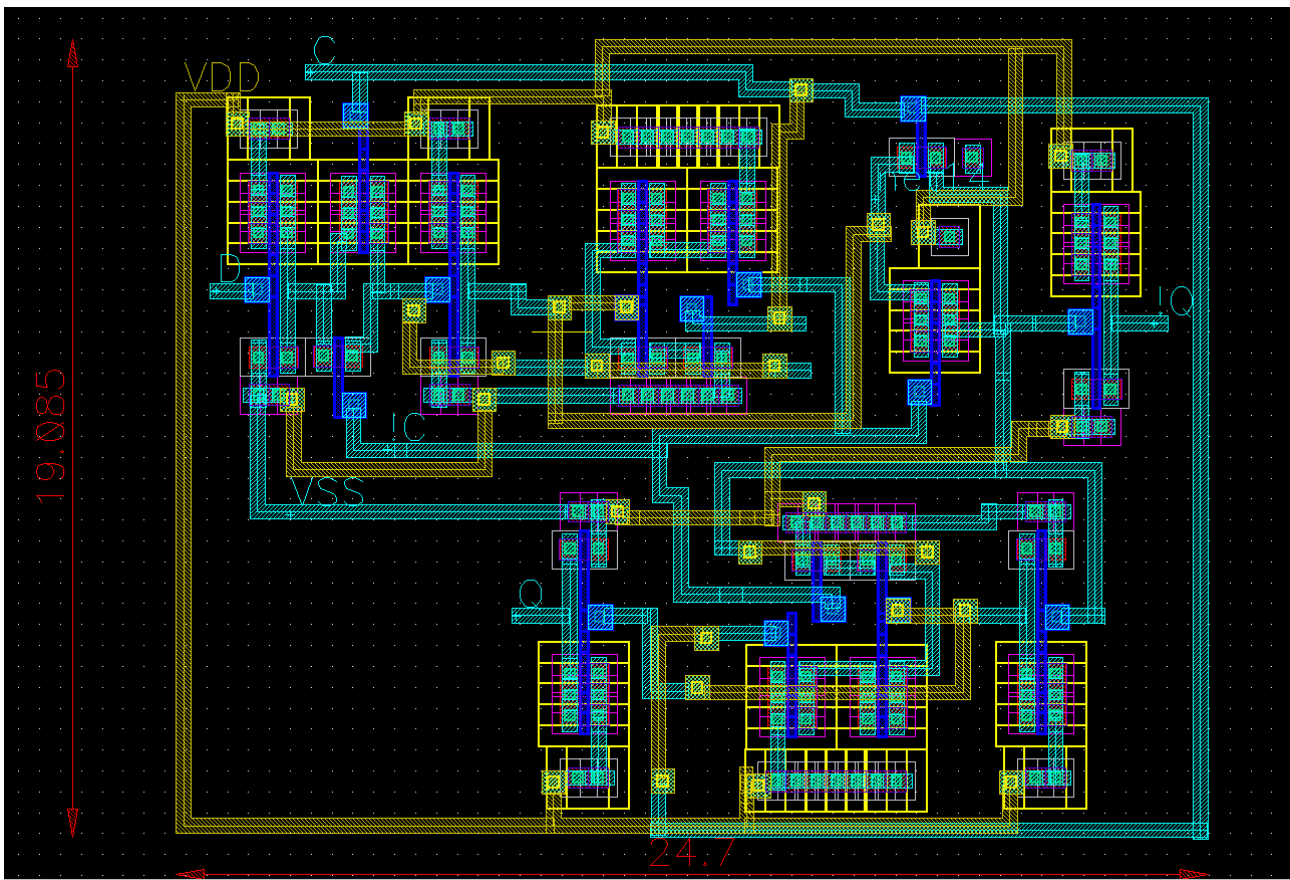


4. Simulate the clock to Q delay tpcq. (7%)

tpcq: 268.6ps



5. Complete the layout of this design. The layout should measure the area. (7%) Note: Area of the layout is the area of the minimum single rectangle that can cover all circuits.
 Area:471.3995(um²)



Calibre - RVE v2021.1.33.19 : hw3_part2.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All No Results Found

Check / Cell Results

DRC Summary Report - hw3_part2.drc.summary

File Edit Options Windows

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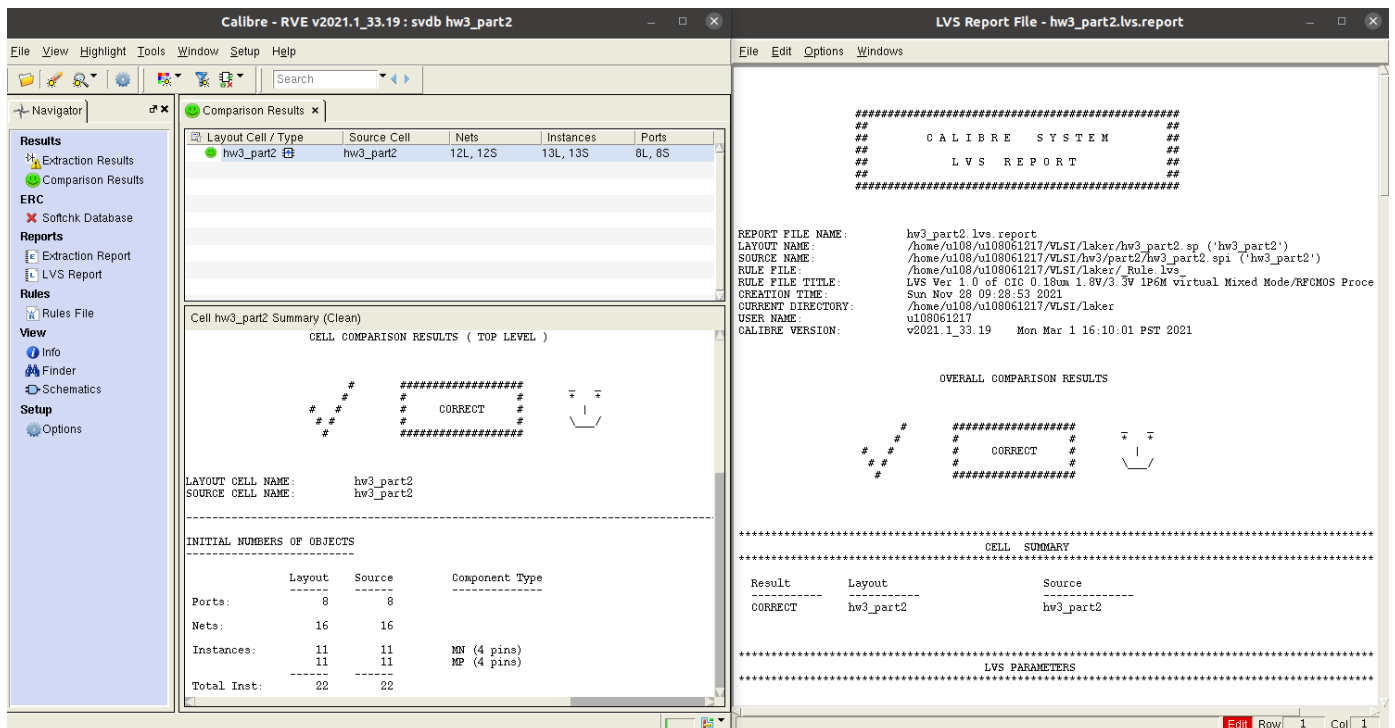
===== CALIBRE: DRC-H SUMMARY REPORT =====
Execution Date/Time: Sun Nov 28 09:25:44 2021
Calibre Version: v2021.1.33.19 Mon Mar 1 16:10:01 PST 2021
Rule File Pathname: /home/u108/u108061217/VLSI/laker/_rule.drc_
Rule File Title:
Layout System: GDS
Layout Path(s): hw3_part2.calibre.db
Layout Primary Cell: hw3_part2
Current Directory: /home/u108/u108061217/VLSI/laker
User Name: u108061217
Maximum Results/Rulecheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: hw3_part2.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: hw3_part2.drc.summary (REPLACE)
Geometry Flaggings: ACUTE = YES SKEW = NO ANGLED = NO OFFGRID = YES
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO

Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: NO

--- RUNTIME WARNINGS ---
Path endsegment length 0.15 at location (4.58,-10.575) in cell hw3_part2 on layer 48 datatype 0 is less
Path endsegment length 0.09 at location (4.52,-10.95) in cell hw3_part2 on layer 48 datatype 0 is less

--- ORIGINAL LAYER STATISTICS ---
LAYER ROM ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER DP ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP ID1 ..... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP ID2 ..... TOTAL Original Geometry Count = 0 (0)
LAYER UP ID0 ..... TOTAL Original Geometry Count = 0 (0)
LAYER BDSP ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER UP ID1 ..... TOTAL Original Geometry Count = 0 (0)
LAYER IOID ..... TOTAL Original Geometry Count = 0 (0)
LAYER IOMARK ..... TOTAL Original Geometry Count = 0 (0)
LAYER TG ..... TOTAL Original Geometry Count = 0 (0)
LAYER TWEL ..... TOTAL Original Geometry Count = 0 (0)
LAYER NWEL ..... TOTAL Original Geometry Count = 2 (58)
LAYER DIFF ..... TOTAL Original Geometry Count = 4 (92)
LAYER PPLUS ..... TOTAL Original Geometry Count = 2 (56)
LAYER WR ..... TOTAL Original Geometry Count = 0 (0)
LAYER PO1 ..... TOTAL Original Geometry Count = 3 (59)
LAYER COUNT ..... TOTAL Original Geometry Count = 7 (151)
LAYER HR ..... TOTAL Original Geometry Count = 0 (0)
LAYER CSD ..... TOTAL Original Geometry Count = 0 (0)

```



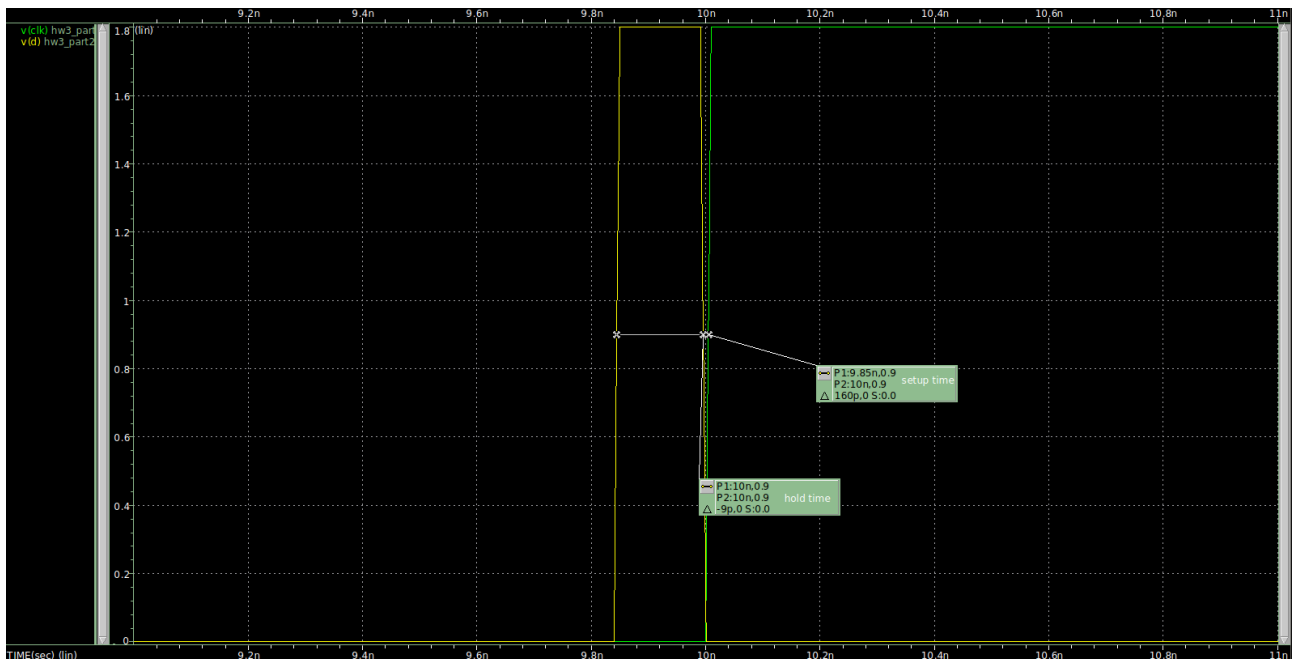
6. Run the post-layout simulation (post-sim) and compare it with pre simulation (2., 3. and 5.) (pre-sim) (7%)

pre-sim:
setup time: 128ps
hold time: -7ps
tpcq: 268.6ps

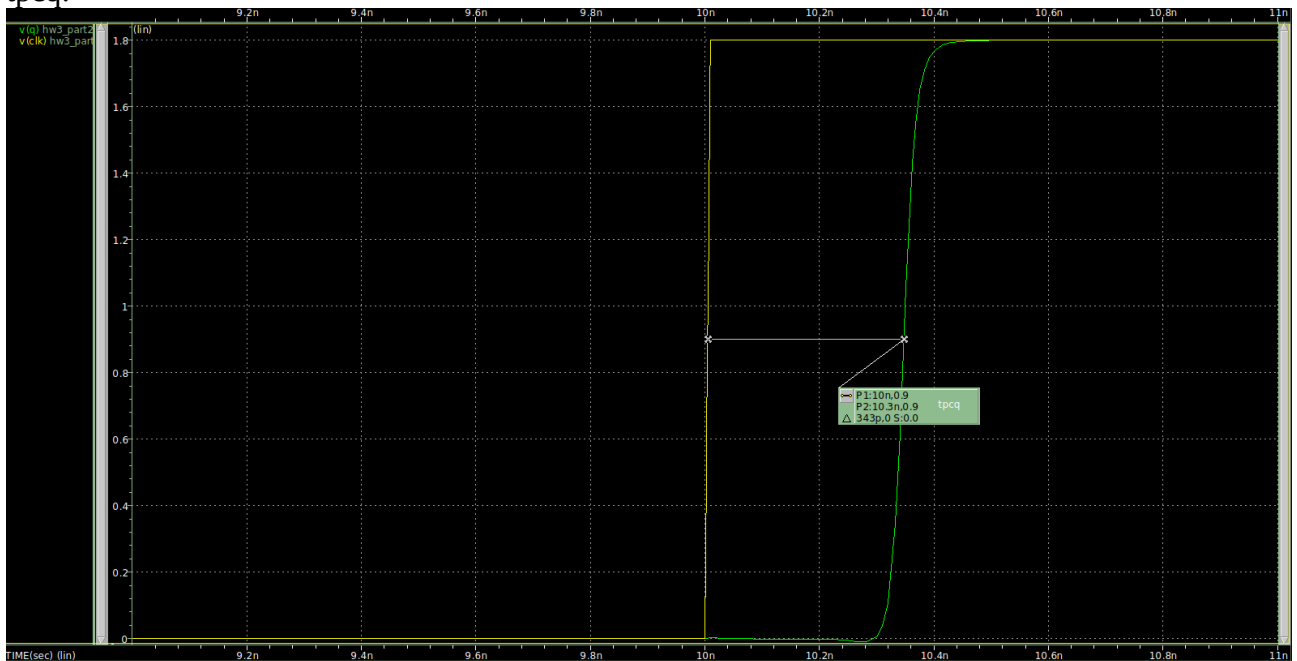
post-sim:
setup time: 160ps
hold time: -9ps
tpcq: 342.7ps

setup time 變大了, hold time 沒很大的變化 (稍微變小), 而 tpcq 也明顯變大, 主要也是考量寄生電阻電容, 影響了 setup 的速度, 並且也使延遲更大。

setup time and hold time:



tpcq:



Part III (15%)

Comment and Compare between Latch in Part I and DFF in Part II. (at least three comparisons) (each for 5%)

1. 首先可以由波形觀察出 Latch 和 DFF 的觸發方式並不相同，latch 的是 level-triggered，在波形中可以看出只有當 clk 是 high 的時候，才是 transparent mode，也就是 s 的訊號會被取樣，然後傳到 Q，而 DFF 則是 edge-triggered，只有在 clk 為 0→1 時，D 的訊號才會被取樣，傳到 Q。

2. 從結果來看 latch 的延遲較小，而從速度上來比較，latch 速度上會比 D flip-flop 快，由 layout 可以看出來 latch 的 Area 明顯小很多，而且用的 transistors 比較少，不用經過如此多的 transistor 所以也不會有太多的延遲，因此 latch 速度也會比 D flip-flop 快。

3.latch 的波相較於 D flip-flop 而言比較不穩定，一改變波形就容易呈現震盪不穩，當 clk 剛改變時 latch 的波形會混亂不穩定，並且 latch 相較之下對雜訊更敏感，抵抗雜訊的能力比 D flip-flop 更弱。

comment:在這個作業當中，主要瞭解到了 flip-flop 和 latch 不同的運作方式，兩者的觸發方式也不同，這些都可以從波形上看出來，並且在設計時 transistor 的 size 可能會影響 setup time 和 hold time 的限制，setup time 和 hold time 在電路的運作中很重要，電路實際運作時還要考慮經過 transistor 所造成的延遲等，所以需要時間去儲存或穩定訊號，如果 setup time 或 hold time 沒有在一定的範圍內，可能會使電路無法跟預期一樣運作，。