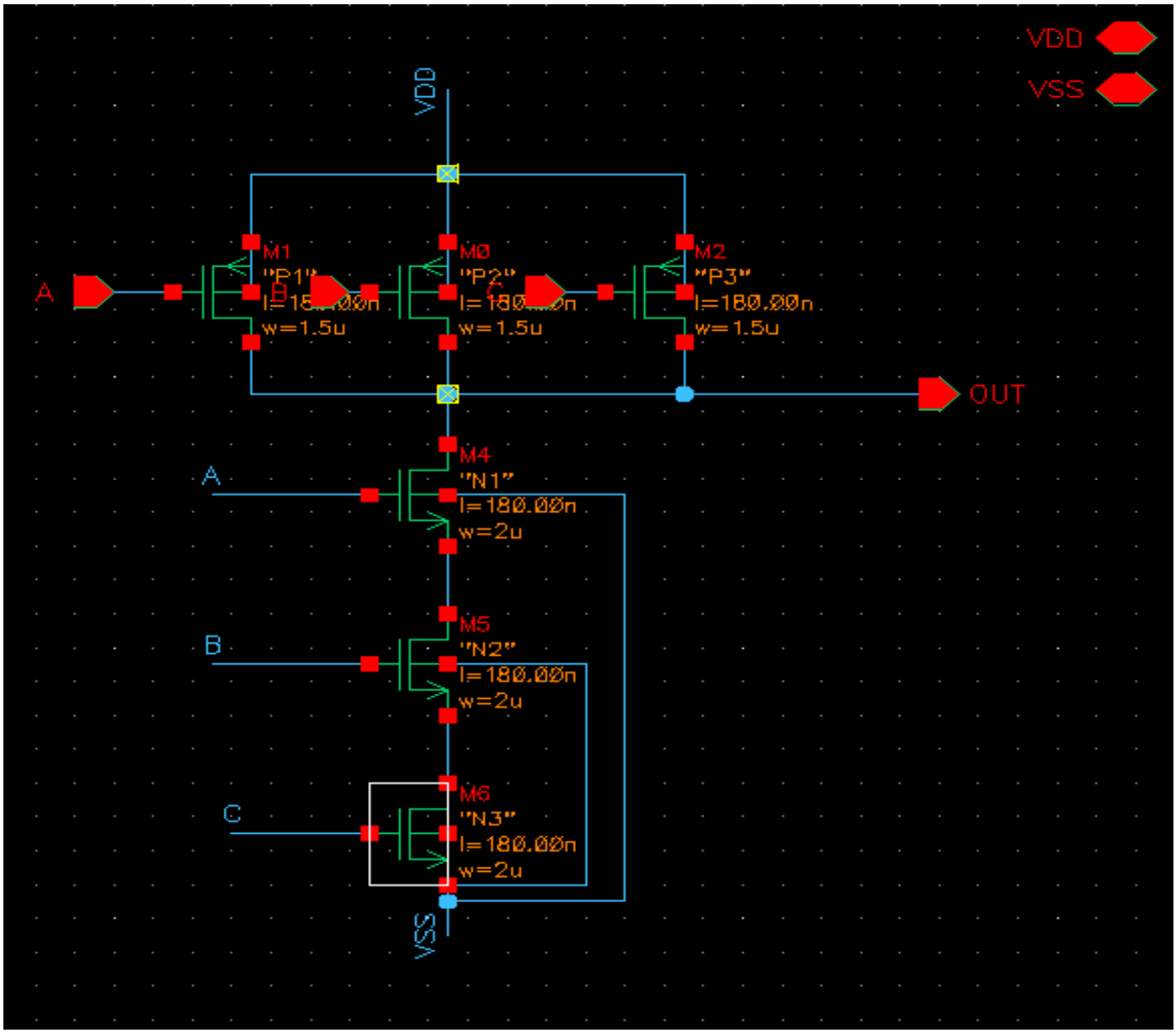
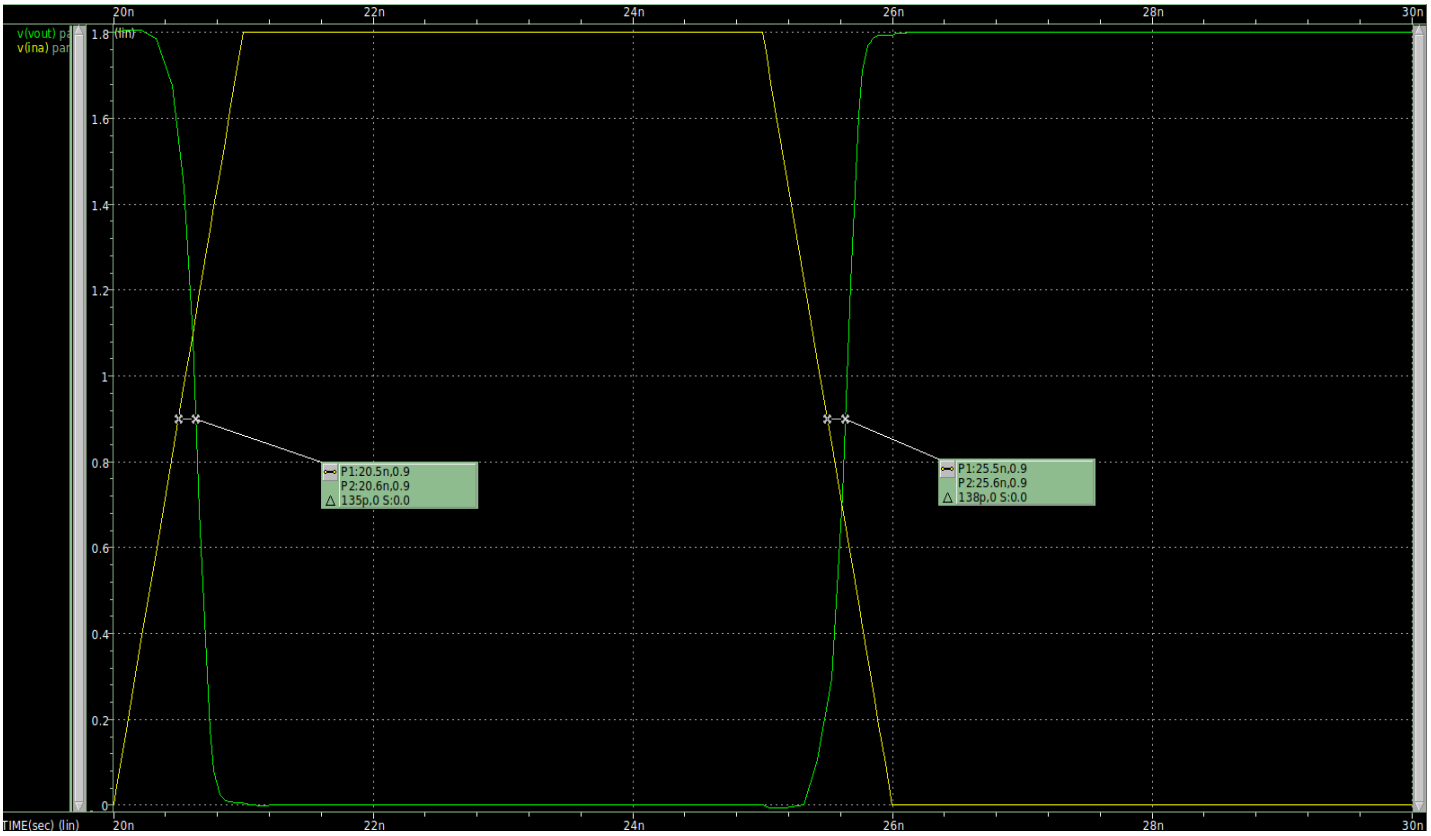
108061217 鍾永桓

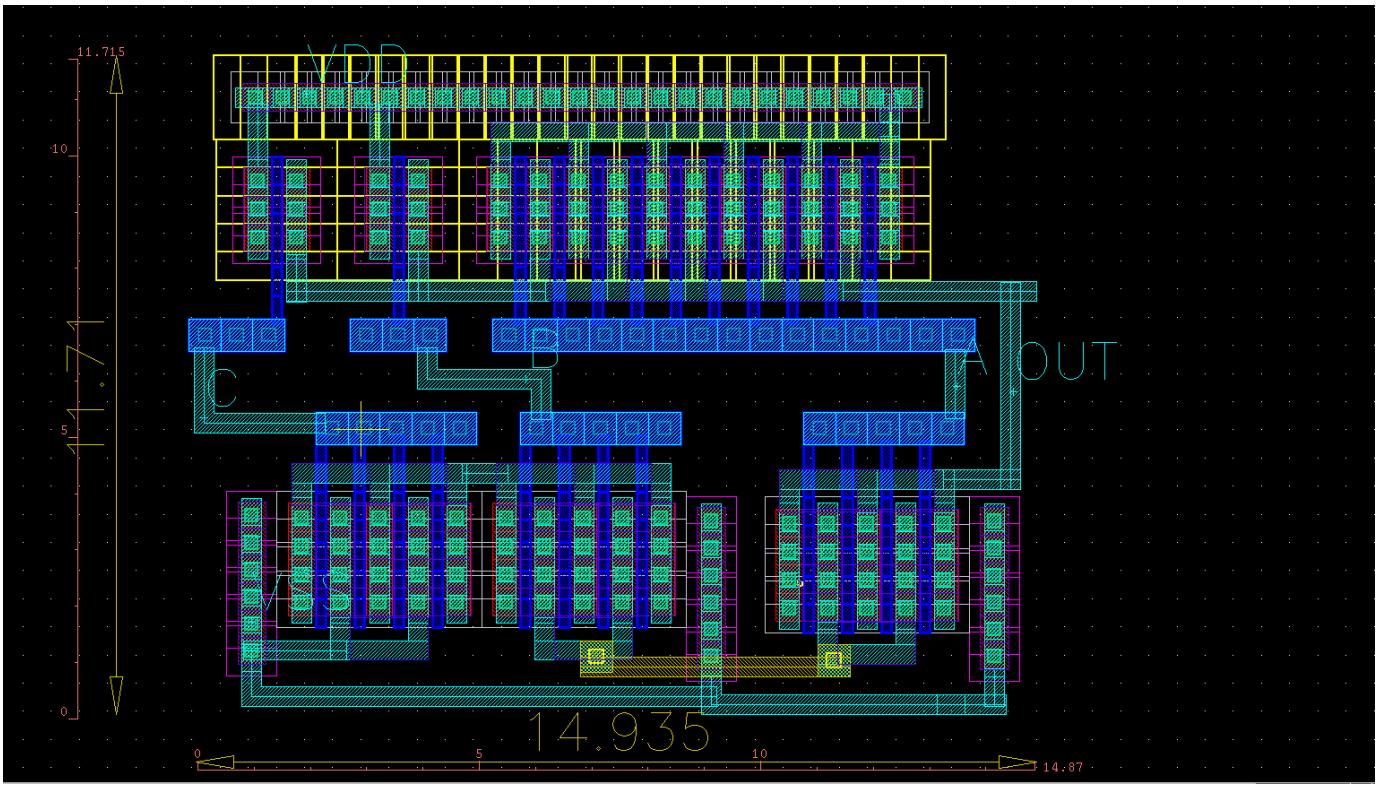
Part I (Combinational Circuit) (50%)

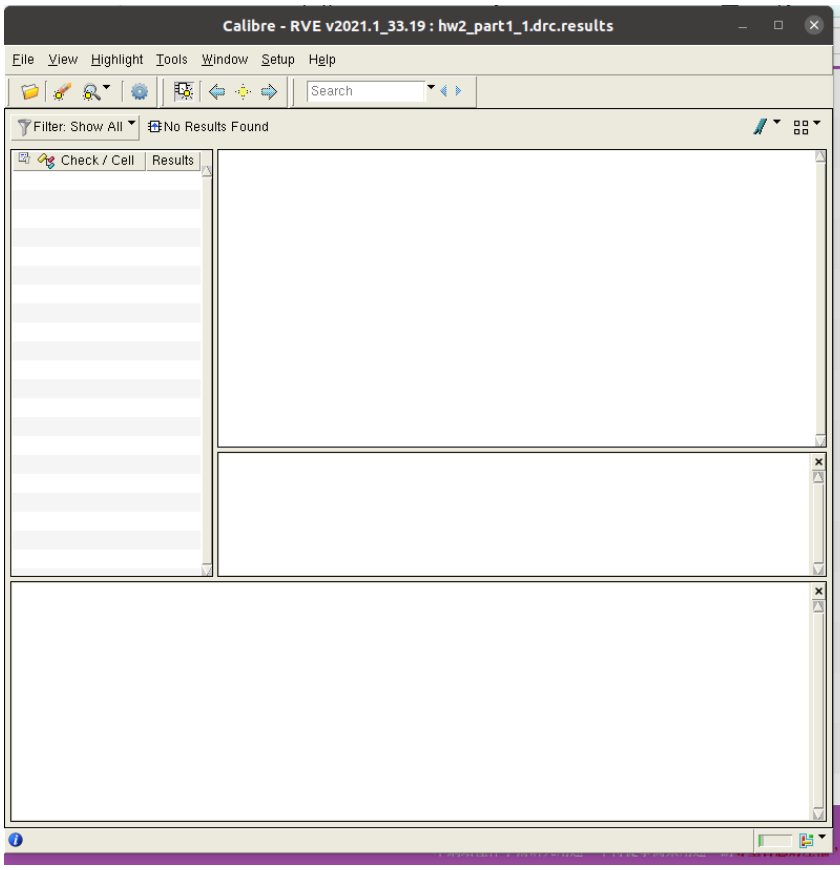
1. Please design a NAND3 shown in Fig. 1 with minimum length (0.18μm) of NMOS and PMOS. Under the condition TT25℃, the logic circuit has the same output rise delay (tpLH) and fall delay (tpHL) as the inverter in HW1 PartI with the following two input patterns. (4%)

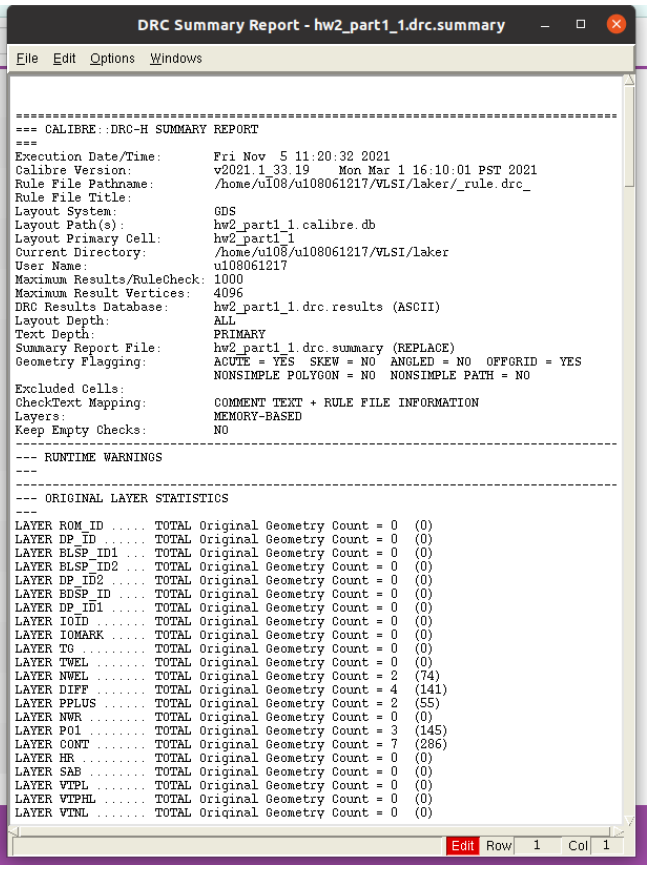
Use pattern (A,B,C)=(1,1,1)→(0,1,1) to find the rise delay (tpLH).
Use pattern (A,B,C)=(0,1,1)→(1,1,1) to find the fall delay (tpHL).
NMOS(A):2u/0.18u,m=4 ; PMOS(A):1.5u/0.18u,m=10 ;
NMOS(B):2u/0.18u,m=4 ; PMOS(B):1.5u/0.18u,m=1;
NMOS(C):2u/0.18u,m=4 ; PMOS(C):1.5u/0.18u,m=1;
tpLH = 134.9ps(和 hw1 part1（135.3ps）的誤差:-0.2%)
tpHL= 137.8ps(和 hw1 part1(130.4ps)的誤差: 5.7%)

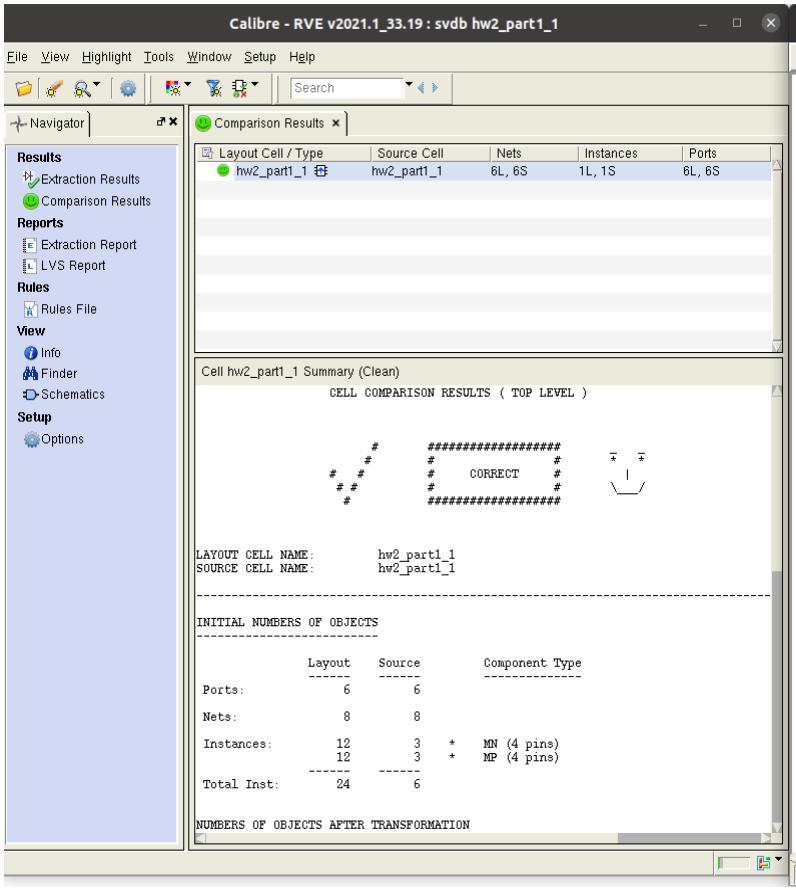


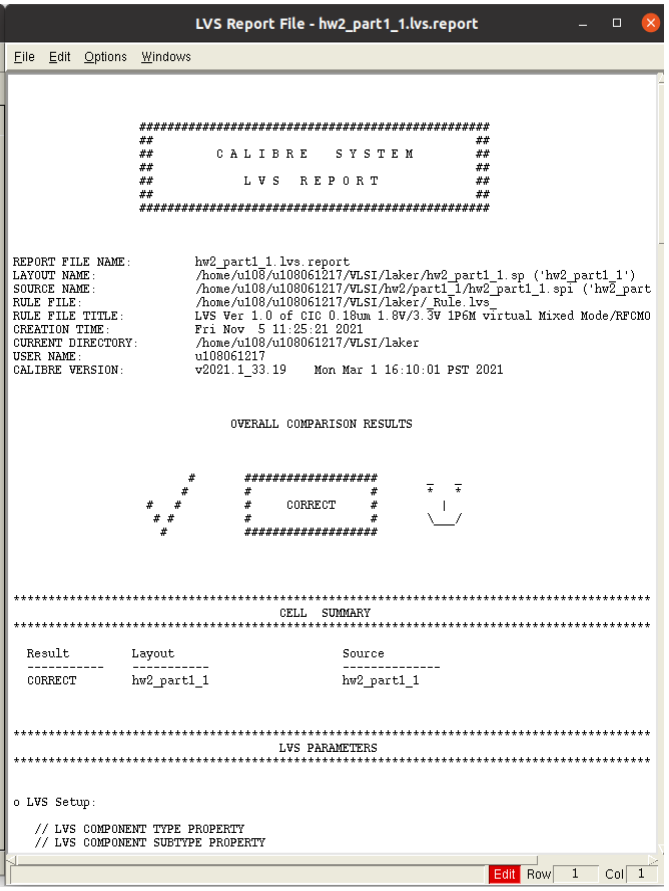

20n
22n
24n
26n
28n
30n
v(vout) pa
v(ina) par
1.8 (lin)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
P1:20.5n,0.9
P2:20.6n,0.9
△ 135p,0 S:0.0
P1:25.5n,0.9
P2:25.6n,0.9
△ 138p,0 S:0.0
TIME(sec) (lin)


11.715
10
5
0
11.71
VDD
C
B
A
OUT
14.935
0
5
10
14.87


Calibre - RVE v2021.1_33.19 : hw2_part1_1.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
No Results Found
Check / Cell
Results


DRC Summary Report - hw2_part1_1.drc.summary
File Edit Options Windows
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Fri Nov 5 11:20:32 2021
Calibre Version: v2021.1_33.19 Mon Mar 1 16:10:01 PST 2021
Rule File Pathname: /home/u108/u108061217/VLSI/laker/_rule.drc_
Rule File Title:
Layout System: GDS
Layout Path(s): hw2_part1_1.calibre.db
Layout Primary Cell: hw2_part1_1
Current Directory: /home/u108/u108061217/VLSI/laker
User Name: u108061217
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: hw2_part1_1.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: hw2_part1_1.drc.summary (REPLACE)
Geometry Flagging: ACUTE = YES SKEW = NO ANGLED = NO OFFGRID = YES
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: NO
--- RUNTIME WARNINGS
--- ORIGINAL LAYER STATISTICS
LAYER ROM_ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP_ID1 ... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP_ID2 ... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID2 ..... TOTAL Original Geometry Count = 0 (0)
LAYER BDSP_ID .... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID1 ..... TOTAL Original Geometry Count = 0 (0)
LAYER IOID ..... TOTAL Original Geometry Count = 0 (0)
LAYER IOMARK ..... TOTAL Original Geometry Count = 0 (0)
LAYER TG ..... TOTAL Original Geometry Count = 0 (0)
LAYER TWEL ..... TOTAL Original Geometry Count = 0 (0)
LAYER NWEL ..... TOTAL Original Geometry Count = 2 (74)
LAYER DIFF ..... TOTAL Original Geometry Count = 4 (141)
LAYER PPLUS ..... TOTAL Original Geometry Count = 2 (55)
LAYER NWR ..... TOTAL Original Geometry Count = 0 (0)
LAYER P01 ..... TOTAL Original Geometry Count = 3 (145)
LAYER CONT ..... TOTAL Original Geometry Count = 7 (286)
LAYER HR ..... TOTAL Original Geometry Count = 0 (0)
LAYER SAB ..... TOTAL Original Geometry Count = 0 (0)
LAYER VTPL ..... TOTAL Original Geometry Count = 0 (0)
LAYER VTPHL ..... TOTAL Original Geometry Count = 0 (0)
LAYER VTNL ..... TOTAL Original Geometry Count = 0 (0)
Edit Row 1 Col 1


Calibre - RVE v2021.1_33.19 : svdb hw2_part1_1
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
hw2_part1_1
hw2_part1_1
6L, 6S
1L, 1S
6L, 6S
Cell hw2_part1_1 Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: hw2_part1_1
SOURCE CELL NAME: hw2_part1_1
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 6 6
Nets: 8 8
Instances: 12 3 * MN (4 pins)
12 3 * MP (4 pins)
Total Inst: 24 6
NUMBERS OF OBJECTS AFTER TRANSFORMATION


LVS Report File - hw2_part1_1.lvs.report
File Edit Options Windows
C A L I B R E S Y S T E M
L V S R E P O R T
REPORT FILE NAME: hw2_part1_1.lvs.report
LAYOUT NAME: /home/u108/u108061217/VLSI/laker/hw2_part1_1.sp ('hw2_part1_1')
SOURCE NAME: /home/u108/u108061217/VLSI/hw2/part1_1/hw2_part1_1.spi ('hw2_part
RULE FILE: /home/u108/u108061217/VLSI/laker/_Rule.lvs_
RULE FILE TITLE: LVS Ver 1.0 of CIC 0.18um 1.8V/3.3V 1P6M virtual Mixed Mode/RFCMO
CREATION TIME: Fri Nov 5 11:25:21 2021
CURRENT DIRECTORY: /home/u108/u108061217/VLSI/laker
USER NAME: u108061217
CALIBRE VERSION: v2021.1_33.19 Mon Mar 1 16:10:01 PST 2021
OVERALL COMPARISON RESULTS
CORRECT
CELL SUMMARY
Result Layout Source
CORRECT hw2_part1_1 hw2_part1_1
LVS PARAMETERS
o LVS Setup:
// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY
Edit Row 1 Col 1

2. Use the NAND3 designed above. Now, change one input from 0V to VDD at once and fix other inputs (see Table 1). Run simulation in different conditions and find output rise delay (tpLH) and fall delay (tpHL). Fill your results in Table 1. (0.5% for each gird, 6% in total)

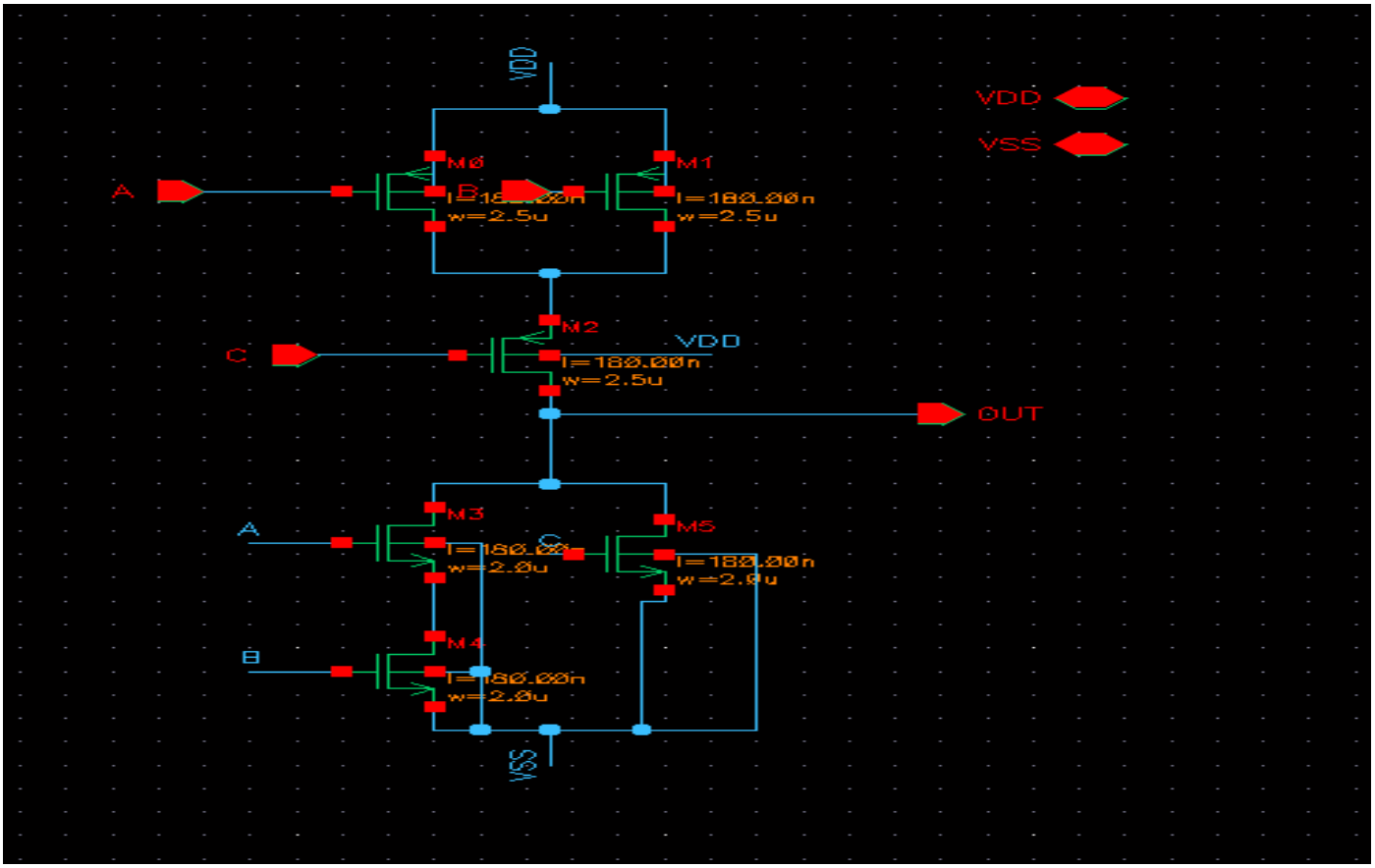
Input A	Input B	Input C	Conclusion	tpLH(ps)	tpHL(ps)
pulse	1	1	SS 125℃	248.5	311.4
			SF 25℃	61.65	297.8
			TT 25℃	137.8	134.9
			FS 25℃	85.97	164.7
			FF -40℃	125.2	99.29
1	pulse	1	SS 125℃	1295	279.6
			SF 25℃	599.6	236.9
			TT 25℃	658.2	71.78
			FS 25℃	620.6	98.88
			FF -40℃	568.8	30.77
1	1	pulse	SS 125℃	1528	276.6
			SF 25℃	686.8	224.8
			TT 25℃	714.3	62.51
			FS 25℃	703.9	92.5
			FF -40℃	597.2	23.17

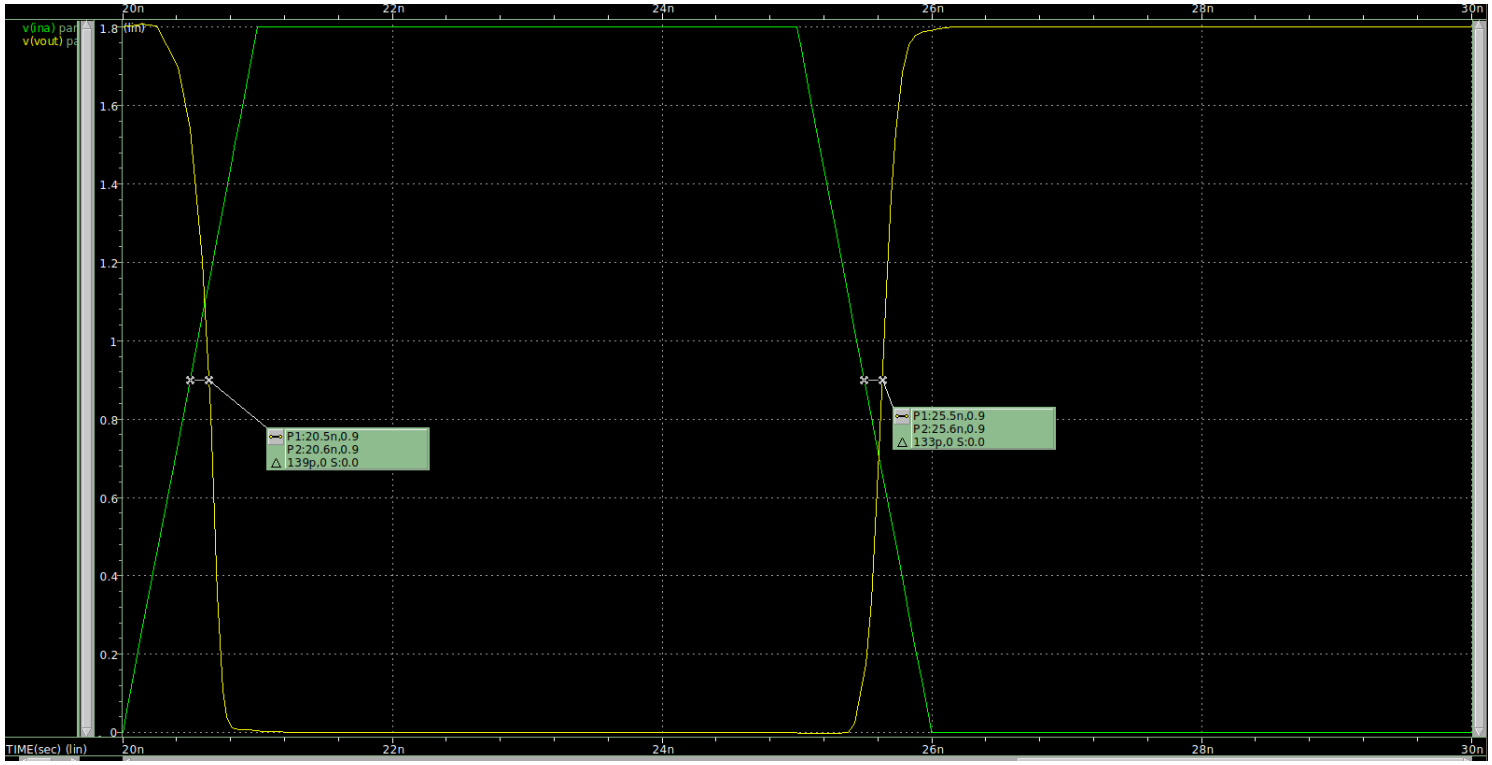
3. Comment what you have observed from Table 1 and give some discussion. (5%) (As long as your discussions are reasonable, you can get all points)

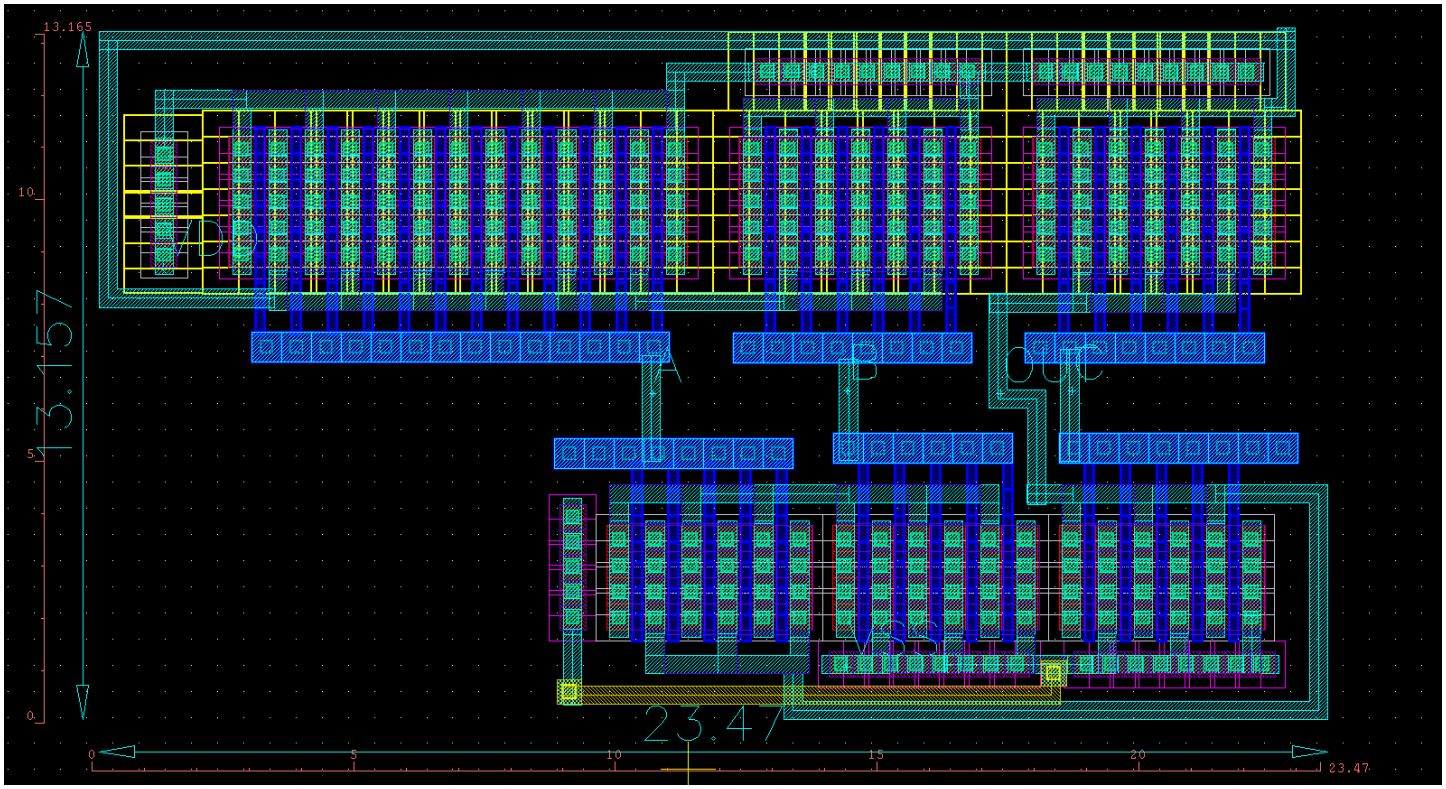
由 table1 的結果可以看出，無論是用Ａ，Ｂ，Ｃ作為 pulse，在 SS 125℃的情況下所得到的 tpLH 和 tpHL 都是最大的，而 FF 所得到的 tpLH 和 tpHL 都是最小的，所以可知在 SS 下 delay 最大，FF 下 delay 最小，此外由這個結果可以看出在相同條件下，以 C 作為 pulse 時 tpLH 會最大，以 A 作為 pulse 則是 tpHL 最大，那是因為由於 A,B,C 作為 input pulse 到 out 的路徑不同，而且本題中 A,B,C 所接到的 gate 的 mos 尺寸差異也很大，所以 delay 也不相等。

4. Please design a logic circuit shown in Fig. 2 with minimum length (0.18μm) of NMOS and PMOS. Under the condition TT25℃, the logic circuit has the same output rise delay (tpLH) and fall delay (tpHL) as the inverter in HW1 PartI with the following two input patterns. (4%)
Note：Output loading Cload = 0.1pF (the same as HW1 Part I)
Use pattern (A, B, C) = (1, 1, 0) → (0, 1, 0) to find the rise delay (tpLH).
Use pattern (A, B, C) = (0, 1, 0) → (1, 1, 0) to find the fall delay (tpHL).

tpLH = 133.3ps(和 hw1 part1（135.3ps）的誤差:-1.5%)
tpHL= 138.6ps(和 hw1 part1(130.4ps)的誤差: 6.3%)
NMOS(A):2u/0.18u,m=5 ; PMOS(A):2.5u/0.18u,m=12 ;
NMOS(B):2u/0.18u,m=5 ; PMOS(B):2.5u/0.18u,m=6;
NMOS(C):2u/0.18u,m=5 ; PMOS(C):2.5u/0.18u,m=6;




v(ina) par
v(vout) pa
1.8 (lin)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
20n
22n
24n
26n
28n
30n
P1:20.5n,0.9
P2:20.6n,0.9
△ 139p,0 S:0.0
P1:25.5n,0.9
P2:25.6n,0.9
△ 133p,0 S:0.0
TIME(sec) (lin)


13.165
10
13.157
5
0
A
B
C
VDD
VSS
23.47
0
5
10
15
20
23.47

5. Given the logic circuit in Fig. 2, please change one input from 0V to VDD at once and fix other inputs (see Table 2). Run simulation in different conditions and fined output rise delay (tpLH) and fall delay (tpHL). Please fill the simulation results in Table 2. (0.5% for each gird, 6% in total)

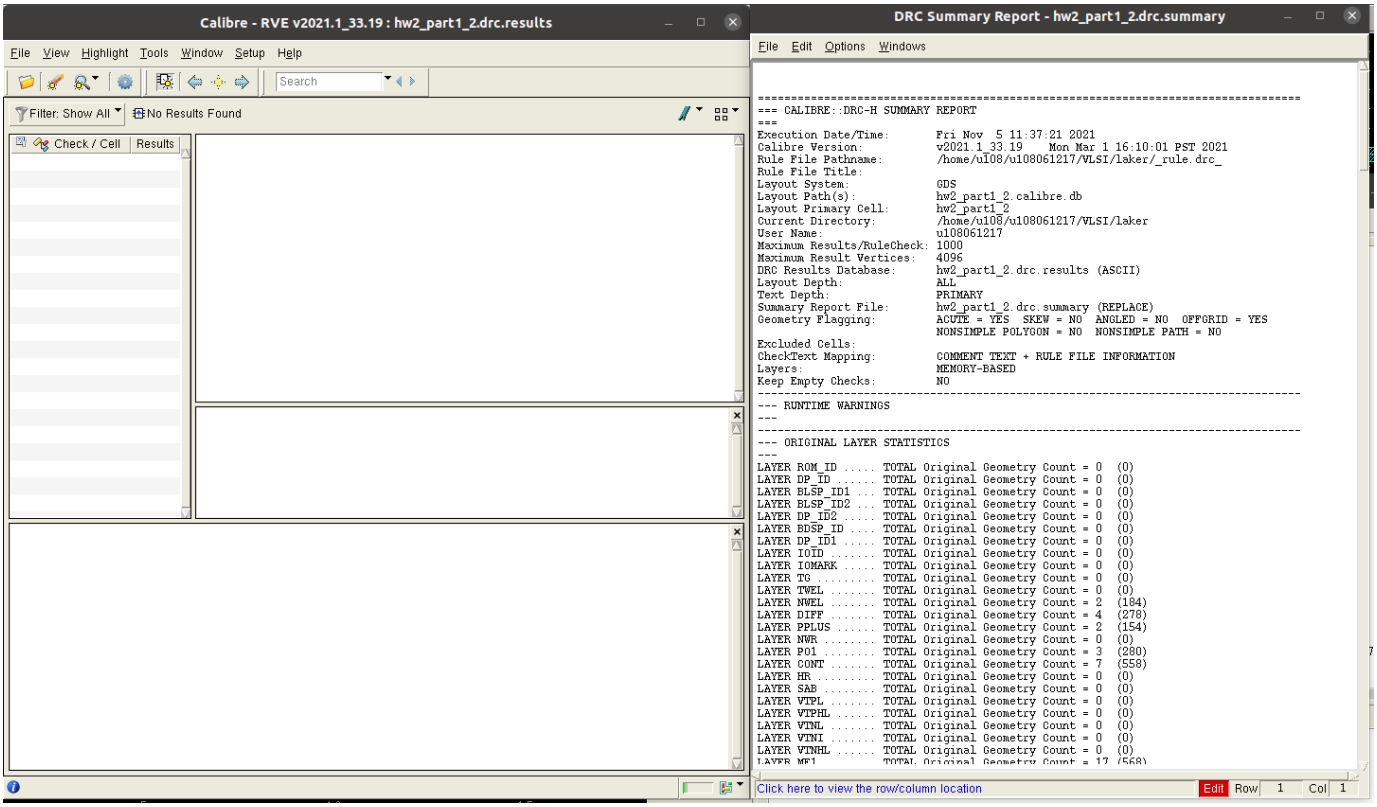
	Input A	Input B	Input C	Conclusion	tpLH(ps)	tpHL(ps)
Case1	pulse	1	0	SS 125℃	267.2	320.4
				SF 25℃	58.3	302.5
				TT 25℃	133.3	138.6
				FS 25℃	106	169.5
				FF -40℃	115.9	106.3
Case2	1	pulse	0	SS 125℃	454.1	279.3
				SF 25℃	171.5	256.8
				TT 25℃	239.2	104.2
				FS 25℃	212.5	130.6
				FF -40℃	210	70.79
Case3	0	1	pulse	SS 125℃	334.8	167.2
				SF 25℃	131.6	175.7
				TT 25℃	205.2	47.69
				FS 25℃	181.1	72.03
				FF -40℃	188.4	23.71

6. Comment what you have observed from Table 2 and give some discussions. (5%) (As long as your discussions are reasonable, you can get all points)

表中很明顯可以看出溫度和 corner 對於 delay 的影響，FF 時 delay 在大多情況下最小而 SS 則在大多情況下 delay 最大，此外不同 case 會影響導通的路徑，它們使用不同的 input pulse，而且開啟不同的路徑，如果電容充放電時路徑不導通可能會使其 delay 很大，由表中的結果可以看出 case2 的 tpLH 在所有情況下都是最大的，可能是由於其A為 1 使以 A 作為 gate input 的 pmos 不導通，所以在 high to low 時阻值很大，所以 case2 時 tpLH 會較大。

7. Complete the layout of Fig. 2. Show the figure of your layout and DRC/LVS report. (10%) and measure the area. (5%) Note: Area of the layout is the area of minimum single rectangle that can cover all circuits

Area: 308.39639um^2


Calibre - RVE v2021.1_33.19 : hw2_part1_2.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
No Results Found
Check / Cell
Results
DRC Summary Report - hw2_part1_2.drc.summary
File Edit Options Windows
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Fri Nov 5 11:37:21 2021
Calibre Version: v2021.1_33.19 Mon Mar 1 16:10:01 PST 2021
Rule File Pathname: /home/u108/u108061217/VLSI/laker/_rule.drc_
Rule File Title:
Layout System: GDS
Layout Path(s): hw2_part1_2.calibre.db
Layout Primary Cell: hw2_part1_2
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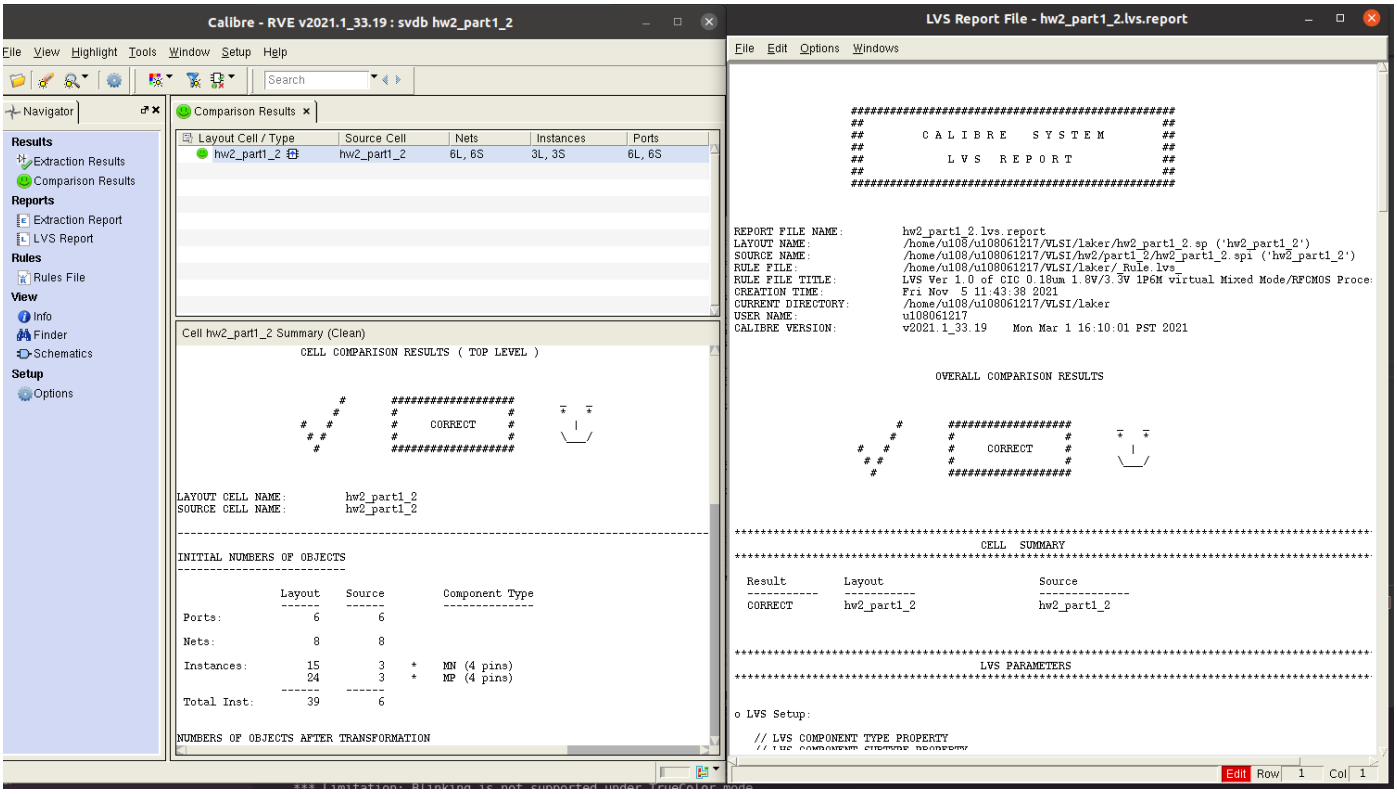
User Name: u108061217
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: hw2_part1_2.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: hw2_part1_2.drc.summary (REPLACE)
Geometry Flagging: ACUTE = YES SKEW = NO ANGLED = NO OFFGRID = YES
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: NO
--- RUNTIME WARNINGS
--- ORIGINAL LAYER STATISTICS
LAYER ROM_ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP_ID1 ... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP_ID2 ... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID2 ..... TOTAL Original Geometry Count = 0 (0)
LAYER BDSP_ID .... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID1 ..... TOTAL Original Geometry Count = 0 (0)
LAYER IOID .... TOTAL Original Geometry Count = 0 (0)
LAYER IOMARK ..... TOTAL Original Geometry Count = 0 (0)
LAYER TG .... TOTAL Original Geometry Count = 0 (0)
LAYER TWEL .... TOTAL Original Geometry Count = 0 (0)
LAYER NWEL .... TOTAL Original Geometry Count = 2 (184)
LAYER DIFF .... TOTAL Original Geometry Count = 4 (278)
LAYER PPLUS ...... TOTAL Original Geometry Count = 2 (154)
LAYER NWR .... TOTAL Original Geometry Count = 0 (0)
LAYER PO1 .... TOTAL Original Geometry Count = 3 (280)
LAYER CONT .... TOTAL Original Geometry Count = 7 (558)
LAYER HR .... TOTAL Original Geometry Count = 0 (0)
LAYER SAB .... TOTAL Original Geometry Count = 0 (0)
LAYER VTPL .... TOTAL Original Geometry Count = 0 (0)
LAYER VTPHL ...... TOTAL Original Geometry Count = 0 (0)
LAYER VTNL .... TOTAL Original Geometry Count = 0 (0)
LAYER VTNI .... TOTAL Original Geometry Count = 0 (0)
LAYER VTNHL ...... TOTAL Original Geometry Count = 0 (0)
Click here to view the row/column location
Edit Row 1 Col 1

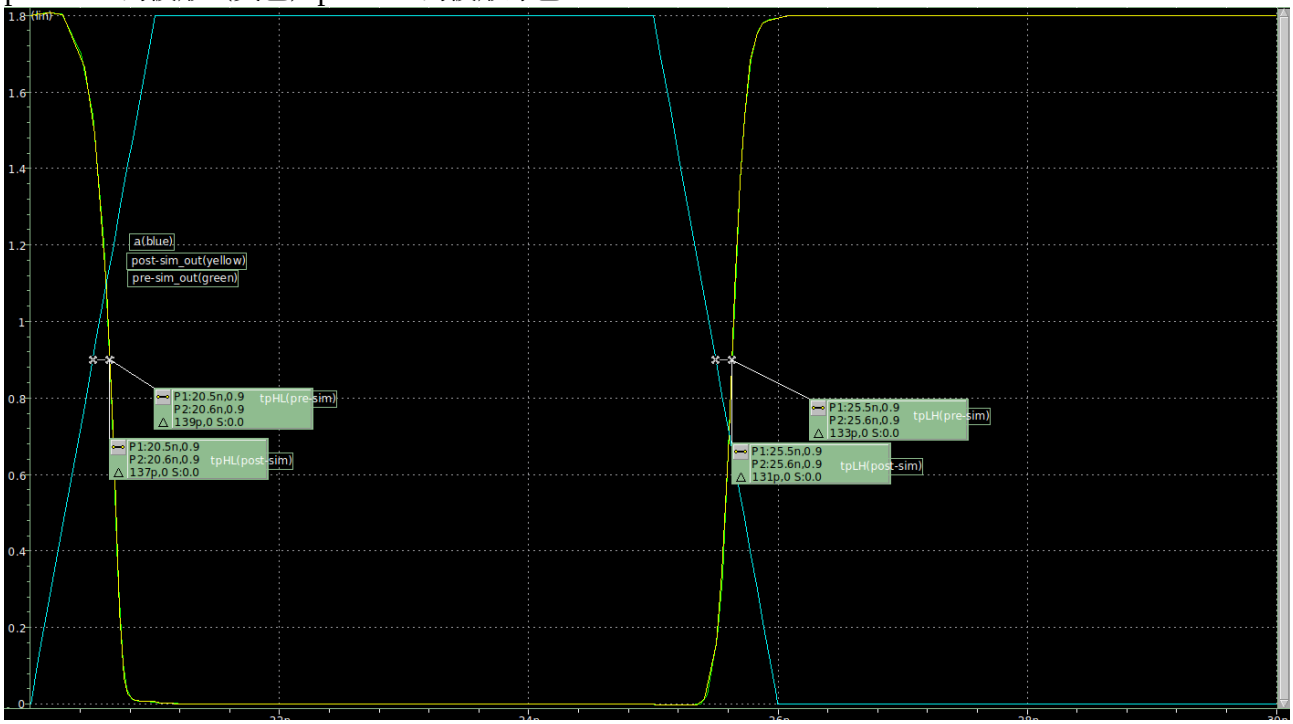

Calibre - RVE v2021.1_33.19 : svdb hw2_part1_2
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
hw2_part1_2
hw2_part1_2
6L, 6S
3L, 3S
6L, 6S
Cell hw2_part1_2 Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: hw2_part1_2
SOURCE CELL NAME: hw2_part1_2
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 6 6
Nets: 8 8
Instances: 15 3 * MN (4 pins)
24 3 * MP (4 pins)
Total Inst: 39 6
NUMBERS OF OBJECTS AFTER TRANSFORMATION
LVS Report File - hw2_part1_2.lvs.report
File Edit Options Windows
C A L I B R E S Y S T E M
L V S R E P O R T
REPORT FILE NAME: hw2_part1_2.lvs.report
LAYOUT NAME: /home/u108/u108061217/VLSI/laker/hw2_part1_2.sp ('hw2_part1_2')
SOURCE NAME: /home/u108/u108061217/VLSI/hw2/part1_2/hw2_part1_2.spi ('hw2_part1_2')
RULE FILE: /home/u108/u108061217/VLSI/laker/_Rule.lvs_
RULE FILE TITLE: LVS Ver 1.0 of CIC 0.18um 1.8V/3.3V 1P6M virtual Mixed Mode/RFCMOS Proce
CREATION TIME: Fri Nov 5 11:43:30 2021
CURRENT DIRECTORY: /home/u108/u108061217/VLSI/laker
USER NAME: u108061217
CALIBRE VERSION: v2021.1_33.19 Mon Mar 1 16:10:01 PST 2021
OVERALL COMPARISON RESULTS
CORRECT
CELL SUMMARY
Result Layout Source
CORRECT hw2_part1_2 hw2_part1_2
LVS PARAMETERS
o LVS Setup:
// LVS COMPONENT TYPE PROPERTY
Edit Row 1 Col 1

Area:13.157um * 23.47um = 308.39639m^2

8. Run post-sim (with R-C-CC extraction), compare the result and waveform with pre-sim. (5%)

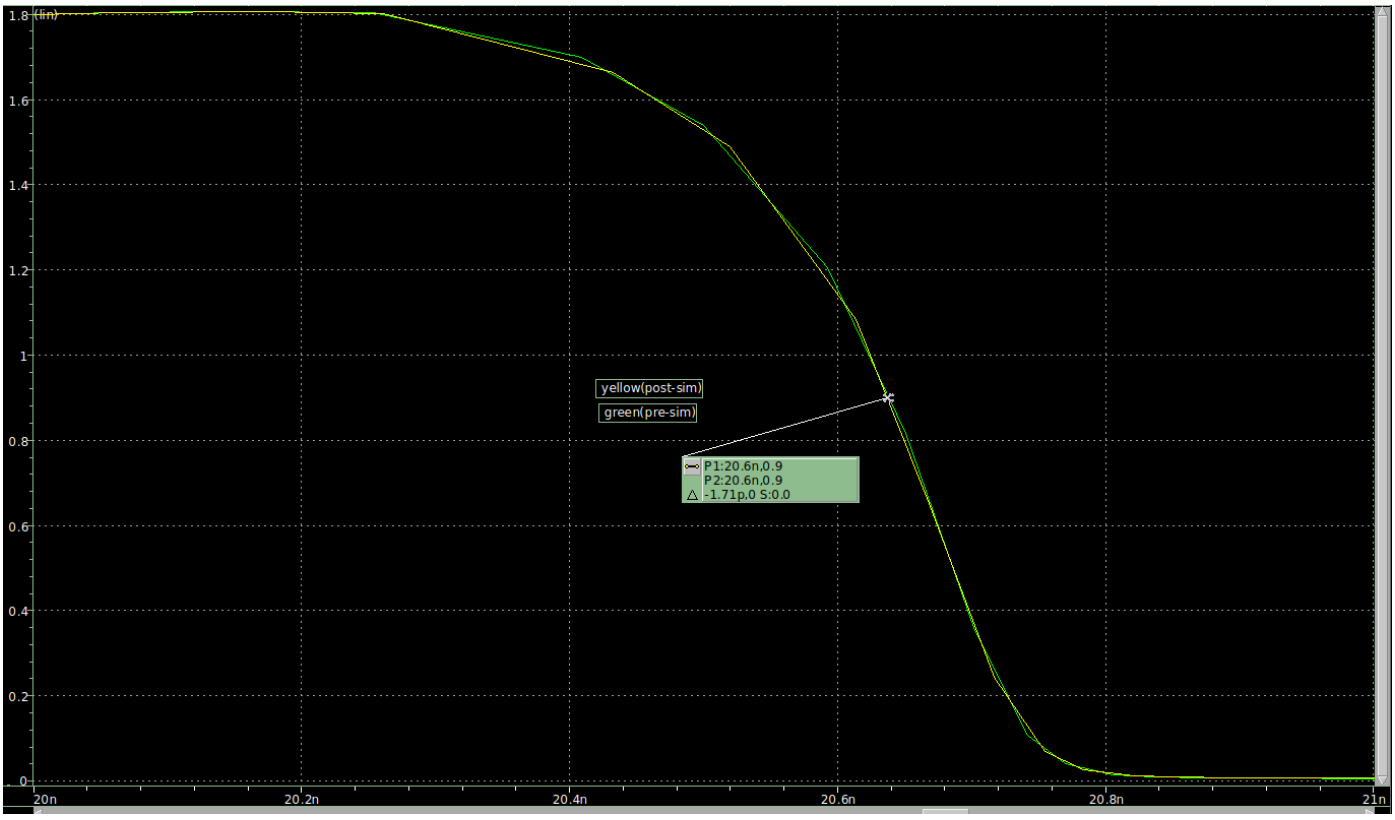
	tpLH(ps)	tpHL(ps)
pre-sim	133.3	138.6
post-sim	131.4	136.9

post-sim 的波形（黃色）pre-sim 的波形綠色

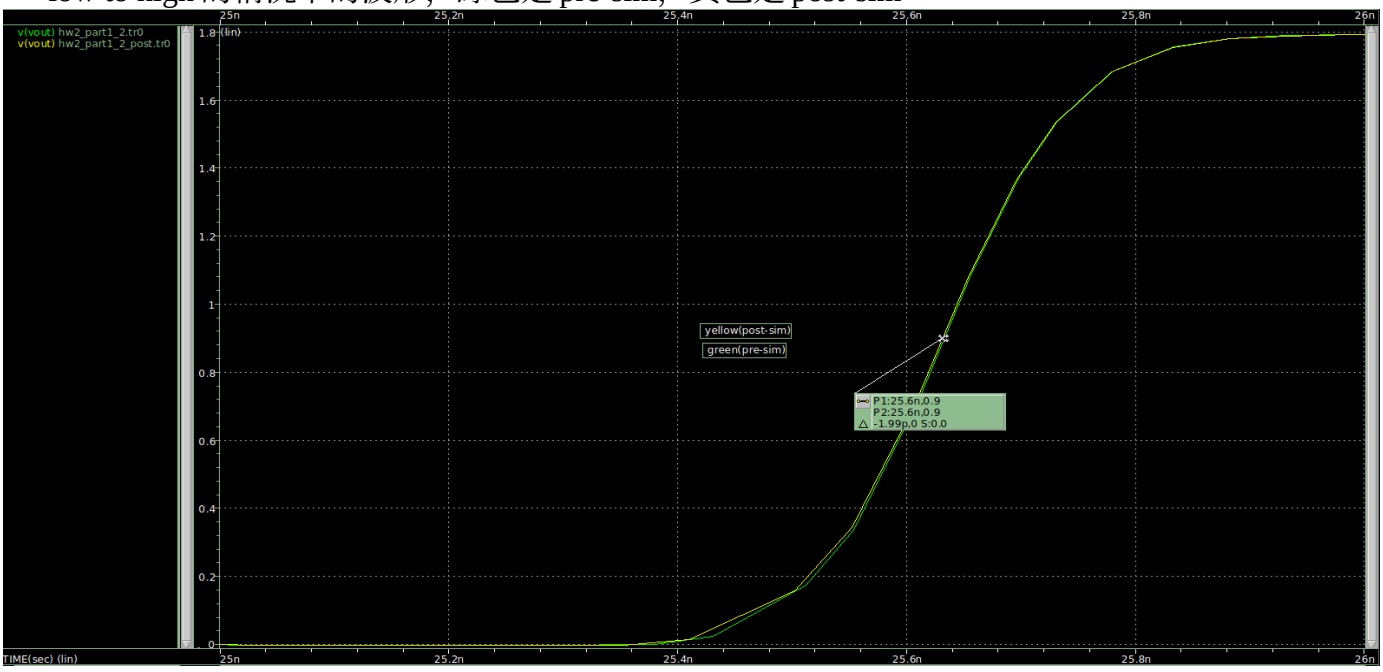


post-sim 和 pre-sim 做比較(因不太明顯，所以放大分成兩張):

high to low 的情況下的波形，綠色是 pre-sim，黃色是 post-sim



low to high 的情況下的波形，綠色是 pre-sim，黃色是 post-sim



由比較結果看出不論 tpLH 還是 tpHL 在 post-sim 之後延遲似乎沒有非常明顯的變化，甚至略下降，波形也幾乎相同，。會變化如此不明顯可能是因為寄生電容的大小相較於C load 而言很小，在這樣的條件下就算考慮寄生電容和電阻，也無法看出太明顯的變化。

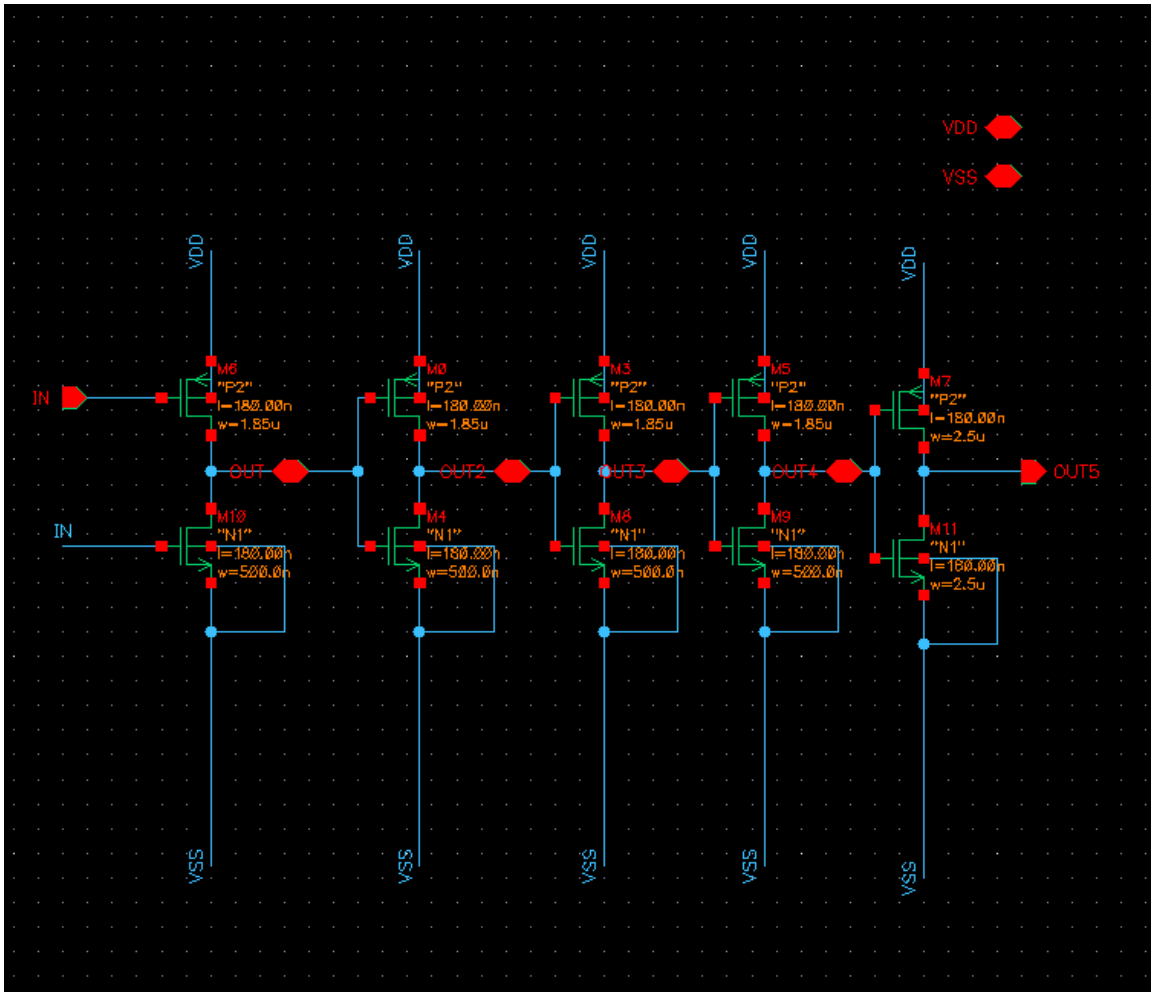
Part II (Inverter chain) (50%)

1. Complete the layout of your inverter chain from HW1 Part II. Show the figure of your layout and DRC/LVS report. (15%) and measure the area. (2.5%)

(Output loading Cload = 10pF)

Bonus: FoM = delay * area (delay will get from post-sim)

FOM:2.8*10^5(um^2*ps)



本題中的 inverter chain 有做如下調整:

hw1:

inverter1:

pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1

inverter2:

pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1

inverter3:

pmos(1.85u/0.18u) ,m=3;nmos(0.5u/0.18u) ,m=3

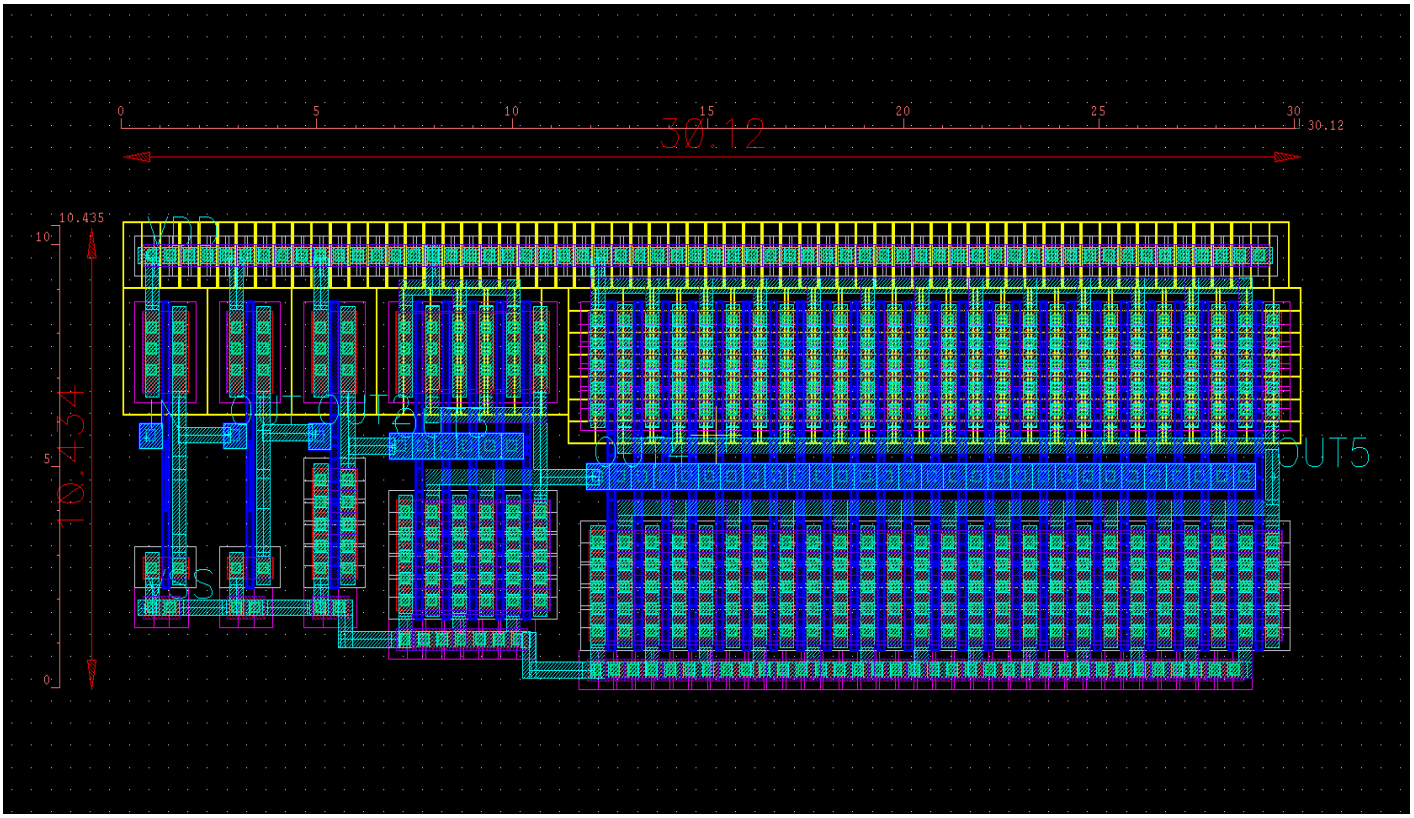
inverter4:

pmos(1.85u/0.18u) ,m=5;nmos(0.5u/0.18u) ,m=5

inverter5:

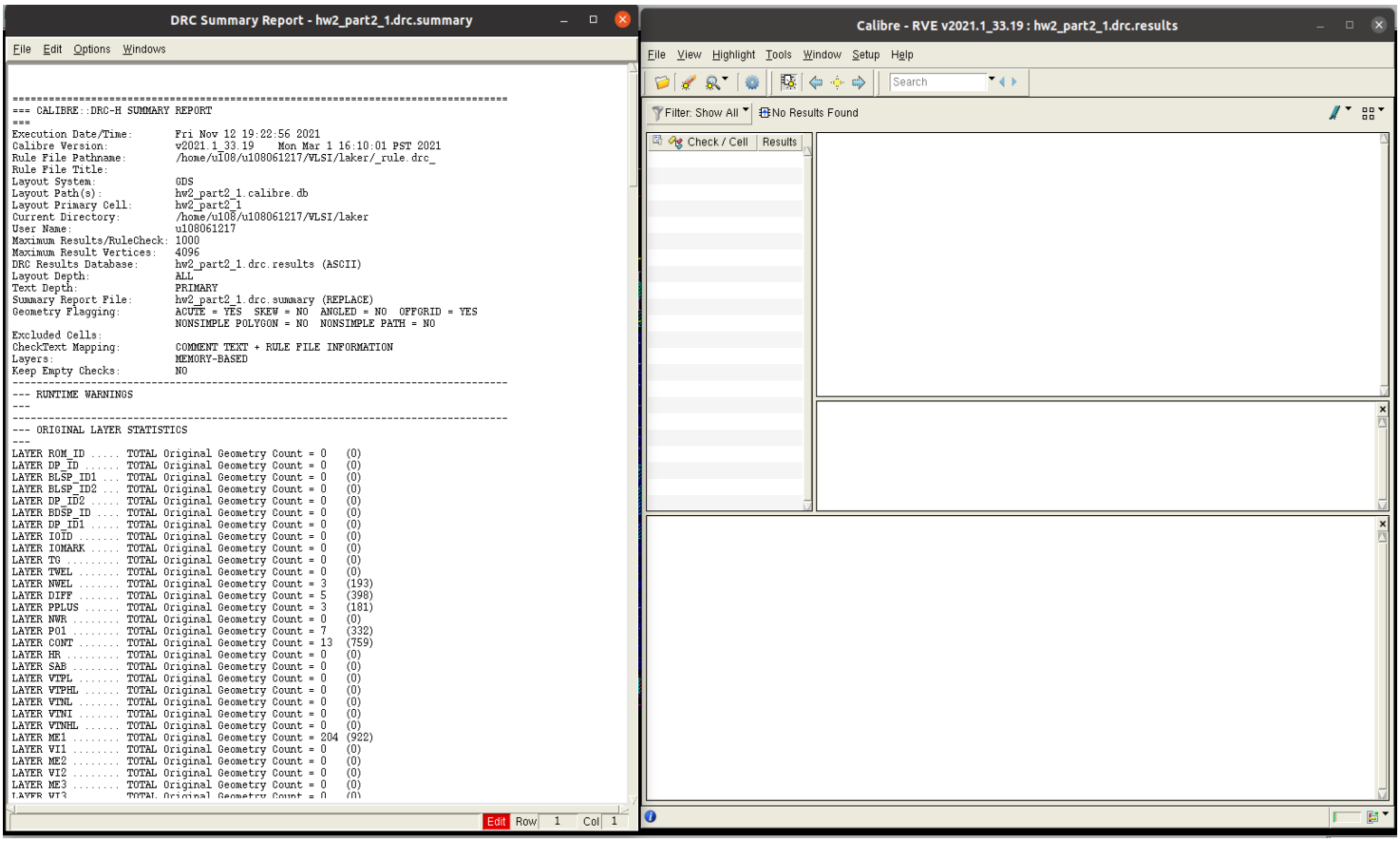
pmos(11.4u/0.18u) ,m=7;nmos(4.2u/0.18u) ,m=7

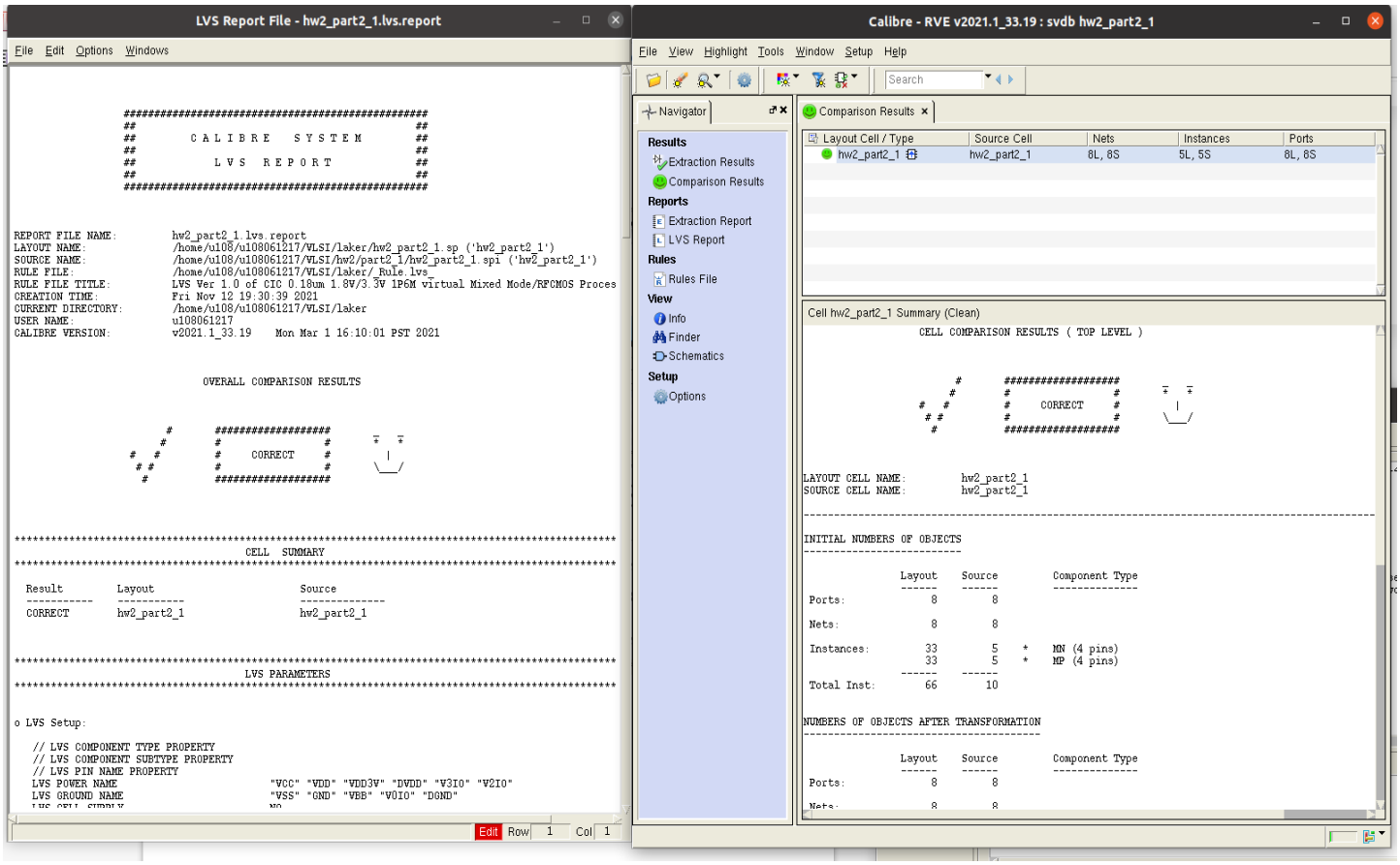
hw2:
inverter1:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter2:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter3:
pmos(1.85u/0.18u) ,m=1;nmos(2.5u/0.18u) ,m=1
inverter4:
pmos(1.85u/0.18u) ,m=5;nmos(2.5u/0.18u) ,m=5
inverter5:
pmos(2.5u/0.18u) ,m=25;nmos(2.5u/0.18u) ,m=25



area:

area = 10.434*30.12 = 314.27208(um^2)

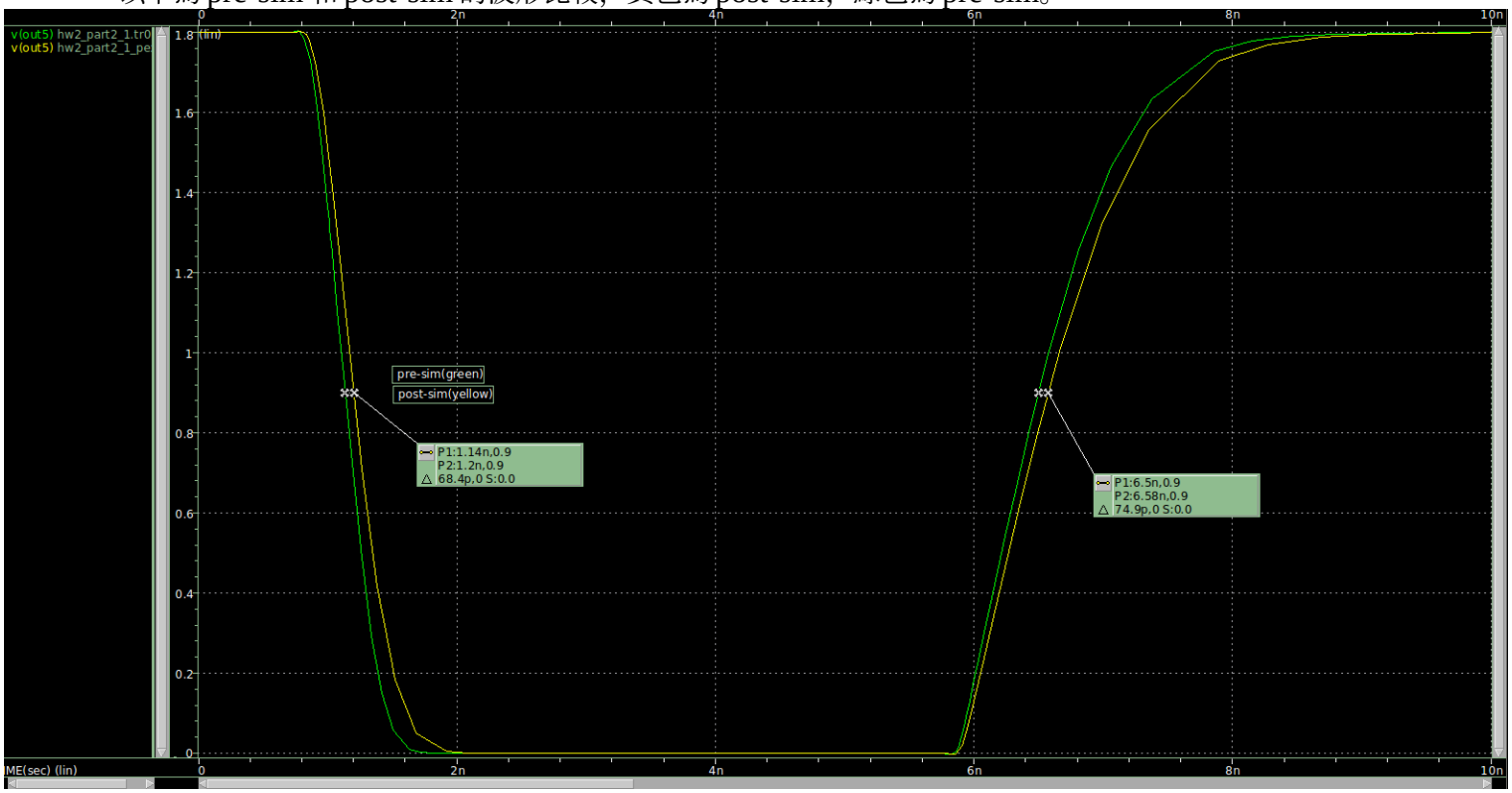

DRC Summary Report - hw2_part2_1.drc.summary
File Edit Options Windows
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Fri Nov 12 19:22:56 2021
Calibre Version: v2021.1_33.19 Mon Mar 1 16:10:01 PST 2021
Rule File Pathname: /home/u108/u108061217/VLSI/laker/_rule.drc_
Layout System: GDS
Layout Path(s): hw2_part2_1.calibre.db
Layout Primary Cell: hw2_part2_1
Current Directory: /home/u108/u108061217/VLSI/laker
User Name: u108061217
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: hw2_part2_1.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: hw2_part2_1.drc.summary (REPLACE)
Geometry Flagging: ACUTE = YES SKEW = NO ANGLED = NO OFFGRID = YES
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: NO
--- RUNTIME WARNINGS
--- ORIGINAL LAYER STATISTICS
LAYER NOM_ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID ..... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP_ID1 ... TOTAL Original Geometry Count = 0 (0)
LAYER BLSP_ID2 ... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID2 ..... TOTAL Original Geometry Count = 0 (0)
LAYER BDSP_ID .... TOTAL Original Geometry Count = 0 (0)
LAYER DP_ID1 ..... TOTAL Original Geometry Count = 0 (0)
LAYER IOID .... TOTAL Original Geometry Count = 0 (0)
LAYER IOMARK ..... TOTAL Original Geometry Count = 0 (0)
LAYER TG .... TOTAL Original Geometry Count = 0 (0)
LAYER TWEL .... TOTAL Original Geometry Count = 0 (0)
LAYER NWEL .... TOTAL Original Geometry Count = 3 (193)
LAYER DIFF .... TOTAL Original Geometry Count = 5 (398)
LAYER PPLUS ...... TOTAL Original Geometry Count = 3 (181)
LAYER NWR .... TOTAL Original Geometry Count = 0 (0)
LAYER PO1 .... TOTAL Original Geometry Count = 7 (332)
LAYER CONT .... TOTAL Original Geometry Count = 13 (759)
LAYER HR .... TOTAL Original Geometry Count = 0 (0)
LAYER SAB .... TOTAL Original Geometry Count = 0 (0)
LAYER VTPL .... TOTAL Original Geometry Count = 0 (0)
LAYER VTPHL ...... TOTAL Original Geometry Count = 0 (0)
LAYER VTNL .... TOTAL Original Geometry Count = 0 (0)
LAYER VTNI .... TOTAL Original Geometry Count = 0 (0)
LAYER VTNHL ...... TOTAL Original Geometry Count = 0 (0)
LAYER ME1 .... TOTAL Original Geometry Count = 204 (922)
LAYER VI1 .... TOTAL Original Geometry Count = 0 (0)
LAYER ME2 .... TOTAL Original Geometry Count = 0 (0)
LAYER VI2 .... TOTAL Original Geometry Count = 0 (0)
LAYER ME3 .... TOTAL Original Geometry Count = 0 (0)
Edit Row 1 Col 1
Calibre - RVE v2021.1_33.19 : hw2_part2_1.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
No Results Found
Check / Cell
Results


LVS Report File - hw2_part2_1.lvs.report
File Edit Options Windows
C A L I B R E S Y S T E M
L V S R E P O R T
REPORT FILE NAME: hw2_part2_1.lvs.report
LAYOUT NAME: /home/u108/u108061217/VLSI/laker/hw2_part2_1.sp ('hw2_part2_1')
SOURCE NAME: /home/u108/u108061217/VLSI/hw2/part2_1/hw2_part2_1.spi ('hw2_part2_1')
RULE FILE: /home/u108/u108061217/VLSI/laker/_Rule.lvs_
RULE FILE TITLE: LVS Ver 1.0 of CIC 0.18um 1.8V/3.3V 1P6M virtual Mixed Mode/RFCMOS Proces
CREATION TIME: Fri Nov 12 19:30:39 2021
CURRENT DIRECTORY: /home/u108/u108061217/VLSI/laker
USER NAME: u108061217
CALIBRE VERSION: v2021.1_33.19 Mon Mar 1 16:10:01 PST 2021
OVERALL COMPARISON RESULTS
CORRECT
CELL SUMMARY
Result Layout Source
CORRECT hw2_part2_1 hw2_part2_1
LVS PARAMETERS
o LVS Setup:
// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY
// LVS PIN NAME PROPERTY
LVS POWER NAME "VCC" "VDD" "VDD3V" "DVDD" "V3IO" "V2IO"
LVS GROUND NAME "VSS" "GND" "VBB" "V0IO" "DGND"
Edit Row 1 Col 1
Calibre - RVE v2021.1_33.19 : svdb hw2_part2_1
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type Source Cell Nets Instances Ports
hw2_part2_1 hw2_part2_1 8L, 8S 5L, 5S 8L, 8S
Cell hw2_part2_1 Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: hw2_part2_1
SOURCE CELL NAME: hw2_part2_1
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 8 8
Nets: 8 8
Instances: 33 5 * MN (4 pins)
33 5 * MP (4 pins)
Total Inst: 66 10
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 8 8
Nets: 8 8

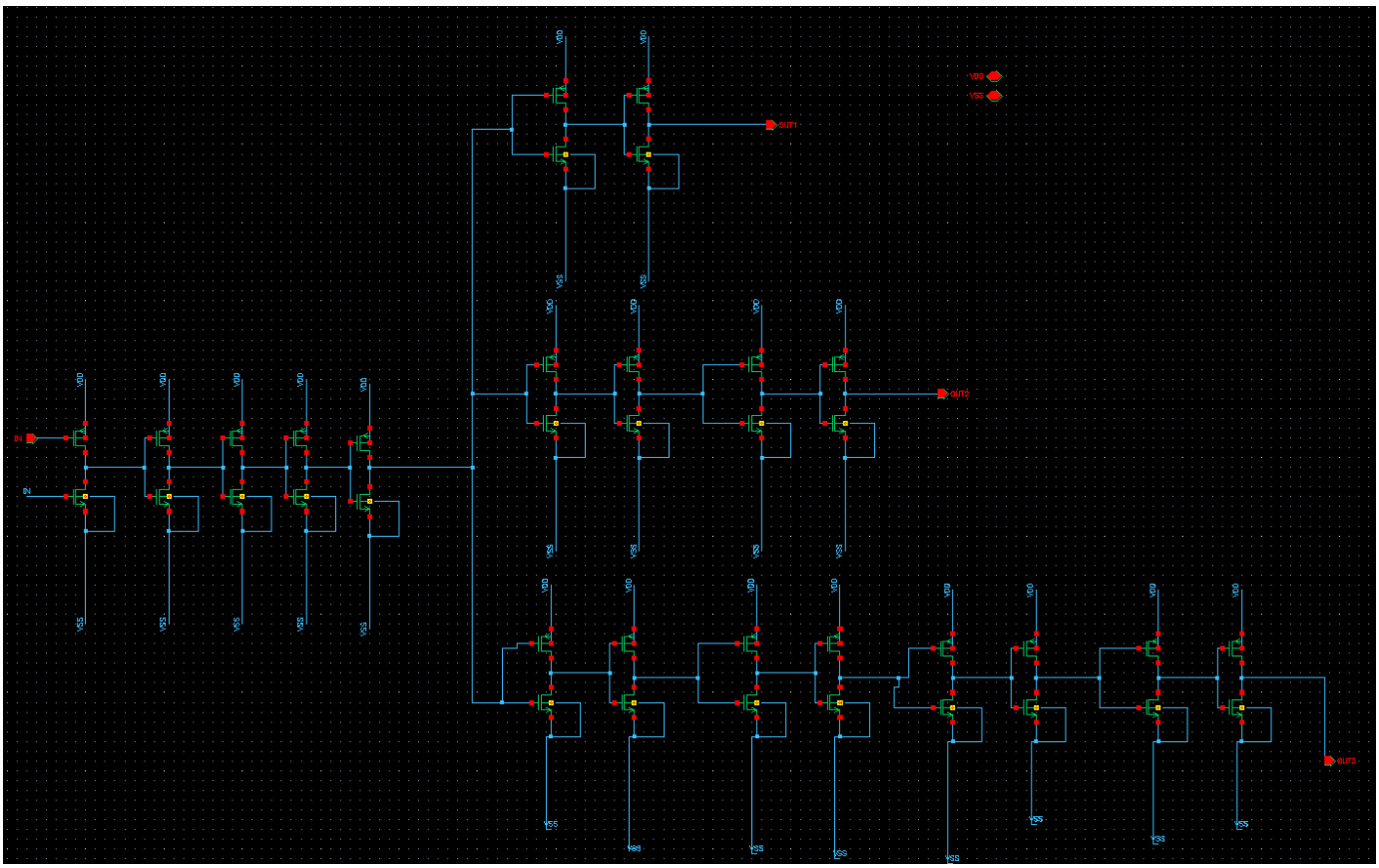
2. Run post-sim (with R-C-CC extraction), compare the result and waveform with pre-sim from HW1 Part II. (5%)

tpHL : from 635.5ps(pre-sim) to 703.9ps(post-sim)
tpLH: from 1003ps(pre-sim) to 1078ps(post-sim)
propagation delay : from 819.2ps(pre-sim) to 890.9ps(post-sim)
delay_time 變化(post-sim - pre-sim):71.7ps
可以看出 post-sim 相較於 pre-sim delay 明顯較大，原因應是因為 pre-sim 所模擬的情況並未考量到寄生電阻和電容的影響，而在 inverter chain 當中，有許的個 inverter 串接在一起，所以會有較大的寄生電阻與電容，post-sim 考量到了這些寄生電阻語電容，這些寄生的電阻電容使 delay 更大。

以下為 pre-sim 和 post-sim 的波形比較，黃色為 post-sim，綠色為 pre-sim。



3. Use different stage as branch to measure the propagation delay. The first half is your inverter chain in HW1 Part II and the last half is three kinds of inverter chain with different stage. (5%) (Output loading Cload = 10pF) Note : The size of first inverter in last half (where the red arrow points) of long inverter chain is fixed : (W/L)n = (0.5um/0.18um), (W/L)p = (1.85um/0.18um).



last half:

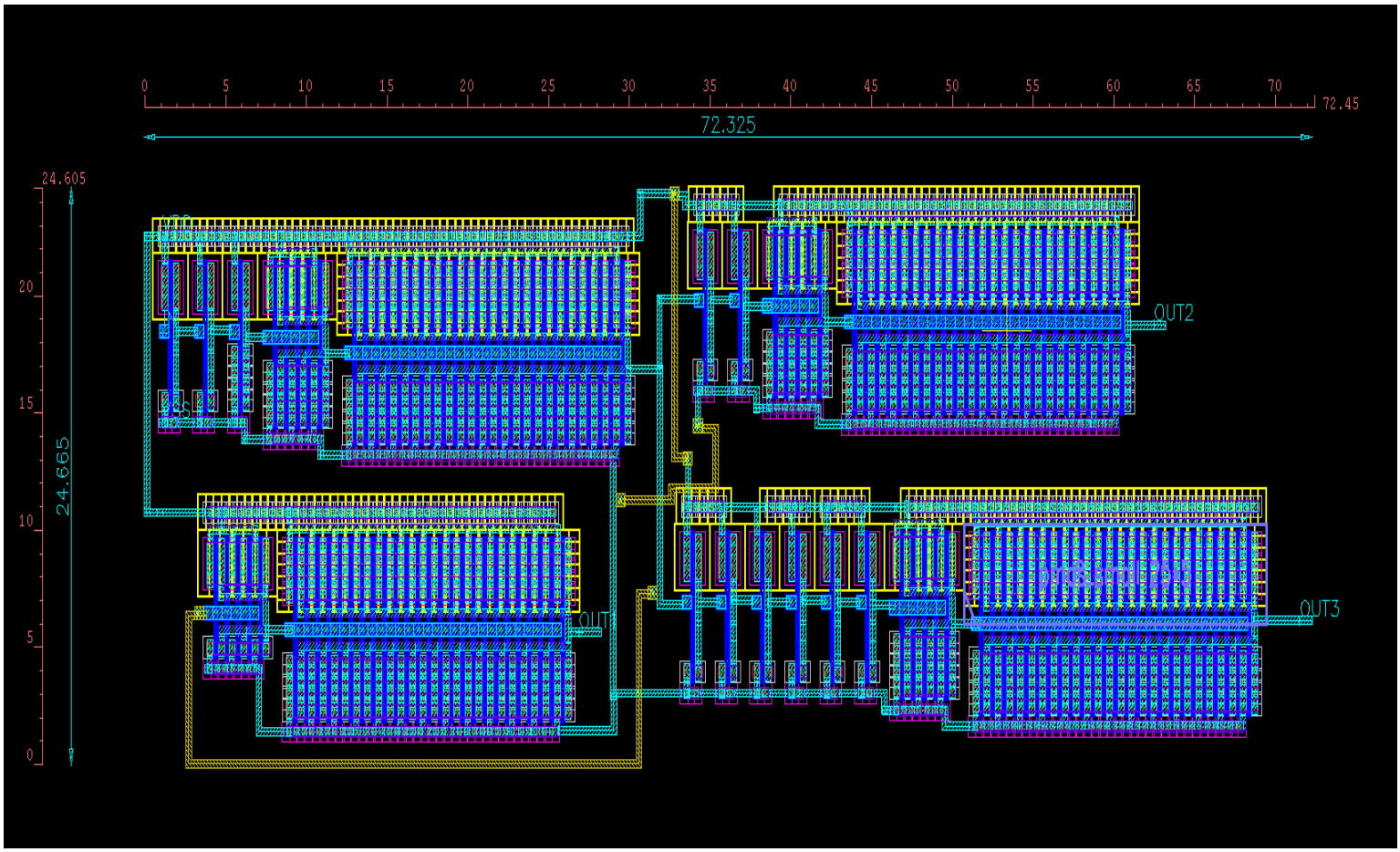
inverter chain1:
inverter1
 pmos(1.85u/0.18u) ,m=5;nmos(0.5u/0.18u) ,m=5
inverter2:
 pmos(2.5u/0.18u) ,m=25;nmos(2.5u/0.18u) ,m=25

inverter chain2:
inverter1:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter2:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter3:
 pmos(1.85u/0.18u) ,m=5;nmos(2.5u/0.18u) ,m=5
inverter4:
 pmos(2.5u/0.18u) ,m=25;nmos(2.5u/0.18u) ,m=25

inverter chain3:
inverter1:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter2:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter3:

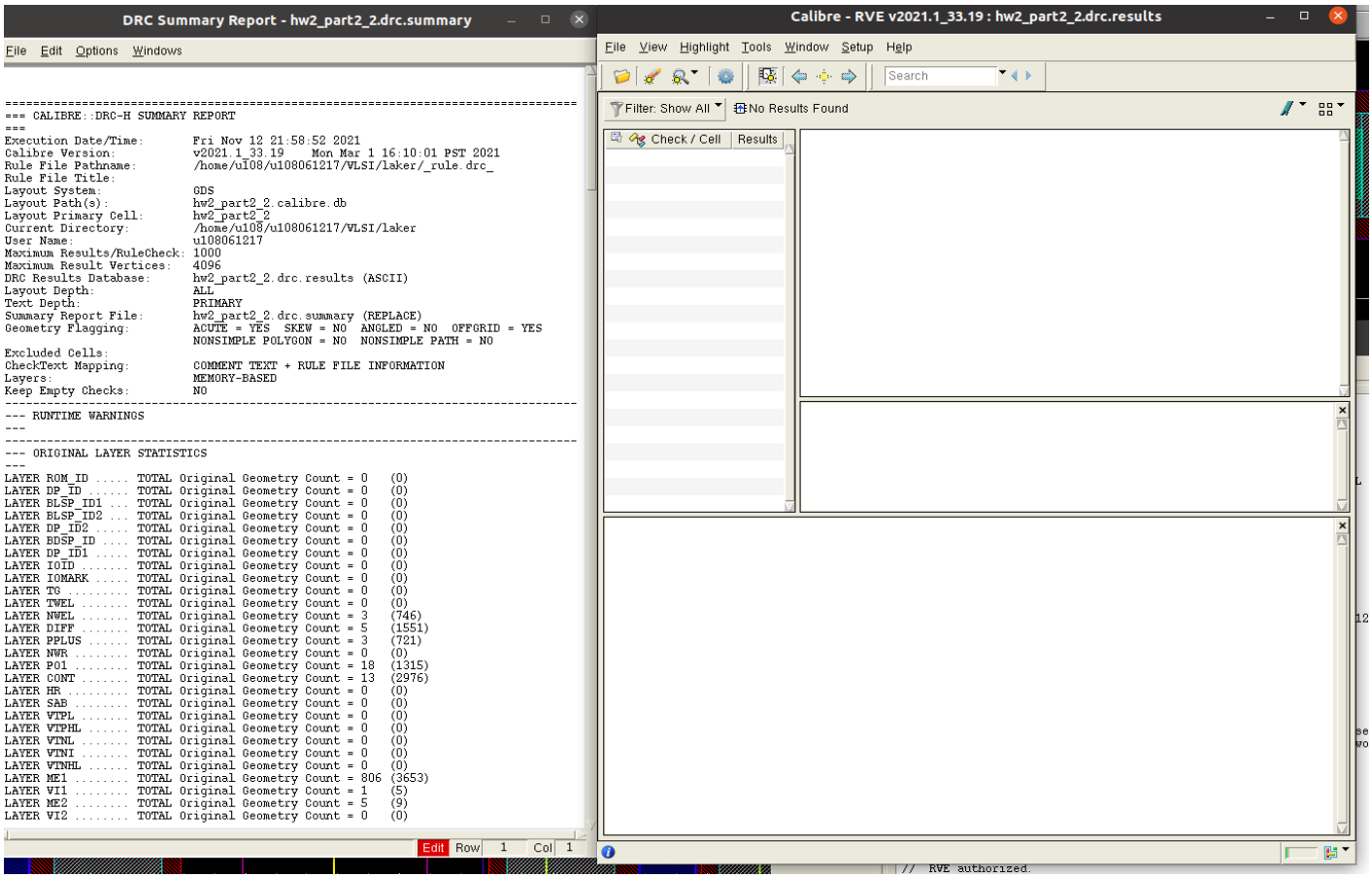
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter4:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter5:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter6:
pmos(1.85u/0.18u) ,m=1;nmos(0.5u/0.18u) ,m=1
inverter7:
pmos(1.85u/0.18u) ,m=5;nmos(2.5u/0.18u) ,m=5
inverter8:
pmos(2.5u/0.18u) ,m=25;nmos(2.5u/0.18u) ,m=25

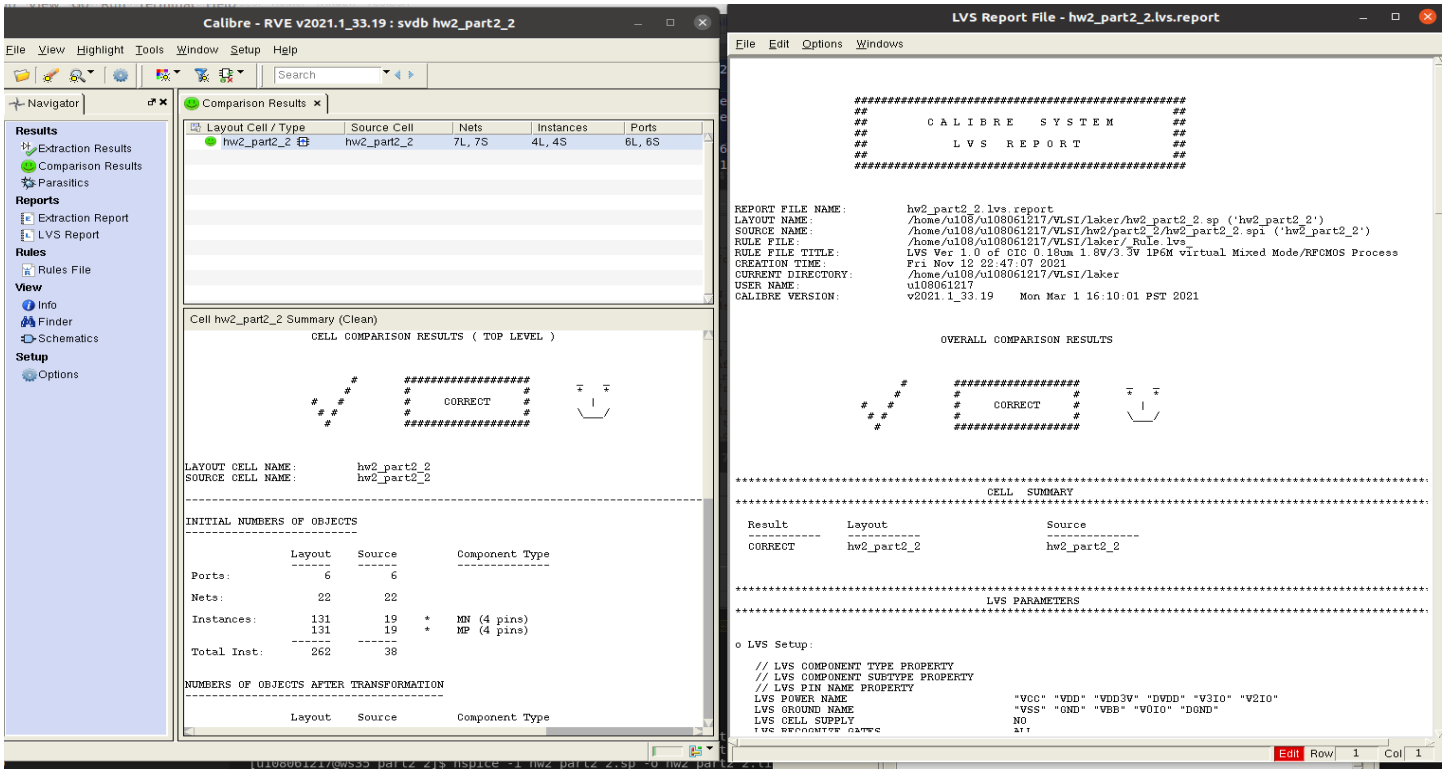
4. Complete the layout of Fig. 3. Show the figure of your layout and DRC/LVS report. (15%) and measure the area. (2.5%)



area:

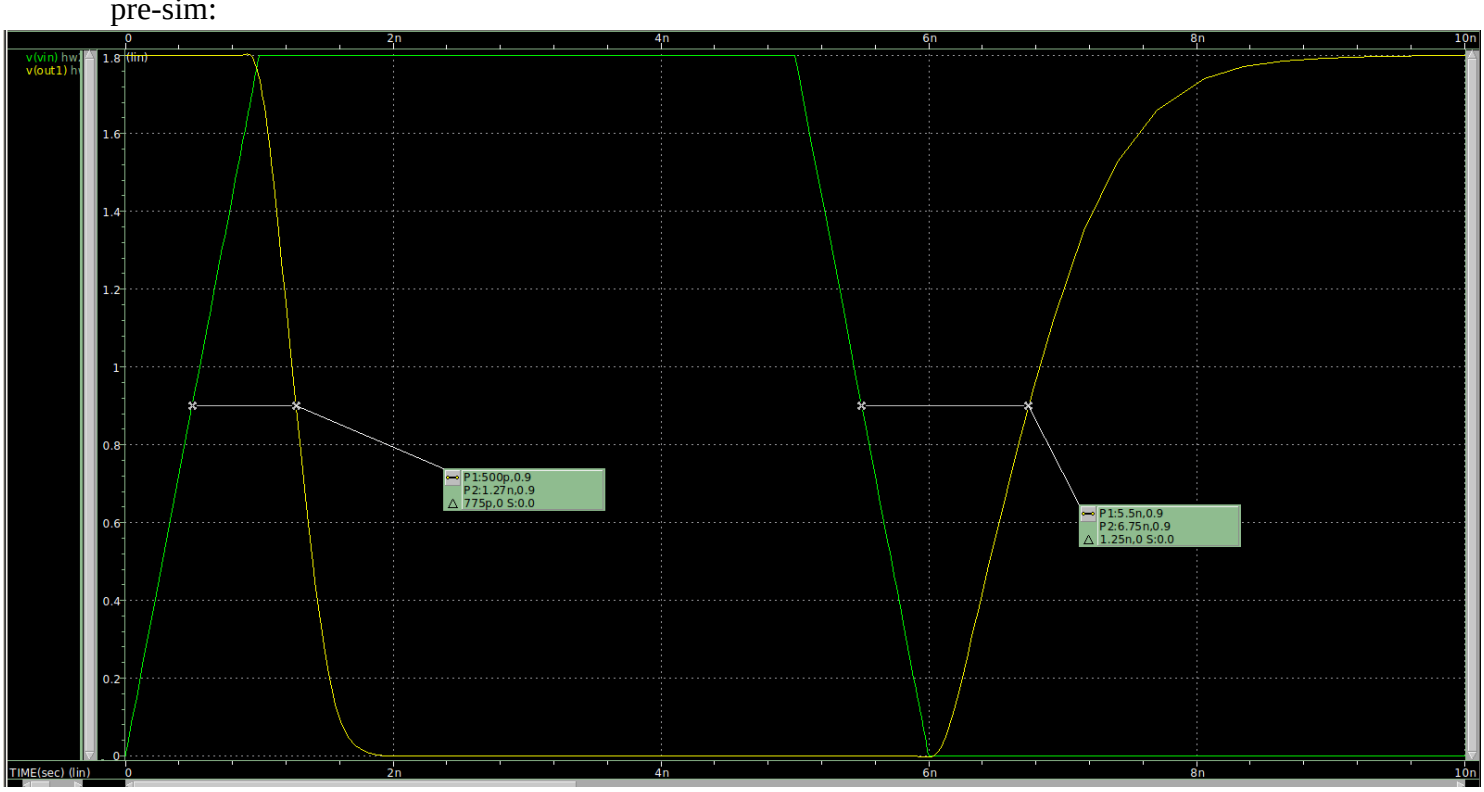
area = 24.665*72.325 = 1783.896125(um^2)



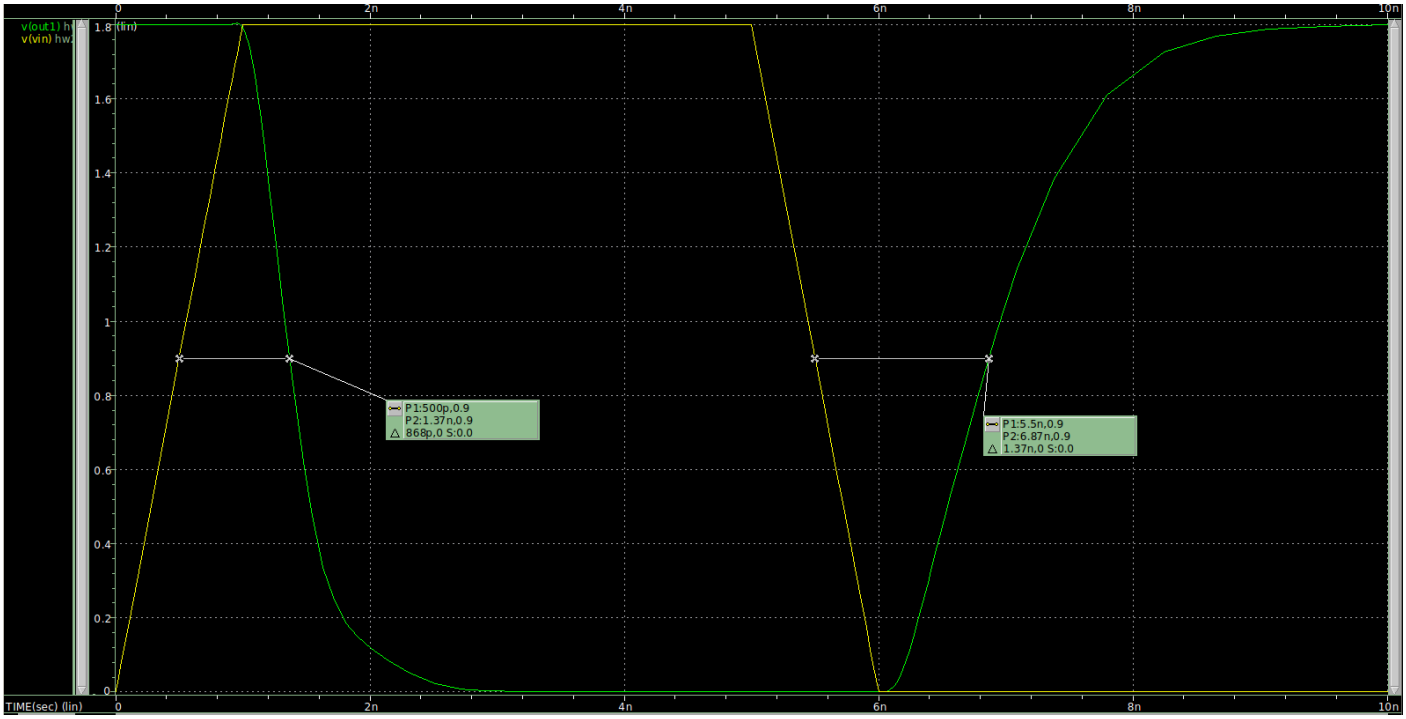


5. Run post-sim (with R-C-CC extraction), compare the delay of three delay chain. (5%)
比較了三個 stage 的結果，可以看出不管後面接哪種，最後的 delay 都會比原來大，而尤其是後半段接上 8 個 inverter 的情況 delay 最大，而且其 post-sim 的 delay 比起 pre-sim 變化也最多，可能是由於後半段接 8 個時 inverter chain 太長了，太長的 inverter chain 會導致 delay 變大，而且太長的 inverter chain 受到寄生電阻和電容的影響特別的明顯，所以才會在 post-sim 後 delay 變化特別大。

inverter chain with 2 stage(last half) pre-sim:1011ps ; post-sim:1118ps;delay_time 變化(pre-sim - post-sim)：107ps(tpHL:747.7ps to 868ps;tpLH:1247ps to 1368ps)
pre-sim:

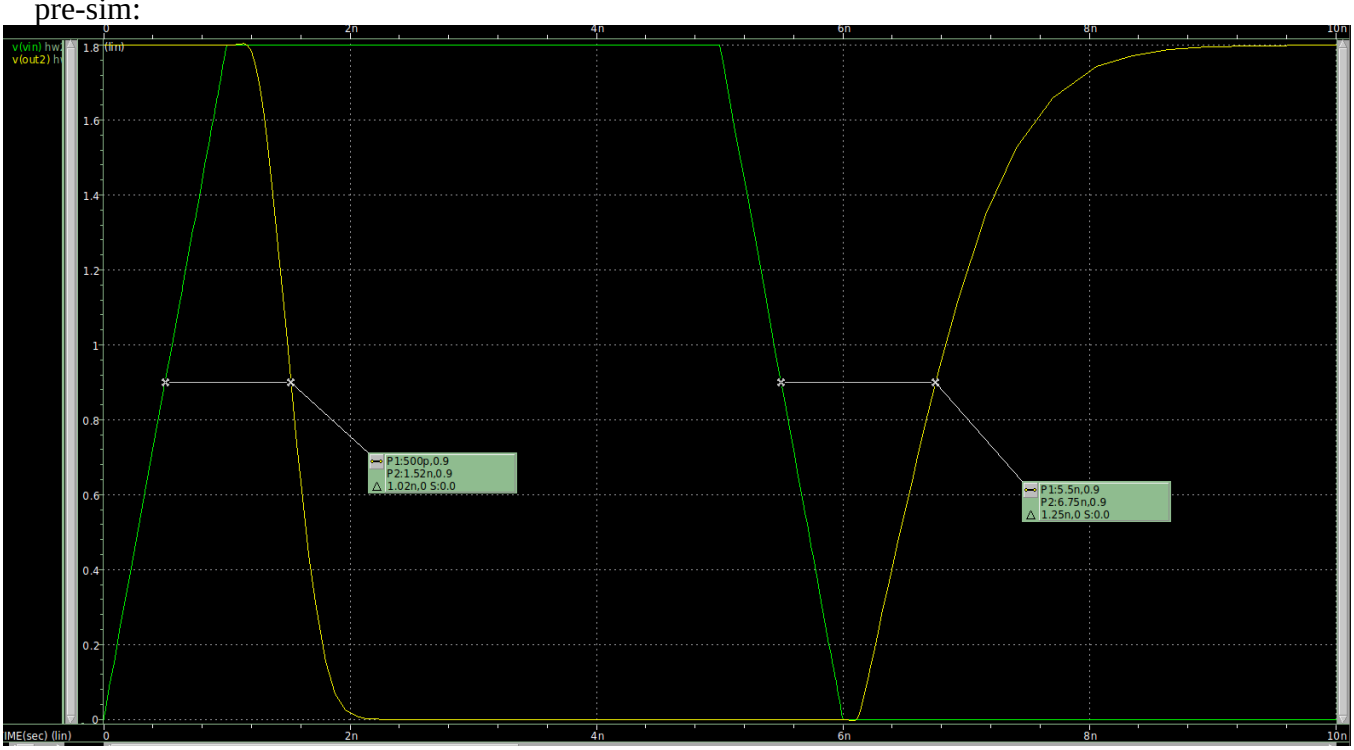


post-sim:

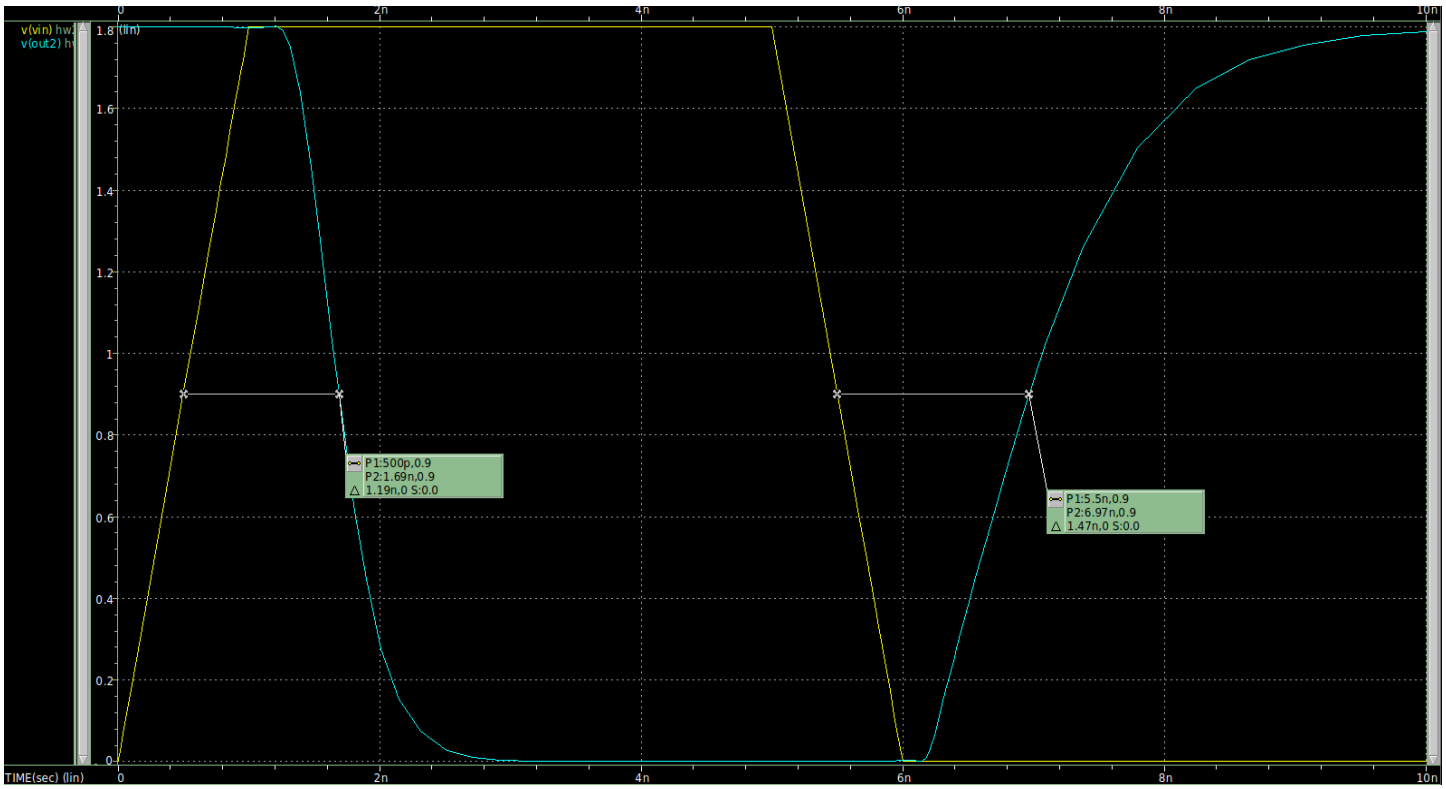


inverter chain with 4 stage(last half) pre-sim:1138ps ; post-sim:1330ps;delay_time 變化(pre-sim - post-sim)：192ps(tpHL:1021ps to 1191ps;tpLH:1254ps to 1469ps)

pre-sim:

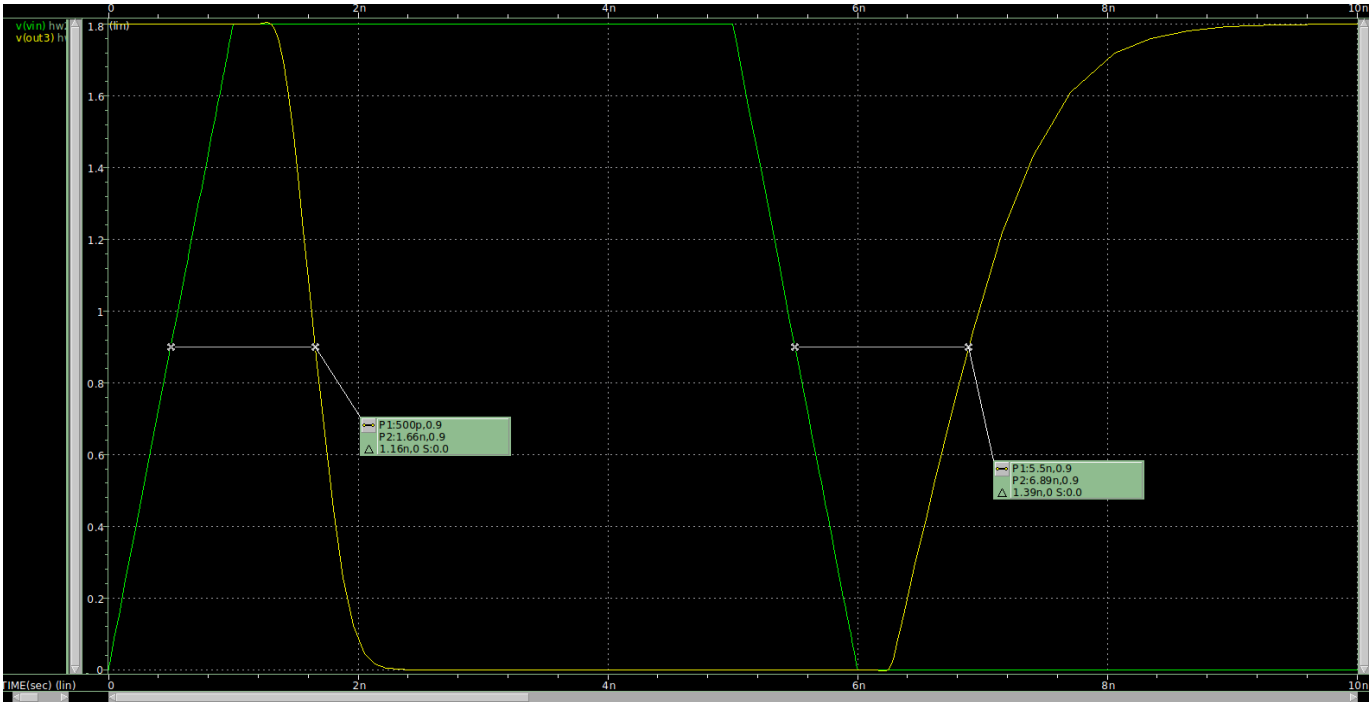


post-sim:

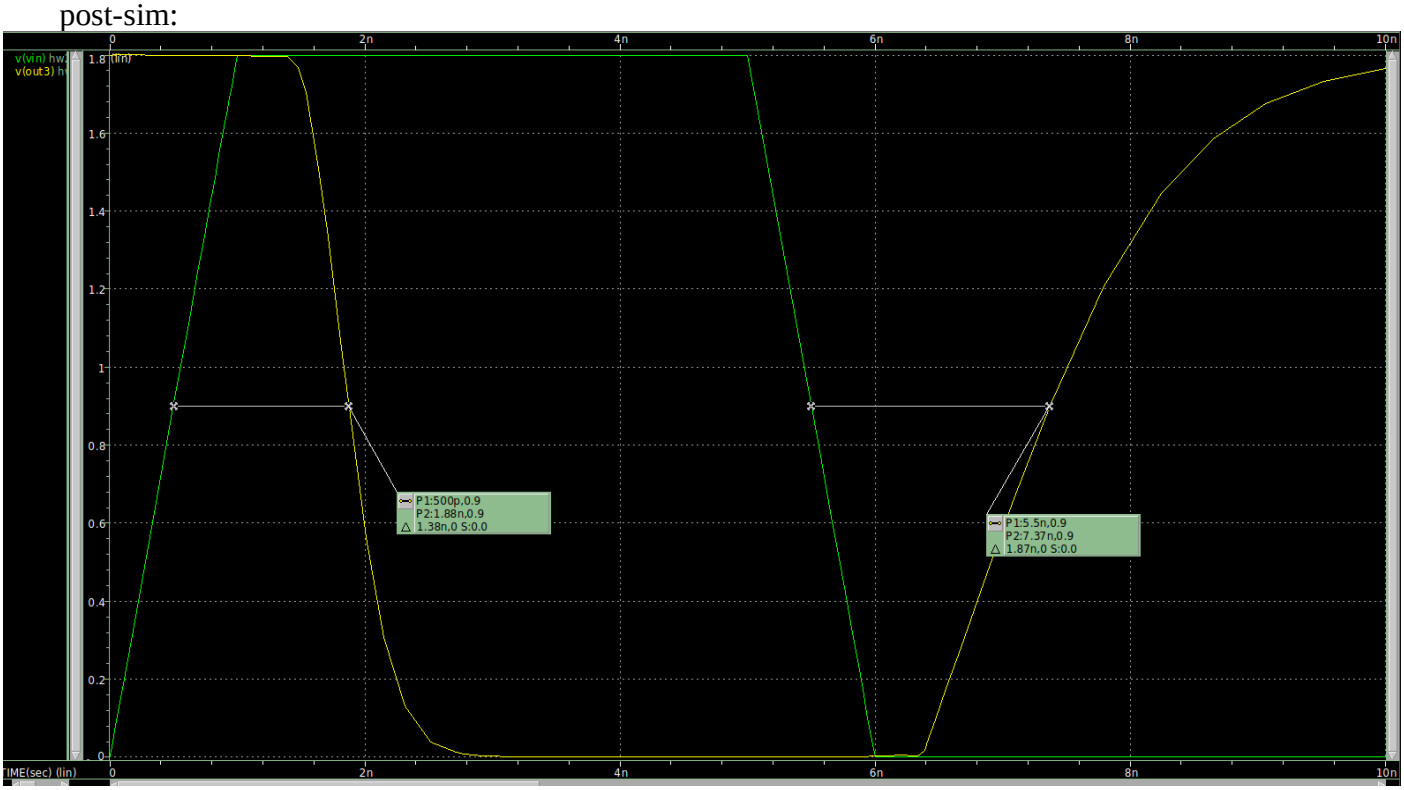


inverter chain with 8 stage(last half) pre-sim:1274ps ; post-sim:1623ps;delay_time 變化(pre-sim - post-sim)： 349ps(tpHL:1157ps to 1375ps;tpLH:1391ps to 1870ps)

pre-sim:



post-sim:



What I have learned in this HW:

在 hw2 中我學到的主要是如何使用 laker 和 composer，並且還學到關於 layout 的規定和格式，此外也觀察到 post-sim 的結果會和如何不同，還有如何實現用 nmos 和 pmos 來表示 logic circuit，和觀察不同長度的 inverter chain 間的差異。